High Step-Up Resonant DC/DC Converter With Balanced Capacitor Voltage for Distributed Generation Systems

Sungho Son, *Student Member, IEEE*, Oscar Andrés Montes, *Student Member, IEEE*, Adrià Junyent-Ferré, *Member, IEEE*, and Minsung Kim, *Member, IEEE*

***Abstract*—We propose a high step-up resonant dc–dc converter that can achieve voltage balance of the resonant capacitors in distributed generation systems. By incorporating a switching mechanism on the secondary side, we achieve high step-up voltage gain with a minimum number of devices and without reverse-recovery problem. An active-clamp circuit installed on the primary side suppresses the surge voltage that occurs at switch components, recycles the energy stored in the leakage inductance, and provides an alternate resonant-current path formed by the leakage inductance and the output resonant capacitors. A dual resonance that occurs at the secondary side of the converter is exploited to reduce the turn-OFF current and switching loss significantly, and to achieve high power conversion efficiency. The resonant capacitor voltages remain in balance because the duty cycle of the primary-side switches is always set to 0.5, regardless of the input voltages and load variations. Design and analysis of the proposed converter are presented, and tests using a 400-W experimental prototype verify its superior performance.**

***Index Terms*—Active clamp, dual series-resonant converter, high step-up, minimum number of devices, voltage unbalance.**

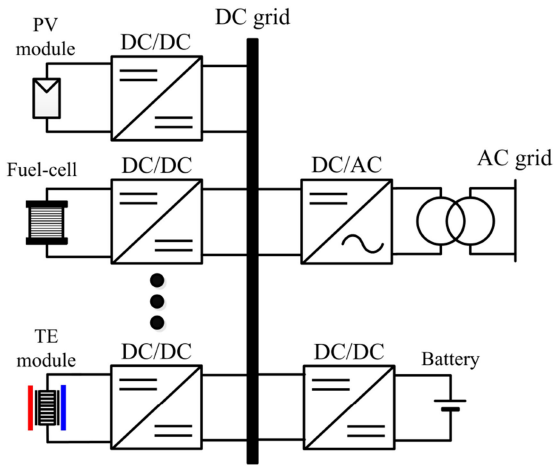

Fig. 1. Configuration of the dc microgrid with multiple energy sources and converters. PV and TE stand for photovoltaic and thermoelectric, respectively.

I. Introduction

In RECENT years, renewable energy based distributed power generation (DG) systems have the potential to meet the demand for electrical energy while mitigating global warming and exhaustion of fossil fuels [1], [2]. DG power systems are usually composed of photovoltaic sources, thermoelectric systems, fuel cells, and wind turbines. However, the output voltages of the energy sources are generally low and vary widely with climatic conditions, such as irradiation, temperature, and wind velocity. These low and variable voltages are required to be boosted first to high-voltage dc to generate the required ac utility voltage [3], [4]. The importance of boosting the dc voltage has increased with the emergence of 400-V dc microgrids powered by multiple energy sources (see Fig. 1).

Use of high step-up dc–dc converters is a suitable solution for this problem [5]–[9]. Theoretically, a conventional boost converter has an unlimited static gain when the duty cycle approaches unity. But, in practice, the step-up voltage gain is limited by the power loss from the switch, the rectifier diode, and the equivalent series resistance of the inductors and capacitors. Moreover, using the extremely high duty cycle may result in serious reverse-recovery problem and degraded power conversion efficiency [10], [11].

Several isolated converters have achieved high step-up conversion ratio by adjusting the turns-ratio of the transformer. Among the various dc/dc topologies, the flyback and forward converters are considered the most attractive due to their simple circuitry and control scheme. However, the leakage inductor of the transformer causes switching loss from the power switches;

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the output diode suffers from serious reverse-recovery, which degrades the conversion efficiency. To solve these problems, flyback and forward dc–dc converters that use an active-clamp circuit have been proposed [12]–[16]. The energy stored in the leakage and the magnetizing inductances of the transformer is recycled, and the main, as well as auxiliary switches, can achieve zero-voltage-switching (ZVS) turn-ON. The clamp circuit also holds the voltage on the power switches at a specific voltage level. Recently, several resonant converters with active-clamp circuits have also been proposed [17], [18] to achieve soft switching. However, because these converters transfer the input power to the output stage only while the main switch is being turned ON or OFF, their transformer utilization is lower than those of other converters, which can deliver input power to the output stage regardless of ON/OFF state.

To improve transformer utilization, a dual series-resonant circuit equipped with both flyback and forward rectifiers has been proposed [19]. It utilizes the transformer more effectively than the sole flyback or sole forward converter does because the dual series-resonant circuit provides power-transfer paths regardless of the main switch ON/OFF state. In addition, the zero-current turn-OFF on the output diode removes its reverse-recovery problem. Unlike flyback or forward converters, it functions as a boost converter so the transformer turns-ratio can be greatly reduced; as a result, leakage inductance and parasitic capacitance are reduced, so voltage or current spikes on the power devices are also reduced. Subsequently, dual series-resonant converters with ZVS turn-ON of all switches have been developed by using coupled inductors [20] or two transformers [21]. However, to attain sufficiently high voltage-conversion gain, these converters [19]–[21] still require an extremely high duty cycle, which causes serious reverse-recovery problem and decreases power conversion efficiency. Moreover, the input voltage is not equal to the clamp capacitor voltage in these converters. Therefore, significant voltage unbalance occurs among the resonant capacitors. This unbalance causes high voltage stress on the resonant capacitors as well as the switching devices and complicates the task of designing a resonance circuit [22], [23].

To overcome these problems, we propose a high step-up resonant dc–dc converter that can achieve voltage balance of the resonant capacitors. By using the switching mechanism that is used in the output-voltage doubler, the proposed converter can achieve high step-up voltage gain with a minimum number of devices and without reverse-recovery problem. An inherent active-clamp circuit suppresses the surge voltage of the switches and recycles the energy stored in the leakage inductance. Also, the proposed converter exploits the resonance to reduce the turn-OFF current and the switching loss considerably. The primary-side switches are modulated with a constant 0.5 duty cycle, regardless of the input voltage and load variations; as a result, the input and clamp capacitor voltages maintain their balance, and thereby achieve voltage balance on the resonance capacitors. We present detailed circuit operations, steady-state analysis, and design guidelines. We also implemented a version of the proposed converter that operates at 40–50 V input and 380 V/400 W output and demonstrated its power conversion efficiency.

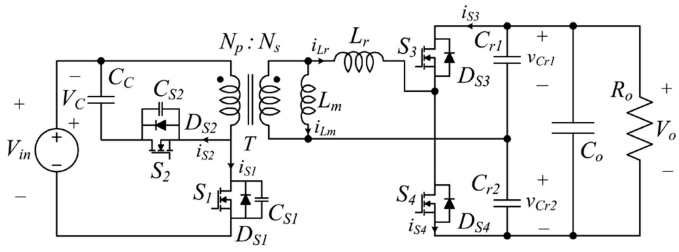

Fig. 2. Circuit diagram of the proposed high step-up resonant dc/dc converter.

The rest of this paper is organized as follows. The circuit operations of the proposed converter are described in Section II, and its steady-state analysis is given in Section III. The design guideline of the proposed converter is described in Section IV. Experimental results and discussions are presented in Section V, and the conclusions are drawn in Section VI.

II. Description of Principle Operation

In the proposed converter (see Fig. 2), the primary side of the power transformer T has two switches S_1 and S_2 with a clamp capacitor C_c. On the secondary side of T, the converter uses a resonant half-bridge circuit that uses two switches S_3 and S_4, two resonant capacitors C_{r1} and C_{r2}, and a resonant inductor L_r that consists of the leakage inductance of the transformer and the additional external inductor.

The primary switches S_1, S_2 operate in a completely complementary way with a constant duty ratio $D_{\rm pri} = 0.5$, and short dead time. Assuming that the switching period is T_s, S_4 is turned ON during the first segment $D_{{\rm sec},b}T_s$ of the first half of T_s, whereas S_3 is turned ON during the first segment $D_{{\rm sec},t}T_s$ of the next half of T_s. The proposed converter fixes the duty cycle $D_{\rm pri}$ of the primary-side switches to 0.5 and controls $D_{{\rm sec},b}$ and $D_{{\rm sec},t}$. This design differs from the conventional dual series-resonant converter that is controlled by adjusting $D_{\rm pri}$.

To derive the characteristic equations of the different operation modes in a steady state, we make the following four assumptions.

1) Switches S_1, S_2, S_3, and S_4 in the proposed converter are ideal except for their reverse body diodes D_{S1}, D_{S2}, D_{S3}, and D_{S4} and output capacitances C_{S1} and C_{S2}.
2) The clamp capacitor C_c and the output capacitor C_o are sufficiently large that the clamp capacitor voltage V_C and the output voltage V_o have no ripple.
3) T is composed of an ideal transformer with a magnetizing inductance L_m and a leakage inductance. L_r is the series connection of the transformer leakage inductance and an external inductance.
4) The resonant capacitors C_{r1} and C_{r2} are identical, with capacitances $C_{r1} = C_{r2}$.

For subsequent development, we define $C_r = C_{r1} + C_{r2}$ and assume that $C_{S1} = C_{S2}$. The operation of the proposed dc–dc converter can be divided into eight different modes, as shown in Fig. 3, along with the corresponding waveforms as given in Fig. 4.

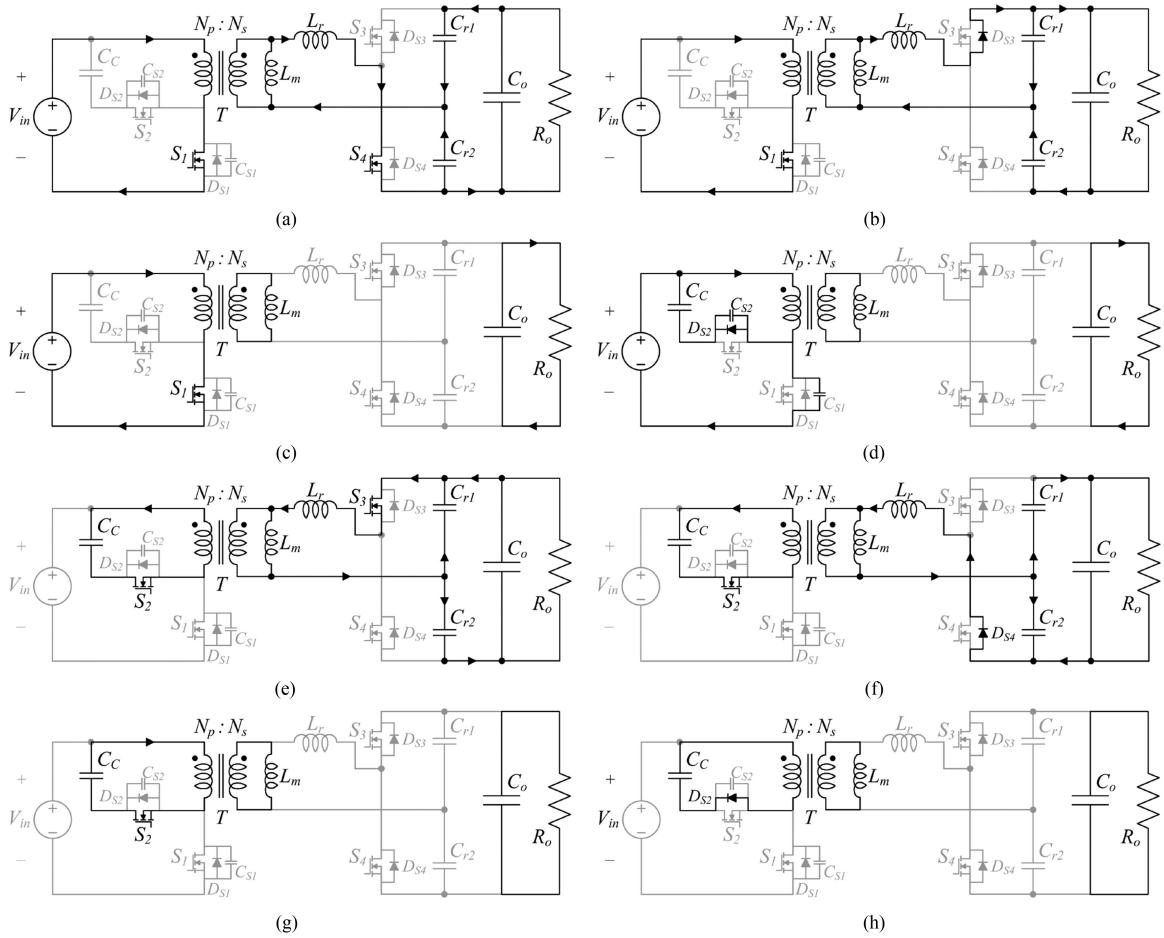

Fig. 3. Operation modes of the proposed converter. (a)–(h) Modes 1–8.

Mode 1 [t_0, t_1]: At the starting t_0, S_1 and S_4 are turned ON. Current i_{Lr} through L_r begins to flow, and voltage v_{Cr1} through capacitor C_{r1} begins to increase from its minimum value. During this interval, the input voltage source, the resonant inductor, and the resonant capacitor form an equivalent closed circuit that boosts the resonant inductor current upward following the sinusoidal waveform. The state equation corresponding to this equivalent circuit can be written as

$$L_r \frac{di_{Lr}(t)}{dt} = nV_{\text{in}} + V_o - v_{Cr1}(t) \tag{1}$$

$$i_{Lr}(t) = C_r \frac{dv_{Cr1}(t)}{dt} \tag{2}$$

with $i_{Lr}(t_0) = 0$ and $v_{Cr1}(t_0) = \frac{V_o}{2} - \Delta V_{Cr}$ where ΔV_{Cr} is the voltage ripple of the resonant capacitor. Solving (1) and (2) yields

$$i_{Lr}(t) = \frac{r_1}{Z_r} \sin\left[w_r(t - t_0)\right] \tag{3}$$

$$v_{Cr1}(t) = nV_{\text{in}} + V_o - r_1 \cos\left[w_r(t - t_0)\right] \tag{4}$$

where $r_1 = \frac{V_o}{2} + \Delta V_{Cr} + nV_{\text{in}}$. The resonant frequency w_r and the characteristic impedance Z_r can be expressed as

$$w_r = \frac{1}{\sqrt{L_r C_r}}, \quad Z_r = \sqrt{\frac{L_r}{C_r}}. \tag{5}$$

Mode 2 [t_1, t_2]: At time t_1, S_4 is turned OFF. The current on the secondary side then flows through D_{S3}. During this interval, the input voltage source, the resonant inductor, and the resonant capacitor form an equivalent closed circuit, and the resonant inductor current goes to zero, following the sinusoidal waveform. The state equation corresponding to this equivalent circuit can be written as

$$L_r \frac{di_{Lr}(t)}{dt} = nV_{\text{in}} - v_{Cr1}(t) \tag{6}$$

$$i_{Lr}(t) = C_r \frac{dv_{Cr1}(t)}{dt}. \tag{7}$$

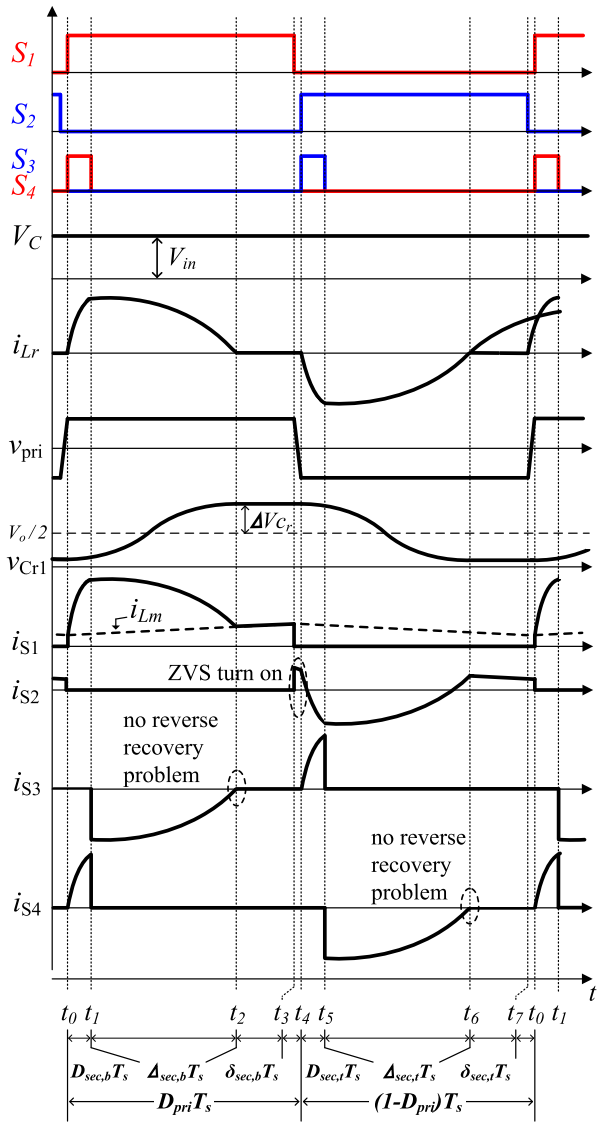

Fig. 4. Waveforms of the proposed converter. $S_{i'}$ is the gate-source voltage of the ith MOSFET.

Solving (6) and (7) yields

$$i_{Lr}(t) = \frac{1}{Z_r}(r_1 \sin[w_r(t-t_0)] - V_o \sin[w_r(t-t_1)]) \quad (8)$$

$$v_{Cr1}(t) = nV_{\text{in}} - r_1 \cos[w_r(t-t_0)] + V_o \cos[w_r(t-t_1)]. \quad (9)$$

Mode 3 [t_2, t_3]: At time t_2, the resonant inductor current is zero, v_{Cr1} is at its maximum, and v_{Cr2} is at its minimum. During this interval, the current that flows through S_1 is i_{Lm} reflected on the primary side. Thus, at time t_3, switch S_1 is turned OFF.

Mode 4 [t_3, t_4]: At time t_3, S_1 is turned OFF and enters the dead-time zone. During this time, i_{Lm} appears as a current source to the primary side, which charges C_{S1}, and at the same time discharges C_{S2} when i_{Lm} passes through D_{S2}. Thus, S_2 is turned ON with ZVS.

Mode 5 [t_4, t_5]: At time t_4, S_2 and S_3 are turned ON. Especially, S_2 is turned ON with ZVS because D_{S2} was conducting in the previous state. i_{Lr} begins to flow, and v_{Cr1} begins to decrease from its maximum value. During this interval, the resonant inductor, the active clamp, and the resonant capacitors form an equivalent closed circuit that boosts the resonant inductor current in the negative direction following the sinusoidal waveform. The state equation corresponding to this equivalent circuit can be written as

$$L_r \frac{di_{Lr}(t)}{dt} = -nV_C - v_{Cr1}(t) \quad (10)$$

$$i_{Lr}(t) = C_r \frac{dv_{Cr1}(t)}{dt} \quad (11)$$

with $i_{Lr}(t_4) = 0$ and $v_{Cr1}(t_4) = \frac{V_o}{2} + \Delta V_{Cr}$. Solving (10) and (11) yields

$$i_{Lr}(t) = -\frac{r_2}{Z_r} \sin[w_r(t-t_4)] \quad (12)$$

$$v_{Cr1}(t) = -nV_C + r_2 \cos[w_r(t-t_4)] \quad (13)$$

where $r_2 = \frac{V_o}{2} + \Delta V_{Cr} + nV_C$.

Mode 6 [t_5, t_6]: At time t_5, S_3 is turned OFF. The current on the secondary side then flows through D_{S4}. During this interval, the input voltage source, the resonant inductor, and the resonant capacitor form an equivalent closed circuit, and the resonant inductor current goes to zero following the sinusoidal waveform. The state equation that corresponds to this equivalent circuit can be written as

$$L_r \frac{di_{Lr}(t)}{dt} = -nV_C + V_o - v_{Cr1}(t) \quad (14)$$

$$i_{Lr}(t) = C_r \frac{dv_{Cr1}(t)}{dt}. \quad (15)$$

Solving (14) and (15) yields

$$i_{Lr}(t) = \frac{1}{Z_r}(r_2 \sin[w_r(t-t_4)] - V_o \sin[w_r(t-t_5)]) \quad (16)$$

$$v_{Cr1}(t) = -nV_C + V_o - r_2 \cos[w_r(t-t_4)] + V_o \cos[w_r(t-t_5)]. \quad (17)$$

Mode 7 [t_6, t_7]: At time t_6, the resonant inductor current is zero, v_{Cr1} is at its minimum, and v_{Cr2} is at its maximum. During this interval, the current that flows through S_2 is i_{Lm} reflected on the primary side. Thus, at time t_7, switch S_2 is turned OFF.

Mode 8 [t_7, t_8]: At time t_7, S_2 is turned OFF and enters the dead-time zone.

III. Steady-State Analysis

A. Calculating Average Capacitor Voltages V_C, V_{Cr1}, and V_{Cr2}

To simplify the steady-state analysis, we neglect the small dead-time segments [t_3, t_4] of mode 4 and [t_7, t_8] of mode 8. To obtain the average voltages of the clamp capacitor V_C, the resonant capacitors V_{Cr1} and V_{Cr2}, we first calculate the clamp

capacitor voltage in the steady state. Applying the voltage–second balance law to the magnetizing inductance as in [19] and [24] yields

$$nV_C(1-D_{\rm pri})T_s = nV_{\rm in}D_{\rm pri}T_s \tag{18}$$

$$\begin{aligned} nV_C(1-D_{\rm pri})T_s &= -\frac{L_m}{L_m+L_r}V_{Cr2}D_{{\rm sec},b}T_s \\ &\quad + \frac{L_m}{L_m+L_r}V_{Cr1}\Delta_{{\rm sec},b}T_s + nV_{\rm in}\delta_{{\rm sec},b}T_s \\ &= \frac{L_m}{L_m+L_r}(-V_{Cr2}D_{{\rm sec},b} + V_{Cr1}\Delta_{{\rm sec},b})T_s \\ &\quad + n\frac{1-D_{\rm pri}}{D_{\rm pri}}V_C\delta_{{\rm sec},b}T_s \end{aligned} \tag{19}$$

$$\begin{aligned} nV_{\rm in}D_{\rm pri}T_s &= -\frac{L_m}{L_m+L_r}V_{Cr1}D_{{\rm sec},t}T_s \\ &\quad + \frac{L_m}{L_m+L_r}V_{Cr2}\Delta_{{\rm sec},t}T_s + nV_C\delta_{{\rm sec},t}T_s \\ &= \frac{L_m}{L_m+L_r}(-V_{Cr1}D_{{\rm sec},t} + V_{Cr2}\Delta_{{\rm sec},t})T_s \\ &\quad + n\frac{D}{1-D}V_{\rm in}\delta_{{\rm sec},t}T_s \end{aligned} \tag{20}$$

where $D_{\rm pri} = D_{{\rm sec},b} + \Delta_{{\rm sec},b} + \delta_{{\rm sec},b}$ and $1 - D_{\rm pri} = D_{{\rm sec},t} + \Delta_{{\rm sec},t} + \delta_{{\rm sec},t}$ (see Fig. 4).

From (18), V_C is determined as

$$V_C = \frac{D_{\rm pri}}{1-D_{\rm pri}}V_{\rm in} \tag{21}$$

and rearranging (19) and (20) yields

$$\begin{aligned} &nV_C\frac{1-D_{\rm pri}}{D_{\rm pri}}(D_{{\rm sec},b}+\Delta_{{\rm sec},b})T_s \\ &= \frac{L_m}{L_m+L_r}(-(V_o - V_{Cr1})D_{{\rm sec},b} \\ &\quad + V_{Cr1}(D_{\rm pri} - D_{{\rm sec},b} - \delta_{{\rm sec},b}))T_s \\ &= \frac{L_m}{L_m+L_r}(V_{Cr1}(D_{{\rm sec},b}+\Delta_{{\rm sec},b}) - V_oD_{{\rm sec},b})T_s \end{aligned} \tag{22}$$

$$\begin{aligned} &nV_{\rm in}\frac{D_{\rm pri}}{1-D_{\rm pri}}(D_{{\rm sec},t}+\Delta_{{\rm sec},t})T_s \\ &= \frac{L_m}{L_m+L_r}(-(V_o - V_{Cr2})D_{{\rm sec},t} \\ &\quad + V_{Cr2}(1 - D_{\rm pri} - D_{{\rm sec},t} - \delta_{{\rm sec},t}))T_s \\ &= \frac{L_m}{L_m+L_r}(V_{Cr2}(D_{{\rm sec},t}+\Delta_{{\rm sec},t}) - V_oD_{{\rm sec},t})T_s. \end{aligned} \tag{23}$$

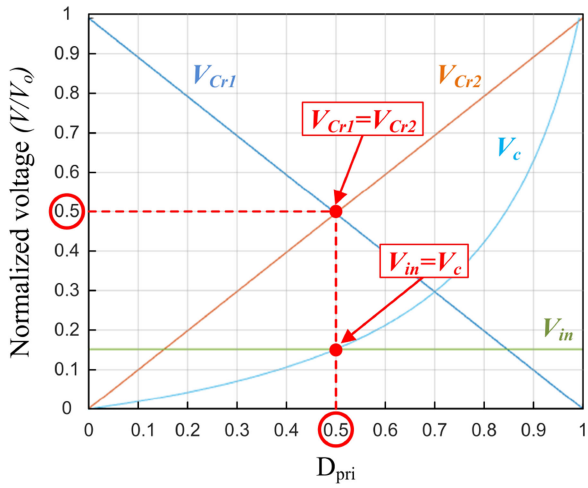

Fig. 5. $V_{\rm in}$, V_C and normalized v_{Cr1}, v_{Cr2} versus primary duty ratio $D_{\rm pri}$.

Substituting (21) into (22) and (23) and rearranging these equations for V_{Cr1} and V_{Cr2} yields

$$\begin{aligned} V_{Cr1} &= \frac{nV_{\rm in}(D_{{\rm sec},b}+\Delta_{{\rm sec},b})\frac{L_m+L_r}{L_m} + V_oD_{{\rm sec},b}}{D_{{\rm sec},b}+\Delta_{{\rm sec},b}} \\ &= nV_{\rm in}\frac{L_m+L_r}{L_m} + \frac{D_{{\rm sec},b}}{D_{{\rm sec},b}+\Delta_{{\rm sec},b}}V_o \end{aligned} \tag{24}$$

$$\begin{aligned} V_{Cr2} &= \frac{nV_C(D_{{\rm sec},t}+\Delta_{{\rm sec},t})\frac{L_m+L_r}{L_m} + V_oD_{{\rm sec},t}}{D_{{\rm sec},t}+\Delta_{{\rm sec},t}} \\ &= nV_C\frac{L_m+L_r}{L_m} + \frac{D_{{\rm sec},t}}{D_{{\rm sec},t}+\Delta_{{\rm sec},t}}V_o. \end{aligned} \tag{25}$$

As described in Fig. 5, the resonant capacitor voltages start to get unbalanced as the primary duty cycle deviates from 0.5. These voltages are even more unbalanced when the duty cycle becomes very high or low. But here, $D_{\rm pri}$ is set to 0.5, so $D_{\rm pri} = 1 - D_{\rm pri} = 0.5$ and $V_C = V_{\rm in}$ in (21). Therefore, V_{Cr1} and V_{Cr2} are equally balanced. $D_{{\rm sec},b}$ is usually set equal to $D_{{\rm sec},t}$, so $D_{{\rm sec},b} = D_{{\rm sec},t} = D_{\rm sec}$; therefore, $\Delta_{{\rm sec},b} = \Delta_{{\rm sec},t} = \Delta_{\rm sec}$ due to symmetric operation of the circuit during the first-half and the second-half periods. Thus, the resonant capacitor voltages are balanced.

B. Calculating Voltage Conversion Ratio

To determine the voltage gain of the proposed converter, we first compute the resonant capacitor voltage ripple ΔV_{Cr} and calculate $\Delta_{\rm sec}T_s$ in terms of $D_{\rm sec}T_s$, where $\Delta_{\rm sec}T_s$ is the time duration during which i_{Lr} falls to zero. By adding V_{Cr1} and V_{Cr2} and substituting $\Delta_{\rm sec}$ into the resulting equation, we then obtain the voltage gain of the proposed converter.

Due to symmetric operation of the voltage doubler in the steady state, the average value of the resonant inductor current

is twice the output current I_o, so

$$\begin{aligned}
I_o &= \frac{V_o}{R_o} = \frac{1}{T_s}\int_{t_0}^{T_s} I_o(\tau)d\tau = \frac{1}{T_s/2}\int_{t_0}^{T_s/2} I_o(\tau)d\tau \\
&= \frac{1}{T_s/2}\int_{t_0}^{T_s/2} \frac{I_{L_r}(\tau)}{2}d\tau = \frac{1}{T_s}\int_{t_0}^{T_s/2} I_{L_r}(\tau)d\tau \\
&= \frac{1}{T_s}\int_{t_0}^{t_1} \frac{r_1}{Z_r}\sin\left[w_r(\tau - t_0)\right]d\tau \\
&\quad + \frac{1}{T_s}\int_{t_1}^{t_2} \frac{r_1}{Z_r}\sin\left[w_r(\tau - t_0)\right]d\tau \\
&\quad + \frac{1}{T_s}\int_{t_1}^{t_2} \frac{V_o}{Z_r}\sin\left[w_r(\tau - t_1)\right]d\tau \\
&= \frac{1}{T_s Z_r}\int_{t_0}^{t_2} r_1\sin\left[w_r(\tau - t_0)\right]d\tau \\
&\quad - \frac{1}{T_s Z_r}\int_{t_1}^{t_2} V_o\sin\left[w_r(\tau - t_1)\right]d\tau \\
&= \frac{C_r}{T_s}\left[r_1(1-\cos\left[w_r(t_2-t_0)\right]) + V_o(\cos\left[w_r(t_2-t_1)\right]-1)\right] \\
&= \frac{C_r}{T_s}\left[r_1 - V_o - r\cos\left[w_r(t_2-t_0)\right] + V_o\cos\left[w_r(t_2-t_1)\right]\right] \\
&= \frac{C_r}{T_s}\left[r_1 - V_o + v_{Cr1}(t_2) - nV_{\text{in}}\right] \\
&= \frac{C_r}{T_s}\left[\frac{V_o}{2} + \Delta V_{Cr} + nV_{\text{in}} - V_o + \frac{V_o}{2} + \Delta V_{Cr} - nV_{\text{in}}\right] \\
&= \frac{2C_r}{T_s}\Delta V_{Cr}. \qquad (26)
\end{aligned}$$

Rearranging (26) for $2\Delta V_{Cr}$ yields

$$2\Delta V_{Cr} = \frac{V_o T_s}{R_o C_r} = \gamma V_o \qquad (27)$$

where $\gamma \triangleq \frac{T_s}{R_o C_r}$.

By using the facts that $i_{Lr}(t_2) = 0$ and $v_{Cr1}(t_2) = \frac{V_o}{2} + \Delta V_{Cr}$ at $t = t_2$, then (8) and (9) imply

$$r_1\sin\left[w_r(t_2 - t_0)\right] - V_o\sin\left[w_r(t_2 - t_1)\right] = 0 \qquad (28)$$

$$\begin{aligned}
&r_1\cos\left[w_r(t_2 - t_0)\right] - V_o\cos\left[w_r(t_2 - t_1)\right] \\
&\quad = nV_{\text{in}} - \left(\frac{V_o}{2} + \Delta V_{Cr}\right) = -r_3 \qquad (29)
\end{aligned}$$

where $r_3 = \frac{V_o}{2} + \Delta V_{Cr} - nV_{\text{in}}$. Squaring both sides of (28) and (29) and adding the resulting equations yields

$$\begin{aligned}
r_3^2 &= r_1^2 + V_o^2 - 2r_1V_o(\cos\left[w_r(t_2 - t_0)\right]\cos\left[w_r(t_2 - t_1)\right] \\
&\quad + \sin\left[w_r(t_2 - t_0)\right]\sin\left[w_r(t_2 - t_1)\right]) \\
&= r_1^2 + V_o^2 - 2r_1V_o\cos\left[w_r(t_1 - t_0)\right]. \qquad (30)
\end{aligned}$$

Defining $M \triangleq \frac{V_o}{2nV_{\text{in}}}$, $A \triangleq \gamma + 1$, and rearranging (30) yields

$$\begin{aligned}
\cos\left[w_r(t_1 - t_0)\right] &= \frac{r_1^2 + V_o^2 - r_2^2}{2rV_o} \\
&= \frac{2nV_{\text{in}}(V_o + 2\Delta V_{Cr}) + V_o^2}{V_o(V_o + 2\Delta V_{Cr} + 2nV_{\text{in}})} \\
&= \frac{2nV_{\text{in}}(V_o + \gamma V_o) + V_o^2}{V_o(V_o + \gamma V_o + 2nV_{\text{in}})} \\
&= \frac{M + 1 + \gamma}{M + 1 + \gamma M} = \frac{M + A}{MA + 1}. \qquad (31)
\end{aligned}$$

Next, moving $V_o\sin\left[w_r(t_2 - t_1)\right]$ and $V_o\cos\left[w_r(t_2 - t_1)\right]$ terms to the right-hand side of (28) and (29), squaring both sides of equations, and adding the resulting equations yields

$$r_1^2 = V_o^2 + r_3^2 - 2V_o r_3\cos\left[w_r(t_2 - t_1)\right] \qquad (32)$$

and rearranging (32) yields

$$\begin{aligned}
\cos\left[w_r(t_2 - t_1)\right] &= \frac{V_o^2 + r_3^2 - r_1^2}{2V_o r_3} \\
&= \frac{M - A}{MA - 1}. \qquad (33)
\end{aligned}$$

From (31) and (33), M is derived as

$$M = \frac{A - \cos\left[w_r(t_1 - t_0)\right]}{A\cos\left[w_r(t_1 - t_0)\right] - 1} = \frac{A - \cos\left[w_r(t_2 - t_1)\right]}{1 - A\cos\left[w_r(t_2 - t_1)\right]}. \qquad (34)$$

Because $t_1 - t_0 = D_{\text{sec}}T_s$ and $t_2 - t_1 = \Delta_{\text{sec}}T_s$ in (34), then

$$\Delta_{\text{sec}}T_s = \frac{1}{w_r}\cos^{-1}\left(\frac{-(A^2+1)\cos\left(w_r D_{\text{sec}}T_s\right) + 2A}{A^2 + 1 - 2A\cos\left(w_r D_{\text{sec}}T_s\right)}\right). \qquad (35)$$

Due to the symmetric operation property of the proposed circuit, $V_{Cr1} = V_{Cr2}$, as in (24) and (25). The output voltage V_o then becomes

$$\begin{aligned}
V_o = V_{Cr1} + V_{Cr2} = 2V_{Cr1} &= 2nV_{\text{in}}\frac{L_m + L_r}{L_m} \\
&\quad + \frac{2D_{\text{sec}}}{D_{\text{sec}} + \Delta_{\text{sec}}}V_o. \qquad (36)
\end{aligned}$$

Rearranging (36) gives

$$M = \frac{V_o}{2nV_{\text{in}}} = \frac{L_m + L_r}{L_m}\cdot\frac{\Delta_{\text{sec}} + D_{\text{sec}}}{\Delta_{\text{sec}} - D_{\text{sec}}} \qquad (37)$$

and substituting (35) into (37) yields

$$\begin{aligned}
M = \frac{V_o}{2nV_{\text{in}}} &= \frac{L_m + L_r}{L_m} \\
&\cdot \frac{\cos^{-1}\left(\frac{-(A^2+1)\cos\left(w_r D_{\text{sec}}T_s\right)+2A}{A^2+1-2A\cos\left(w_r D_{\text{sec}}T_s\right)}\right) + w_r D_{\text{sec}}T_s}{\cos^{-1}\left(\frac{-(A^2+1)\cos\left(w_r D_{\text{sec}}T_s\right)+2A}{A^2+1-2A\cos\left(w_r D_{\text{sec}}T_s\right)}\right) - w_r D_{\text{sec}}T_s}. \qquad (38)
\end{aligned}$$

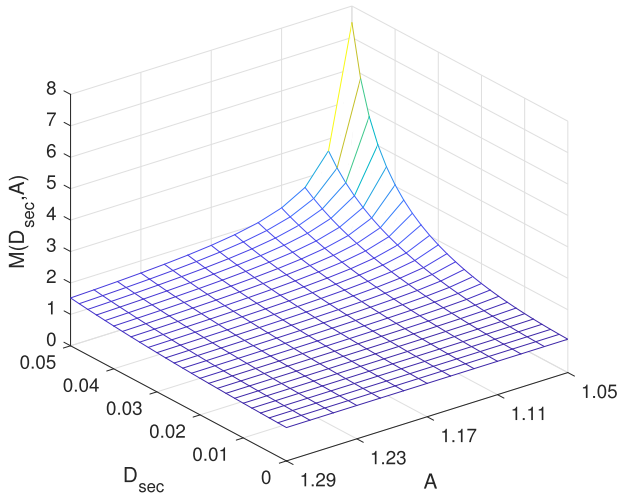

Fig. 6. 3-D graph of M versus $D_{\rm sec}$ and A.

A three-dimensional (3-D) graph of M with respect to A and $D_{\rm sec}$ is shown in Fig. 6. M reaches its minimum at 1 when $D_{\rm sec}$ is 0 and increases as $D_{\rm sec}$ increases.

IV. Design Guideline

The key design parameters of the proposed converter are the resonant capacitance and inductance, the transformer turns ratio, and the switch rating. We now introduce the design guideline of these parameters.

A. Resonant Capacitance and Resonant Inductance

To guarantee proper operation of the converter, we must choose C_r that satisfies

$$\Delta V_{Cr} \le V_{Cr}/2 = V_o/4. \tag{39}$$

Substituting (27) into (39) yields

$$C_r \ge \frac{2T_s}{R_o}. \tag{40}$$

Next, achieving zero-current turn-OFF switching of the diodes requires

$$D_{\rm sec}T_s + \Delta_{\rm sec}T_s < \frac{1}{2}T_s. \tag{41}$$

Multiplying w_r and taking the cosine on both sides of (41) yields

$$\begin{aligned}&\cos\left(D_{\rm sec}T_s w_r + \Delta_{\rm sec}T_s w_r\right) > \cos\left(\frac{1}{2}T_s w_r\right)\\ &\quad \text{if} \quad \frac{1}{2}T_s w_r < \pi\\ &\cos\left(D_{\rm sec}T_s w_r + \Delta_{\rm sec}T_s w_r\right) < \cos\left(\frac{1}{2}T_s w_r\right)\\ &\quad \text{if} \quad \frac{1}{2}T_s w_r > \pi.\end{aligned} \tag{42}$$

TABLE I
Parameters and Components of the Prototype

Parameters	Symbols	Value
Input voltage range	V_{in}	40 – 50 V
Nominal input voltage	V_{in_nom}	45 V
Output voltage	V_o	380 V
Output power	P_o	400 W
Switching frequency	f_s	50 kHz
Resonant frequency	f_r	42.73 kHz
Transformer turns ratio	N_p:N_s	10:38
Magnetizing inductance	L_m	1.127 mH
Resonant inductance	L_r	69.38 μH
Resonant capacitance	C_{r1}, C_{r2}	100 nF
Input capacitance	C_{in}	560 μF
Clamp capacitance	C_c	10 μF
Output capacitance	C_o	20 μF
Components	**Symbols**	**Part number**
Primary-side switches	S_1, S_2	IPP051N15N5
Secondary-side switches	S_3, S_4	UJC06505K
Transformer core	T	PQ4040

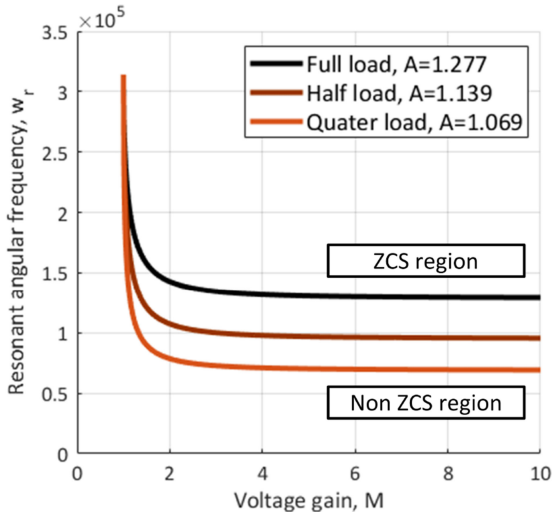

Fig. 7. Region for ZCS diode turn-OFF of S_3 and S_4.

Applying the cosine angle sum formula yields

$$\begin{aligned}&\cos\left(D_{\rm sec}T_s w_r + \Delta_{\rm sec}T_s w_r\right)\\ &\quad = \cos\left(D_{\rm sec}T_s w_r\right)\cos\left(\Delta_{\rm sec}T_s w_r\right)\\ &\qquad - \sin\left(D_{\rm sec}T_s w_r\right)\sin\left(\Delta_{\rm sec}T_s w_r\right)\\ &\quad = \frac{M+A}{MA+1}\cdot\frac{M-A}{MA-1}\\ &\qquad + \frac{\sqrt{(A-1)(A+1)(M-1)(M+1)}}{MA+1}\\ &\qquad \cdot\frac{\sqrt{(A-1)(A+1)(M-1)(M+1)}}{MA-1}\\ &\quad = \frac{2M^2 - M^2A^2 - 1}{M^2A^2 - 1}.\end{aligned} \tag{43}$$

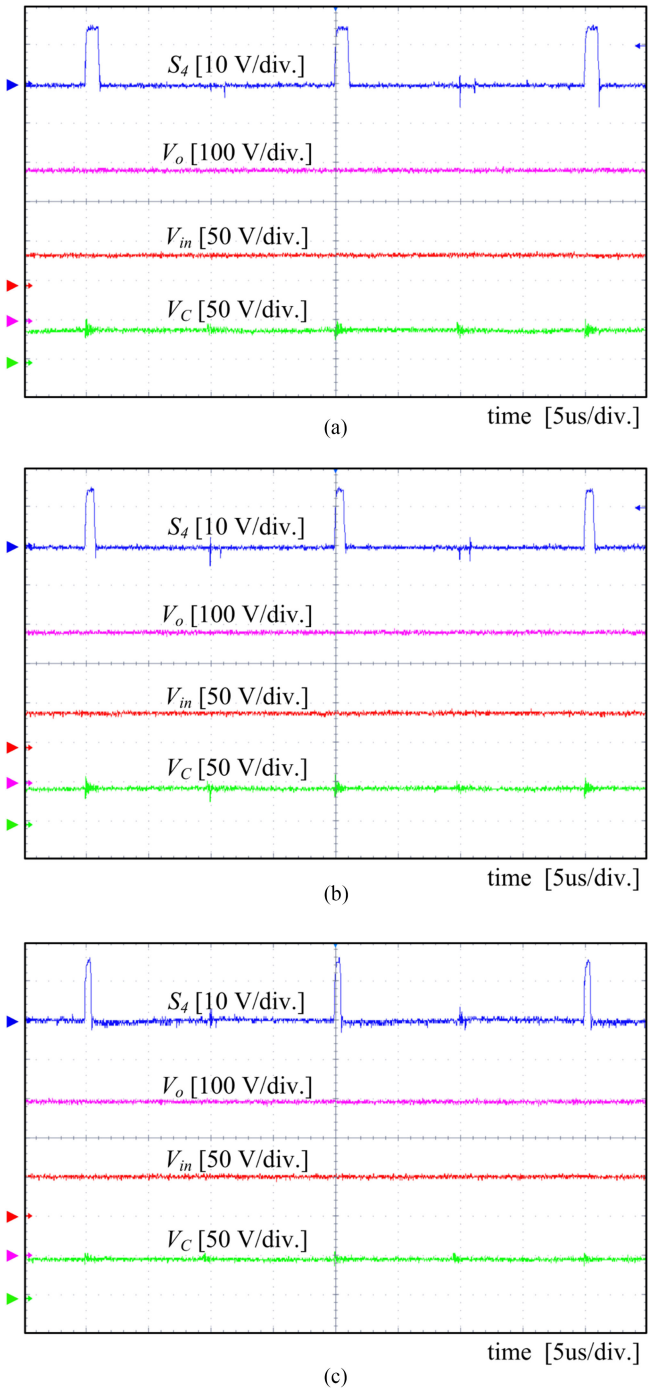

Fig. 8. Experimental waveforms of S_4, V_o, $V_{\rm in}$, and V_C at full load. (a) $V_{\rm in} = 40$ V. (b) $V_{\rm in} = 45$ V. (c) $V_{\rm in} = 50$ V.

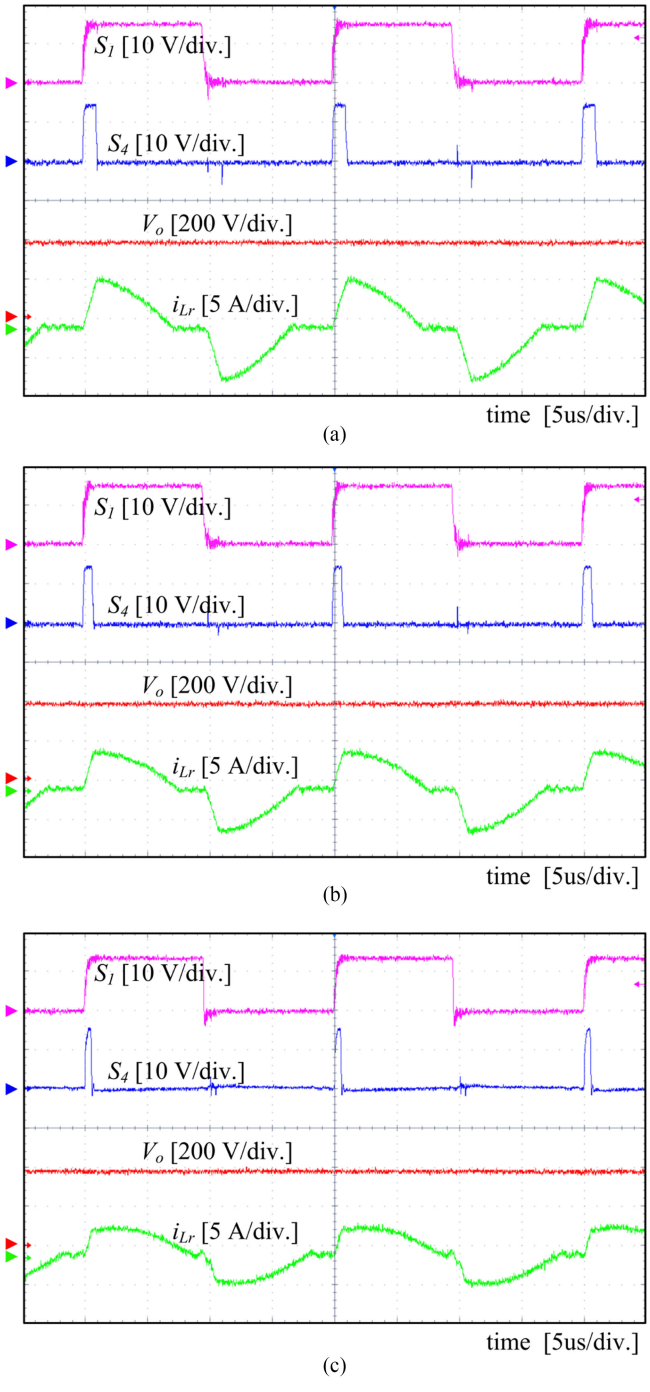

Fig. 9. Experimental waveforms of S_1, S_4, V_o, and i_{Lr} at full load. (a) $V_{\rm in} = 40$ V. (b) $V_{\rm in} = 45$ V. (c) $V_{\rm in} = 50$ V.

Substituting (43) into (42) yields

$$\begin{aligned} \frac{2M^2 - M^2A^2 - 1}{M^2A^2 - 1} &> \cos\left(\frac{1}{2}T_s w_r\right), \quad \text{if} \quad \frac{1}{2}T_s w_r < \pi \\ \frac{2M^2 - M^2A^2 - 1}{M^2A^2 - 1} &< \cos\left(\frac{1}{2}T_s w_r\right), \quad \text{if} \quad \frac{1}{2}T_s w_r > \pi \end{aligned} \tag{44}$$

and rearranging (44) results in

$$w_r > \frac{2}{T_s}\cos^{-1}\left(\frac{2M^2 - M^2A^2 - 1}{M^2A^2 - 1}\right). \tag{45}$$

Applying the parameters (see Table I) to (45), we can determine the region that guarantees ZCS diode turn-OFF of the S_3 and S_4 (see Fig. 7). The right-hand side of (45) decreases as the voltage gain increases. Consequently, if w_r satisfies (45) even when M is at its minimum 1 ($M = M_{\rm min} = 1$), ZCS turn-OFF

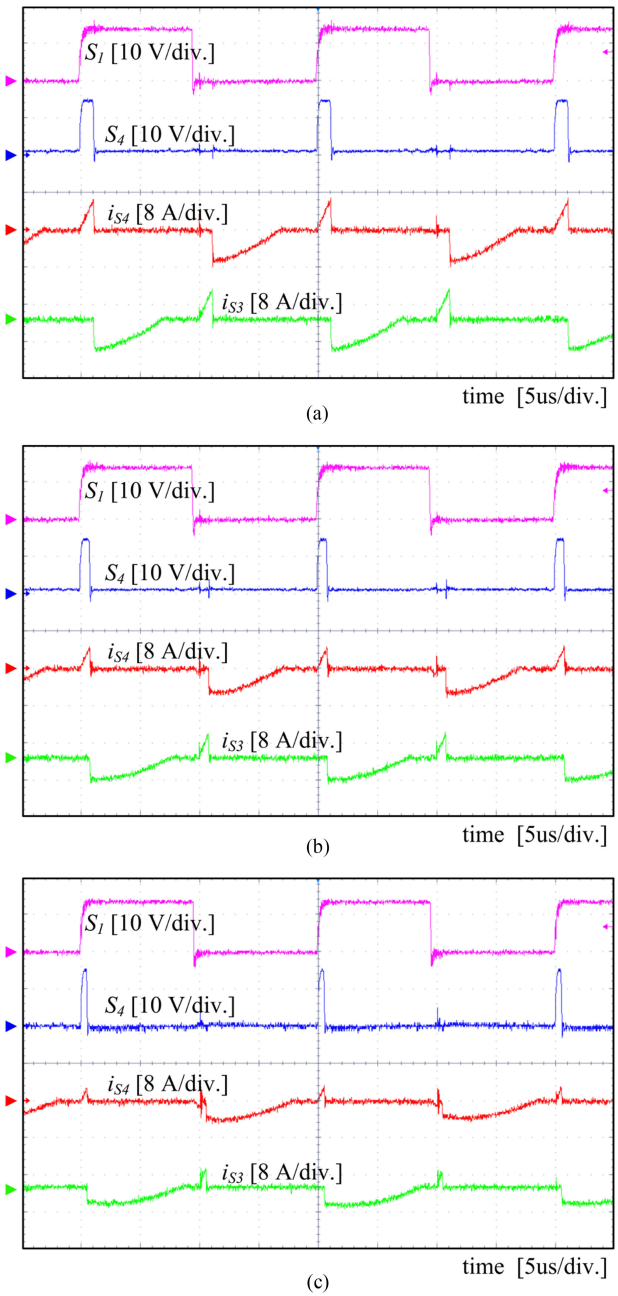

Fig. 10. Experimental waveforms of S_1, S_4, i_{S3}, and i_{S4} at full load. (a) $V_{\text{in}} = 40$ V. (b) $V_{\text{in}} = 45$ V. (c) $V_{\text{in}} = 50$ V.

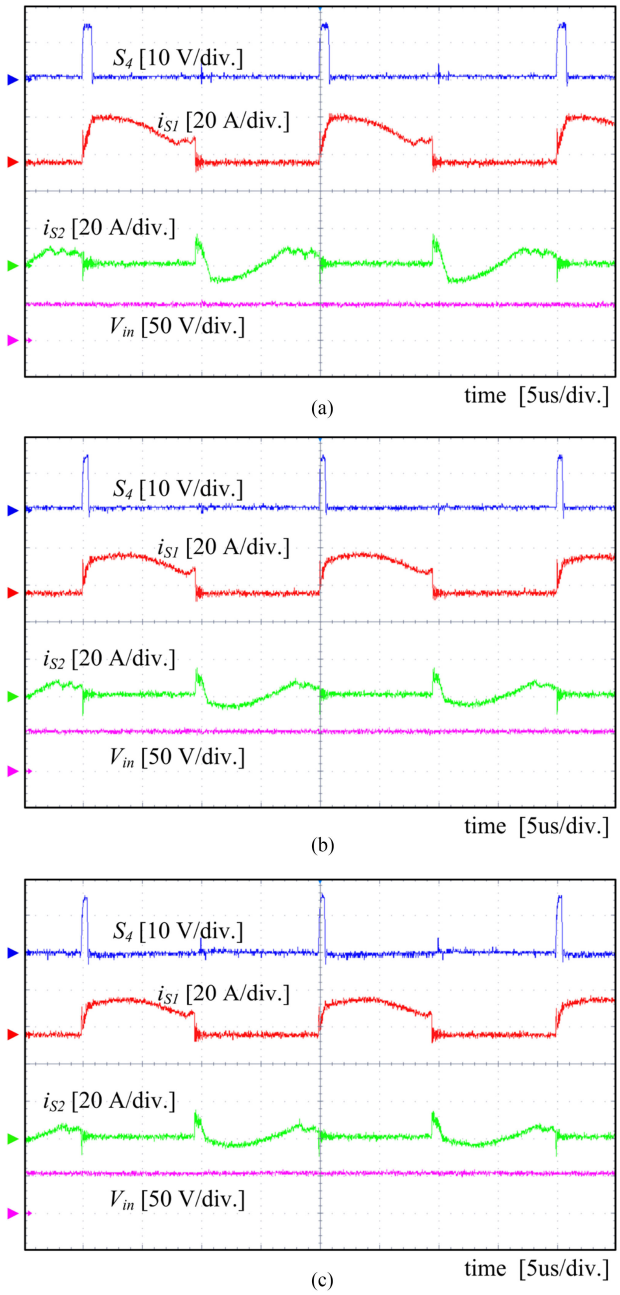

Fig. 11. Experimental waveforms of S_4, i_{S1}, i_{S2}, and V_{in} at full load. (a) $V_{\text{in}} = 40$ V. (b) $V_{\text{in}} = 45$ V. (c) $V_{\text{in}} = 50$ V.

of the diodes is guaranteed. Equation (45) then becomes

$$w_r > \frac{2\pi}{T_s} \tag{46}$$

and we can determine L_r from (5) and (46) as

$$L_r \leq \frac{T_s^2}{4\pi^2 C_r}. \tag{47}$$

L_r must satisfy (47), but at the same time, should be selected as large as possible to keep the peak of i_{Lr} as small as possible during the boost mode. If the peak of i_{Lr} is too large, S_3 and S_4 incur turn-OFF losses, so the power conversion efficiency decreases.

B. Transformer Turns Ratio

The turns ratio of the transformer ($n = N_s/N_p$) can be selected from the voltage gain of the proposed converter. Rearranging (38) yields

$$n \leq \frac{V_o}{2 \cdot M_{\min} \cdot V_{\text{in\_max}}} = \frac{V_o}{2V_{\text{in\_max}}} \tag{48}$$

where $M_{\min} = 1$ is the minimum value of M.

C. Selection of S_1, S_2

The voltage stresses are exerted on switches S_1 and S_2; these values are the maximum values of V_{S1} and V_{S2}, and are equal

to the sum of input voltage $V_{\rm in}$ and clamp capacitor voltage V_C

$$V_{S1,\max} = V_{S2,\max} = V_{\rm in} + V_C = \frac{V_{\rm in}}{1 - D_{\rm pri}}. \quad (49)$$

Because the duty ratios are the same for the primary-side switches, both of the primary-side switch S_1 and S_2 have the same voltage stress as $2V_{\rm in}$.

Also, the sum of the average current of S_1 and S_2 is equal to the average input current $I_{\rm in,av}$

$$i_{S1,\rm av} = i_{S2,\rm av} = I_{\rm in,av} \approx \frac{2nM}{\eta} I_o \quad (50)$$

where η is the power conversion efficiency. The peak value of the switch currents is equal to that of the primary currents, which can be approximated as

$$i_{S1,\max} = i_{S2,\max} \approx n i_{Lr}(t_1) = \frac{nr_1}{Z_r} \sin\left[w_r(t_1 - t_0)\right]. \quad (51)$$

D. Selection of S_3, S_4

The voltage stresses exerted on switches S_3 and S_4 are equal to the difference between V_{Cr1} and transformer secondary voltage $V_{\rm sec}$

$$\begin{aligned} V_{S3,\max} &= V_{S4,\max} = v_{Cr1}(t_4) - v_{\rm sec}(t_4) \\ &= nV_{\rm in} - r_1 \cos\left[w_r(t_4 - t_0)\right] + V_o \cos\left[w_r(t_4 - t_1)\right] + nV_C \\ &= 2nV_{\rm in} - r_1 \cos\left[w_r(t_4 - t_0)\right] + V_o \cos\left[w_r(t_4 - t_1)\right]. \end{aligned} \quad (52)$$

The peak value of the switch currents is equal to that of the secondary currents, which can be expressed as

$$i_{S3,\max} = i_{S4,\max} \approx i_{Lr}(t_1) = \frac{r_1}{Z_r} \sin\left[w_r(t_1 - t_0)\right]. \quad (53)$$

V. Experimental Results and Discussions

To evaluate the performance of the proposed converter, we conducted experimental tests using a 400-W prototype converter (see Table I) with input voltage $V_{\rm in} = 40$–50 V; output voltage $V_o = 380$ V; rated output power $P_o = 400$ W. The digital control algorithm is implemented using a TMS320F28377D microcontroller. The resonant capacitor and resonant inductor were selected as $C_{r1} = C_{r2} = 100$ nF, and $L_r = 69.38$ μH to guarantee ZCS resonant operation for S_3, S_4.

The waveforms (see Fig. 8) of S_4, V_o, $V_{\rm in}$, and V_C show the clamp capacitor voltage variation as the input voltage varies. The clamp capacitor voltage is almost the same as the input voltage. The waveforms (see Fig. 9) of S_1, S_4, V_o, and i_{Lr} show the onset of resonance as the secondary switch is turned ON. When the secondary switch is turned ON, L_r is charged and i_{Lr} increases almost linearly. When the secondary switch is turned OFF, L_r is discharged and i_{Lr} decreases in a sinusoidal way. The resonance ends when $i_{Lr} = 0$. The waveforms (see Fig. 10) of S_1, S_4, i_{S3}, and i_{S4} show that when the secondary switch is turned ON, the current flows through S_3 and S_4. When the secondary switch is turned OFF, the current begins to flow through D_{S3} and D_{S4}, and D_{S3} and D_{S4} get turned OFF at zero current, so the reverse-recovery problem does not occur. The waveforms (see Fig. 11) of S_4, i_{S1}, i_{S2}, and $V_{\rm in}$ show that

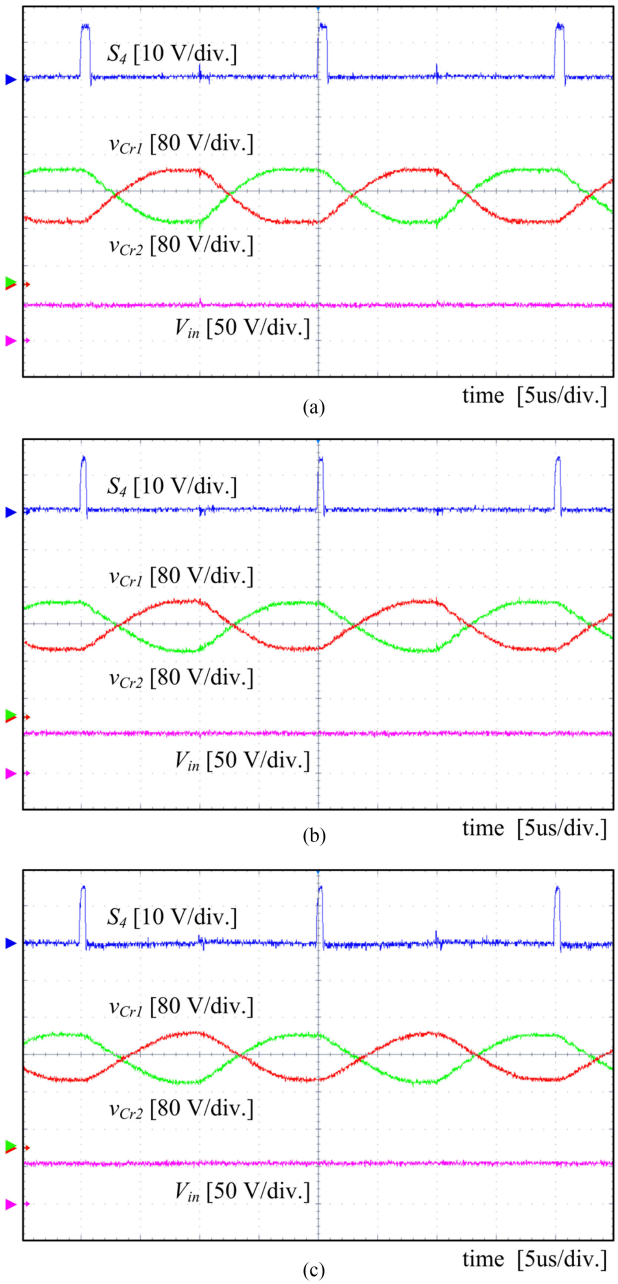

Fig. 12. Experimental waveforms of S_4, v_{Cr1}, v_{Cr2}, and $V_{\rm in}$ at full load. (a) $V_{\rm in} = 40$ V. (b) $V_{\rm in} = 45$ V. (c) $V_{\rm in} = 50$ V.

i_{S2} becomes negative when the primary switch is turned OFF, so ZVS of the clamp switches is achieved. The waveforms (see Fig. 12) of S_4, v_{Cr1}, v_{Cr2}, and $V_{\rm in}$ show that because $D_{\rm pri}$ is set to 0.5, $V_C = V_{\rm in}$, so the voltage balance of v_{Cr1} and v_{Cr2} is achieved.

We compared the calculated voltage gain and the experimental voltage gain (see Fig. 13). Theoretically, the clamp capacitor voltage V_C should be equal to $V_{\rm in}$, but it is slightly smaller than $V_{\rm in}$ due to the parasitic resistances on the primary side. Also, the resulting experimental output voltage is slightly smaller than the calculated voltage gain because of the parasitic resistances of the circuit. Even though there is a slight difference, in

TABLE II
COMPARISON OF THE PROPOSED CONVERTER TO OTHER CONVERTERS

Items		[18]	[19]	[20]	[21]	Proposed converter
Topology		Flyback + active clamp	Dual resonant + active clamp	Dual resonant + active clamp + coupled inductor	Dual resonant + active clamp + two transfor -mers	Dual resonant + active clamp + active volta -ge doubler
Operation modes		Buck-boost	Boost	Boost	Boost	Boost
Number of compo -nents	Switches	3	2	2	2	4
	Diodes	0	2	2	2	0
	Capacitors	1	3	3	4	3
	Transformer winding	2	2	4	4	2
Voltage gain		$\frac{nD}{1-D}$	$\frac{n}{1-D}$	$\frac{n(1+n)}{1-D}$	$\frac{n}{1-D}$	$2nM$
Peak efficiency		94.5 %	96.1 %	$\simeq$ 93.0 %	91.7 %	96.97 %
Rated power		45 W	400 W	400 W	400 W	400 W
Cost		Low	Medium	Medium	Medium	Medium
Circuit design		Simple	Medium	Complex	Complex	Medium
Voltage balancing ($V_{in} \neq V_{in\_nom}$)		-	Unbalanced	Unbalanced	Unbalanced	Balanced

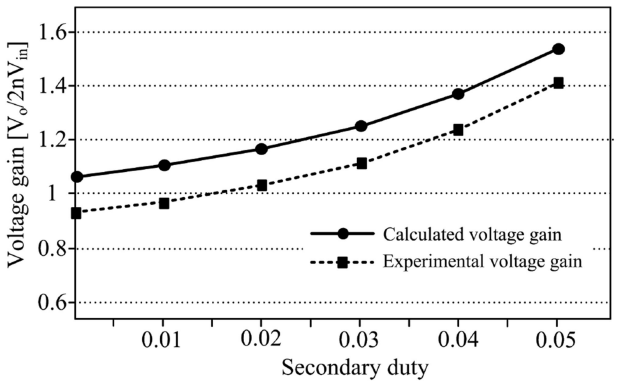

Fig. 13. Comparison between the calculated and experimental voltage gains.

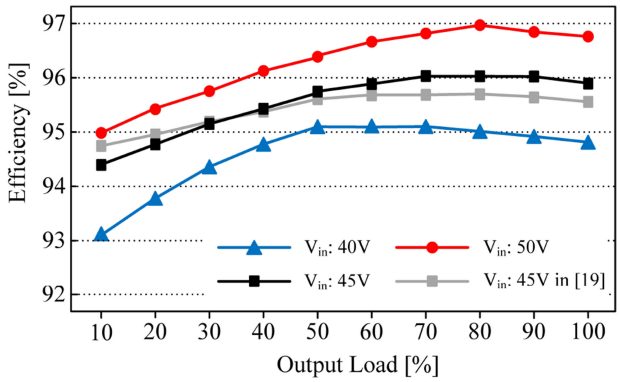

Fig. 14. Measured power conversion efficiency curve of the proposed converter and [19] with respect to the output load.

agreement with the calculated voltage gain, the similar tendency is observed in the measured voltage gain.

Power conversion efficiency was measured using a Yokogawa WT330 digital power meter at input voltages of 40, 45, and 50 V (see Fig. 14). The proposed converter achieved the maximum efficiency of 96.97% and the California Energy Commission weighted efficiency of 95.70% under nominal input voltage 45 V. Measured efficiency of [19] is less than that of the proposed one at the heavy load. But the measured efficiency of [19] becomes higher than that of the proposed one at the light load because the reverse recovery does not largely occur at the light load in [19]. Fig. 15 shows the power loss distribution of the proposed converter at full load. From Fig. 15, the primary switch loss takes 30.99% and the secondary switch loss takes 37.28% of the total power loss.

We then compared the complexity and electrical characteristics of different resonant converters (see Table II). The converter introduced in [18] adopted the secondary-side resonance

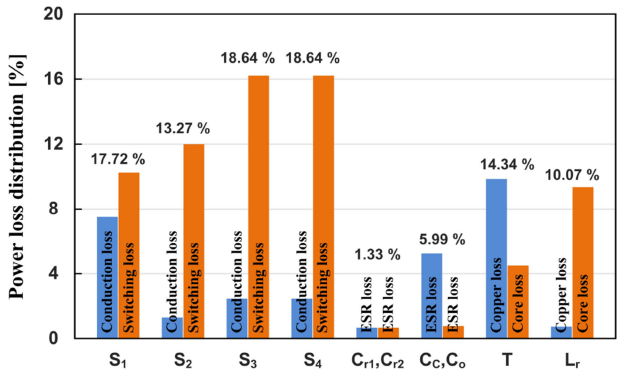

Fig. 15. Power loss distribution in the proposed converter at full load.

scheme on the active-clamp flyback converter to reduce root-mean-square current values and improve the performance of the synchronous rectifier operation. Xue and Zhang [18] use fewer semiconductor devices, than the proposed device, but

power transfer is activated only when the main switch is turned OFF. The dual series-resonant converter in [19] requires fewer switching components than the proposed converter, but voltage step-up capability is limited and the resonant capacitor voltages are not in balance. Compared with [20] and [21], the proposed converter requires fewer passive components, achieves higher voltage gain, and attains voltage balance of the resonant capacitors.

VI. Conclusion

This paper presented a high step-up resonant dc–dc converter that achieves capacitor voltage balance for distributed generation systems. By using a switching operation on the secondary side, the proposed converter achieved high step-up voltage gain with the minimum number of devices. A series-resonant circuit at the secondary side reduced switching losses considerably, thereby attaining the high power conversion efficiency over the entire range of operation. Furthermore, the duty cycle of the primary-side switches is fixed at 0.5, so the voltages of the resonant capacitors are well balanced. A comprehensive analysis of the converter operation is presented along with detailed practical design guidelines. To confirm the validity of the proposed converter, a 400-W prototype converter was built and used for experiments. In the designated operation range, it achieved 96.97% peak efficiency.

Acknowledgment

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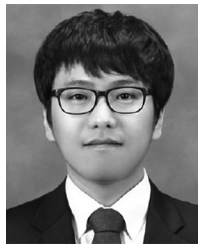

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