Fully Integrated Low-Power Energy Harvesting System With Simplified Ripple Correlation Control for System-on-a-Chip Applications

Minseob Shim, *Student Member, IEEE*, Junwon Jeong, *Student Member, IEEE*, Junyoung Maeng, *Student Member, IEEE*, Inho Park, *Student Member, IEEE*, and Chulwoo Kim, *Senior Member, IEEE*

***Abstract*—This paper presents a fully integrated energy harvesting (EH) system that even includes an input capacitor and a simplified ripple correlation control (RCC) maximum power point tracking (MPPT) method for low-power system-on-a-chip applications. The proposed system implements the RCC block with a charge pump (CP) that can be integrated into the chip, instead of the inductive switching converter that is commonly used for conventional RCC methods. The CP changes the input impedance by changing the size of the flying capacitor to ensure system reliability. The simplified RCC method is implemented using a low-power analog divider operated in a subthreshold region. A test chip fabricated in a 180 nm CMOS process achieves over 95% MPPT accuracy with a very small input capacitor of 5 nF and a low quiescent current of 2.6 μA. The chip size of the entire system is 8 mm^2, and the harvested power range is from 6 μW to 1.4 mW.**

***Index Terms*—Energy harvesting (EH), fully integrated, low power, maximum power point tracking (MPPT), photovoltaic (PV) cells, ripple correlation control (RCC).**

I. Introduction

SMALL, battery-operated devices such as wearable devices, wireless sensor nodes for Internet-of-Things, mobile devices, and implantable bio-devices can benefit significantly from energy harvesting (EH) as batteries do not need to be replaced as often. Photovoltaic (PV) cells are widely used in energy harvesting systems because they can easily generate the electrical power from various light sources, and many types of PV cells fulfill application demands or environmental conditions by changing the cell structure or using different elements such as mono/polycrystalline [1], [2], thin film [3]–[5], III–V [6], amorphous [7], [8], or perovskite [9]. Each PV cell has a high-power conversion efficiency that can reduce the cell area and weight or

Manuscript received April 1, 2018; accepted July 24, 2018. Date of publication August 5, 2018; date of current version March 29, 2019. This work was supported by the National Research Foundation of Korea through the Korean Government within the Ministry of Science, ICT and Future Planning under Grant 2016R1E1A1A02922127. Recommended for publication by Associate Editor P. S. Shenoy. *(Corresponding author: Chulwoo Kim.)*

The authors are with the Department of Electrical Engineering, Korea University, Seoul 02841, South Korea (e-mail:

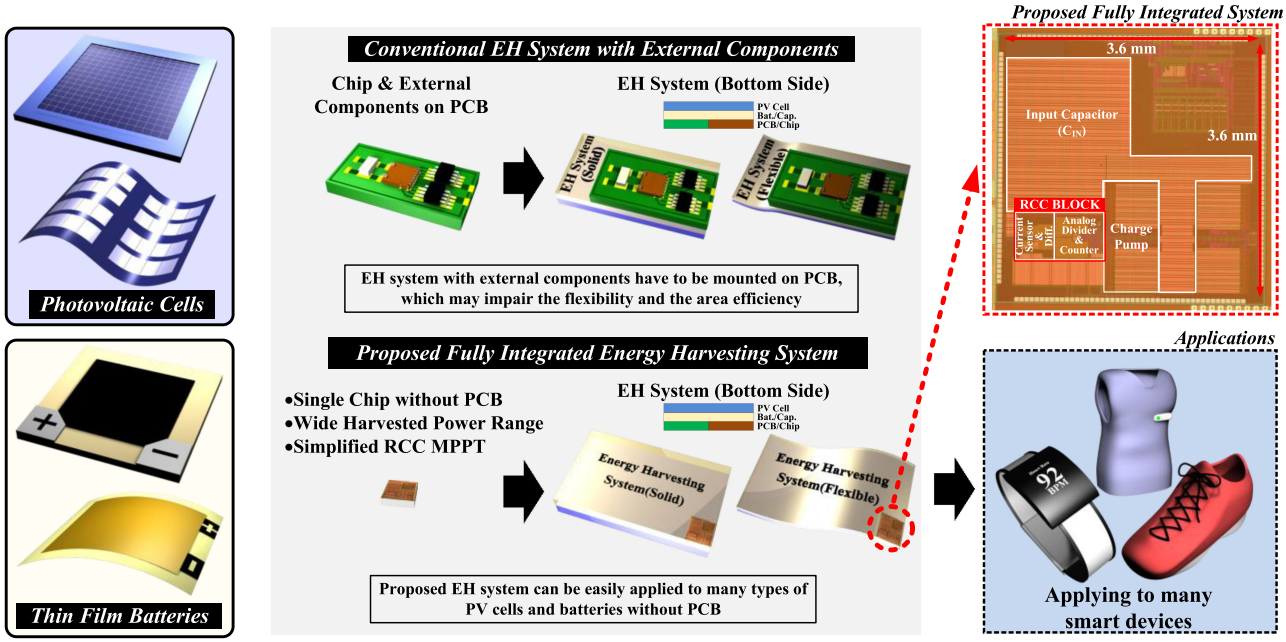


Fig. 1. Advantages of the fully integrated system that can improve the utility of many applications. (a) PV cells and thin film batteries/capacitor of the solid and flexible types. (b) Comparison of the EH system with external components and the fully integrated EH system. (c) Fabricated chip of the fully integrated EH system with a simplified RCC MPPT method and many smart devices, which can apply the fully integrated EH system.

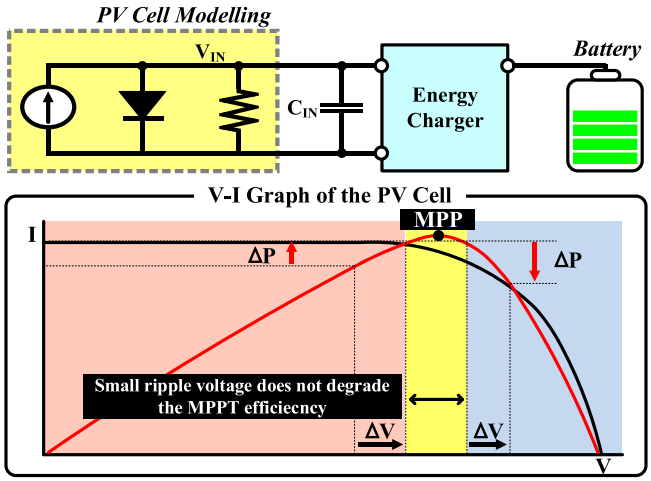


Fig. 2. Maximum power point of the photovoltaic cell.

external components such as a current sensor, passive components, and amplifiers. Additionally, RCC methods are commonly implemented in the switching converter with a bulky inductor to cover a large input power over a few watts, and because they utilize an analog multiplier [27], [28], which has a complex structure, it is not suitable for low-power systems. To address this problem, the proposed system not only fully integrates the entire system into a single chip with 3.6 mm × 3.6 mm size by applying the RCC method to the charge pump (CP)—which can cover a wide harvested power range from 6 μW to 1.4 mW instead of inductive switching converter—but also maximizes the power extraction from the PV cell using a simple algorithm and low-power consumption.

This paper is organized as follows. Section II describes the simplified RCC method using a low-power analog divider, and the impedance matching of the CP is presented after explaining the conventional RCC method. Section III presents measurement results and comparison tables obtained from conventional RCC methods and other low-power energy harvesting systems to show that the RCC system is suitable for low-power applications. The paper is concluded in Section IV.

II. Fully Integrated Energy Harvesting System With a Simplified RCC Method

A. Conventional RCC Method for MPPT

Fig. 3 shows the principle of the RCC method. The RCC uses the time derivative of the voltage between the harvester output and a battery charger ($V_{\rm IN}$) and the power graph ($P_{\rm IN}$) to calculate the MPP. It compares the time derivatives of $V_{\rm IN}$ and $P_{\rm IN}$ ($\dot{V}_{\rm IN}$ and $\dot{P}_{\rm IN}$) such that when $\dot{V}_{\rm IN}$ and $\dot{P}_{\rm IN}$ have different polarities, $V_{\rm IN}$ is higher than the MPP voltage ($V_{\rm MPP}$); otherwise, $V_{\rm IN}$ is lower than $V_{\rm MPP}$. The relationship between $V_{\rm IN}$ and $P_{\rm IN}$ can be expressed as follows:

$$\left.\begin{array}{ll} \dot{V}_{\rm IN} \times \dot{P}_{\rm IN} = & \\ \dot{V}_{\rm IN} \times (\dot{V}_{\rm IN} \times I_{\rm IN} + V_{\rm IN} \times \dot{I}_{\rm IN}) > 0, & V_{\rm IN} < V_{\rm MPP} \\ \dot{V}_{\rm IN} \times (\dot{V}_{\rm IN} \times I_{\rm IN} + V_{\rm IN} \times \dot{I}_{\rm IN}) < 0, & V_{\rm IN} > V_{\rm MPP} \end{array}\right\}. \quad (1)$$

From these simple equations, the RCC method can calculate the actual MPP value, which requires only the present battery charger input voltage and current. Therefore, it does not require any stored or preprogrammed values. To calculate the MPP,

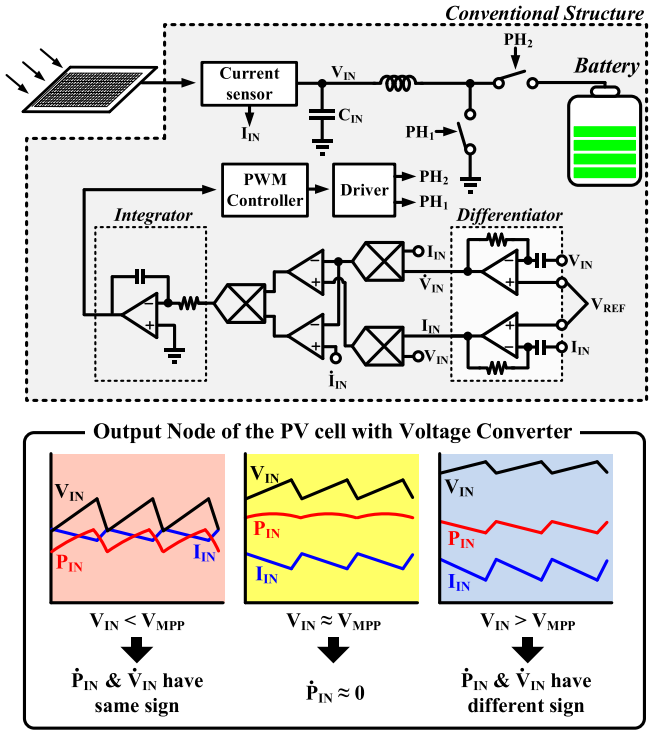


Fig. 3. Conventional structure and principle of the ripple correlation control MPPT method.

two differentiators and three multipliers are needed. The four-quadrant analog multiplier [27] or analog multiplier with some amplifiers [28] is commonly used. However, the four-quadrant analog multiplier requires many MOSFET stacks for each current path, and the amplifier-based analog multiplier has a complex structure with many components. Therefore, it can comprise a large portion of the total power dissipation of the harvesting system by reducing the area efficiency and the input voltage range.

B. Structure and Principle of the Proposed Fully Integrated EH System With Simplified RCC

Fig. 4 shows the overall architecture of the fully integrated energy harvesting system with the simplified RCC method. The proposed system integrates not only all control blocks for battery charging but also the input capacitor C_{IN}. The PV cell of the indoor target generates tens of μW to a few mW. Therefore, on-chip capacitors with nF sizes can be used, and it suppresses the ripple voltage under 10% of the input voltage with a switching frequency in the hundreds of kHz and increases the MPPT speed because of the small size of the input capacitor. Therefore, the fully integrated energy harvesting system, incorporating the integration of the input capacitor, reduces the design cost and increases the area efficiency.

The proposed system uses the CP instead of the inductive switching converter, which is commonly used for the conventional RCC method because it can be easily implemented in the chip. The time interval of the discharging phase is very short; therefore, the proposed RCC method senses the V_{IN} and I_{IN} values during the charging phase. In this case, the time derivative of V_{IN} ($\dot{V}_{IN}$) always has a positive sign; thus, (1) can be expressed as

$$\left.\begin{aligned}(\dot{V}_{IN} \times I_{IN} + V_{IN} \times \dot{I}_{IN}) > 0, \quad V_{IN} < V_{MPP}\\ (\dot{V}_{IN} \times I_{IN} + V_{IN} \times \dot{I}_{IN}) < 0, \quad V_{IN} > V_{MPP}\end{aligned}\right\} \tag{2}$$

where $\dot{V}_{IN}$ and $\dot{I}_{IN}$ have the opposite sign. Therefore, (2) can be further simplified as

$$\left.\begin{aligned}\left|\frac{\dot{V}_{IN}}{V_{IN}}\right| > \left|\frac{\dot{I}_{IN}}{I_{IN}}\right|, \quad V_{IN} < V_{MPP}\\ \left|\frac{\dot{V}_{IN}}{V_{IN}}\right| < \left|\frac{\dot{I}_{IN}}{I_{IN}}\right|, \quad V_{IN} > V_{MPP}\end{aligned}\right\}. \tag{3}$$

Equation (3) shows that two analog dividers can be used to calculate the MPP instead of the three multipliers mentioned earlier. Fig. 4 also shows the differentiator structure consisting of the one amplifier, resistor, and capacitor, and it converts the time derivative of the input signal to the dc voltage based on the reference voltage (V_{REF}). Two differentiators are needed to sense the time derivative of V_{IN} and I_{IN}, and the conversion gain of the differentiator does not affect the equation for RCC if they have the same conversion gain. Both the input signal and feedback loop are applied to the minus port of the amplifier. Thus, the time derivative of the input signal and the converted dc voltage has opposite signs. The equation error is not due to ripple voltage of I_{IN} because the time derivative of I_{IN} has a negative sign during the charging state. However, the time derivative of V_{IN} has a positive sign, and it introduces the error when we compare the values of $\dot{V}_{IN}/V_{IN}$ and $\dot{I}_{IN}/I_{IN}$. For this reason, V_{IN} is applied to the differentiator through the negative unit gain buffer.

Most energy harvesting systems are self-biased; therefore, the input or output voltage of the power converter is used for the supply voltage control blocks. However, the supply voltage can be changed depending on the harvesting environment, and it can reduce the reliability of the circuit operation. Therefore, the proposed system adopts a system clock generator with a supply voltage (V_{DD}) tolerance to account for the supply voltage changing problem and a low-power voltage multiplexer [29] that chooses the higher voltage between the input and output voltage of the CP (V_{IN}, V_{OUT}). This is because a higher voltage should be used for the switching control of the CP; however, V_{IN} can be higher than V_{OUT} during the start-up phase.

C. Low-Power Analog Divider for a Simplified RCC Method

Fig. 5(a) shows the analog divider, which consists of two *V–I* converters and one current divider. Both *V–I* converter and current divider have very simple structures with a few MOSFETs, and each current path is composed of two MOSFET stacks; thus, they can be operated well when the supply voltage is small. The differentiator outputs $\dot{V}_{IN}$ and $\dot{I}_{IN}$ have an offset value caused by the V_{REF} voltage and it introduces the calculation error in the RCC method, as shown in Fig. 5(b). To solve this problem, the *V–I* converter, which has a mirroring part [30], is used to remove the offset value and increase the MPP calculation accuracy. The V_{IN} and I_{IN} values do not need this mirroring part; however, it has a ripple caused by the charging and discharging phase of C_{IN}. Therefore, an *RC* filter is used before applying

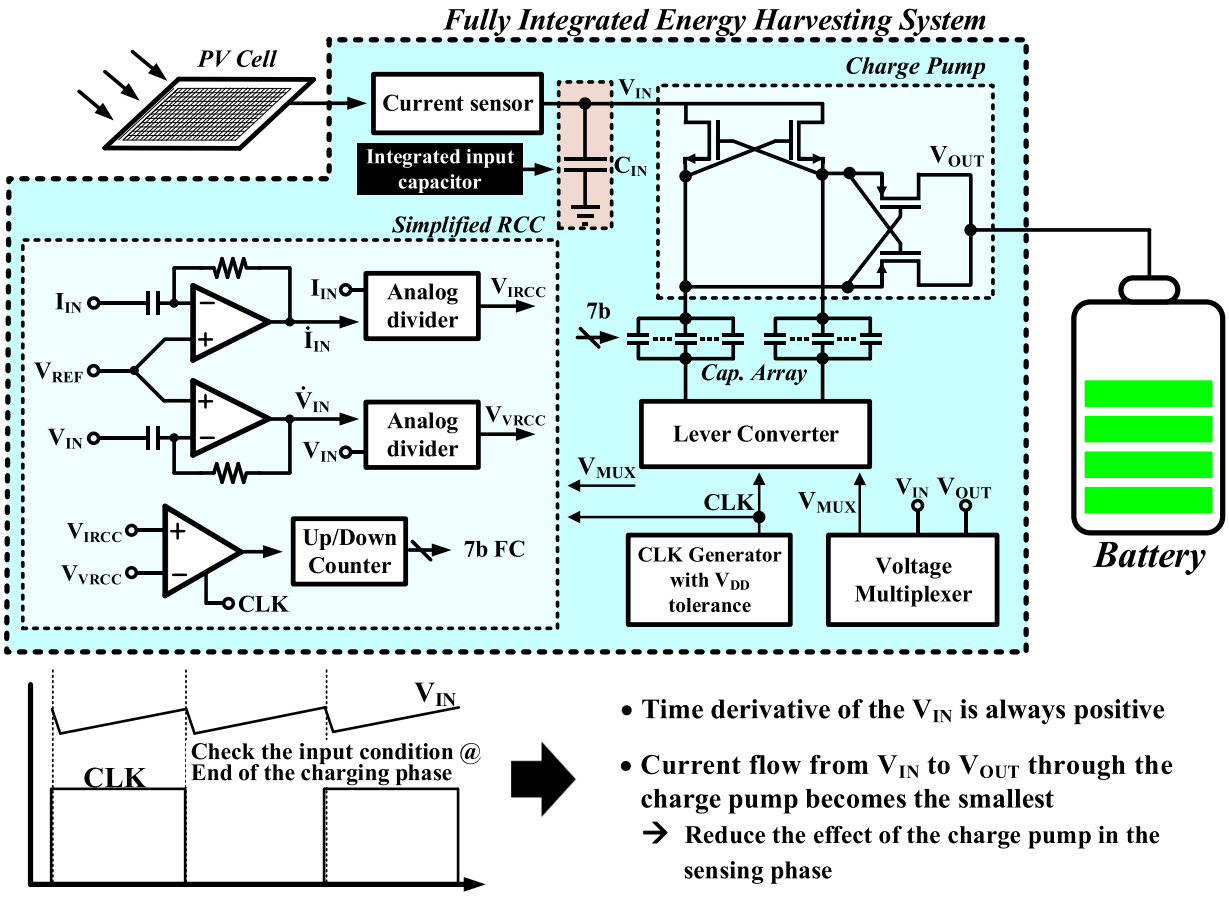


Fig. 4. Overall block diagram of the fully integrated EH system with the simplified RCC method.

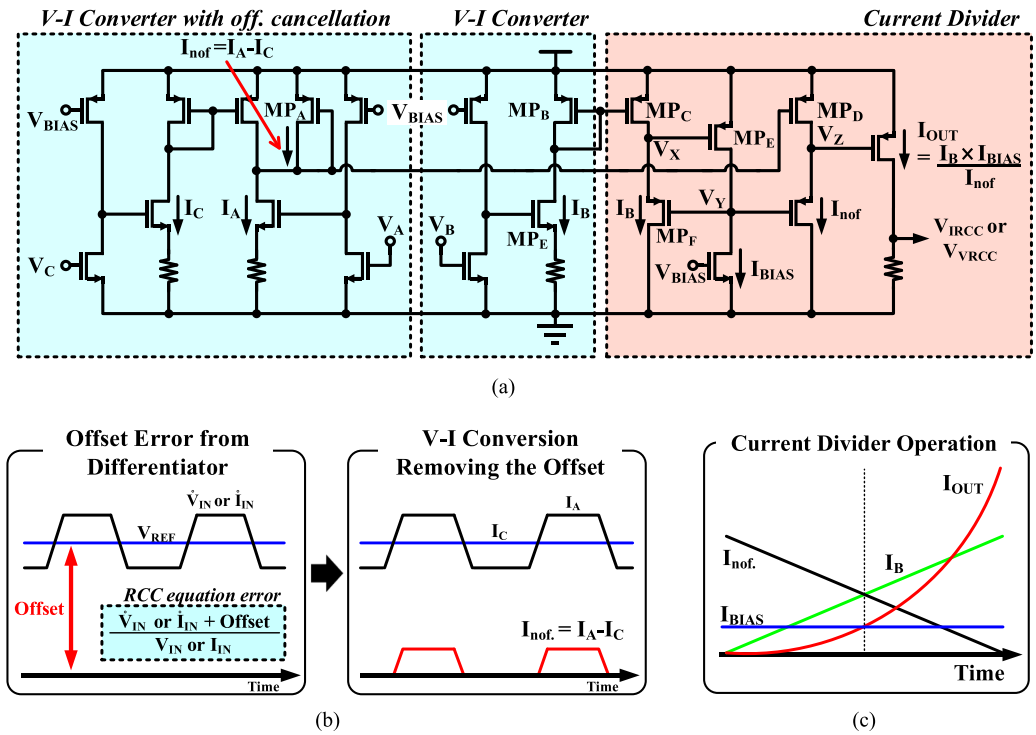


Fig. 5. Structure and operation of the analog divider. (a) Structure of the proposed analog divider. (b) Offset cancelation at *V–I* conversion. (c) Current divider operation.

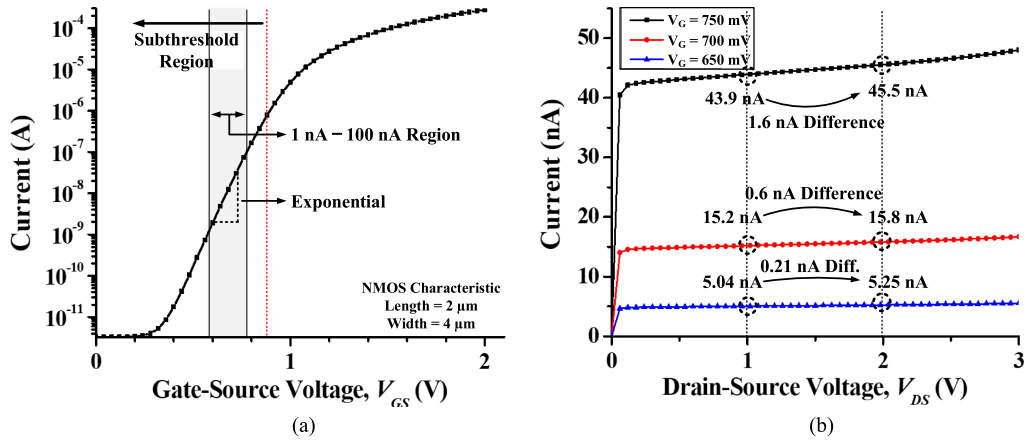


Fig. 6. Simulation results of the N-MOSFET current versus (a) gate–source voltage and (b) drain–source voltage.

the $V_{\rm IN}$ and $I_{\rm IN}$ values to the *V–I* converter. The current divider has a very simple structure with only seven MOSFETs and one resistor. The proposed analog divider has a total of ten current paths from the supply voltage to the ground. Therefore, each current path should consume a very small current, of a sub-μA level, and the divider is operated in the subthreshold region for the low-power design. In the subthreshold region, the MOSFET generates a tiny current, and even the small gate–source voltage ($V_{\rm GS}$) is lower than the threshold voltage ($V_{\rm TH}$); however, it exhibits an exponential dependence on $V_{\rm GS}$ [31], [32], as shown in Fig. 6(a). The MOSFET current is also affected by the drain–source voltage ($V_{\rm DS}$) of the MOSFET (channel length modulation) [31], [32], as shown in Fig. 6(b). However, this effect can be reduced by increasing the length of the MOSFET; furthermore, the node voltage changes V_X, V_Y, and V_Z of the current divider are small during the dividing operation because nodes V_X and V_Y consist of a negative feedback loop by $\rm MP_E$ and $\rm MP_F$, and the small voltage change V_Z is needed to control the output current ($I_{\rm OUT}$) owing to the operation in the subthreshold region. For example, if we simulate the N-MOSFET with a length of 2 μm and a width of 4 μm, then it requires approximately 200 mV $V_{\rm GS}$ voltage to change the MOSFET current from 1 to 100 nA. However, the change in current is only approximately 3% when $V_{\rm DS}$ is changed from 1 to 2 V. Therefore, the channel length modulation can be neglected and the MOSFET current can be derived as

$$I_{\rm MOS} = I_{\rm sub} \cdot e^{\left(\frac{qV_{\rm GS}}{nkT}\right)} \quad \left(\frac{kT}{q}: \text{thermal voltage}, n = \frac{C_{\rm ox}+C_{\rm dep}}{C_{\rm ox}}\right) \tag{4}$$

where kT/q is the thermal voltage V_T, $C_{\rm ox}$ is the gate oxide capacitance, and $C_{\rm dep}$ denotes the depletion capacitance between the channel and the substrate. If the MOSFET size for the current mirroring between $\rm MP_A$ and $\rm MP_D$ is the same, the current of $\rm MP_D$ is $I_{\rm nof}$ and the current of $\rm MP_C$ is I_B. All the P-MOSFET in the current divider are of the same size. Therefore, $I_{\rm OUT}$ can be expressed as

$$\left.\begin{aligned} &I_{\rm BIAS} = I_{\rm sub} \cdot e^{\left(\frac{q(VDD-V_X)}{nkT}\right)}, \ln\left(\frac{I_{\rm BIAS}}{I_{\rm sub}}\right) = \left(\frac{q(VDD-V_x)}{nkT}\right) \\ &\ln\left(\frac{I_B}{I_{\rm sub}}\right) = \frac{qV_X}{nkT} - \frac{qV_Y}{nkT}, \\ &\frac{qV_Y}{nkT} = \frac{qVDD}{nkT} - \ln\left(\frac{I_{\rm BIAS}}{I_{\rm sub}}\right) - \ln\left(\frac{I_B}{I_{\rm sub}}\right) \\ &\ln\left(\frac{I_{\rm nof}}{I_{\rm sub}}\right) = \frac{qV_Z}{nkT} - \frac{qV_Y}{nkT}, \\ &\frac{qV_Z}{nkT} = \ln\left(\frac{I_{\rm nof}}{I_{\rm sub}}\right) + \frac{qVDD}{nkT} - \ln\left(\frac{I_{\rm BIAS}}{I_{\rm sub}}\right) - \ln\left(\frac{I_B}{I_{\rm sub}}\right) \\ &I_{\rm OUT} = I_{\rm sub} \cdot e^{\left(\frac{q(VDD-V_Z)}{nkT}\right)} = \frac{I_{\rm BIAS} \cdot I_B}{I_{\rm nof}}, \\ &I_{\rm OUT} \propto \frac{I_B}{I_{\rm nof}}, \text{ and } I_{\rm BIAS}@I_B = I_{\rm nof} \end{aligned}\right\}. \tag{5}$$

This equation shows that the current $I_{\rm OUT}$ is proportional to $I_B/I_{\rm nof}$ and it can be operated as the current divider, as shown in Fig. 5(c). The current $I_{\rm OUT}$ can be easily converted to the voltage ($V_{\rm IRCC}$ or $V_{\rm VRCC}$) using a resistor, and $V_{\rm IRCC}$ and $V_{\rm VRCC}$ are applied to the clocked comparator to control the capacitor array of the CP.

The entire set of MOSFETs in the analog divider is operated in the subthreshold region, and each current path has nA or tens of nA level value. Additionally, the bias current $I_{\rm BIAS}$ can control the $I_{\rm OUT}$ current level using (5). For this reason, the power consumption of the divider can be very low, and the current value of each path can be easily controlled by changing $I_{\rm BIAS}$ or mirroring ratio.

D. Impedance Matching With the Capacitor Array

To regulate the voltage of $V_{\rm IN}$ to $V_{\rm MPP}$, the input impedance ($Z_{\rm IN}$) of the CP should be matched. Fig. 7(a) shows that most energy harvesting systems with a CP change the switching frequency ($f_{\rm CLK}$) or the number of stages ($N_{\rm STAGE}$). However, the frequency change can reduce the MPPT accuracy, and the power dissipation of RCC control blocks needs to be designed for the fastest frequency. For this reason, the proposed system adopts a ramp generator with $V_{\rm DD}$ tolerance [29] to maintain the constant switching frequency without any voltage regulator, such as a low-dropout regulator and changes the size of the flying capacitor ($C_{\rm SIZE}$) to control the input impedance of the CP. Fig. 7(b)

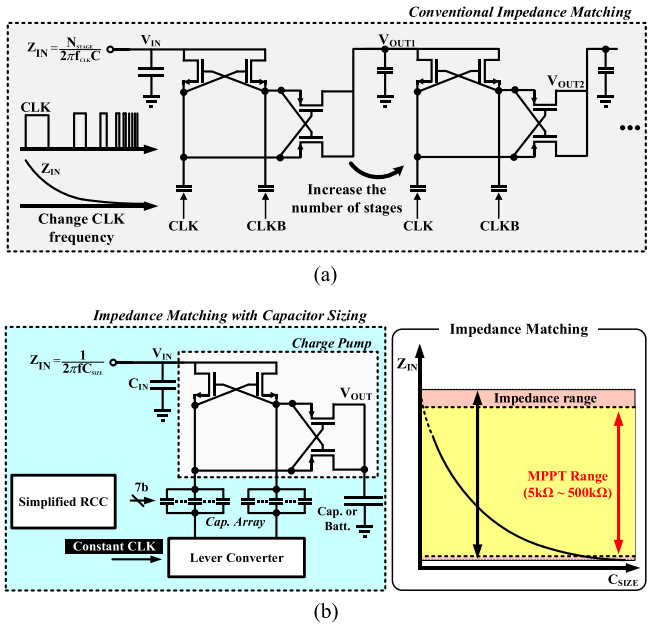


Fig. 7. Input impedance control of the charge pump. (a) Conventional EH systems with charge pump change the clock frequency or the number of stages for the input impedance control of the charge pump. (b) Simplified RCC system uses the 7-bit capacitor array control for input impedance control of the charge pump. The input impedance ranges from 4 to 512 kΩ.

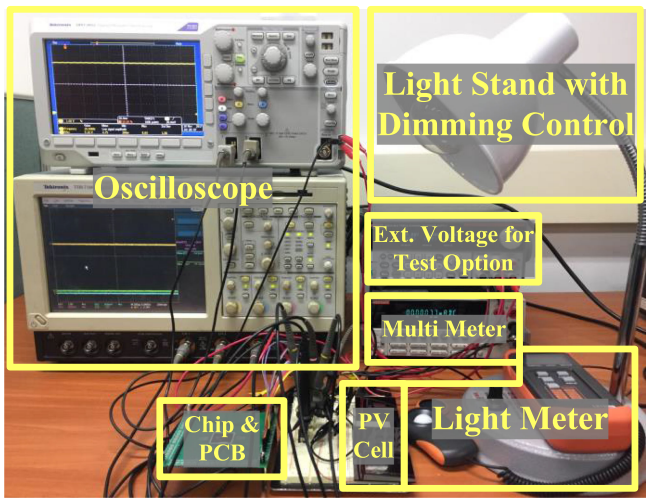


Fig. 8. Test environment of the RCC EH system.

shows the flying capacitor array designed using a binary capacitor sizing approach featuring seven control bits, and it can cover a few kilo-ohms to hundreds of kilo-ohms. This is sufficient to cover the range of tens of μW to a few mW for low-power applications.

III. Measurement

Fig. 8 shows the test environment setup for the proposed system. AM-1815 and AM-1816 indoor-type PV cells are used for the test. A light stand can control the light intensity with the analog lever. The light intensity can be controlled from 10 to 2000 lx, and the PV cell generates a few micro-watts to a few milli-watts power. The MPP of the harvester in the different light density conditions is sensed using a Keithley 2000 multimeter and the variable resistor. The dc power supply is used to control test options such as the ramp generator frequency, the output driver voltage level, and the current source level.

Fig. 9(a) and (b) shows that the MPPT operation when the input power ($P_{\rm IN}$) of the harvesting system from the PV cell is changed from 15 μW to 1.5 mW or 1.5 mW to 15 μW, respectively. The MPPT operation is done within tens of a millisecond with the impedance matching using the capacitor array control. The MPPT accuracy ($\eta_{\rm MPPT}$) and the power conversion efficiency of the CP ($\eta_{\rm conv}$) can be defined as

$$\eta_{\rm MPPT} = \frac{P_{\rm IN}}{P_{\rm MPP}}, \ \eta_{\rm conv} = \frac{P_{\rm OUT}}{P_{\rm IN}} \tag{6}$$

where $P_{\rm MPP}$ is the measured maximum power from the PV cell and $P_{\rm OUT}$ is the harvested power of the EH system. The MPPT circuits of the system change the capacitor size for the impedance matching, and the input ripple voltage is suppressed under 10% of the voltage at the MPP. Thus, the tracking accuracy is larger than 95% of the overall input power range, as shown in Fig. 9(c). Fig. 9(c) also shows the power conversion efficiency of the CP and the peak conversion efficiency is 74.6%.

The proposed system integrates all control blocks and power converter, including an input capacitor of 5 nF, by applying the RCC method to the CP. Therefore, the system can reduce design cost and increase area efficiency. The RCC algorithm of the proposed system is much simpler compared with other conventional RCC methods. The analog divider, which is the key block of the RCC control block, is operated in the subthreshold region; thus, whole circuits are efficiently implemented using some MOSFETs and *RC* components, and it can cover ultralow power applications, as shown in Table I. The simplified RCC method is also presented to calculate the correct MPP with a small input power and large ripple condition compared to the other EH systems with RCC; additionally, they cover the wide harvested power range (approximately 230 times from minimum to maximum) with a very simple structure.

Table II shows the performance comparison with other low-power energy harvesting systems that have a different MPPT method. The proposed system can cover a wider harvested power range among the CP-type EH systems, and the total capacitance size per the harvested power is small compared with other low-power EH systems. The EH system with a ripple voltage sensing method [33] dissipates very low power. However, this method has to use the preprogrammed look-up table (LUT), and it can reduce the utility of the system by limiting the types of the PV cell. A dual-output energy harvesting with an output voltage monitoring MPPT method [34] also has a lower quiescent current; however, this method must increase the number of MPPT circuits, comprising a sample and hold circuit for output voltage monitoring, hill-climbing logic, control voltage generator, and voltage-controlled oscillator, when the number of output is increased. The EH system with the FVOC method [18] has the highest power conversion efficiency; however, it uses a bulky inductor and input capacitor. The two-dimensional hill-climbing method [15] also has a good power conversion efficiency;

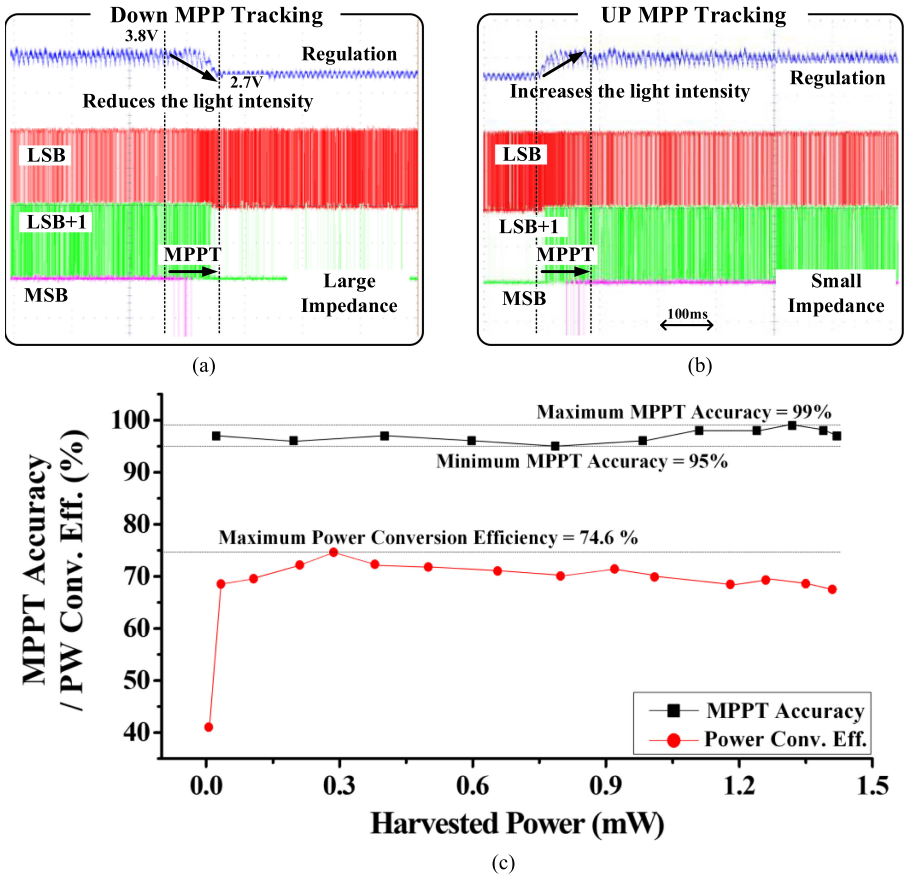


Fig. 9. Measurement results of the simplified RCC MPPT. (a) Down MPPT. (b) Up MPPT. (c) MPPT accuracy and the power conversion efficiency of the CP in the whole harvested power range.

TABLE I
PERFORMANCE COMPARISON TABLE WITH RCC EH SYSTEMS

	This Work	Midya, PESC 1996 [19]	Lim, EL 2000 [20]	Esram, TPE 2006 [23]	Kimball, TPE 2008 [24]	Bazzi, TPE 2014 [25]	Barth, TPE 2015 [26]
Process	0.18 µm CMOS	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip
Converter Type	Boost CP	Inductive Boost	Inductive Boost	Inductive Boost	Inductive Boost	Inductive Boost	Inductive Buck
Input Voltage (V)	0.8 – 5 V	< 20 V	< 14 V	< 20 V	< 20 V	Not reported	< 18 V
Harvested Power (P_{OUT})	6 µW– 1.4 mW	< 33.27 W	< 9.75 W	< 40 W	< 34.6 W	< 123 W	< 25.4 W
MPPT Algorithm	Simplified RCC	RCC	RCC	RCC	Discrete-Time RCC	RCC with Extremum Seeking Control	Dithering Digital RCC
RCC Implementation	1 Neg. UG buffer 2 Differentiator 2 Analog Div. 1 Clk. Comparator	2 Amplifier 2 Differentiator 3 Multiplier 2 Comparator	4 Amplifier 2 Differentiator 1 Multiplier	2 Inverting Amp. 2 HPF 1 Integrator 2 Multiplier	16-bit Micro Cont. (ADC, Multiplier) 4 Switches	DSP (2 HPF, 2 Mult., Discrete Integ.)	Micro cont. (ADC) 3 Signal Amp. 2 LPF
Impedance Matching	# of Flying Cap.	Duty cycle	Duty cycle	Duty cycle	Duty cycle	Duty cycle	Duty cycle
MPPT Accu. (P_{IN} / P_{MPP}) Max./Min. (%)	99 / 95	100 / 97.9	100 / 96.5	96.3 / 94	98.3 / 97.5	99.4 / 97.4	99.97 / 99.3
Input capacitor	5 nF	22 µF	470 µF	10 µF	Not Reported	Not Reported	88 µF
Fully Integrated Control blocks /with Input Capacitor	Yes	No	No	No	No	No	No

TABLE II
PERFORMANCE COMPARISON TABLE WITH LOW-POWER EH SYSTEMS

	This Work	Lee, VLSIC 2013 [33]	Ozaki, JSSC 2015 [34]	Chen, ISSCC 2015 [18]	Liu, JSSC 2016 [15]
Process	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.5 µm CMOS	0.18 µm CMOS
Converter Type	Boost CP	Boost CP	Boost CP	Inductive Buck/Boost	Reconfigurable CP
Input Voltage (V)	0.8 – 5 V	0.25 – 0.35 V *	0.35 – 0.6 V	3.6 V **	0.45 – 3 V
Harvested Power (µW)	6 – 1400	0.02 – 1.4	< 396	10 – 15000	< 50
MPPT Algorithm	Simplified RCC	Ripple Voltage Sensing with LUT	Output Voltage Monitoring	Fractional VOC	2-Dimension Hill-Climbing
Impedance Matching	# of Flying Cap.	Conversion Ratio	Frequency	Recycling	Frequency, # of stages
MPPT Accu. (P_{IN} / P_{MPP}) Max./Min. (%)	99 / 95	98 / 94.6	Not Reported	Not Reported	98.3 / 97.5
Peak Power Conversion Eff. (P_{IN} / P_{OUT}, %)	74.6	Not Reported	75.8	93	81
Quiescent Current or Power Consumption	2.6 µA	34 nW	510 nA	Not Reported	3.84 µW
Fully Integrated Control blocks /with Input Capacitor	Yes	Yes	Yes	No	Yes
Total Capacitor (nF) ***	6.25	Not Reported	4.05	4700	2.05 ****

*Optimum input voltage range.
**Regulated input voltage of the converter at measurement.
***Total integrated capacitance in the chip.
****Storage capacitor only. The capacitance of the CP is not reported.

however, the power consumption of the control block is relatively high considering the harvested power range.

IV. CONCLUSION

The proposed EH system with a simplified RCC technique is fabricated in a 180-nm CMOS process, and it can incorporate a fully integrated energy harvesting system including an input capacitor. The proposed method uses a very simple algorithm that only compares the ratios $\dot{V}/V$ and $\dot{I}/I$; additionally, the analog divider consumes a very small current because of its operation in the subthreshold region. Therefore, the proposed system can achieve a meaningful performance for low-power applications using a low quiescent current of 2.6 μA. The simplified RCC method adopts the CP as the power converter instead of the inductive switching converter for integration, and it can match the input impedance by changing the flying capacitor array size, which can cover from 2 to 500 kΩ. The tracking accuracy is larger than 95% and the peak power conversion efficiency of the power converter is 74.6% with the wide harvested power range from 6 μW to 1.4 mW. The size of $C_{\rm IN}$ is only 5 nF, and the total capacitor size of 6.25 nF including the CP is relatively small when we consider the harvested power range. The whole chip area is 8 mm^2; however, the control block of the RCC occupies only the small area of 0.56 mm^2.

ACKNOWLEDGMENT

The chip fabrication was supported by the IC Design Education Center, South Korea.

REFERENCES

[1] K. Yoshikawa *et al.*, "Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%," *Nature Energy*, vol. 2, Mar. 2017, Art. no. 17032.
[2] J. Benick *et al.*, "High-efficiency n-type HP mc silicon solar cells," *IEEE J. Photovolt.*, vol. 7, no. 5, pp. 1171–1175, Sep. 2017.
[3] T. Kato *et al.*, "Enhanced efficiency of Cd-free Cu(In,Ga)(Se,S)2 mini-module via (Zn,Mg)O second buffer layer and alkali post treatment," in *Proc. 44th IEEE Photovolt. Spec. Conf.*, Nov. 2017, vol. 7, pp. 1773–1780.
[4] First Solar, "First solar builds the highest efficiency thin film PV cell on record," 2014. [Online]. Available: http://investor. firstsolar.com/news-releases/news-release-details/first-solar-builds-highest-efficiency-thin-film-pv-cell-record.
[5] K. Sun *et al.*, "Beyond 9% efficient kesterite Cu2ZnSnS4 solar cell: Fabricated by using Zn1-xCdxS buffer layer," *Adv. Energy Mater.*, vol. 6, Apr. 2016, Art. no. 1600046.
[6] B. M. Kayes *et al.*, "27.6% conversion efficiency, a new record for single junction solar cells under 1 sun illumination," in *Proc. 37th IEEE Photovolt. Spec. Conf.*, Jun. 2011, pp. 4–8.
[7] T. Matsui *et al.*, "Development of highly stable and efficient amorphous silicon based solar cells," in *Proc. 28th Eur. Photovolt. Sol. Energy Conf.*, Jan. 2013, pp. 2213–2217.
[8] H. Sai *et al.*, "Effect of front TCO layer on properties of substrate-type thin-film microcrystalline silicon solar cells," *IEEE J. Photovolt.*, vol. 5, no. 6, pp. 1528–1533, Nov. 2015.
[9] W. S. Yang *et al.*, "Iodide management in formamidinium-lead-halide–based perovskite layers for efficient solar cells," *Science*, vol. 356, pp. 1376–1379, Jun. 2017.
[10] A. Q. Jiang *et al.*, "A resistive memory in semiconducting BiFeO3 thin-film capacitors," *Adv. Mater.*, vol. 23, pp. 1277–1281, Jan. 2011.
[11] M. F. El-Kady *et al.*, "Laser scribing of high-performance and flexible graphene-based electrochemical capacitors," *Science*, vol. 335, pp. 1326–1330, Mar. 2012.
[12] M. Kaempgen *et al.*, "Printable thin film supercapacitors using single-walled carbon nanotubes," *Nano Lett.*, vol. 9, pp. 1872–1876, Apr. 2009.
[13] A. Patil *et al.*, "Issue and challenges facing rechargeable thin film lithium batteries," *Mater. Res. Bull.*, vol. 43, pp. 1913–1942, Aug. 2008.

[14] T. Esram and P. Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 439–449, Jun. 2007.
[15] X. Liu, L. Huang, K. Ravichandran, and E. Sánchez-Sinencio, "A highly efficient reconfigurable charge pump energy harvester with wide harvesting range and two-dimensional MPPT for internet of things," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1302–1312, May 2016.
[16] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 963–973, Jul. 2005.
[17] J. J. Schoeman and J. D. van Wyk, "A simplified maximal power controller for terrestrial photovoltaic panel arrays," in *Proc. 13th Annu. IEEE Power Electron. Spec. Conf.*, 1982, pp. 361–367.
[18] H.-J. Chen *et al.*, "An energy-recycling three-switch single-inductor dual-input buck/boost dc-dc converter with 93% peak conversion efficiency and 0.5mm^2 active area for light energy harvesting," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2015, pp. 374–375.
[19] P. Midya *et al.*, "Dynamic maximum power point tracker for photovoltaic applications," in *Proc. 27th Annu. IEEE Power Electron. Spec. Conf.*, Jun. 1996, vol. 2, pp. 1710–1716.
[20] P. T. Krein, "Ripple correlation control, with some applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, 1999, pp. 283–286.
[21] D. L. Logue and P. T. Krein, "Optimization of power electronic systems using ripple correlation control: A dynamic programming approach," in *Proc. IEEE Power Electron. Spec. Conf.*, 2001, pp. 459–464.
[22] Y. H. Lim and D. C. Hamill, "Simple maximum power point tracker for photovoltaic arrays," *Electron. Lett.*, vol. 36, no. 11, pp. 997–999, May 2000.
[23] T. Esram, J. W. Kimball, P. T. Krein, P. L. Chapman, and P. Midya, "Dynamic maximum power point tracking of photovoltaic arrays using ripple correlation control," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1282–1291, May 2006.
[24] J. W. Kimball and P. T. Krein, "Discrete-time ripple correlation control for maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2353–2361, Sep. 2008.
[25] A. Bazzi and P. Krein, "Ripple correlation control: An extremum seeking control perspective for real-time optimization," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 988–995, Feb. 2014.
[26] C. Barth and R. Pilawa-Podgurski, "Dithering digital ripple correlation control for photovoltaic maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4548–4559, Aug. 2015.
[27] Z. Wang, "A CMOS four-quadrant analog multiplier with single-ended voltage output and improved temperature performance," *IEEE J. Solid-State Circuits*, vol. 26, no. 9, pp. 1293–1301, Sep. 1991.
[28] V. Riewruja and A. Rerkratn, "Analog multiplier using operation amplifier," *Indian J. Pure Appl. Phys.*, vol. 48, pp. 67–70, Jan. 2010.
[29] M. Shim, J. Kim, J. Jeong, S. Park, and C. Kim, "Self-powered 30 μW to 10 mW piezoelectric energy harvesting system with 9.09 ms/V maximum power point tracking time," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2367–2379, Oct. 2015.
[30] C. F. Lee and P. K. T. Mok, "A monolithic current-mode CMOS dc-dc converter with on-chip current-sensing technique," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 3–14, Jan. 2004.
[31] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2001.
[32] J. Rabaey *et al.*, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, NJ, USA: Pearson, 2003.
[33] I. Lee *et al.*, "A ripple voltage sensing MPPT circuit for ultra-low power microsystems," in *Proc. VLSI Circuits Symp. Dig. Tech. Papers*, 2013, pp. C228–C229.
[34] T. Ozaki, T. Hirose, H. Asano, N. Kuroki, and M. Numa, "Fully-integrated high-conversion-ratio dual-output voltage boost converter with MPPT for low-voltage energy harvesting," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2398–2407, Oct. 2016.

Minseob Shim (S'13) was born in Seoul, South Korea, in 1988. He received the B.S. degree in electrical engineering in 2012 from Korea University, Seoul, South Korea, where he is currently working toward the integrated M.S. and Ph.D. degree.

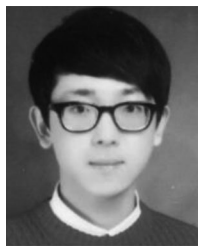
His research interests include integrated power management systems, low-voltage analog and mixed-signal integrated circuits, and analog-to-digital converter designs.

Junwon Jeong (S'12) received the B.S. degree in electrical engineering in 2012 from Korea University, Seoul, South Korea, where he is currently working toward the integrated M.S. and Ph.D. degree.

His research interests include integrated power management system designs, low-voltage low-power complementary metal–oxide–semiconductor analog circuit designs, energy harvesting circuit designs, and fuel gauging circuit designs.

Junyoung Maeng (S'14) received the B.S. degree in electrical engineering from Hongik University, Seoul, South Korea, in 2014. He is currently working toward the integrated M.S. and Ph.D. degree in electrical engineering at Korea University, Seoul, South Korea.

His research interests include integrated power management system designs, low-power complementary metal–oxide–semiconductor analog circuit designs, energy harvesting circuit designs, and dc–dc converters.



Inho Park (S'16) received the B.S. degree in electrical engineering in 2016 from Korea University, Seoul, South Korea, where he is currently working toward the integrated M.S. and Ph.D. degree.

His research interests include integrated power management systems, energy-harvesting circuit designs, and high-voltage silicon-based power converters.

Chulwoo Kim (S'98–M'02–SM'06) received the B.S. and M.S. degrees in electronics engineering from Korea University, Seoul, South Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2001.

In 1999, he was an Intern with the Design Technology, Intel Corporation, Santa Clara, CA, USA. In 2001, he joined the IBM Microelectronics Division, Austin, TX, USA, where he was involved in cell processor design. Since 2002, he has been with the School of Electrical Engineering, Korea University, where he is currently a Professor. He was a Visiting Professor with the University of California at Los Angeles in 2008 and with the University of California at Santa Cruz in 2012. He has coauthored two books, namely, *CMOS Digital Integrated Circuits: Analysis and Design* (McGraw Hill, 4th ed., 2014) and *High-Bandwidth Memory Interface* (Springer, 2013). His current research interests include wireline transceivers, memory, power management, and data converters.

Dr. Kim was a recipient of the Samsung HumanTech Thesis Contest Bronze Award in 1996, the ISLPED Low-Power Design Contest Award in 2001 and 2014, the DAC Student Design Contest Award in 2002, the SRC Inventor Recognition Awards in 2002, the Young Scientist Award from the Ministry of Science and Technology of Korea in 2003, the Seoktop Award for Excellence in Teaching in 2006 and 2011, the ASP-DAC Best Design Award in 2008, the Special Feature Award in 2014, and the Korea Semiconductor Design Contest: Ministry of Trade, Industry and Energy Award in 2013. He served on the Technical Program Committee of the IEEE International Solid-State Circuits Conference. He served as a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He is currently on the Editorial Board of the IEEE TRANSACTIONS ON VLSI SYSTEMS. He was elected as the Distinguished Lecturer of the IEEE Solid-State Circuits Society for 2015–2016.