Experimental Investigation of Linear Cumulative Damage Theory With Power Cycling Test

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***Abstract*—In this paper, several power cycling tests under single or combined test conditions were undertaken to investigate the applicability of linear cumulative damage theory in the lifetime prediction of power semiconductor devices. The validity of this theory was verified by an experimental method for one lifetime limit, which is an increase of forward voltage at load current by 5%. The corresponding failure mechanism is the degradation of bond wire contacts.**

***Index Terms*—Insulated-gate bipolar transistor (IGBT), lifetime prediction, linear cumulative damage theory, Miner's rule, power cycling test.**

I. Introduction

THE lifetime of power semiconductor devices is generally predicted under the assumption of a linear cumulative damage. More than 90 years ago, the concept of linear cumulative damage theory was first proposed by Palmgren in the investigation of the lifetime of roller bearings [1]. In 1945, Miner expressed this concept in a mathematical form, which is named Miner's rule [2]. For the power semiconductor devices, the load profile often incorporates active (caused by active operation) and passive temperature cycles (often caused by the variation of ambient temperature). By analyzing the given mission profile using a cycle counting algorithm, as for example presented in [3], the corresponding varying stresses can be reduced into a set of repeated load conditions. The total lifetime limit is considered to have been reached, if the sum of the lifetime consumption of all the load conditions reaches one, as for example presented in [4] and [5]. As originally stated in [2], the linear cumulative damage theory was only studied for aluminum alloys, whose failure limit is considered to be the inception of the first crack (when observed). The accuracy of the lifetime prediction for a given test object based on the linear cumulative damage theory may well depend on the definition of failure mechanism and damage state. Standard power modules with Al wire bonding and soft soldering have different failure modes. In a power cycling test, Al bond wire and solder layers are their main weak points (see Fig. 1). In order to improve the power cycling lifetime of power modules, some advanced packaging technologies were introduced in recent years, such as Cu wire bonding, Al-cladded Cu wires, silver sintering, and diffusion soldering [6]. In [7], silver sintering or diffusion soldering for the die attach and Cu wire bonding for the chip upper side connection have shown the potential to eliminate the weak points of standard power modules. For the test samples without baseplate in [7], the delamination of the direct copper bonding (DCB) copper was found to be the main failure mechanism. In the standard power cycling test, an increase of the forward voltage at load current by 5% (mainly caused by degradation of bond wire contacts), an increase of thermal resistance by 20% (mainly caused by delamination of solder layers), or loss of switching or blocking capability are usually defined as the lifetime limit [8].

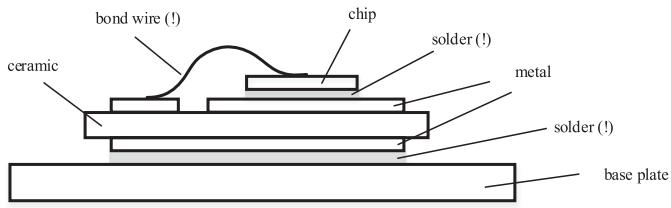

Fig. 1. Stacking of a classical power module with base plate [degradation sensitive components marked with (!)].

In a power cycling test, the stress conditions are defined by the temperature swing ΔT_{j}, the minimal junction temperature T_{jmin}, and the load pulse duration t_{on}. In contrast to the varying load conditions of a power module in the application, the load conditions (load current I_{L}, and pulse duration t_{on}) as well as the cooling conditions (coolant temperature T_{inlet} and flowrate $\dot{V}$) are kept constant during a power cycling test, which derive the lifetime under the given testing conditions. With results of several power cycling tests, lifetime model such as [9], [10], and [11] can be made. In order to check the applicability of linear cumulative damage theory in the lifetime prediction with the lifetime model driven from power cycling test results, tests under different stress conditions have to be performed. In [12], superimposed power cycling tests under different stress conditions were performed on transfer molded intelligent power modules. The linear cumulative damage theory was verified by several

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inverter tests and the main failure mechanism under the tested conditions was found to be bond wire cracks. Scheuermann and Hecht [13] indicated that the application of Miner's rule leads to an underestimation of the lifetime, if different failure mechanisms are triggered by each test condition in an interleaved test.

In the standard dc power cycling tests, only the conduction losses of a device at a high-load current are used to generate heat in the semiconductor chips, which evokes thermomechanical stresses in the power module due to the presence of temperature gradient and the coefficient of thermal expansion mismatch of different material layers. In order to reduce the test duration, a higher temperature swing is usually preferred, which means a higher load current and/or a longer load pulse duration. In this case, a different failure mode could be triggered due to the high-load current or long-load pulse duration, which is maybe not relevant in the real application. The benefit of the standard dc power cycling test is the possibility to determine the chip temperature by using $V_{\mathrm{CE}}(T)$ method [14]. Since the thermal characterization of the power module is usually performed by using $V_{\mathrm{CE}}(T)$ method as well, the dc power cycling test results can be directly used for the lifetime prediction.

However, due to the aforementioned possible drawback of the standard dc power cycling test, that a different failure mode could be triggered, some research groups have proposed inverter power cycling tests with switching losses and high dc-link voltage, which is closer to the application than the standard dc power cycling test [15], [16]. The limitation of the inverter test is the device temperature measurement. Optical methods or other temperature sensitive electrical parameters could be used during the inverter operation; however, further efforts are needed when implementing power cycling test results to the lifetime prediction. In [17], the dc power cycling test with superimposed high-frequency operation was introduced. In this case, device temperature measurement using $V_{\mathrm{CE}}(T)$ method is possible and the part of the switching losses is adjustable. Since the high voltage peak is caused by turning OFF the high load current with stray inductance, only the turn-OFF losses can be produced during the high-frequency operation, and therefore, this test principle is only suitable for the devices such as MOSFET or insulated-gate bipolar transistor (IGBT), which can be actively turned OFF.

In this paper, a series of standard dc power cycling tests under single and combined stress conditions were undertaken with standard 300 A 1200 V IGBT modules in half-bridge configuration. The IGBT modules used in this paper are standard power modules with Cu baseplate (see Fig. 1). The semiconductor chips are attached to the DCB substrates by soft solders and the DCB substrates are connected to the Cu baseplate by soft solders as well. The surface connection of the semiconductor chips is realized with 400-μm Al bond wires. Detailed information about the material and geometry of the layers in the standard power modules can be found in [8]. Based on the publication results, more than 60% of the power cycling tests of power modules from 1994 until now were performed on IGBTs [18]. Therefore, the aforementioned IGBT modules are chosen for the investigation in this paper.

TABLE I
SUMMARY OF THE TEST CONDITIONS

Test No.	ΔT_{j} in K	T_{jmin} in °C	t_{on} in s
1	100	50	2
2	50	100	1
3	100	50	15
4	50% expectation of test 1 + test 2 until EOL		
5	50% expectation of test 3 + test 2 until EOL		
6	test 1 and test 2 in 20% steps until EOL		

The forward voltage drop of IGBT V_{CE} at load current before turn-OFF (about 5 ms) was measured for every cycle in order to monitor the degradation of the bond wire connection. To determinate thermal resistance (between chip and heat sink) R_{thjs} for showing the health state of solder layers, reference temperature was measured 2 mm beneath the surface of heat sink with thermocouples. For the measurement of chip temperature, $V_{\mathrm{CE}}(T)$ method with a measurement current of 100 mA is used. Due to the required time for the recombination of excess charge carriers after conducting high current, a measurement delay of 500 μs is used in the power cycling test to ensure a correct measurement of maximal virtual junction temperature $T_{j\max}$. Details on measurement requirements in the power cycling test are given in [19].

Table I represents a short overview of the test series. The test conditions were defined in a way to trigger mainly the aging of the bond wire connections, i.e., inducing end of life (EOL) via an increase of forward voltage at load current by 5%.

Tests 1–3 were designed to derive lifetime cycles of the target IGBTs under the given single test conditions. In tests 4–6, devices under test (DUTs) were stressed under combined test conditions from two of the previous power cycling tests under single test conditions. To eliminate the influences of adjustment of test conditions in the startup phase, the first 10% measurement data were not used to calculate the initial point of forward voltage V_{CE} and thermal resistance R_{thjs} (100% value). The 100% values of V_{CE} and R_{thjs}, which will directly determine the failure limit, are average of the corresponding measurement data from the cycles representing 10% to 20% of the total cycle number of each sample, when the test is considered to run under stable conditions.

II. SINGLE POWER CYCLING TEST

In the first part of this paper, three single power cycling tests were performed. The test results of tests 1–3 are shown in Figs. 2–8. Table II gives a summary of the obtained lifetime of all DUTs in test 1 with $\Delta T_{\mathrm{j}} = 100\,\mathrm{K}$ and $T_{\mathrm{jmin}} = 50\,^{\circ}\mathrm{C}$.

Considering the slight differences of the realized test conditions (ΔT_{j} and T_{jmin}), all test samples have reached a similar lifetime. The EOL cycle is denoted by an increase of the forward voltage at load current by 5%. The mean lifetime of the DUTs under the test condition of test 1 is defined as N1 and all cycles of the DUTs in test 1 are normalized to this mean lifetime N1. The same evaluation procedure was done for tests 2 and 3, i.e., N2 and N3 represent the mean lifetimes of DUTs under the test conditions of tests 2 and 3. Table III and Table IV

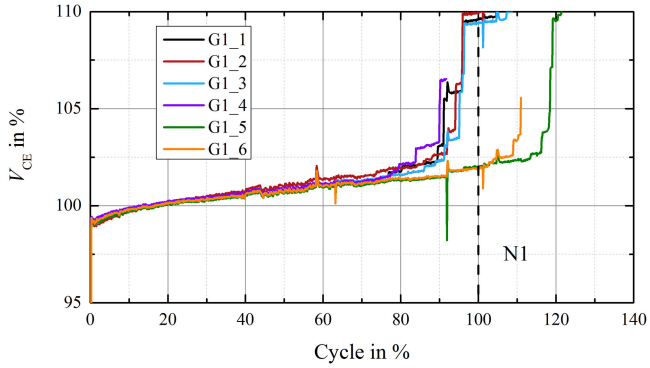


Fig. 2. V_{CE} trend of DUTs in test 1 ($t_{on} = 2\,s$, $\Delta T_j = 100\,K$, and $T_{jmin} = 50\,°C$).

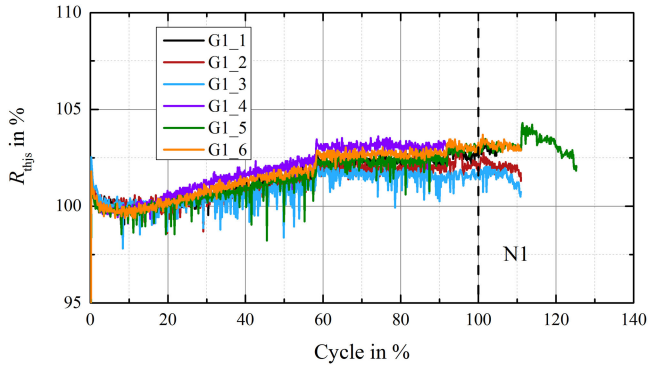


Fig. 3. R_{thjs} trend of DUTs in test 1 ($t_{on} = 2\,s$, $\Delta T_j = 100\,K$, and $T_{jmin} = 50\,°C$).

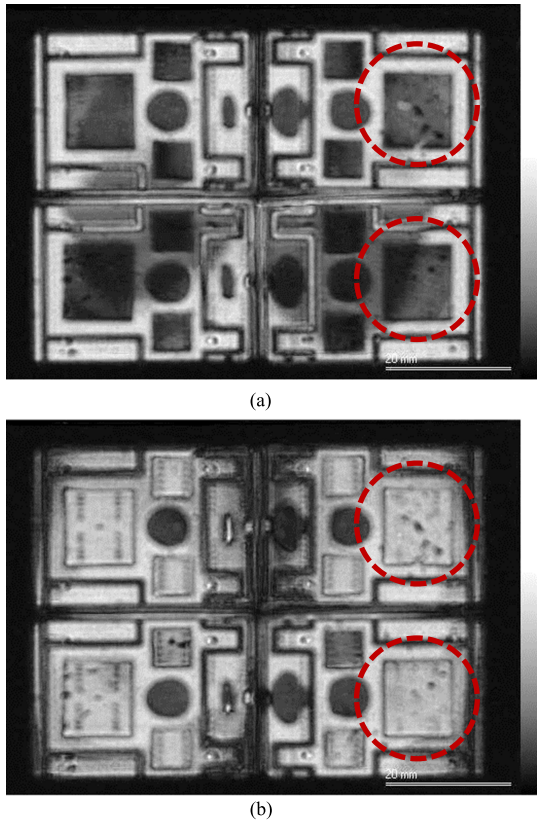


Fig. 4. SAM images of (a) chip solder and (b) chip surface of one the DUT after test 1 (chips in red mark were tested).

TABLE II
RESULT OF TEST 1

Label	EOL Cycle in % N1	ΔT_j in K	T_{jmin} in °C
G1_1	91.1	99.2	49.4
G1_2	94.2	98.0	50.1
G1_3	95.1	98.1	49.7
G1_4	90.0	99.4	49.1
G1_5	118.6	97.6	48.5
G1_6	111.0	98.5	49.2

TABLE III
RESULT OF TEST 2

Label	EOL Cycle in % N2	ΔT_j in K	T_{jmin} in °C
G2_1	99.9	51.5	100.7
G2_2	111.7	51.0	101.1
G2_3	95.6	52.3	100.4
G2_4	106.3	51.3	100.5
G2_5	95.8	52.5	100.2
G2_6	90.7	52.3	100.0

give summaries of the obtained lifetime of all DUTs in test 2 and test 3 respectively.

In the performed power cycling tests, devices of the same type under the same test condition have a varied lifetime of about ±10%. The mean power cycling lifetime of the devices in test 2 is about ten times higher than the mean lifetime in test 1 (N2 ≈ 10·N1). In test 3, same devices have achieved only half of the power cycling lifetime as in test 1 (N1 ≈ 2·N3). The test conditions of tests 1–3 were chosen in order to deduce the power cycling lifetime, which differ significantly from each other. In this case, the impact of the fluctuation of the test results is much lower than the impact of the test conditions and the fluctuation of the test results has no significant influence on the effect studied in this paper.

As can be seen from the scanning acoustic microscope (SAM) images shown in Fig. 4, the regularly arranged bond stitches are no more clearly recognizable on the tested IGBT chip surface after test 1. The loss of visibility of bond stitch in a SAM image can be typically induced by two effects: either solder degradation, which leads to a reflection of the ultrasonic signal already in the solder layer before reaching the bond interface, or bond wire lift-off. Since no sign of solder fatigue, neither chip solder nor system solder, can be observed in the ultrasonic images, lifted bond wires on the stressed chip surface can be confirmed. The SAM images shown in this paper were made by using a 35-MHz transducer with a focal length of 40 mm (in the water). The SAM equipment used is the SAM 400 from PVA TePla. The SAM images fit well with the gained online monitoring data shown in Fig. 3, where increase of R_{thjs} remains below 5%. The stepwise increase of the forward voltage at the end of the test shown in Fig. 2 is a typical evidence of bond wire lift-off during the test. All DUTs in this paper revealed the same failure signature, i.e., bond wire lift-off is the failure mechanism leading to EOL in all applied power cycling tests within this paper. In Fig. 11, tested IGBT chip from tests 2, 3, and 5 are shown. Clear bond wire lift-offs can be observed.

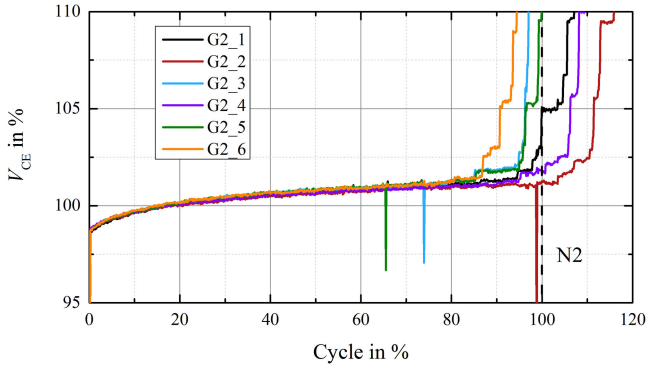


Fig. 5. V_{CE} trend of DUTs in test 2 ($t_{on} = 1$ s, $\Delta T_j = 50$ K, and $T_{jmin} = 100$ °C)

TABLE IV
RESULT OF TEST 3

Label	EOL Cycle in % N3	ΔT_j in K	T_{jmin} in °C
G3_1	96.8	105.4	50.1
G3_2	99.3	103.9	49.9
G3_3	93.5	106.5	49.8
G3_4	102.0	105.6	49.8
G3_5	110.6	104.3	49.7
G3_6	97.8	103.8	49.2

Similar to test 1, no clear degradation of solder layers can be found after test 2 with $t_{on} = 1$ s (see Fig. 6) and test 3 with $t_{on} = 15$ s (see Fig. 8). It has to be mentioned that the set junction temperature swings ΔT_j in test 3 are slightly above the target value of 100 K (see Table IV, about 5 K higher). For the desired target test condition ($\Delta T_j = 100$ K), the real lifetime cycle should be longer than N3.

III. COMBINED POWER CYCLING TEST

As the single power cycling tests have shown, bond interface limits the lifetime of the DUTs under the three test conditions. The combination of these parameters allows for a validation of applicability of Miner's rule for power semiconductor devices. In test 4, the DUTs were first tested under the test conditions of test 1 for about 50% of N1 (the cycles until EOL in test 1). After that, the DUTs were stressed under the test conditions of test 2 until EOL. The set test conditions of DUTs in test 4 are shown in Table V (part 1) and Table VI (part 2).

The V_{CE} trend of the DUTs during the whole test 4 is shown in Fig. 9. Because the DUTs were tested in two parts with different load current and different temperature, their forward voltage drops V_{CE} were, therefore, different. To visualize the continuing change of V_{CE}, the end value of V_{CE} as percentage of part 1 is taken as the initial value of part 2. At the point of changing test conditions from test 1 to test 2 (about 50% of the expectation), fluctuation of measurement data can be observed due to the restart of the test. The test system needs again some time to reach the thermal equilibrium. DUTs in test 4 have achieved in average about 109.9% of the lifetime expectation, which is simply calculated from results of test 1 (N1) and test 2 (N2) without considering the difference in achieved test conditions.

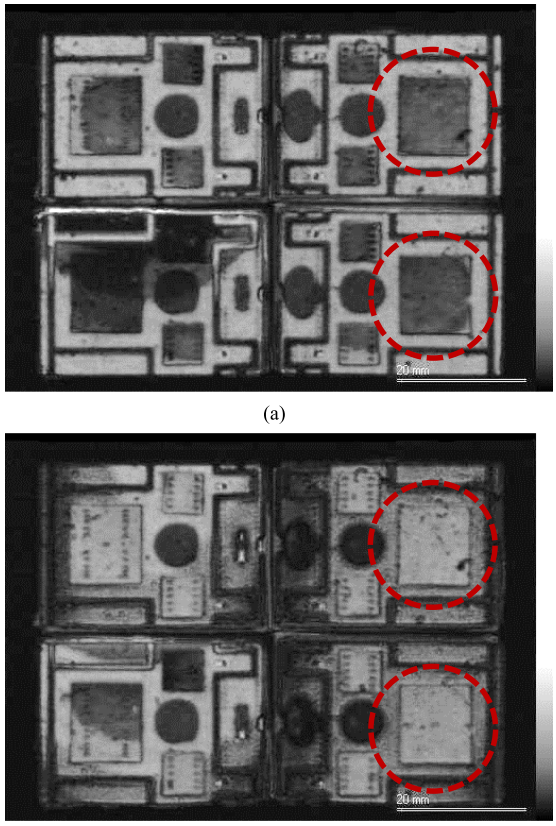


Fig. 6. SAM images of (a) chip solder and (b) chip surface of one the DUT after test 2 (chips in red mark were tested).

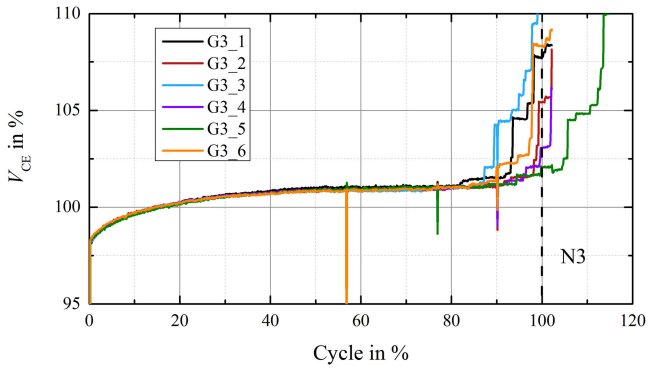
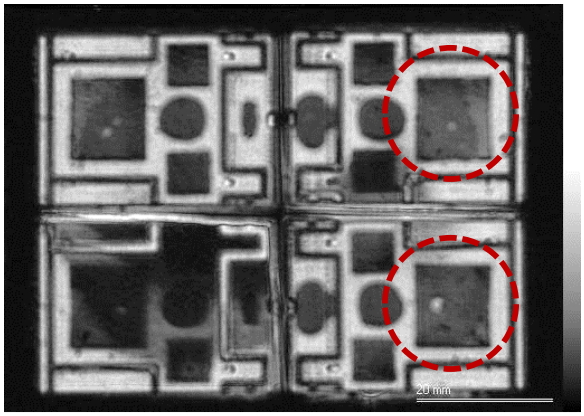


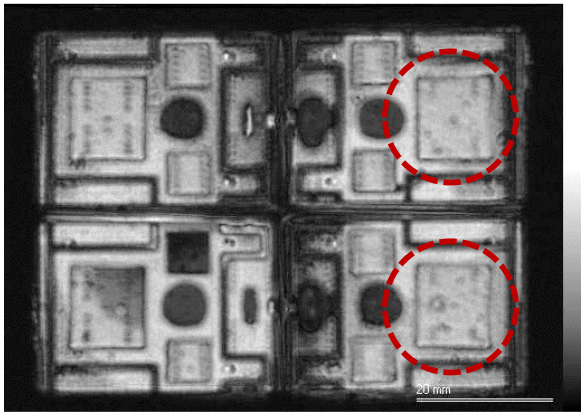
Fig. 7. V_{CE} trend of DUTs in test 3 ($t_{on} = 15$ s, $\Delta T_j = 100$ K, and $T_{jmin} = 50$ °C).

In test 5, the DUTs were first tested under the test conditions of test 3 for about 50% N3 cycles. In the second part, the DUTs were stressed under the test conditions of test 2 until EOL. The set test conditions of DUTs in test 5 are shown in Table VII (part 1) and Table VIII (part 2). The V_{CE} trend of the DUTs during test 5 is shown in Fig. 10. DUTs in test 5 have achieved in average about 118.6% of the expected lifetime.

A comparison of the tested IGBT chip from tests 2, 3, and 5 (test 2 + test 3) is shown in Fig. 11. All the tested chips have bond wire lift-off in the middle region of the chip, where the



(a)



(b)

Fig. 8. SAM images of (a) chip solder and (b) chip surface of one the DUT after test 3 (chips in red mark were tested).

TABLE V
RESULT OF TEST 4 PART 1

Label	Cycle in % N1	ΔT_j in K	T_{jmin} in °C
G4_1	49.7	98.9	50.5
G4_2	49.7	98.2	50.8
G4_3	49.7	100.4	50.5
G4_4	49.7	97.2	49.6
G4_5	49.7	102.8	50.8
G4_6	49.7	103.3	52.9

TABLE VI
RESULT OF TEST 4 PART 2

Label	EOL Cycle in % N2	ΔT_j in K	T_{jmin} in °C
G4_1	64.3	50.2	101.1
G4_2	76.7	49.8	101.7
G4_3	73.7	50.7	100.7
G4_4	55.7	49.8	100.1
G4_5	44.3	51.7	101.0
G4_6	46.6	50.5	101.9

TABLE VII
RESULT OF TEST 5 PART 1

Label	Cycle in % N3	ΔT_j in K	T_{jmin} in °C
G5_1	48.4	103.7	50.1
G5_2	48.4	102.9	50.7
G5_3	48.4	104.6	51.6
G5_4	48.4	102.4	50.2
G5_5	48.4	100.5	49.7
G5_6	48.4	105.1	50.3

TABLE VIII
RESULT OF TEST 5 PART 2

Label	EOL Cycle in % N2	ΔT_j in K	T_{jmin} in °C
G5_1	65.9	50.9	101.1
G5_2	82.2	50.7	102.6
G5_3	70.5	50.2	102.3
G5_4	63.7	50.0	101.4
G5_5	78.5	50.1	100.4
G5_6	60.4	50.9	101.1

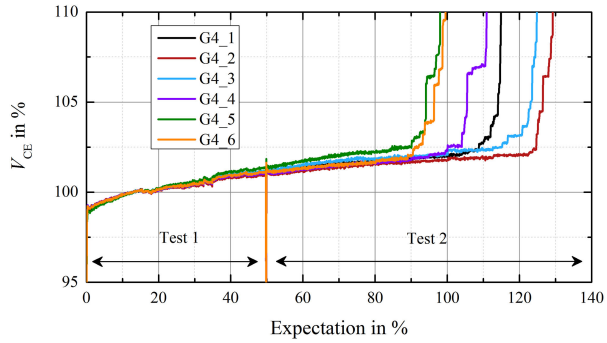


Fig. 9. V_{CE} trend of DUTs in test 4 (50% of test 1 + test 2 until EOL).

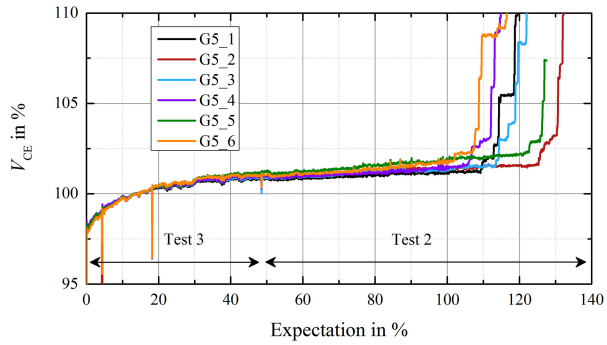
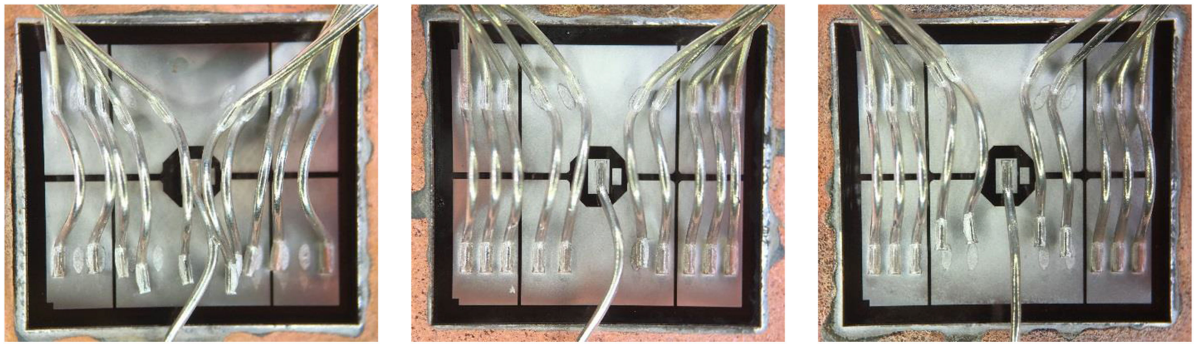


Fig. 10. V_{CE} trend of DUTs in test 5 (50% of test 3 + test 2 until EOL).

temperature is higher and the temperature swing is larger during the test. In this paper, combined power cycling tests show always the same failure mechanism as in the single power cycling tests.

In test 6, all the DUTs were tested under test conditions of test 1 and 2 alternately in 20% steps. V_{CE} developed in the DUTs during test 6 is shown in Fig. 12. Every time when test was restarted due to the change of test condition or failure of devices, fluctuation of measurement data can be found. The DUTs in test 6 have achieved in average about 100.6% of the expected lifetime.

In tests 4 and 5, the total achieved lifetime cycles are some degree higher than expectations based on the linear cumulative damage theory. For test 4, the difference between the test result and prediction is small (about +10%), which lies in the range of the lifetime distribution of several devices in one single test. Linear accumulation of damage can be confirmed for mixing these conditions, which can also be confirmed by test 6. For test 5, the difference is more significant (about +19%). It should, however, be noted that the set average ΔT_j of the test conditions in both the first and second half of test 5 is slightly lower compared to the corresponding values of tests 1 and 3 (roughly 1.5



(a) (b) (c)

Fig. 11. Tested IGBT chip from (a) test 2, (b) test 3 and (c) test 5.

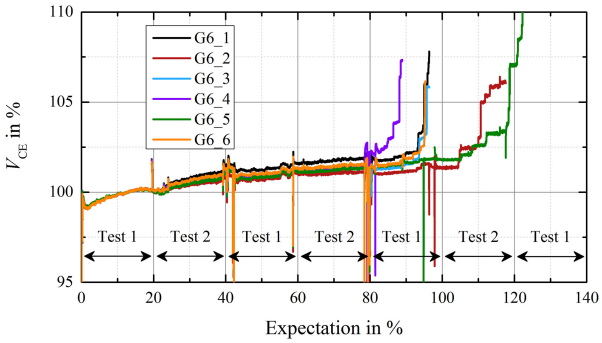


Fig. 12. V_{CE} trend of DUTs in test 6 (test 1 and test 2 in 20% steps).

K). This could account for the higher total lifetime in test 5

$$N_f \sim \Delta T_j^{\alpha}. \tag{1}$$

In most lifetime models of power module (for example, [9]–[11]), ΔT_j dependence of the power cycling lifetime N_f is given with a Coffin–Manson exponent α as shown in (1), which lies typically between -4.2 and -5. In CIPS 08 model [10], a Coffin–Manson exponent of -4.416 is driven for IGBT modules, which are similar to the test objects in this paper. If this Coffin–Manson exponent from CIPS 08 model is used to correct the aforementioned difference between realized test conditions of different tests, DUTs from tests 4 and 5 have achieved only 7% power cycles more than the expectation based on the linear cumulative damage theory.

Besides, the strong difference in heating time of the two parts of test 5 (15 s versus 1 s) might lead to a slightly different thermomechanical stress regarding impact scale inside power module, so that a simple linear accumulation of the lifetime consumption is a very conservative approach. An extreme example of this effect are the test results shown in [13]; due to the completely independent failure modes, the devices in the superimposed power cycling test have achieved a much higher lifetime than the expectation based on the linear cumulative damage theory.

Furthermore, Edwards [20] has shown that Miner's rule can give an inaccurate estimate of the lifetime of aluminum alloy under variable amplitude loadings (ΔT_j in a power cycling test). The effect of geometric residual stresses would play a role in the cumulative damage behavior. In a step test with positive varying mean stress (tests 4 and 5: monotonically increasing mean junction temperature T_{jm}), the total achieved lifetime has been shown to be higher than the expected lifetime based on the linear cumulative damage theory. In a test with well-mixed loading (test 6 as well as most applications), linear cumulative damage theory will give a more accurate prediction of the lifetime than in the step test, such as tests 4 or 5.

IV. Conclusion

As shown in this paper, DUTs under combined test conditions have similar test results with the lifetime expectation based on linear cumulative damage theory. The validity of this theory in the lifetime prediction of power semiconductor devices was verified by an experimental method, if considering the aging of the bond wire connection as one separated failure mechanism. As mentioned before, an increase of thermal resistance by 20% is another important failure criterion in the power cycling test, which is mainly caused by the degradation of solder layers. The degradation of solder layers or bond wires will accelerate the aging of each other at the same time. However, the solder layers and bond wires are separate parts in power modules, which are believed to have relatively independent lifetimes. With varying heating time, the scale and intensity of thermomechanical stress occurring in a power module are changing. A set of repeated load conditions driven from mission profile could lead to different failure modes. In this case, a lifetime prediction based on linear cumulative damage theory is believed to be too conservative. Thus, further study with focus on the mixture of these two failure mechanisms is still a matter of great interest.

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