Letters

Dual-Channel Push–Pull Isolated Resonant Gate Driver for High-Frequency ZVS Full-Bridge Converters

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***Abstract*—In this letter, a new zero-current-switching (ZCS) dual-channel push–pull isolated resonant gate driver (DPIRGD) is proposed to drive a pair of power MOSFET in one bridge leg operating at high-switching frequency. The characteristics of the proposed DPIRGD include capability to provide two isolated complementary drive signals, low-gate drive loss, and high reliability of the turn-OFF status. Compared to the previous gate driver suitable for the zero-voltage-switching full-bridge converters, the proposed DPIRGD achieves similar gate drive loss but implements low components enabling to reduce the drive cost and increase the reliability. The operation principle, loss analysis, optimum design, and comparison study of the DPIRGD are presented in detail. The experimental results are shown to verify the effectiveness of the proposed concept. This solution has achieved nearly 70.7% reduction in gate drive power loss compared to the conventional voltage-source drive circuit.**

***Index Terms*—Full-bridge converters, high frequency, push-pull, resonant gate driver.**

I. Introduction

THE gate driver forms a significant interface between a power electronic stage and a control end. The increasing demand for high efficiency, high power density, low cost and size, etc., impels to increase the switching frequency. However, this will lead to increase the gate drive loss, which is proportional to rise up with the conventional voltage-source driver (VSD) [1]. At high switching frequency and low-power application, such as several hundred watts and below, the effect of the gate drive loss on the overall converter becomes more pronounced. In order to recover the gate-driver loss dissipated in the gate resistance of VSD, many resonant gate drivers (RGDs) have been proposed during the past two decades [2]–[4].

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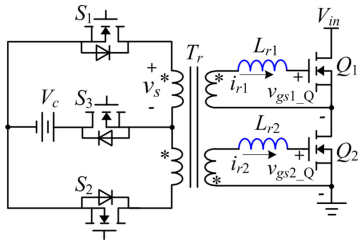

Fig. 1. Proposed DPIRGD.

II. Proposed Resonant Gate Drive Circuit

Fig. 1 illustrates the proposed DPIRGD, which consists of three drive switches S_1-S_3, the drive HF transformer T_r, and two resonant inductors L_{r1} and L_{r2}. L_{r1} and L_{r2} can be the leakage inductances of the drive HF transformer T_r. Q_1 and Q_2 represent the high-side and low-side switches in one bridge leg, respectively.

Fig. 2(a) shows the key waveforms of the proposed DPIRGD including the gate signals v_{g1}–v_{g3} for three drive switches S_1-S_3, the HF transformer winding voltage v_s, and the secondary-side resonant currents i_{r1} and i_{r2} along with the gate-to-source voltages v_{gs1_Q} and v_{gs2_Q}. The winding voltage v_s is decided by the ON/OFF states of three drive switches S_1-S_3. i_{r1} and i_{r2} are the resonant currents through two resonant inductors L_{r1} and L_{r2}, and they are also the gate driving current of MOSFET Q_1 and Q_2, respectively. It is noted that currents i_{r1} and i_{r2} are sinusoidal and discontinuous resulting in the reduction of conduction loss of the drive circuit itself.

The operation principle of the proposed DPIRGD consists of six intervals during one switching cycle as shown in Fig. 2(b)(1)–(6). Primary-side current i_p is the sum of $|\, i_{r1}\,|$ and $|\, i_{r2}\,|$. It is assumed that the ratio of T_r is 1:1 and the input capacitance is $C_{gs1\_Q} = C_{gs2\_Q} = C_{gs\_Q}$. Each interval is analyzed as follows.

Interval 1 [t_0-t_1]: In this interval, S_1 and S_3 are in the ON state, as shown in Fig. 2(b)(1). The winding voltage v_s is clamped to $-V_c$. Since the ratio of the drive HF transformer 1:1 and the polarities of secondary windings are opposite connection, voltages v_{gs1_Q} and v_{gs2_Q} of Q_1 and Q_2 are initially charged at $-V_c$ and V_c, respectively, and, thus, Q_1 is in OFF state and Q_2 is in ON state during this stage. Note that $-V_c$ can prevent the false trigger in one bridge leg.

Interval 2 [t_1-t_2]: At t_1, S_3 turns OFF with zero-current switching (ZCS) and S_2 turns ON with ZCS because of $i_{r1} = i_{r2} = i_p = 0$ and $v_s = 0$. Then, the resonance between C_{gs1_Q} and L_{r1}, C_{gs2_Q} and L_{r2} starts, respectively, due to the initial energy stored in the C_{gs1_Q} and C_{gs2_Q}. Currents i_{r1} and i_{r2} and voltages v_{gs1_Q} and v_{gs2_Q} increase sinusoidally, as illustrated in Fig. 2(b)(2). During this stage, the current i_p circulates among S_1 and S_2 and no current passes through the input dc power supply. It implies that the input dc power supply provides no electric power to the gate driver theoretically. So the gate drive loss can be reduced dramatically by this RGD.

During this interval, Q_1 and Q_2 work at the complementary mode. Considering loop resistance R_p including the winding resistance, the bonding and gate-pattern resistances inside the driven MOSFET, the voltage v_{gs1_Q} can be expressed by

$$v_{gs1\_Q}(t) = -\frac{V_c\omega_r}{\omega}e^{-\lambda t}\sin(\omega t+\theta) \tag{1}$$

where

$$\lambda = \frac{R_p}{2L_r}, \omega_r = \frac{1}{\sqrt{L_r C_{gs\_Q}}}, \omega = \sqrt{\omega_r^2-\lambda^2}, \theta = \arctan\frac{\omega}{\lambda},$$

$$T_R = 2\pi\sqrt{L_r C_{gs\_Q}}. \tag{2}$$

At $t = t_2 = T_R/2$, v_{gs1_Q} reaches the maximum value V_{c1} during the turn-ON process. Because of the resistance power loss in the resonant loop, there is a voltage drop ΔV_c during this process. From (1) and (2), the value of ΔV_c is given by

$$\Delta V_c = V_c\Big[1+\frac{\omega_r}{\omega}e^{-\lambda T_R/2}\sin(\omega T_R/2+\theta). \tag{3}$$

At t_2, v_{gs1_Q} reaches V_{c1} and v_{gs2_Q} gets to $-V_{c1}$, respectively, so Q_1 turns ON and Q_2 turns OFF.

Interval 3 [t_2-t_3]: At t_2, since the currents i_{r1} and i_{r2} reach 0, S_1 turns OFF and S_3 turns ON with ZCS. After t_2, the winding voltage v_s is clamped to V_c, and, thereby, C_{gs1_Q} is actively charged to V_c and C_{gs2_Q} is actively charged to $-V_c$, as shown in Fig. 2(b)(3). Then, v_{gs1_Q} and v_{gs2_Q} are clamped to V_c and $-V_c$, respectively, at t_3.

After t_3, the next three intervals start working. The equivalent circuits are shown in Fig. 2(b)(4)–(6) and the operation principle is exactly the same as that of interval Fig. 2(b)(1)–(3).

III. Loss Analysis and Design Consideration

A. Gate Dive Loss Analysis With the Proposed DPIRGD

Considering the circuit components producing power consumptions, Fig. 3 illustrates the equivalent power loss model of the proposed DPIRGD, where $R_{\rm DS}(\rm on)$ is the ON-state resistance and $C_{\rm oss}$ is the output capacitance in the drive switches S_1-S_3, and R_{gs} is the sum of the winding resistance and bonding and internal gate resistance inside the driven Q_1 (Q_2).

According to the analysis of interval 3, the input dc power supply provides a small amount of electric to charge C_{gs1_Q} from V_{c1} to V_c, which is equal to $C_{gs\_Q}V_c\Delta V_c$ for the turn-ON transition. The same energy is required for the turn-OFF process. So the electric power to compensate for the voltage drop ΔV_c is

$$P_{c\_\rm DPIRGD} = 2f_s C_{gs\_Q}V_c\Delta V_c \tag{4}$$

where f_s is the switching frequency of S_1 and S_2.

S_1-S_3 still produce additional power loss like gate drive loss $P_{g\_\rm DPIRGD}$ and power consumption $P_{\rm Coss\_DPIRGD}$ caused by the output capacitance $C_{\rm oss}$. They can be calculated by

$$P_{g\_\rm DPIRGD} = 4f_s Q_{gs\_S}V_{gs\_S} \tag{5}$$

$$P_{\rm Coss\_DPIRGD} = 5C_{\rm oss}V_c^2 f_s \tag{6}$$

where Q_{gs_S} and V_{gs_S} are the gate charge and gate voltage of S_1-S_3.

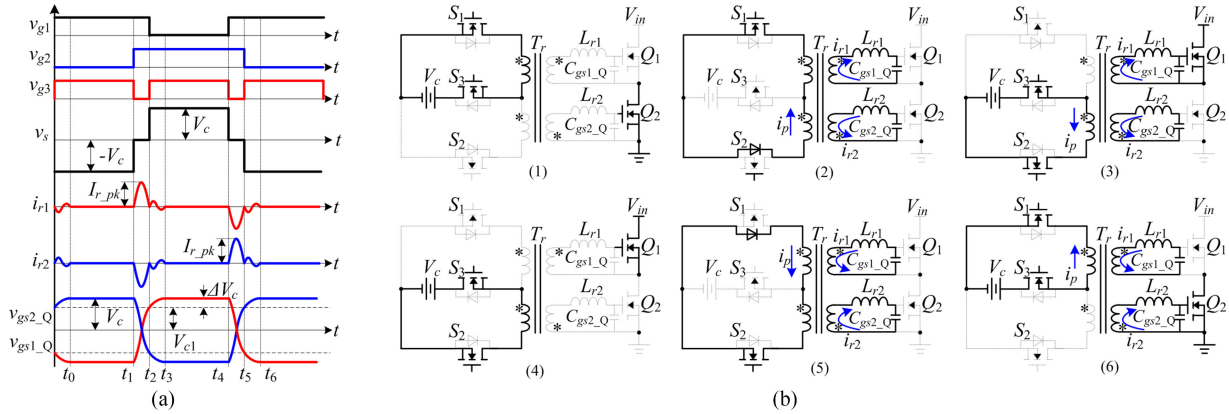

Fig. 2. (a) Key waveforms of the proposed DPIRGD. (b) Equivalent circuits of each interval during one switching cycle: (1) Interval 1 $[t_0 - t_1]$, (2) interval 2 $[t_1 - t_2]$, (3) interval 3 $[t_2 - t_3]$, (4) interval 4 $[t_3 - t_4]$, (5) interval 5 $[t_4 - t_5]$, and (6) interval 6 $[t_5 - t_6]$.

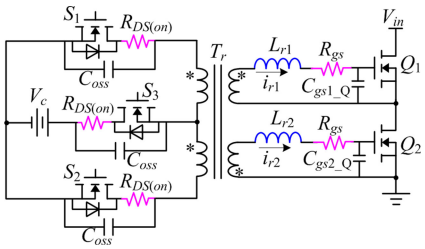

Fig. 3. Power loss model of the proposed DPIRGD.

The core loss of drive HF transformer can be modeled by using the Steinmetz equation

$$P_{Tr\_\mathrm{Core}} = C_m f_s^{\alpha} B_M^{\beta} V_e \tag{7}$$

where C_m, α, and β are coefficients related to core material, B_M is the peak flux density, and V_e is the effective core volume of the core.

The conduction loss of the drive HF transformer can be written by

$$P_{Tr\_\mathrm{Con}} = 4 \cdot I_{r1\_\mathrm{rms}}^2 (R_{\mathrm{DC}} + R_{\mathrm{AC}}) \tag{8}$$

$$I_{r1\_\mathrm{rms}} = \sqrt{\frac{1}{T_s}\int_0^{\frac{\pi}{\omega}} \left[\frac{V_c}{\omega} e^{-\lambda t}\sin(\omega t)\right]^2 dt} \tag{9}$$

where I_{r1_rms} is the RMS current of the winding, and R_{DC} and R_{AC} are dc and ac resistances of windings, respectively. According to the loss model presented in [13], the approximation for the ac resistance R_{AC} of a round conductor of radius r_o and dc resistance R_{DC} can be given by

$$R_{\mathrm{AC}} = R_{\mathrm{DC}}\left(1 + \frac{(r_o/\delta)^4}{48 + 0.8(r_o/\delta)^4}\right) \tag{10}$$

$$\delta = 1/\sqrt{\pi f_s \mu \sigma} \tag{11}$$

where δ is the skin depth, μ is the magnetic permeability, and σ is the conductivity of the conductor material.

Thus, the total drive HF transformer loss is expressed by

$$P_{Tr\_\mathrm{DPIRGD}} = P_{Tr\_\mathrm{Core}} + P_{Tr\_\mathrm{Con}}. \tag{12}$$

From (4)–(12), the total gate drive loss P_{DPIGRD} for driving two MOSFETs in one bridge leg with the proposed DPIRGD is

$$P_{\mathrm{DPIRGD}} = 2P_{c\_\mathrm{DPIRGD}} + P_{g\_\mathrm{DPIRGD}} + P_{\mathrm{Coss\_DPIRGD}} + P_{Tr\_\mathrm{DPIRGD}}. \tag{13}$$

B. Turn-OFF Loss of the Proposed DPIRGD

In ZVS FB converter, there only exists turn-OFF loss in practical circuit during switching procedure for the driven Q_1 and Q_2. The turn-OFF loss $P_{\mathrm{off\_DPIRGD}}$ presented in [11] can be used here due to similar transition, which can be given as

$$P_{\mathrm{off\_DPIRGD}} = [f_s V_{ds} I_d (Q_{pl} - Q_{th} + Q_{gd})]/(2\,|I_{\mathrm{avg}}|) \tag{14}$$

$$|I_{\mathrm{avg}}| = \left(\int_{t_{pl}}^{t_{th}} I_{r\_pk}\sin t dt\right) \Big/ (t_{th} - t_{pl}) \tag{15}$$

where

$$I_{r\_pk} = V_c\sqrt{C_{gs\_Q}/L_r}, t_{pl} = \arccos(V_{p1}/V_c),$$
$$t_{th} = \arccos(V_{th}/V_c). \tag{16}$$

C. Design Consideration

In the proposed DPIRGD, the resonant inductance L_r is the key component, which determines the turn-ON/turn-OFF time and the overall loss of the gate drive loss and turn-OFF loss for the Q_1 and Q_2. Thus, the above two rules need to follow when selecting an optimal resonant inductance.

1) To Ensure Enough Turn-ON/Turn-OFF Time: The value of L_r affects the rising time t_{on} and falling time t_{off} of the driven MOSFET. Fig. 4 shows the t_{on} and t_{off} during the switching transition and the total turn-ON/turn-OFF time t_{sw} can be expressed as

$$t_{\mathrm{sw}} = t_{\mathrm{on}} + t_{\mathrm{off}} \le \pi\sqrt{L_r C_{gs}} \tag{17}$$

where C_{gs_Q} represents the equivalent capacitance [1], which is

$$C_{gs\_Q} = (Q_{g1\_Q} + Q_{g2\_Q})/(V_c + V_{c1}) \tag{18}$$

where Q_{g1_Q} is the gate charge from $-V_c$ to 0 and Q_{g2_Q} is the gate charge from 0 to V_{c1}.

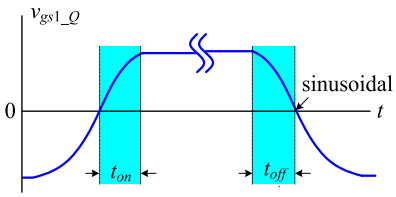

Fig. 4. t_{on} and t_{off} during the switching process.

TABLE I
DESIGN PARAMETERS OF THE PROPOSED DPIRGD

Gate Drive Circuit	Gate drive voltage, V_c	V_c=15 V
	Switching frequency, f_s	f_s=500 kHz
	Drive MOSFET,S_1~S_3	AO3422(Q_{gs_S}=2.6 nC, R_{DS}(on)=160 mΩ, C_{oss}=31 pF)
	Gate drive voltage of S_1~S_3,	V_{gs_S}=4.5 V
	Drive HF transformer	EE13/PC40 (turns ratio 1:1, litz wire with r_o=0.15mm, measured DC resistance 15mΩ)
Converter Topology	Voltage across MOSFET, V_{ds}	180 VDC
	MOSFET turn-off current, I_d	I_d=5.5 A
	Power MOSFET, Q_1~Q_4	IPA50R190CE (V_{ds}=550 V, I_D=24.8 A, V_{th}=3V, V_{pl}=5.4 V)
	Internal gate resistance, R_g	R_g=3 Ω
	Equivalent capacitance, C_{gs_Q}	C_{gs_Q}=3.83 nF
	Gate total charge, Q_{g1_Q}+Q_{g2_Q}	115nC

The required total turn-ON/turn-OFF time t_{sw} for the given MOSFET can be estimated by

$$t_{sw} = \frac{Q_{g1\_Q} + Q_{g2\_Q}}{i_{g\_avg}} = \frac{Q_{g1\_Q} + Q_{g2\_Q}}{\int_0^{\pi} I_{r\_pk} \sin(\omega_r t) d(\omega_r t)}. \quad (19)$$

2) To Minimize the Overall Power Loss: The overall power loss includes the gate drive loss P_{DPIGRD} and switching loss P_{off_DPIRGD} given by (13) and (14). For a pair of MOSFET, the total power consumption for driving two MOSFETs P_{sum} is

$$P_{sum} = 2P_{off\_DPIRGD} + P_{DPIRGD}. \quad (20)$$

A design example is used to demonstrate the optimal considerations above. The parameters are listed in Table I, which agree with the following experimental prototype. Based on the device datasheet, the gate charge $Q_{g1\_Q} + Q_{g2\_Q}$ can be calculated about 115 nC, and the equivalent linear gate capacitance C_{gs_Q} is calculated as 3.83 nF. The internal gate resistance R_g is 3 Ω, which can be regarded as R_p due to mOhm level of the winding resistance plus the bonding resistance. If the average charging current is estimated about 1 A, the required total turn-ON/turn-OFF time t_{sw} can be estimated about 115 ns by (16), (19), and the minimal L_r can be further obtained by (17), i.e., 350 nH. Via using mathematical software Mathcad, from (13), (14), and (20), the P_{DPIGRD}, P_{off_DPIRGD}, and P_{sum} as functions of the resonant inductance L_r can be illustrated as Fig. 5. From Fig. 5, it can be seen that the P_{DPIGRD} is reduced with the increase of L_r, and the decreasing slew rate of P_{DPIGRD} tends to be slow when L_r becomes large. However, as L_r increases,

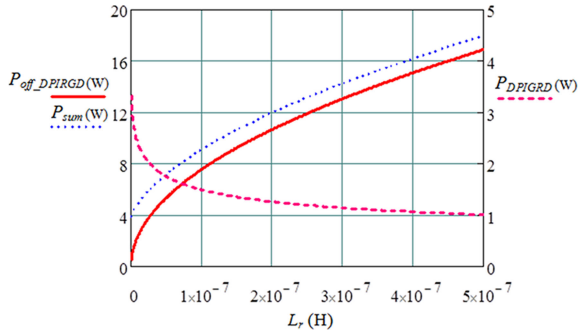

Fig. 5. P_{DPIGRD}, P_{off_DPIRGD}, and P_{sum} as functions of the resonant inductance L_r.

TABLE II
COMPARISON WITH THE REPORTED RGDS SUITABLE FOR THE FB CONVERTER

	RGD in [7]	RGD in [11]	Proposed DPIRGD
Num. of drive switches	16	8	6
Num. of independent DC supplies	4	1	1
Switching of drive switches	ZCS	ZCS	ZCS
Range of gate drive voltage	$-V_c$~$+V_c$	$-V_c$~$+V_c$	$-V_c$~$+V_c$

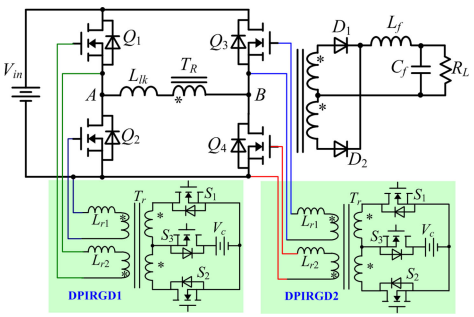

Fig. 6. Schematic of the FB converter with the proposed DPIRGD.

the P_{off_DPIRGD} and P_{sum} also increase because the P_{off_DPIRGD} is the dominate part in comparison with the P_{DPIGRD}. So the resonant inductance L_r should be selected as small as possible to minimize the P_{sum}. Here, the value of L_r is designed about 350 nH.

D. Comparison Between the Proposed DPIRGD and the Reported RGDs for FB Converter

Among the existing RGDs, the topologies presented in [7] and [11] have respective advantages applied in the FB converter at high frequency, and their performance comparison with the proposed DPIRGD is listed in Table II. It can be seen that these three gate-driver topologies are the considerable candidates for the FB converter due to the advantages of ZCS switching of drive switches and negative gate drive voltage preventing the false trigger. However, the RGD in [7] needs 16 drive switches and four independent dc supplies and the RGD in [11] requires eight drive switches and one indepen-

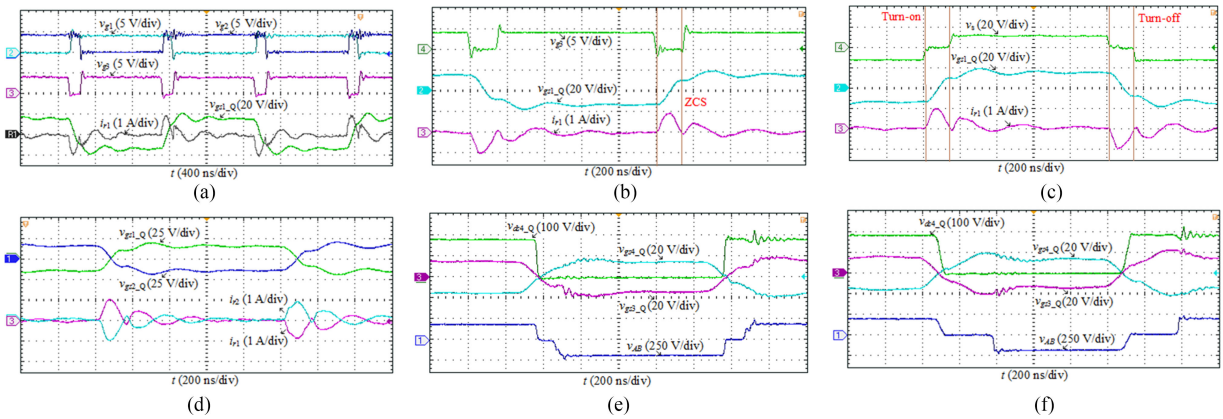

Fig. 7. Measured key waveforms of the prototype. (a) $v_{g1} - v_{g3}$, i_{r1}, and v_{gs1_Q}. (b) v_{g3}, i_{r1}, and v_{gs1_Q}. (c) v_s, i_{r1}, and v_{gs1_Q}. (d) v_{gs1_Q}, v_{gs2_Q}, and i_{r1}, i_{r2}. (e) v_{gs3_Q}, v_{gs4_Q}, v_{ds4_Q}, and v_{AB} under full load and $V_{in} = 180$ V. (f) v_{gs3_Q}, v_{gs4_Q}, v_{ds4_Q}, and v_{AB} under 1/2 load at $V_{in} = 190$ V.

dent dc supply for an FB converter. Note that the proposed DPIRGD only needs six drive switches and one independent dc supply. Obviously, this can minimize the cost and increase the reliability.

IV. Experimental Results

To verify the proposed DPIRGD strategy, one 180–190–V dc input, 48-V dc/10-A output, and 500-kHz ZVS phase-shifted FB converter prototype with this DPIRGD has been built. The schematic of this prototype is shown in Fig. 6. Some specifications are listed in Table I. In addition, the turns ratio of HF transformer T_R is 3:1; the output inductance L_f is 20 μH; the output capacitance C_f is 100 V/2200 μF; and the rectifier diode DSSK60-02A is adopted and the resonant inductors L_{r1} and L_{r2} utilize the leakage inductance of the drive HF transformer, which are measured about 352 and 353 nH, respectively.

The key experimental waveforms have been tested with the proposed DPIRGD. Fig. 7(a) shows the waveforms of v_{g1}–v_{g3}, i_{r1}, and v_{gs1_Q}. i_{r1} and v_{gs1_Q} are sinusoidal, which coincide well with the theoretically waveforms shown in Fig. 2(a). Fig. 7(b) illustrates the waveforms of v_{g3}, i_{r1}, and v_{gs1_Q}. It is observed that the half resonant period is about 120 ns, which nearly matches with the designed value. In addition, S_3 can realize ZCS turn ON/OFF. This implies that S_1 and S_2 can also achieve ZCS turn ON/OFF due to its switching after S_3. Fig. 7(c) shows the relationship between the v_s, i_{r1}, and v_{gs1_Q}. Obviously, it can be seen that the resonance only happens during the interval of $v_s = 0$. In this stage, the proposed DPIRGD utilizes the *LC* resonance to recycle the gate electrical energy of the driven switch, and, therefore, the gate drive loss can be reduced significantly compared to the conventional VSDs. Fig. 7(d) shows the waveforms of i_{r1}, i_{r2} and v_{gs1_Q} and v_{gs2_Q}. It is observed that the v_{gs1_Q} and v_{gs2_Q} are complementary and the i_{r1} and i_{r2} are exactly opposite. The negative voltage is -15 V improving the reliability. Also, there is no voltage overlap between the v_{gs1_Q} and v_{gs2_Q} implying that the short-through issue can be eliminated in the FB converter. This waveform shows that the proposed DPIRGD can drive two switches in one bridge leg with the simple circuit structure. Fig. 7(e) illustrates the lagging leg of ZVS phase-shifted FB converter gate drive voltages v_{gs3_Q} and v_{gs4_Q}, drain-source voltage v_{ds4_Q}, and the winding voltage v_{AB} of the transformer under the full load with input voltage $V_{in} = 180$ V. It is observed that the v_{ds4_Q} reaches 0, and then, the v_{gs4_Q} is applied to turn-ON Q_4 with ZVS. Fig. 7(f) shows that under 1/2 load with the input voltage $V_{in} = 190$ V. These waveforms show that the voltage v_{AB} is modulated by the phase-shifted strategy. Note that the Q_4 loses ZVS turn ON due to small energy stored in the leakage inductance of transformer, which agree the features of the widely used ZVS FB converter.

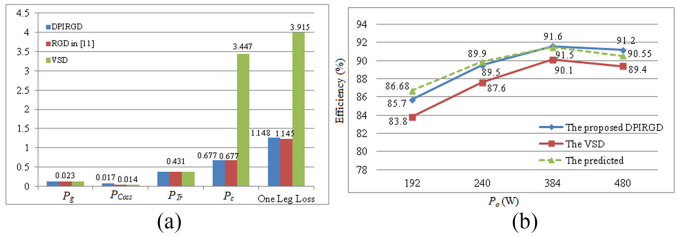

Fig. 8. (a) Gate drive loss comparison. (b) Overall efficiency comparison.

Based on the aforementioned loss model and the loss calculated models in [11], Fig. 8(a) shows the corresponding gate drive loss distribution regarding the same specifications in Table I. It shows that the proposed DPIRGD has the similar gate drive loss with the RGD presented in [11] and both of them achieve nearly 70.7% reduction in gate drive loss compared to the conventional transformer coupled VSD. However, the proposed DPIRGD uses three instead of four small-rated drive switches adopted in [11], which imply that it can reduce the corresponding gate driver and control source, further reduce the drive cost, and increase the reliability for high frequency ZVS FB converters.

Fig. 8(b) shows the tested and calculated overall efficiency comparison between the proposed DPIRGE and the conventional VSD transformer coupled shown in [11] under V_{in}=180 V, $V_o = 48$ V, and $f_s = 500$ kHz. It can be seen at 480 W, the effi-

ciency can be improved from 89.4% to 91.2% (an improvement of 1.8%). Also, it can be observed that the tested values coincide with the predicted values approximately and the proposed DPIRGD has higher efficiency in overall load range in comparison with the conventional VSD.

V. Conclusion

A new DPIGRD for a pair of MOSFET is proposed. The proposed DPIRGD can provide two complementary gate drive signals driving two MOSFETs with the negative gate voltage, which prevent the short-through problem and improve the turn-OFF reliability. The working principle, loss analysis, optimal design, and comparison study with the similar RGDs for the FB converter are discussed. Finally, one 180–190-V input, 48-V output, and 500-kHz ZVS phase-shifted FB converter with the proposed DPIRGD was built to verify the effectiveness. In comparison with the conventional VSD, the efficiency of this proposed DPIRGD achieves an improvement of 1.8% at full load, and realizes nearly 70.7% reduction in gate drive loss.

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