DC–DC Boost Converter With a Wide Input Range and High Voltage Gain for Fuel Cell Vehicles

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***Abstract*—In fuel cell vehicles, the output voltage of the fuel cell source is typically much lower than the voltage required by the dc bus, and also this output voltage drops significantly as the output current increases. In order to match the output voltage of the fuel cell source to the dc bus voltage, a new dc–dc boost converter with a wide input range and high voltage gain is proposed to act as the required power interface, which reduces voltage stress across the power devices and operates with an acceptable conversion efficiency. A prototype rated at 300 W/400 V has been developed and the maximum efficiency of the proposed converter was measured as 95.01% at 300 W. Experimental results are presented to validate the effectiveness of the proposed converter.**

***Index Terms*—Boost dc–dc converter, fuel cell vehicles, high voltage gain, switched-capacitor (SC), wide input range.**

I. Introduction

AS NONRENEWABLE resources such as oil, gas, and coal become scarce, more and more research is focused on the problem of high energy usage and society's dependence on fossil fuels [1]–[3]. Additionally, the number of automobiles continues to increase in most countries, causing a significant rise in air pollution. Vehicles powered by fuel cell sources may help to reduce transport's dependence on oil and reduce polluting emissions [4]. The fuel cells can utilize hydrogen or natural gas, to achieve a high energy density, and can potentially generate "clean" electricity with high efficiency. However, unlike batteries, which have a fairly constant output voltage, the output voltage of fuel cells drops significantly with an increase of

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the difference in potential between the ground points of the input voltage source side and the load side is a high-frequency pulsewidth modulation voltage, because instead of a common ground structure, there is a diode located between the ground points of the input voltage source side and the load side. As a result, it may introduce issues associated with *du*/*dt* and these may limit its applications [21], [22].

The Z-source dc–dc boost converter has the potential for a high voltage gain. A Z-source dc–dc converter with a cascaded SC has been presented in [23]. This topology can improve the voltage gain of the Z-source dc–dc boost converter by using the voltage multiplier function of the SC. However, the drawbacks of the converter are obvious, such as the penalty of the discontinuous input current and the different ground points between the input voltage source side and the load side. Moreover, the power semiconductors will see a high voltage stress when the duty cycle approaches zero. In a similar way, switched-inductor techniques can also be used in dc–dc converters to achieve a high voltage gain as presented in [24] and [25], but they often need large numbers of inductors. Therefore, the volume and cost of these converters will be increased.

To address these issues, a new nonisolated high ratio step-up dc–dc converter is proposed in this paper, which has the following features.

1) It reduces the voltage stress across the power devices and has a common ground between the input and output sides.
2) The two power switches turn ON and OFF simultaneously. As a result, the control of the converter is simple, and power switches with low ON-state resistance can be employed.
3) The system operates with a high voltage gain and a wide input voltage range and does not use any extreme values for its duty cycle.

This paper is organized as follows. In Section II, the configuration and operating principles of the proposed converter are presented. The voltage gain is analyzed in Section III. In Section IV, the voltage and current stresses are calculated. The design of the components is presented in Section V, and in Section VI, the dynamic modeling is established. Experimental results and analysis are presented in Section VII to validate the features of the proposed converter. Section VIII presents the conclusion.

II. Operating Principles of the Proposed Converter

A. Configuration of the Proposed Converter

The high voltage gain dc–dc boost converter is shown in Fig. 1. It comprises two active power switches (Q_1 and Q_2), five power diodes (D_3–D_7), two inductors (L_1 and L_2), and five capacitors (C_1–C_5). The fuel-cell source U_{in} and the inductor L_1 are connected in series to charge capacitors C_1 and C_2 in parallel. Inductor L_2 is another energy storage component that is used to realize a high voltage gain. The ladder-type voltage multiplier (capacitors C_3–C_5 and diodes D_5–D_7) can improve the voltage gain further and reduces the voltage stress across the power semiconductors on the high voltage side.

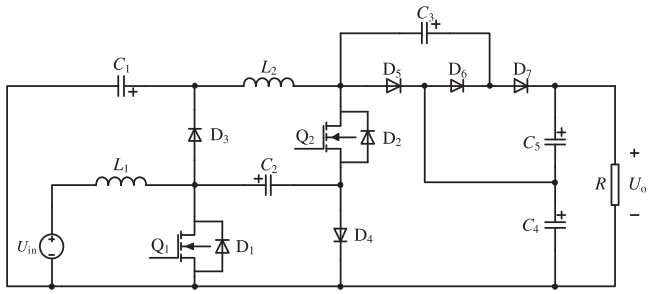

Fig. 1. Topology of the proposed converter.

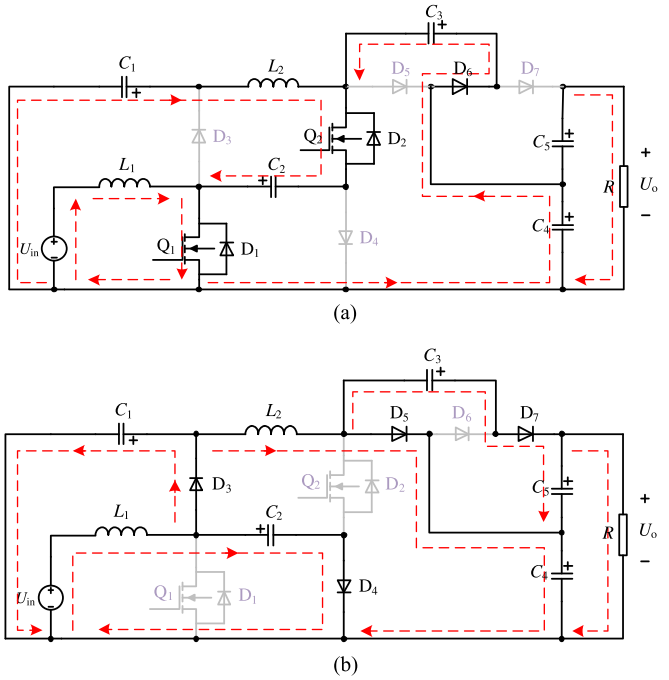

Fig. 2. Switching states of the proposed converter. (a) Switching state I. (b) Switching state II.

B. Operating Principles of the Proposed Converter

The gate signals of the two power switches (Q_1, Q_2) are identical—Q_1 and Q_2 are turned ON and OFF simultaneously. Therefore, there are two switching states in each switching period, which are shown in Fig. 2.

1) *Switching state I*. As shown in Fig. 2(a), Q_1 and Q_2 turn ON, L_1 is charged by the dc source U_{in} (i.e., U_{in}–L_1–Q_1), and L_2 is charged by C_1 and C_2 in series (i.e., C_1–L_2–Q_2–C_2–Q_1). Meanwhile, C_3 is charged by C_2 and C_4 in series (i.e., C_4–D_6–C_3–Q_2–C_2–Q_1).
2) *Switching state II*. As shown in Fig. 2(b), Q_1 and Q_2 turn OFF, C_1 and C_2 are charged in parallel by the dc source and L_1 (i.e., U_{in}–L_1–D_3–C_1, and U_{in}–L_1–C_2–D_4). At the same time, C_4 is charged by the dc source, L_1, and L_2 in series (i.e., U_{in}–L_1–D_3–L_2–D_5–C_4). In addition, C_4 and C_5 are charged by the dc source, L_1, L_2, and C_3 (i.e., U_{in}–L_1–D_3–L_2–C_3–D_7–C_5–C_4), as well as through the load *R*. The output voltage U_o is equal to the total voltages across C_4 and C_5.

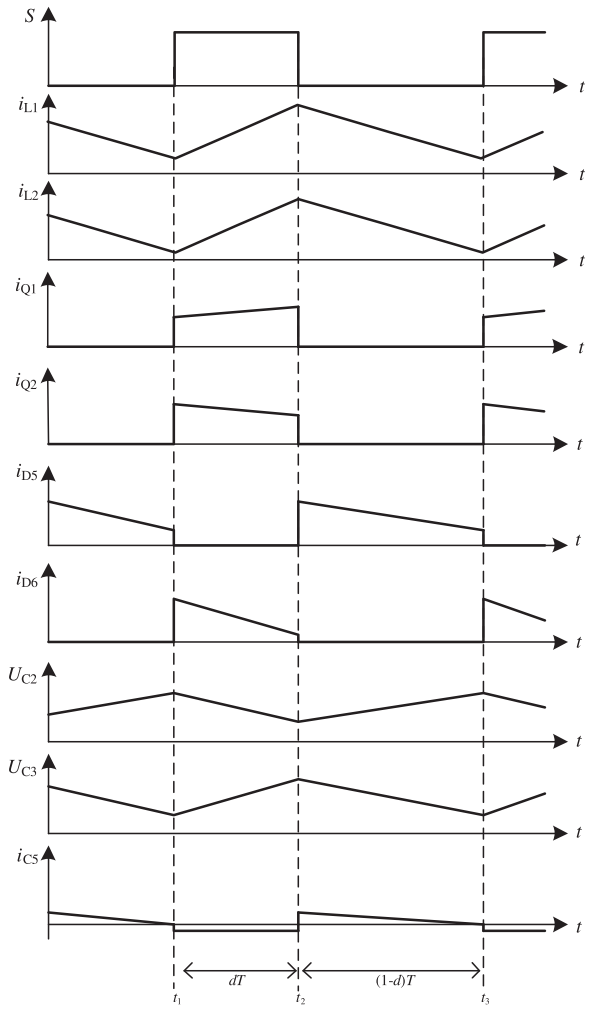

Fig. 3. Key operating waveforms of the proposed converter.

According to the key operating waveforms of the proposed converter shown in Fig. 3, the inductor currents i_{L1} and i_{L2} have the same energy transfer process. When $S = 1$, power switches Q_1, Q_2 and diode D_6 are turned ON. The current i_{Q1} increases linearly, while i_{Q2} and i_{D6} decrease linearly. The output capacitor current i_{C5} is negative, which means C_5 is discharged. When $S = 0$, power switches Q_1, Q_2, and diode D_6 are turned OFF. The currents i_{D5} and i_{C5} decrease linearly. The capacitor voltage fluctuations reflect the charging and discharging processes. It can be seen from the capacitor voltages U_{C2} and U_{C3} that capacitors C_2 and C_3 have the opposite charging and discharging states.

III. Steady-State Voltage Gain Analysis

If the switching period for the power switches is *T,* then *dT* is the ON-state period, and (1 – *d*) *T* is the OFF-state period, where *d* is the duty cycle of the power switches. It is assumed that the capacitor voltage and the inductor current are constant during each switching period, and the forward voltage drop and the ON-state resistance of the power semiconductors are ignored.

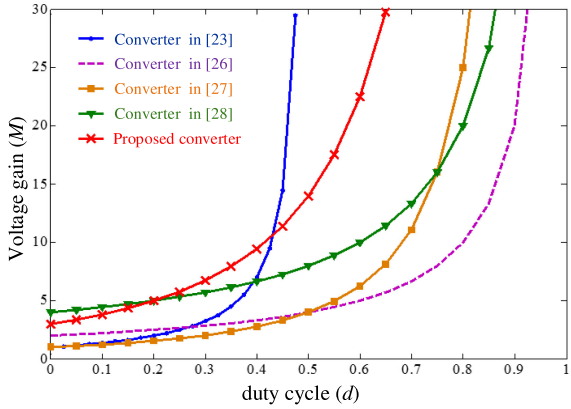

Fig. 4. Comparisons of voltage gain as a function of the duty cycle for different converter topologies.

The following equation can be derived according to the volt-second balance principle for inductors L_1 and L_2:

$$\begin{cases} U_{\text{in}} \times dT + (U_{\text{in}} - U_{C2}) \times (1-d)T = 0 \\ (U_{C1} + U_{C2}) \times dT + (U_{C2} - U_{C4}) \times (1-d)T = 0. \end{cases} \tag{1}$$

The voltage relationship between the output and capacitor voltages can be found, in terms of the two switching states, which are shown in Fig. 2.

$$\begin{cases} U_{C1} = U_{C2} \\ U_{C3} = U_{C5} = U_{C2} + U_{C4} \\ U_o = U_{C4} + U_{C5} \end{cases} \tag{2}$$

As a result, the output voltage U_o can be obtained from (1) and (2) as follows:

$$U_o = \frac{3+d}{(1-d)^2} U_{\text{in}} = M \times U_{\text{in}} \tag{3}$$

where *M* is the conversion ratio, i.e., the voltage gain. Equation (3) shows that the proposed converter can theoretically obtain a high and wide voltage gain range. The voltage gain as a function of the duty cycle for the proposed converter has been compared to the converters in [23] and [26]–[28], and these are shown in Fig. 4. It can be concluded that the voltage gain of the proposed converter is higher than the converters in [26]–[28], especially when $d > 0.2$. Although the converter in [23] has a better voltage gain curve, the low conversion efficiency and the noncommon ground will cause more power losses and increased *du*/*dt* issues, which is analyzed in Table III. Considering the voltage gain, the efficiency, and the common ground together, the proposed converter in this paper has the advantages of a high and wide voltage gain range, an acceptable conversion efficiency, and a common ground.

TABLE I
VOLTAGE STRESSES ACROSS THE POWER DEVICES

Component	Q_1	Q_2	D_3	D_4
Voltage stress	$\frac{1-d}{3+d}U_o$	$\frac{1+d}{3+d}U_o$	$\frac{1-d}{3+d}U_o$	$\frac{1-d}{3+d}U_o$
Component	D_5	D_6	D_7	C_1
Voltage stress	$\frac{2}{3+d}U_o$	$\frac{2}{3+d}U_o$	$\frac{2}{3+d}U_o$	$\frac{1-d}{3+d}U_o$
Component	C_2	C_3	C_4	C_5
Voltage stress	$\frac{1-d}{3+d}U_o$	$\frac{2}{3+d}U_o$	$\frac{1+d}{3+d}U_o$	$\frac{2}{3+d}U_o$

TABLE II
CURRENT STRESSES ACROSS THE POWER DEVICES

Component	Q_1	Q_2	D_3	D_4
Current stress	$\frac{1+3d-d^2-d^3}{d(1-d)^2}I_o$	$\frac{1+d}{d(1-d)}I_o$	$\frac{2}{(1-d)^2}I_o$	$\frac{1+d}{(1-d)^2}I_o$
Component	D_5	D_6	D_7	C_1
Current stress	$\frac{1}{1-d}I_o$	$\frac{1}{d}I_o$	$\frac{1}{1-d}I_o$	$\frac{\sqrt{4d-4d^2}}{(1-d)^2}I_o$
Component	C_2	C_3	C_4	C_5
Current stress	$\frac{1+d}{\sqrt{d(1-d)^3}}I_o$	$\frac{1}{\sqrt{d(1-d)}}I_o$	$\frac{1+d}{\sqrt{d(1-d)}}I_o$	$\sqrt{\frac{d}{1-d}}I_o$

IV. ANALYSIS OF COMPONENT ELECTRICAL STRESS

A. Voltage Stress Analysis

According to the analysis of each of the operation states in Fig. 2 and the voltage gain in (3), the voltage stresses across the power devices can be deduced, as shown in Table I.

Therefore, the voltage stresses across the active power switches Q_1 and Q_2 are less than half of the output voltage U_o. For diodes D_3 and D_4, the voltage stresses are less than one-third of U_o, whilst the voltage stresses across D_5–D_7 are less than two thirds of U_o, as well as the voltage stresses across capacitors C_1–C_5. The voltage stresses across C_1 and C_2 are less than one-third of U_o. The voltage stress across C_4 is less than half of the output high voltage U_o, whilst the voltage stresses across C_3 and C_5 are less than two thirds of U_o.

B. Current Stress Analysis

Using the current analysis in Fig. 2 and Kirchhoff's current laws, the current stresses across the power devices can also be obtained, as shown in Table II.

The current stresses across the power devices are related to the operating duty cycle d (usually between 0.2 and 0.4). For instance, the maximum current stress across active power switch Q_2 is $7.5I_o$. Therefore, it can be used as a reference in the component parameters design section. Note also that the current stresses across Q_1–D_7 are mean values, the current stresses across capacitors C_1–C_5 are root mean square values.

The comparison of the proposed converter with other existing high voltage gain dc–dc boost converters is shown in Table III. It can be seen that the proposed converter achieves a high and wide voltage gain range by increasing the number of diodes by a small amount. The converter in [23] can achieve a high voltage gain when the duty cycle approaches 0.5, but the converter will suffer from a high voltage stress, which is almost equal to the output voltage when the duty cycle d is close to zero. In addition, the converter in [23] has a poor efficiency compared to the other converters. Compared with the converters in [26] and [27], the proposed converter is more suitable for applications requiring a large step-up ratio. Considering the selection of the power switches, the converter in [27] will have its maximum device voltage stress (which is higher than half of the output voltage) when $d \neq 0.5$, whereas the maximum voltage stress across the power switches is less than half of the output voltage in the proposed converter. Considering the selection of the diodes, the maximum voltage stress across the diodes for the proposed converter is lower than that of the converters in [26] and [27]. Although the converter in [28] has the advantage of the lower voltage stress, it does not have a common ground between the input and the output sides and this may cause additional *du/dt* issues.

V. COMPONENT PARAMETERS DESIGN

A. Design of the Power Switches and Diodes

The design of the power switches and diodes should refer to the most severe conditions that the semiconductor devices will operate in. Assuming that the maximum required voltage gain is 10 and the load power is 400 W, the duty cycle d and the output current I_o can be obtained as follows:

$$\begin{cases} d = 0.42 \\ U_o = 400 \text{ V} \\ I_o = 1 \text{ A}. \end{cases} \tag{4}$$

It can be deduced from Tables I and II that the maximum mean voltage stresses across Q_1 and Q_2 are 70 and 166 V, respectively, and the maximum mean current stresses on Q_1 and Q_2 are 16.5 and 6.2 A, respectively. Similarly, it can be derived from Tables I and II that the maximum mean voltage stress across D_3 and D_4 is 70 V, which is equal to that of Q_1. In addition, the maximum mean current stress on D_3 and D_4 is 5.8 A, and the maximum mean voltage and current stresses on D_5–D_7 are 234 V and 1.9 A, respectively.

B. Design of the Inductors and Capacitors

Assuming that the maximum required current ripple in the inductors is ΔI_L, the inductances can be calculated when L is in the charging state as follows:

$$L = u_L \frac{dt}{di_L} \tag{5}$$

TABLE III
COMPARISONS AMONG THE PROPOSED CONVERTER AND OTHER HIGH VOLTAGE GAIN CONVERTERS

Topology	Converter in [23]	Converter in [26]	Converter in [27]	Converter in [28]	Proposed converter
Number of power switches	1	1	2	2	2
Number of diodes	3	2	2	4	5
Number of inductors	3	2	2	2	2
Number of capacitors	5	3	2	4	5
Voltage-gain	(1+*d*)/(1-2*d*)	2/(1-*d*)	1/(1-*d*)^2	4/(1-*d*)	(3+*d*)/(1-*d*)^2
Maximum voltage stress across power switches	U_o/(1+*d*)	U_o	dU_o or (1-*d*)U_o	U_o/4	(1+*d*)U_o/(3+*d*)
Maximum voltage stress across diodes	U_o/(1+*d*)	U_o	U_o	U_o/2	2U_o/(3+*d*)
Common ground	No	Yes	Yes	No	Yes
Conversion efficiency	50.2%~80.4%	88%~95%	88%~93%	94.32%~96.05%	90.06%~95.01%

where $di_L = \Delta I_L$, $dt = d \times T = d/f_s$ (f_s is the switching frequency). The inductances of L_1 and L_2 can be derived as

$$\begin{cases} L_1 = \frac{d \times U_{\text{in}}}{\Delta I_{L1} \times f_s} \\ L_2 = \frac{4d \times U_{\text{in}}}{(1-d)^2 \times \Delta I_{L2} \times f_s}. \end{cases} \tag{6}$$

If it is assumed that the maximum acceptable voltage ripple across the capacitor is ΔU_c, the capacitances of the five capacitors in the proposed converter can be calculated as

$$C = i_C \frac{dt}{du_C} \tag{7}$$

where $\mathrm{d}t = d \times T = d/f_s$, i_c is the corresponding current flowing through the capacitor, C is the capacitance, and $du_c = \Delta U_c$. The capacitances of the five capacitors can be calculated as

$$\begin{cases} C_1 = \frac{2d \times I_o}{(1-d) \times \Delta U_{C1} \times f_s} \\ C_2 = \frac{(1+d) \times I_o}{(1-d) \times \Delta U_{C2} \times f_s} \\ C_3 = \frac{I_o}{\Delta U_{C3} \times f_s} \\ C_4 = \frac{(1+d) \times I_o}{\Delta U_{C4} \times f_s} \\ C_5 = \frac{d \times I_o}{\Delta U_{C5} \times f_s}. \end{cases} \tag{8}$$

VI. DYNAMIC MODELING

It is assumed that the power semiconductors, inductors, and capacitors are analyzed for operation under ideal conditions. The average model and the small-signal model can be obtained by using the state-space averaging method [29]–[31]. The capacitances are set such that $C_1 = C_2 = C_3 = C_4 = C_5 = C$ to simplify the analysis. The inductances are defined as L_1 and L_2,

$$\begin{cases} \begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{du_{C1}(t)}{dt} \\ \frac{du_{C2}(t)}{dt} \\ \frac{du_{C3}(t)}{dt} \\ \frac{du_{C4}(t)}{dt} \\ \frac{du_{C5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-r}{L_2} & \frac{1}{L_2} & \frac{1}{L_2} & 0 & 0 & 0 \\ 0 & -\frac{1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C} & 0 & -\frac{1}{Cr} & \frac{1}{Cr} & -\frac{1}{Cr} & 0 \\ 0 & 0 & 0 & \frac{1}{Cr} & -\frac{1}{Cr} & \frac{1}{Cr} & 0 \\ 0 & 0 & 0 & -\frac{1}{Cr} & \frac{1}{Cr} & -\frac{R+r}{CRr} & -\frac{1}{CR} \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{CR} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{\text{in}}(t) \\ u_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & u_{C1}(t) & u_{C2}(t) & u_{C3}(t) & u_{C4}(t) & u_{C5}(t) \end{bmatrix}^T \end{cases} \tag{9}$$

the load resistance is R, and $u_{\text{in}}(t)$, $u_o(t)$, and d are the input variable, the output variable, and the control variable, respectively. $i_{L1}(t)$, $i_{L2}(t)$, $u_{C1}(t)$, $u_{C2}(t)$, $u_{C3}(t)$, $u_{C4}(t)$, and $u_{C5}(t)$ are the state variables. According to Fig. 2(a), C_2, C_3, and C_4 are connected in series in the loop circuit when Q_1 and Q_2 turn ON. It means the sum of voltages across C_2, C_3, and C_4 is 0. There is an invalid state variable ($u_{C2}(t) + u_{C3}(t) + u_{C4}(t) = 0$, i.e., there are only two independent variables) in this loop circuit. By including the equivalent series resistance (e.g., $r_1 = r = 0.1\,\Omega$) in the same loop circuit, the coupling among C_2, C_3, and C_4 can be removed to avoid the invalid state variable. Similarly, as shown in Fig. 2(b), C_1 and C_2 are connected in parallel when Q_1 and Q_2 turn OFF, and this means the voltages across C_1 and C_2 should be equal, i.e., there is another invalid state variable. The coupling relationship between C_1 and C_2 can also be removed to avoid the invalid state variable ($u_{C1}(t) + u_{C2}(t) = 0$), by including the equivalent series resistance (e.g., $r_2 = r = 0.1\,\Omega$) in the loop circuits.

When $S = 1$, the ON-state period is $d \times T$, and the state space average model can be obtained as (9) shown at the bottom of the previous page.

When $S = 0$, the OFF-state period is $(1 - d) \times T$, and the state space average model can be written as (10) shown at the bottom of this page.

Combining (9) with (10), the average model of the converter can be obtained as (11) shown at the bottom of this page.

The state variables, the input variable, the output variable, and the control variable can be described by the small-signal disturbance variables as

$$\begin{cases} i_{L1}(t) = I_{L1} + \hat{i}_{L1}(t) \\ i_{L2}(t) = I_{L2} + \hat{i}_{L2}(t) \\ u_{C1}(t) = U_{C1} + \hat{u}_{C1}(t) \\ u_{C2}(t) = U_{C2} + \hat{u}_{C2}(t) \\ u_{C3}(t) = U_{C3} + \hat{u}_{C3}(t) \\ u_{C4}(t) = U_{C4} + \hat{u}_{C4}(t) \\ u_{C5}(t) = U_{C5} + \hat{u}_{C5}(t) \\ u_{\text{in}}(t) = U_{\text{in}} + \hat{u}_{\text{in}}(t) \\ u_o(t) = U_o + \hat{u}_o(t) \\ d = D + \hat{d} \end{cases} \tag{12}$$

where I_{L1}, I_{L2}, U_{C1}, U_{C2}, U_{C3}, U_{C4}, U_{C5}, U_{in}, U_o, and D are the steady-state components, and $\hat{i}_{L1}(t)$, $\hat{i}_{L2}(t)$, $\hat{u}_{C1}(t)$, $\hat{u}_{C2}(t)$, $\hat{u}_{C3}(t)$, $\hat{u}_{C4}(t)$, $\hat{u}_{C5}(t)$, $\hat{u}_{\text{in}}(t)$, $\hat{u}_o(t)$, and $\hat{d}$ are the corresponding small-signal disturbance variables. Therefore, from (11) and (12), the small-signal model of the converter can be written as (13) shown at the bottom of next page.

Using (13) and the experimental parameters shown in Table IV, when the duty cycle $d = 0.4$, the control-to-output transfer function can be transformed from the time domain to

$$\begin{cases} \begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{du_{C1}(t)}{dt} \\ \frac{du_{C2}(t)}{dt} \\ \frac{du_{C3}(t)}{dt} \\ \frac{du_{C4}(t)}{dt} \\ \frac{du_{C5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & -\frac{1}{L_2} & 0 \\ 0 & 0 & -\frac{1}{Cr} & \frac{1}{Cr} & 0 & 0 & 0 \\ \frac{1}{C} & -\frac{1}{C} & \frac{1}{Cr} & -\frac{1}{Cr} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{Cr} & 0 & \frac{1}{Cr} \\ 0 & \frac{1}{C} & 0 & 0 & 0 & -\frac{1}{CR} & -\frac{1}{CR} \\ 0 & 0 & 0 & 0 & \frac{1}{Cr} & -\frac{1}{CR} & -\frac{R+r}{CRr} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{\text{in}}(t) \\ u_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & u_{C1}(t) & u_{C2}(t) & u_{C3}(t) & u_{C4}(t) & u_{C5}(t) \end{bmatrix}^T \end{cases} \tag{10}$$

$$\begin{cases} \begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{du_{C1}(t)}{dt} \\ \frac{du_{C2}(t)}{dt} \\ \frac{du_{C3}(t)}{dt} \\ \frac{du_{C4}(t)}{dt} \\ \frac{du_{C5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{d-1}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{rd}{L_2} & \frac{d}{L_2} & \frac{1}{L_2} & 0 & \frac{d-1}{L_2} & 0 \\ 0 & -\frac{d}{C} & \frac{d-1}{Cr} & \frac{1-d}{Cr} & 0 & 0 & 0 \\ \frac{1-d}{C} & -\frac{1}{C} & \frac{1-d}{Cr} & -\frac{1}{Cr} & \frac{d}{Cr} & -\frac{d}{Cr} & 0 \\ 0 & 0 & 0 & \frac{d}{Cr} & -\frac{1}{Cr} & \frac{d}{Cr} & \frac{1-d}{Cr} \\ 0 & \frac{1-d}{C} & 0 & -\frac{d}{Cr} & \frac{d}{Cr} & \left[-\frac{1}{CR} - \frac{d}{Cr}\right] & -\frac{1}{CR} \\ 0 & 0 & 0 & 0 & \frac{1-d}{Cr} & -\frac{1}{CR} & \left[\frac{d}{Cr} - \frac{R+r}{CRr}\right] \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{\text{in}}(t) \\ u_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & u_{C1}(t) & u_{C2}(t) & u_{C3}(t) & u_{C4}(t) & u_{C5}(t) \end{bmatrix}^T \end{cases} \tag{11}$$

TABLE IV
EXPERIMENTAL PARAMETERS

Component	parameter	Cost
Input voltage (U_{in})	40~80 V	
Output voltage (U_o)	400 V	
Rated power	300 W	
Switching frequency (fs)	20 kHz	
Power switch Q_1	IRFP250N	\$2.43
Power switch Q_2	IXTH88N30P	\$10.48
Diode D_3/ D_4	DSEC60-03A	\$2.53×2
Diode D_5/ D_6/ D_7	DPF60IM400HB	\$3.47×3
Electrolytic capacitor C_1/ C_2	540 μF	\$0.95×4
Film capacitor C_3/ C_5	20 μF	\$3.8×2
Film capacitor C_4	40 μF	\$6.32
Inductor L_1	330 μH	\$6.8
Inductor L_2	1 m H	\$7.28
Other cost (PCB, heat sink, power supply etc.): \$30		
Total cost: \$90		

the complex frequency domain as in (14) shown at the bottom of this page.

And the zero-pole modeling of the control-to-output transfer function can be obtained as in (15) shown at the bottom of this page.

It is usually necessary to reduce the order of the dynamic model (keeping a reasonable approximation) to simplify further analysis. Therefore, (15) can be reduced as follows from the seventh to the fifth order by appropriate pole-zero cancellation: (16) shown at the bottom of next page.

The Bode diagram of the proposed converter is shown in Fig. 5. It can be seen that the curves of the original and the simplified model are approximately the same. In order to achieve stable operation, a voltage loop PI controller needs to be designed and this is now described.

Based on (16), the voltage loop control scheme for the proposed converter can be obtained, as shown in Fig. 6. $G'_{\mathrm{ZPK}}(s)$ is the transfer function of the converter, $G_c(s)$ is the voltage

$$
\begin{cases}
\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{u}_{C1}(t)}{dt} \\ \frac{d\hat{u}_{C2}(t)}{dt} \\ \frac{d\hat{u}_{C3}(t)}{dt} \\ \frac{d\hat{u}_{C4}(t)}{dt} \\ \frac{d\hat{u}_{C5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{d-1}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{rd}{L_2} & \frac{d}{L_2} & \frac{1}{L_2} & 0 & \frac{d-1}{L_2} & 0 \\ 0 & -\frac{d}{C} & \frac{d-1}{Cr} & \frac{1-d}{Cr} & 0 & 0 & 0 \\ \frac{1-d}{C} & -\frac{1}{C} & \frac{1-d}{Cr} & -\frac{1}{Cr} & \frac{d}{Cr} & -\frac{d}{Cr} & 0 \\ 0 & 0 & 0 & \frac{d}{Cr} & -\frac{1}{Cr} & \frac{d}{Cr} & \frac{1-d}{Cr} \\ 0 & \frac{1-d}{C} & 0 & -\frac{d}{Cr} & \frac{d}{Cr} & \left[-\frac{1}{CR}-\frac{d}{Cr}\right] & -\frac{1}{CR} \\ 0 & 0 & 0 & 0 & \frac{1-d}{Cr} & -\frac{1}{CR} & \left[\frac{d}{Cr}-\frac{R+r}{CRr}\right] \end{bmatrix} \begin{bmatrix} \\ \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{u}_{C1}(t) \\ \hat{u}_{C2}(t)\hat{u}_{C3}(t) \\ \hat{u}_{C4}(t) \\ \hat{u}_{C5}(t) \end{bmatrix} \\
+ \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{u}_{\mathrm{in}}(t) + \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{r}{L_2} & \frac{1}{L_2} & 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C} & \frac{1}{Cr} & -\frac{1}{Cr} & 0 & 0 & 0 \\ -\frac{1}{C} & 0 & -\frac{1}{Cr} & 0 & \frac{1}{Cr} & -\frac{1}{Cr} & 0 \\ 0 & 0 & 0 & \frac{1}{Cr} & 0 & \frac{1}{Cr} & -\frac{1}{Cr} \\ 0 & -\frac{1}{C} & 0 & -\frac{1}{Cr} & \frac{1}{Cr} & -\frac{1}{Cr} & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{Cr} & 0 & \frac{1}{Cr} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ U_{C1} \\ U_{C2} \\ U_{C3} \\ U_{C4} \\ U_{C5} \end{bmatrix} \hat{d} \\
\hat{u}_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) & \hat{i}_{L2}(t) & \hat{u}_{C1}(t) & \hat{u}_{C2}(t) & \hat{u}_{C3}(t) & \hat{u}_{C4}(t) & \hat{u}_{C5}(t) \end{bmatrix}^T
\end{cases}
\tag{13}
$$

$$
G_{u_o d}(s) = \left.\frac{\hat{u}_o(s)}{\hat{d}(s)}\right|_{\hat{u}_{\mathrm{in}}(s)=0} = \frac{-5.7\times10^{-20}s^6 - 7.1\times10^{-15}s^5 - 1.6\times10^{-10}s^4 + 5.9\times10^{-7}s^3 + 0.01\times10^{-2}s^2 - 0.04s + 14000}{1.69\times10^{-25}s^7 + 3.91\times10^{-20}s^6 + 2.67\times10^{-15}s^5 + 5.16\times10^{-11}s^4 + 1.08\times10^{-8}s^3 + 1.73\times10^{-4}s^2 + 2.78\times10^{-3}s + 9.34} \tag{14}
$$

$$
G_{\mathrm{ZPK}}(s) = \frac{-3.4\times10^5\times(s+9.2\times10^4)\times(s+3.2\times10^4)\times(s+8.5\times10^3)\times(s-8.8\times10^3)\times(s^2-53s+1.1\times10^6)}{(s+1.2\times10^5)\times(s+7.7\times10^4)\times(s+3.2\times10^4)\times(s^2+13s+5.5\times10^4)\times(s^2+22s+3.3\times10^6)} \tag{15}
$$

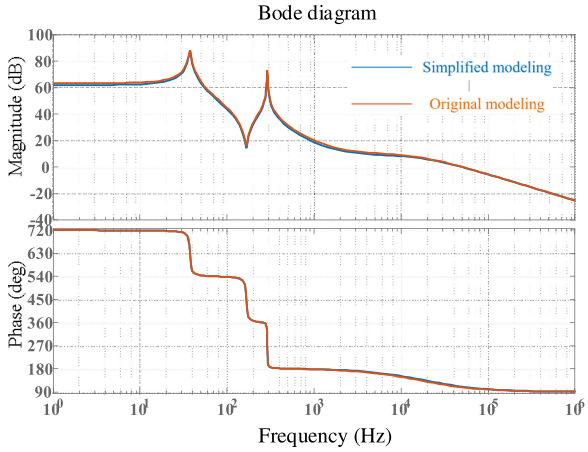

Fig. 5. Bode diagram of the proposed converter.

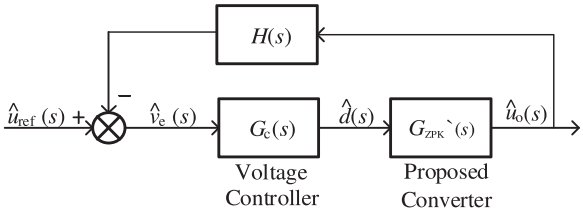

Fig. 6. Voltage loop control scheme for the proposed converter.

controller transfer function (i.e., a PI controller), as shown in (17), and $H(s)$ is the feedback transfer function. Therefore, the voltage controller can be designed for the proposed converter to achieve suitable static and dynamic performances.

$$G_c(s) = K_p + K_i \frac{1}{s}. \tag{17}$$

For this work, $K_p = 0.0013$ and $K_i = 0.00033$.

Using this voltage loop PI controller, the bode diagram of the proposed converter voltage loop is shown in Fig. 7. It can be seen that the phase margin is 50.4° (i.e., greater than 0) when the gain is 0 dB, and therefore, the converter can theoretically achieve stable operation.

VII. Experimental Results and Analysis

In order to validate the feasibility and effectiveness of the proposed converter, a 300 W experimental prototype has been developed, as shown in Fig. 8. The parameters of the experimental converter are listed in Table IV. An adjustable dc source with a range of $U_{\text{in}} = 40$–120 V is used to emulate the fuel cell stack source. The voltage loop of the converter is controlled by a TMS320F28335 DSP controller. Hybrid power switches (MOSFETs IRFP250N and IXTH88N30P) are employed in the low and the high voltage sides, respectively.

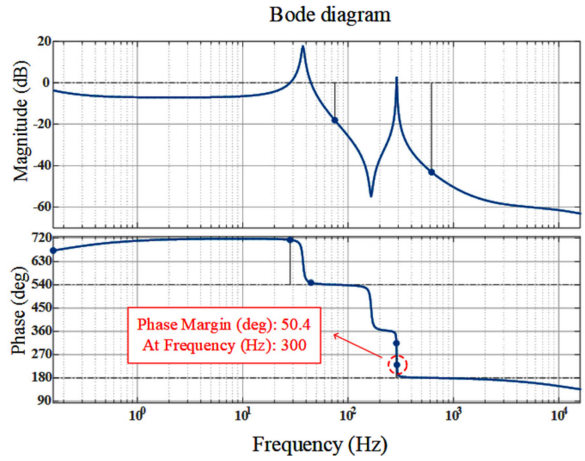

Fig. 7. Bode diagram of proposed converter voltage control loop.

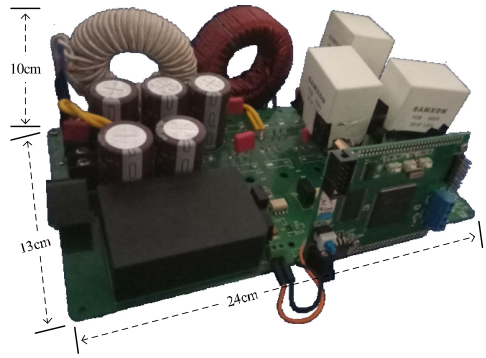

Fig. 8. Experimental prototype.

DSEC60-03A diodes are used on the low voltage side and DPF60IM400HB diodes are used on the high voltage side. In addition, the switching frequency is 20 kHz, the inductors are $L_1 = 330\,\mu$H and $L_2 = 1$ mH respectively (the inductances are increased to keep the current continuous), the electrolytic capacitances are $C_1 = C_2 = 540\,\mu$F, and the film capacitances are $C_3 = C_5 = 20\,\mu$F, $C_4 = 40\,\mu$F. The input voltage U_{in} is variable from 40 to 80 V, the reference output voltage is 400 V, and the load resistance is $R = 533\ \Omega$ (i.e., the rated power = 300 W).

The voltage stresses across Q_1 and Q_2 and the inductor current i_{L1} in the steady state are shown in Fig. 9, when $U_{\text{in}} = 40$ V and $U_o = 400$ V. From Fig. 9(a), it is clear that when $U_{Q1} = 0$, i_{L1} increases linearly. When $U_{Q1} \approx 65$ V, i_{L1} decreases linearly. The average value of i_{L1} is about 8 A, while the ripple rate is about 12.5%. Similarly, Fig. 9(b) shows that the inductor current i_{L2} has the same trend as i_{L1}: the average value of i_{L2} is approximately 3.5 A, and the voltage stress across Q_2 is 165 V, which is less than half of the output voltage (400 V). The input

$$G'_{\text{ZPK}}(s) = \frac{-3.4 \times 10^5 \times (s + 8.5 \times 10^3) \times (s - 8.8 \times 10^3) \times (s^2 - 53s + 1.1 \times 10^6)}{(s + 1.2 \times 10^5) \times (s^2 + 13s + 5.5 \times 10^4) \times (s^2 + 22s + 3.3 \times 10^6)} \tag{16}$$

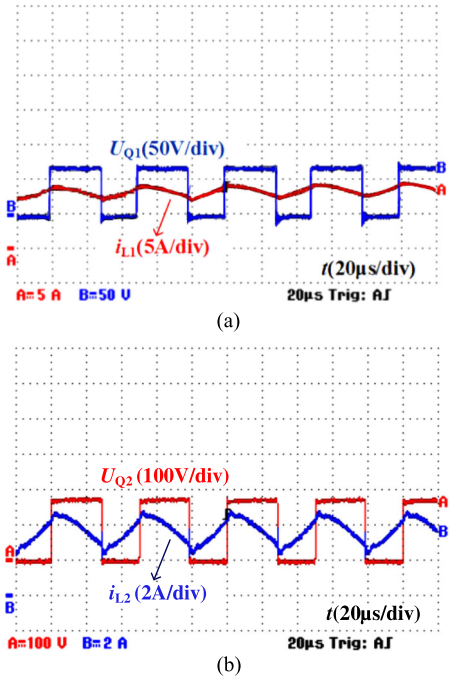

Fig. 9. Inductor currents and voltage stresses across power switches. (a) Inductor current i_{L1} and voltage stress U_{Q1}. (b) Inductor current i_{L2} and voltage stress U_{Q2}.

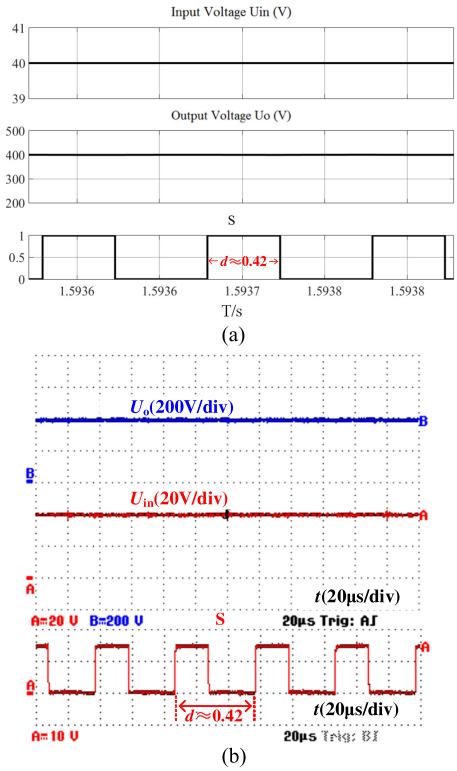

Fig. 10. Input voltage U_{in} and output voltage U_o when voltage gain is 10. (a) Simulated. (b) Measured.

voltage and the output voltage are shown in Fig. 10 where the voltage gain is 10, and it can be seen that the proposed converter can achieve a high voltage gain. Fig. 10(a) shows the simulated result, and Fig. 10(b) shows the experimental result. Furthermore, according to Fig. 10(a), the duty cycle d in the simulation is 0.42. Thus, the duty cycle d in the experimental result is also approximately 0.42—a good correlation. The voltage stresses across the low voltage diodes D_3 and D_4 are shown in Fig. 11. It is clear that the voltage stresses across D_3 and D_4 are low—the same as U_{Q1}. The voltage stress across the high side diodes and the output voltage are shown in Fig. 12. It can be seen that all the voltage stresses across the high side diodes D_5–D_7 are equal and are about half of the output voltage.

The voltage loop control maintains the output voltage at 400 V in the steady state. In addition, the output voltage can still be kept at 400 V even when the input voltage changes significantly, which is seen in Fig. 13, where the input voltage is changed from 80 to 40 V over 16 s and the output voltage stays at approximately 400 V (i.e., a voltage gain increases from 5 to 10). Therefore, the proposed converter can realize a high step-up ratio and a wide step-up voltage gain range during dynamic operation with a variable input voltage.

The conversion ratio is an important parameter that reflects the actual operating performance of the converter. Based on (3), Fig. 14 shows the gain curves derived from theory and from the experimental measurements. Neglecting the parasitic impedances, the theoretical curve is calculated using (3) and is, in general, higher than the experimentally measured curve for different duty cycles (0.2–0.5). The measured gain curve has a good match with the theoretical curve, which shows the

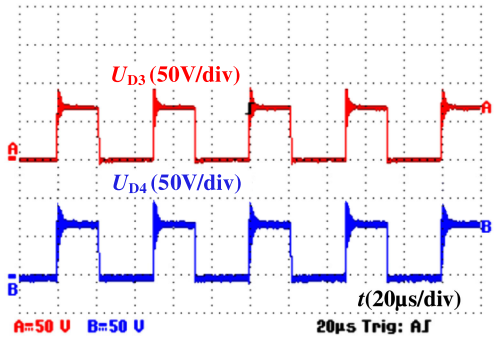

Fig. 11. Voltage stresses across low voltage diodes D_3 and D_4.

practicability of the proposed converter from an experimental perspective.

The efficiency measured by a Power Analyzer (Yokogawa-WT3000) with different voltage gains is shown in Fig. 15: the output voltage is $U_o = 400$ V, and the output power P_o varies from 200 to 400 W. The maximum efficiency is 95.01%, when $U_{\text{in}} = 80$ V and $P_o = 300$ W, i.e., the voltage gain is 5. The minimum efficiency is 90.06%, when $U_{\text{in}} = 40$ V and $P_o = 400$ W, i.e., the voltage gain is 10. The efficiency decreases as the voltage gain increases, because the increase in input current causes larger switching losses.

The calculated loss distribution [32] for the experimental system for $U_{\text{in}} = 40$ V, $U_o = 400$ V, and $P_o = 300$ W is

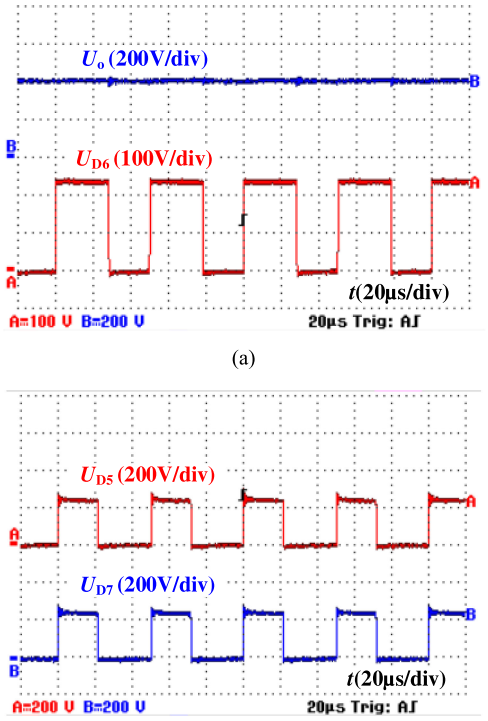

Fig. 12. Voltage stresses across high side diodes and output voltage. (a) Voltage stress across D_6 and output voltage U_o. (b) Voltage stresses across D_5 and D_7.

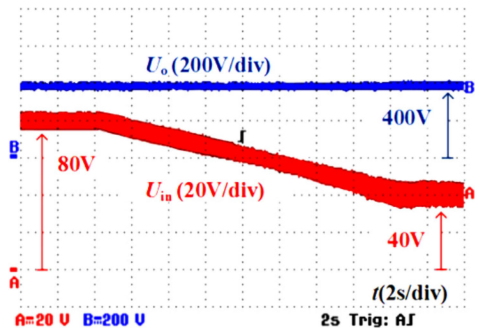

Fig. 13. Output voltage U_o with the input voltage U_{in} changed from 80 to 40 V in the dynamic state.

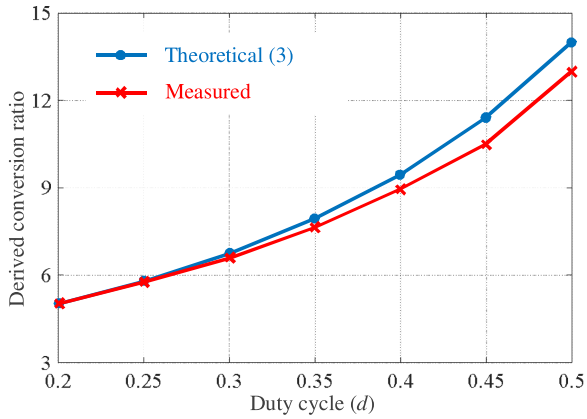

Fig. 14. Derived conversion ratio against the duty cycle under two different conditions.

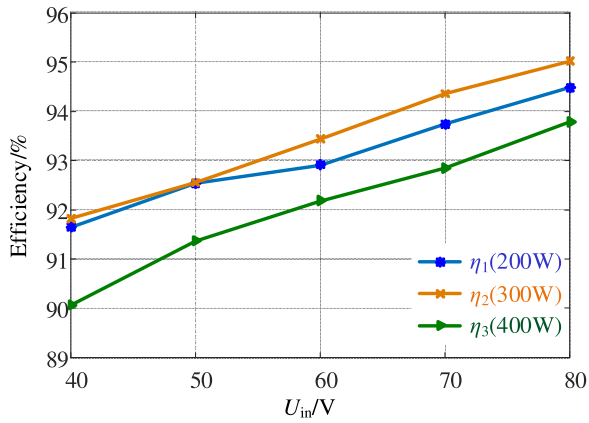

Fig. 15. Measured efficiency of the proposed converter when $U_o = 400$ V and $P_o = 200$–400 W.

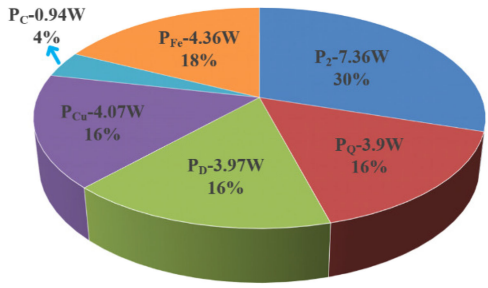

Fig. 16. Calculated loss distributions for experiment under $U_{\text{in}} = 40$ V, $U_o = 400$ V, and $P_o = 300$ W (P_2: turn-ON and turn-OFF losses of Q_1 and Q_2, P_Q: conduction losses of Q_1 and Q_2, P_D: conduction losses of D_3–D_7, P_{Cu}: copper losses of L_1 and L_2, P_C: capacitor losses of C_1–C_5, and P_{Fe}: core losses of L_1 and L_2).

shown in Fig. 16. The total losses of the proposed converter are 24.6 W. The turn-ON and turn-OFF (switching) losses of the power switches Q_1 and Q_2 (i.e., $P_2 = 7.36$ W) account for 30% of the total losses. The conduction losses of all diodes D_3–D_7 (i.e., $P_D = 3.97$ W) account for 16% of the total losses, which is nearly equal to the conduction loss of power switches Q_1 and Q_2 (i.e., $P_Q = 3.9$ W). In addition to the conduction losses of the semiconductors, the copper losses P_{Cu} of inductors L_1 and L_2 are 4.07 W, which account for 16% of the total losses. The core losses of inductors L_1 and L_2 (i.e., $P_{\text{Fe}} = 4.36$ W) account for 18% of the total losses. The capacitor losses of C_1–C_5 are $P_C = 0.94$ W, which account for 4% of the total losses.

VIII. Conclusion

A high voltage gain dc–dc boost converter with a wide input range, continuous input current, and common ground points between the input side and the load side has been proposed in this paper. The voltage stress across the main power switches is

lower than half of the output voltage. In addition, the proposed converter can keep the output voltage at 400 V using a voltage control loop, when the input voltage changes from 80 to 40 V. Therefore, it is suitable for the power interface between a fuel cell source and the dc bus for the motor drive in fuel cell vehicles.

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