An Overview of Modular Multilevel Converters in HVDC Transmission Systems With STATCOM Operation During Pole-to-Pole DC Short Circuits

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***Abstract*—Fault-current handling capability of the modular multilevel converters (MMCs) under dc-cable short-circuit conditions is a major concern for the MMC applications on the high-voltage direct-current (HVDC) transmission systems, where the MMCs based on half-bridge submodules (SMs) cannot block the fault currents to protect the converter devices. In this paper, a comprehensive review for the fault-ride-through capability of the HVDC transmission systems based on the MMCs adopting different SM schemes is presented, where the MMCs can block the fault currents and compensate the reactive currents to the electric grid during the dc faults. An analysis of the dc short-circuit faults in the MMC is introduced and then the operation principle of different SM circuits building the MMC for blocking the fault currents is highlighted. The fault-tolerant operation of these MMC schemes as static synchronous compensator to enhance the ac grid stability during the dc faults is also investigated. A comparison in terms of investment cost, loss, volume, and controllability for various MMC topologies is performed. Comprehensive simulation results for the most promising topologies of the MMC with a capability of fault-ride through under dc-fault conditions are finally presented.**

***Index Terms*—DC short-circuit faults, fault-handling capability, high-voltage direct-current (HVDC) transmission systems, modular-multilevel converters, static synchronous compensator (STATCOM), submodules (SMs).**

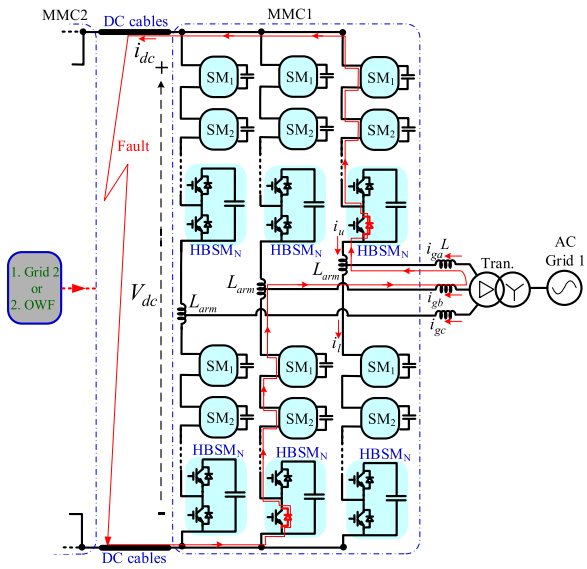

Fig. 1. Typical MMC using HBSMs in HVDC system and current path at DC short-circuit fault.

I. Introduction

THE modular multilevel converters (MMCs) built by the simplest unit of the half-bridge submodules (HBSMs) have been the first and most preferred choice for the medium- and high-voltage applications since the MMCs offer remarkable advantages, such as easy scalability, high-quality output voltages, less filter size, etc., compared to the other power electronic converters [1]–[9]. A major shortcoming of the HBSM-based MMC is lack of fault-current handling capability under the short-circuit faults in the applications of the high-voltage direct-current (HVDC) transmission systems, which may cause damage to the semiconductor devices and other components of the MMC [10]–[18]. Due to the aforementioned drawback, the HBSM-based MMCs are restricted for the applications of the HVDC transmission systems, especially with overhead lines, where the pole-to-pole (P2P) short circuits occasionally occur. Fig. 1 shows a typical point-to-point HVDC transmission system based on MMC with HBSMs, where a fault-current path formed from ac side through freewheeling diodes to dc side is also depicted.

Using circuit breakers (CBs) is a traditional solution to isolate the fault currents with the converters. However, this method requires additional devices and components installed in the system, which causes an increase of the system cost, loss, and footprint [19]–[21]. In addition, the response of ac CBs is low and the technology of the dc CBs for high-voltage and high-power applications is still under development [22]–[32]. The CBs are used to

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simply isolate the faults. Alternative providing the fault-current blocking capability is based on the SM circuits embedded into the MMCs, which have attracted a significant attention recently. A remarkable effort from researchers to introduce new MMC topologies for preventing the device damage due to fault currents has been demonstrated in many published articles [33]–[43]. The MMC topologies with the fault-handling capability are based on full-bridge submodules (FBSM), a hybrid of HBSMs and FBSMs or unipolar-voltage full-bridge submodules (uFBSM), clamp-double submodules (CDSM), series-connected double submodules (SCDSM), alternative-arm converter (AAC), hybrid-arm bipolar MMC (UHA-BMMC) based on the uFBSMs, etc. By deactivating the IGBTs (insulated-gate bipolar translators) in these MMCs, a reverse-biased voltage in the fault current path is created to decay the fault currents and then block them when the reverse-biased voltage is sufficient to block the conduction of freewheeling diodes. This cannot be performed in the MMCs based on the HBSMs only. With the above action, the fault energy stored in the reactors can be absorbed in the SM capacitors, where additional arrestors are not required to consume the fault-stored energy [24], [45], [46].

In addition, in order to enhance the grid stability, the MMCs not only block all the IGBTs to isolate the fault currents during the short-circuit conditions, but are also encouraged to actively support the grid by compensating the reactive current to the power system [47]–[55]. During the fault, the HVDC-link voltage may be collapsed. So, the active power cannot be transferred between the dc side and ac grid, which may result in the instability of the grid [47]. For doing so, the power electronic converters are operated in a tolerant-control mode as static synchronous compensator (STATCOM) for regulating the reactive power and staying in service continuously, which assists in recovering the normal operation of the HVDC-MMCs after fault clearance. In the tolerant-operation mode, the control strategies and the modulation techniques of the MMCs should be modified appropriately. It is worth to mention that the presented MMC technologies and control strategies can benefit many configurations and control strategies for enhancing the fault-ride-through operation of the HVDC system [56]–[61].

The main aim of this paper is to present a general overview and comprehensive understanding of the MMCs based on various SM circuits such as the FBSMs, the hybrid scheme of FBSMs and HBSMs, the CDSMs, the SCDSMs, and the AAC. These MMCs can not only block the fault currents but also provide the reactive currents to the electric grid during the dc-fault conditions. The operation principle of the MMCs based on the aforementioned SM circuits for the fault-ride-through capability is investigated, where the control strategies and the modulation techniques for these MMC schemes are also highlighted. A comparison in terms of cost, loss, and footprint of the MMCs is analyzed and the controllability and reactive power compensation capability of the MMCs under fault conditions are covered also. The contribution of the study is a comprehensive analysis of the fault-tolerant operation of the MMCs, which then introduces the promising topologies of the MMCs applying to the HVDC transmission systems with a fault-handling capability.

The rest of the paper is outlined as follows. A comprehensive analysis and a derivation of fault current equations for the MMCs under the short-circuit faults are introduced in Section II, where the topologies of the MMCs based on different SM circuits are also introduced. Fault-current blocking principle of these MMCs is described in Section III. Section IV presents the STATCOM operation of the above MMCs with the modification of control strategies and modulation techniques. An overall comparison among the MMCs is performed in Section V. Section VI shows the simulation results for typical MMCs under the fault conditions. Finally, the discussions and conclusions are made in Sections VII and VIII, respectively.

II. MMC-Based HVDC Transmission Systems With DC-Cable Short-Circuit Faults

A. MMC Based on Different SM Circuits

Fig. 1 shows a typical configuration of an HVDC transmission system utilizing the MMCs for connecting the two grids or an offshore wind farm and an onshore grid. The three-phase MMC consists of six arms, where each converter arm is constituted by N series-connected SMs and an inductor [62]–[64]. So far, several different SM circuit topologies have been introduced, which are briefly reviewed as follows.

1) MMC Based on HBSMs: The simplest and original circuit for the SMs of MMCs is the half-bridge, which consists of a complementary switch pair and a dc capacitor, as shown in Fig. 2(a). The HBSM-based MMC is considered as the standard topology of the MMC with the lowest power loss and capital cost due to the simplest structure of the SM, which is required to produce two output voltage levels for the normal operation of the MMC. In order to avoid the damage of the switches in the HBSM-based MMCs due to the fault currents during dc short-circuit faults, two thyristors (SCRs) are utilized by parallel connection with the lower IGBT of the HBSM as shown in Fig. 2(b) [65]. Under normal operation, the SCRs are turned OFF. When the short-circuit fault is detected, the SCRs are turned ON, which conduct the fault current and bypass the freewheeling diodes in the HBSM. By this configuration of the SM, the dc short-circuit condition is decoupled with the ac grid voltage, where an ac short circuit is created through the SCRs. However, the fault current cannot be completely isolated in the converter, which may damage the other components of the converter system and the fault is fatal. A coordination operation of the HBSM-based MMC with the dc CBs is employed to limit the fault currents increasing excessively before activating the dc CBs with a consideration of the delay time of the dc CB switches [29], [30], [32]. Even though the coordination strategy of the HBSM-based MMC with the dc CBs offers an effective protection scheme, this solution just assists to isolate the faults and protect the system devices, where no reactive power compensation and SM capacitor voltage balancing during the dc fault are performed. This coordinated configuration is not investigated in this paper.

2) MMC Based on FBSMs: The FBSM is a duplication of the HBSM with only one dc capacitor as shown in Fig. 2(c) [37], [66]–[68], where the FBSM can produce three levels of output voltage with negative, zero, and positive values of the SM capacitor voltage. At a dc short-circuit fault, when all of the IGBTs of the SMs are deactivated, the capacitor voltages of

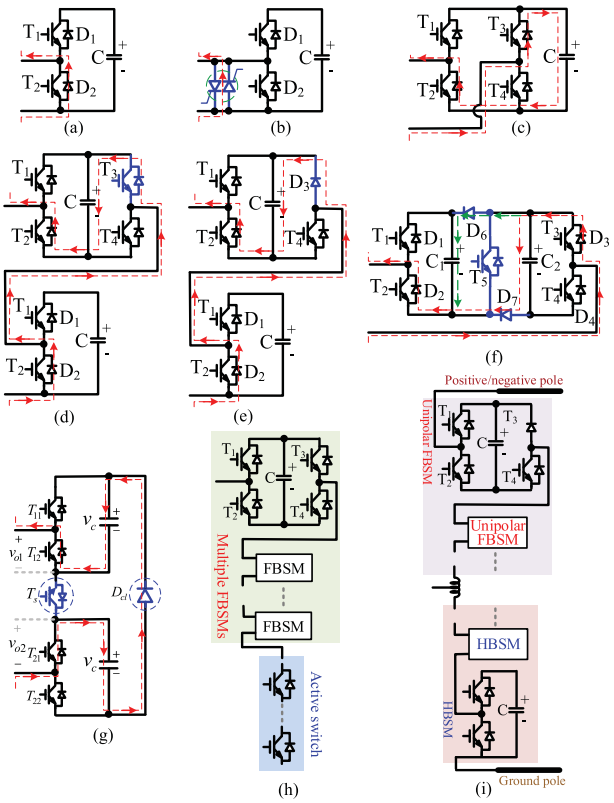

Fig. 2. Submodule circuits for MMC. (a) HBSM. (b) HBSM with thyristors. (c) FBSM. (d) Hybrid scheme of HBSM and FBSM. (e) Hybrid topology of HBSM and uFBSM. (f) CDSM. (g) SCDSM. (h) AAC. (i) UHA-BMMC.

the SMs in the upper and lower arms in different legs produce reverse-biased voltages for blocking the freewheeling diodes as shown in Fig. 2(c). As a result, the fault currents from the ac side are decaying and blocked. Thus, the MMCs configured by the FBSMs provides current fault blocking capability. However, the number of switches is doubled compared with the HBSM, which causes significantly higher power losses and an increase in both the cost and size of the converter.

3) MMC Employed a Hybrid Scheme Based on the HBSMs With Either FBSMs or Unipolar FBSMs: A motivation of proposing the hybrid scheme of the SMs in the MMCs is to reduce the number of semiconductor devices, which results in a reduction of converter power losses and cost, while the fault-handling capability of the MMCs is still performed. A hybrid SM constituting the converter arm of the MMC is shown in Fig. 2(d), which utilizes a combination of HBSM and FBSM connected in series [13], [42], [43]. For this structure, the hybrid SM-based MMC possesses the dc-fault current blocking capability, while offering lower losses and cost compared to the FBSM-MMC. However, the reverse-biased voltage is lower than that of the FBSM-MMC.

The number of semiconductor devices in the hybrid scheme can be further reduced by replacing the FBSMs by unipolar FBSMs (uFBSM) as shown in Fig. 2(e), where the diode D_3 is utilized in the uFBSM instead of the IGBT T_3 in the FBSM. The uFBSM can operate as the FBSM, which produces the output voltage levels of zero and dc voltage of SM capacitor, v_c, under normal operation and creates the reverse-biased voltage as blocking all IGBTs under fault conditions as shown in Fig. 2(e).

4) MMC Based on CDSMs: An alternative SM was proposed in [34] called clamped double SM as shown in Fig. 2(f), which utilizes an IGBT (T_5) for series connection of two consecutive HBSMs in the normal operation and two additional diodes for clamping the SM capacitor voltages under the faults. The T_5 remains in the on-state all the time during the normal operation. When a short-circuit fault is detected, all of the switches are switched OFF. Then, the clamp-double SMs can produce reverse-biased voltages through one of two SM capacitors or both two SM capacitors connected in parallel to drive the fault currents to zero. In this structure, two single diodes and one IGBT are required, which may cause more size and volume of the converter when assembled.

5) MMC Based on SCDSMs: The SCDSM is constituted by two typical HBSMs (T_{11}, T_{12} for HBSM_1 and T_{21}, T_{22} for HBSM_2), which are connected in series through additional IGBT T_s and only one diode D_{cl} instead of two separated single diodes in the CDSM as shown in Fig. 2(g) [36]. The T_s is switched ON all the time during the normal operation, where the SCDSM is operated as two normal HBSMs. Unlike the CDSM, the SCDSM can create a reverse-biased voltage of $2v_c$ to assist blocking the fault currents, when all the IGBTs are turned OFF.

6) Alternative Arm Converter: The AAC characterizes the features of the two-level converter with alternating the conduction of either upper or lower arm of the multilevel converters. The AAC arm consists of an active switch controlling the current direction and the FBSMs connected in series to produce the multilevel output voltages in positive and negative side [32], [69], [70]. Fig. 2(h) shows the configuration of the AAC arm, where the active switch is realized by series-connected single IGBTs.

7) Hybrid-Arm Bipolar MMC Based on HBSMs and Unipolar-Voltage FBSM: Another structure of the MMC called the UHA-BMMC is applied in the HVDC systems with bipolar configuration composing of the positive, ground, and negative poles. The UHA-BMMC employs a combination of the HBSMs and the unipolar FBSMs, where the ground pole of the HVDC system are connecting to the uFBSM-based converter arms, and the other poles are connecting to the arms based on the uFBSMs [39]. Fig. 2(i) illustrates one leg of the hybrid-arm bipolar MMC. The HVDC based on the hybrid-arm bipolar MMCs is able to stay in service with the reactive power regulation under both the P2G (pole-to-ground) and P2P faults.

B. DC-Cable Fault Analysis in MMC-Based HVDC Systems

The P2P short-circuit fault is the most server condition in the HVDC transmission systems, which causes extremely high currents in the system and damages the semiconductor devices within a short time. Meanwhile, the P2G faults do not cause excessively high current flowing through the semiconductor devices in the MMC-based HVDC transmission systems, which adopt the Y/Δ transformers with the delta connection in the converter side [48], [51], [52], [65], [71]–[75]. The main concern of this work is to operate the MMCs as STATCOM to compensate the reactive currents to the electric grid under the P2P short-

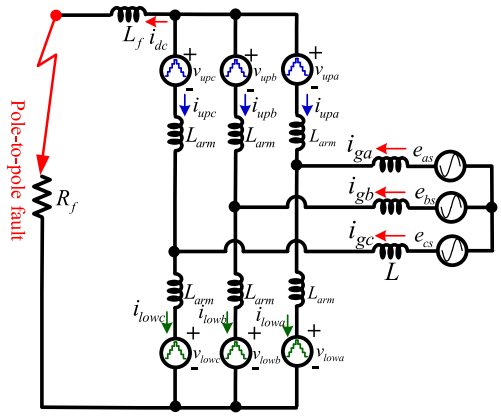

Fig. 3. MMC prior to the fault detection for dc short-circuit conditions.

circuit conditions. When the P2P fault occurs, the MMC prior to the fault detection is demonstrated through ac voltage sources formed by the SM capacitor voltages in the upper and lower arms as shown in Fig. 3 [35], [76]–[79]. From Fig. 3, the three-phase voltage equations of the MMC can be expressed as follows:

$$e_{ab} = L\frac{d}{dt}(i_{ga} - i_{gb}) - L_{\rm arm}\frac{d}{dt}(i_{{\rm up}a} + i_{{\rm low}b}) - v_{{\rm up}a} - v_{{\rm low}b} + L_f\frac{di_{\rm dc}}{dt} + R_f i_{\rm dc} \quad (1)$$

$$e_{bc} = L\frac{d}{dt}(i_{gb} - i_{gc}) - L_{\rm arm}\frac{d}{dt}(i_{{\rm up}b} + i_{{\rm low}c}) - v_{{\rm up}b} - v_{{\rm low}c} + L_f\frac{di_{\rm dc}}{dt} + R_f i_{\rm dc} \quad (2)$$

$$e_{ca} = L\frac{d}{dt}(i_{gc} - i_{ga}) - L_{\rm arm}\frac{d}{dt}(i_{{\rm up}c} + i_{{\rm low}a}) - v_{{\rm up}c} - v_{{\rm low}a} + L_f\frac{di_{\rm dc}}{dt} + R_f i_{\rm dc} \quad (3)$$

where e_{ab}, e_{bc}, and e_{ca} are the phase-to-phase voltages of the grid, i_{gx} $(x = a, b, c)$ are the converter phase currents, $i_{{\rm up}x}$ and $i_{{\rm low}x}$ are the upper/lower arm currents, respectively, $v_{{\rm up}x}$ and $v_{{\rm low}x}$ are the upper- and lower-arm voltages, and $i_{\rm dc}$ is the dc-cable current. R_f and L_f are the fault resistance and inductance, respectively, L and $L_{\rm arm}$ are the input filter and arm inductances of the MMC, respectively.

A summation of (1)–(3) yields the following:

$$\left(L_f + \frac{2}{3}L_{\rm arm}\right)\frac{di_{\rm dc}}{dt} + R_f i_{\rm dc} = Nv_c \quad (4)$$

where v_c is the SM capacitor voltage, N is the number of SMs per converter arm, and the following assumptions are made for the MMC operation before deactivating all the IGBTs in the MMC. The three-phase system is balanced and the voltages and capacitances of the SM capacitors of the MMC, v_c, and C, respectively, are identical, which are expressed through the following equations:

$$e_{ab} + e_{bc} + e_{ca} = 0 \quad (5)$$

$$i_{ga} + i_{gb} + i_{gc} = 0 \quad (6)$$

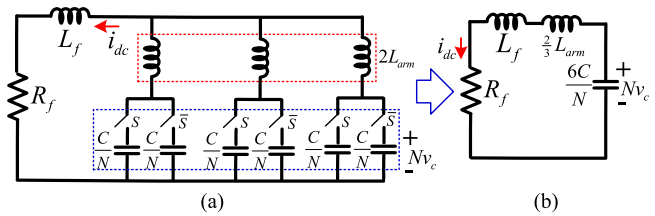

Fig. 4. Simplified equivalent circuit of MMC under the P2P fault.

$$v_{{\rm up}a} + v_{{\rm up}b} + v_{{\rm up}c} = \frac{3}{2}Nv_c \quad (7)$$

$$v_{{\rm low}a} + v_{{\rm low}b} + v_{{\rm low}c} = \frac{3}{2}Nv_c. \quad (8)$$

It is seen from Fig. 3 and (4) that the fault current flowing through the dc cable is mainly caused by discharging the capacitors of the SMs with on-state condition, where the phase currents from the ac-source side are negligible for contributing to the dc-cable current. Prior to the fault detection, the SMs of the MMC are still switched according to the modulation operation, where the number of the on-state SMs per a converter leg is N from total $2N$ SMs per leg. This means that at a certain moment within the switching cycle, there is N SM-capacitors connected in series per a leg, while the other N SM-capacitors are floating. The SM capacitors in either connecting or floating mode are changing according to the modulation. Thus, the equivalent capacitance of a converter leg at the certain moment is C/N, where its average value within a switching period will be $2C/N$ due to the alternative operation of the $2N$ SM capacitors. The equivalent circuit in Fig. 3 under the P2P short-circuit condition can be redrawn as Fig. 4(a) with three legs connected in parallel, where S and $\bar{S}$ being complementary represent for the on-state and off-state SMs, respectively. Then, through the Thevenin equivalent with the assumption of identical voltages of all SM capacitors, Fig. 4(b) shows the simplified equivalent circuit of the MMC prior to the fault detection, where the equivalent capacitance of the MMC before switching OFF all IGBTs is determined as $6C/N$ and the initial dc voltages at the fault occurrence instant is Nv_c [80], [81]. From Figs. 3 and 4(b), the relationship of the dc-fault current, arm currents, and SM-capacitor voltages can be expressed as follows:

$$i_{\rm dc} = -(i_{{\rm up}a} + i_{{\rm up}b} + i_{{\rm up}c}) = -\frac{6C}{N}\frac{d(Nv_c)}{dt} = -6C\frac{dv_c}{dt}. \quad (9)$$

$$i_{\rm dc} = -(i_{{\rm low}a} + i_{{\rm low}b} + i_{{\rm low}c}) = -\frac{6C}{N}\frac{d(Nv_c)}{dt} = -6C\frac{dv_c}{dt}. \quad (10)$$

Assuming that the dc fault occurs at $t = 0$ and the initial conditions of the capacitor voltages and dc-cable current are $Nv_c(0) = V_{\rm dc}$ and $i_{\rm dc}(0) = I_{\rm dc0}$, respectively, where $V_{\rm dc}$ is the HVDC-link voltage. Then, from Fig. 4, the response of the dc-cable current can be expressed as follows [12], [35]:

$$i_{\rm dc}(t) = -\frac{I_{\rm dc0}\omega_0}{\omega}e^{-\delta t}\sin(\omega t - \beta) + \frac{V_{\rm dc}e^{-\delta t}}{\omega(L_f + \frac{2}{3}L_{\rm arm})}\sin(\omega t) \quad (11)$$

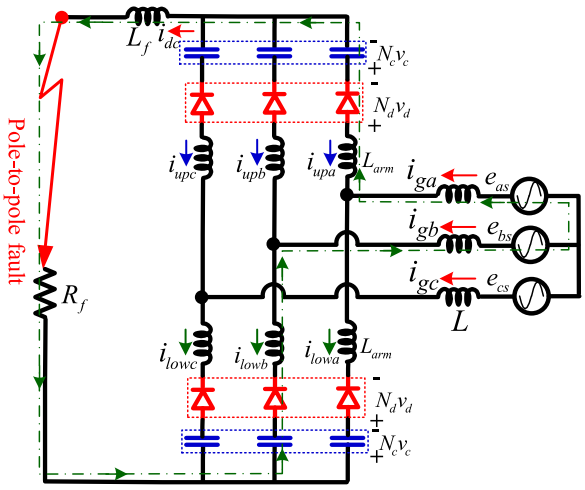

Fig. 5. MMC circuit as switching off all IGBTs under dc short-circuit conditions.

where

$$\delta = 0.5R_f / \left(L_f + \frac{2}{3}L_{\rm arm}\right)$$

$$\omega_0 = \sqrt{N/\left(6C\left(L_f + \frac{2}{3}L_{\rm arm}\right)\right)}, \omega = \sqrt{\omega_0^2 - \delta^2}$$

and $\beta = \arctan(\omega/\delta)$.

III. Fault-Current Blocking Principle of MMCs With Different SM Circuits

As analyzed above, before deactivating all the IGBTs of the MMC, the dc-cable current is increased quickly. Normally, a current threshold value, $I_{\rm dcmax}$, is set to protect the devices and detect the fault when the fault current reaches the $I_{\rm dcmax}$. Assuming that the dc fault is detected within a short duration t_d, based on (11), the dc-fault current reaches a certain current level as follows:

$$i_{\rm dc}(t_d) = I_{\rm dc\,max}. \tag{12}$$

For the MMC based on the HBSMs, the converter fault response under the dc short-circuit condition can be divided into five stages including discharge (as presented in Section II-B), free-wheeling, three-diode rectifier, four-diode rectifier, and fault current decay [82]. In this paper, the analysis of the dc-fault currents from the MMCs based on different modified SMs after switching OFF all the IGBTs is taken into account, where the response of the dc-fault currents can be different depending on the structures of the MMCs and the number of modified SMs added. Then, the condition for the MMCs to obtain a fault-handling capability is determined. With the MMCs based on the SM topologies presented in Fig. 2, after blocking the IGBTs, the SM capacitors are inserted in the fault-current path to create a reverse-biased voltage, which causes to turn OFF the freewheeling diodes. The equivalent circuit of the MMCs with the modified SMs for fault current blocking is illustrated in Fig. 5, where the fault-current paths formed from the phase-to-phase voltage in the ac side to the short-circuit point in the dc side through N_c capacitors of the SMs and N_d freewheeling diodes per arm connected in series are depicted for the short-circuit conditions.

The response of the fault current while switching all the IGBTs OFF can be expressed through the grid voltages and SM capacitor voltages for the P2P short circuits as follows:

$$2N_d v_d = e_{xy} - 2N_c v_c - L\frac{d}{dt}\left(i_{gx} - i_{gy}\right) + L_{\rm arm}\frac{d}{dt}\left(i_{{\rm up}x} + i_{{\rm low}y}\right) - L_f\frac{di_{\rm dc}}{dt} - R_f i_{\rm dc} \tag{13}$$

where v_d is the forward voltage of the freewheeling diodes and $e_{xy}(x, y = a, b, c; x \neq y)$ is the phase-to-phase grid voltage. The converter phase currents, arm currents, and the dc-cable current will be reduced and decay to zero if the total capacitor voltage of the modified SMs, which is $2N_c v_c$, inserted into the fault-current path inversely, is highly sufficient to stop the conduction of the SM freewheeling diodes. To obtain this, the diode forward voltage, $2N_d v_d$, has to be nonpositive.

1) Assuming the forward-biased voltage of the diode being zero and the voltage drops on the fault resistor and inductors negligible, from (13), the condition of the number of SM capacitors, N_c, for blocking the fault current at the P2P short-circuit condition is determined as follows:

$$N_c \geq \frac{E_{ll,\max}}{2V_{c\rm SM}} \tag{14}$$

where $E_{ll,\max}$ is the magnitude of the grid phase-to-phase voltage and $V_{c\rm SM}$ is the SM-capacitor voltage rating.

It is noted that the relation of the dc voltage and grid voltage is normally selected for the normal operation of the MMC as follows [83]–[87]:

$$E_{\rm mag} = \frac{1}{2}M_{\max}V_{\rm dc} \tag{15}$$

where $M_{\max}$ is a maximum value of the modulation index, which is typically about 0.8. It is noted that the modulation index can be increased if the appropriated common mode voltage term is added. So, from (14), (15), and $V_{\rm dc} = NV_{c\rm SM}$, the condition of the SM capacitor number for the fault-current blocking can be rewritten as follows:

$$N_c \geq 0.346\ {\rm N}. \tag{16}$$

Because of the presence of the inductances in the fault-current path, the currents of the converter arms and phases and the fault current will be decayed to zero within a certain duration, when all the IGBTs are blocked. These currents also satisfy the conditions presented in (6), (9), and (10). By writing (18) for three different grid line-to-line voltages and adding together, the fault current characteristic for the P2P fault can be expressed as follows:

$$2N_c v_c + \left(L_f + \frac{2}{3}L_{\rm arm}\right)\frac{di_{\rm dc}}{dt} + R_f i_{\rm dc} = 0. \tag{17}$$

The simplified equivalent circuit of the MMCs with the modified SMs for inserting the SM capacitors into the path of fault current is illustrated in Fig. 6. At the instance of fault detection, $i_{\rm dc}(t_d) = I_{\rm dc\,max}$, and the SM capacitor voltage is assumed to

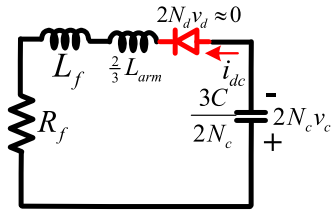

Fig. 6. Simplified equivalent circuit of MMC with all IGBTs blocked under the P2P fault.

be identical at $V_{c\mathrm{SM}}$, the fault current is obtained as follows:

$$i_{\mathrm{dc}}(t)=\frac{I_{\mathrm{dc\,max}}\omega_0}{\omega}e^{-\delta t}\sin(\omega t-\beta)-\frac{2N_cV_{c\mathrm{SM}}e^{-\delta t}}{\omega(L_f+\frac{2}{3}L_{\mathrm{arm}})}\sin(\omega t) \tag{18}$$

where

$$\delta=0.5\,R_f/\left(L_f+\frac{2}{3}L_{\mathrm{arm}}\right)$$

$$\omega_0=\sqrt{N_c/\left(6C\left(L_f+\frac{2}{3}L_{\mathrm{arm}}\right)\right)},\omega=\sqrt{\omega_0^2-\delta^2}$$

and $\beta=\arctan(\omega/\delta)$.

It is seen in (18) that the fault-current blocking time, ΔT_{bl}, where the fault current reaches to zero ($i_{\mathrm{dc}}(t_d+\Delta T_{\mathrm{bl}})=0$), is dependent on the number of SM capacitors as well as the SM number, inserted into the fault-current path. Under the short-circuit fault, the reverse-biased voltage for the freewheeling diodes is $2N_cv_c$.

2) As analyzed above, with the MMC based on FBSMs, the number of SM capacitors per arm inserted into the fault-current path as turning OFF all the IGBTs is maximum ($N_c=N$) and the reverse-biased voltage is $2V_{\mathrm{dc}}$. This MMC topology offers the shortest time to isolate the fault current compared with the other ones.
3) Meanwhile, the MMCs based on the equal number of HBSMs and FBSMs or uFBSMs, the CDSM-based MMC, and the MMC with *N/4* SCDSMs and *N/2* HBSMs per arm provide the same number of SM capacitors ($N_c=N/2$) inserting to the fault-current path for creating the reverse-biased voltages of V_{dc} under the cases of P2P faults. Based on (16), these MMC structures satisfy to block the fault currents under fault conditions, where the fault-current blocking time for the three MMCs is similar. If the numbers of FBSMs, uFBSMs, and SCDSMs in the MMCs are increased, then the current-blocking time will be shortened. However, the MMC based on the CDSMs is not able to increase the number of SM capacitors inserted into the fault path higher than *N*/2 per arm. In addition, while switching OFF five IGBTs of the CDSM, two capacitors of the CDSM may be connected in parallel, if two capacitor voltages are similar. This causes a slightly longer time to for the fault current to be decayed to zero fully.
4) With the AAC, since stacks of the cells based on the FBSMs can produce the negative voltage, so the AAC can operate at different conditions compared to the conventional MMC, where a relationship of the grid voltage and dc bus voltage for the energy balance between the two sides should be subject to the following [33]:

$$E_{\mathrm{mag}}=\frac{2}{\pi}V_{\mathrm{dc}}\text{ or }E_{ll,\max}=\frac{2\sqrt{3}}{\pi}V_{\mathrm{dc}}. \tag{19}$$

With this structure, the condition of the number of SM capacitors per arm for handling the fault current is recalculated as follows:

$$N_c\geq\frac{\frac{2\sqrt{3}}{\pi}V_{\mathrm{dc}}}{2V_{c\mathrm{SM}}}=\frac{\sqrt{3}}{\pi}\frac{V_{\mathrm{dc}}}{V_{c\mathrm{SM}}}. \tag{20}$$

So, the FBSM number, N_c, per arm in the AAC is a tradeoff among its cost, power loss, volume, and dc-fault handling performance. It is noted that in the AAC, $N_cV_{c\mathrm{SM}}$ may be different from V_{dc} and the modulation index of the AAC is higher than that of the standard MMCs.

5) The fault-current handling capability of the UHA-BMMC is obtained by the reverse-biased voltage of $NV_{c\mathrm{SM}}$, which is produced through *N* uFBSM capacitor voltages in the converter arm connected to the positive/negative poles as shown in Fig. 2(i). In this configuration, since one of the two dc terminals of the MMCs is grounded, the converter output terminal voltages contain a dc component, which is half the dc bus voltage of the MMC corresponding to one-fourth of the HVDC-link voltage [39]. The condition for stopping the conduction of the freewheeling diodes of the UHA-BMMC in the P2P short circuits is expressed as follows:

$$NV_{c\mathrm{SM}}\geq\frac{1}{4}V_{\mathrm{dc}}+E_{\mathrm{mag}}\text{ or }E_{\mathrm{mag}}\leq\frac{1}{4}V_{\mathrm{dc}}. \tag{21}$$

6) The MMCs based on the three-level crossed-connected, five-level crossed-connected, clamp single SMs (CSSM) and unidirectional current H-bridge sub-modules, which are modified from the FBSM and CDSM, also possess a fault-current blocking capability [11], [88], [89]. The reverse-biased voltage and blocking time are also dependent on the number of modified SMs, which can insert the SM capacitors into the fault-current path. A recent structure, called as lattice modular multilevel converter (LMMC), was introduced in [90], which can utilize all the SM capacitors to create the reverse-biased voltage like the FBSM. This topology can be operated with lower power loss even when compared to the HBSM-based MMC. However, the LMMC requires using the reversed-blocking IGBTs and single IGBTs instead of IGBT modules, which causes a challenge for the converter assembly in terms of footprint and volume.

IV. Fault-Tolerant Control of MMCs With STATCOM Operation

As discussed, the MMCs in the HVDC systems are required not only to be capable of blocking the fault currents but also to compensate the reactive currents for enhancing the ac voltage regulation and grid stability during the faults. When a short circuit between two terminals of the MMC occurs, the HVDC-link voltage drops to mostly zero depending on the dc-line impedance and fault resistance. In this scenario, the MMC

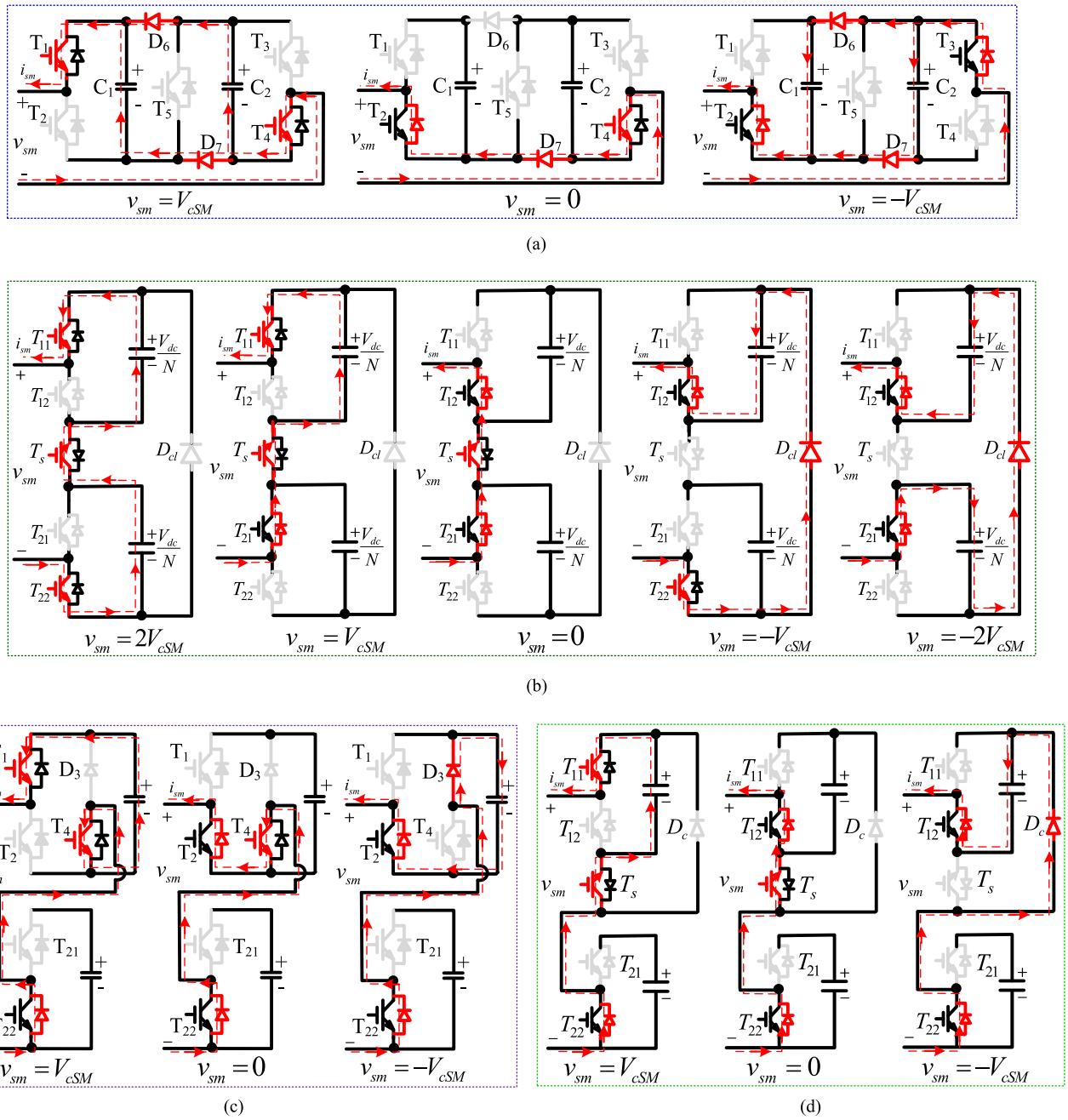

Fig. 7. Equivalent circuits and current paths for different voltage levels with (a) CDSM, (b) SCDSM, (c) uFBSM, and (d) CSSM in the case of dc fault conditions.

cannot deliver the real power to the dc side and the MMC becomes a star-connected arm configuration like a cascade multilevel converter. For obtaining the fault-tolerant control with a STATCOM function of the MMC to compensate the reactive power, the arms of MMC are required to be capable of generating bipolar voltages, by which the converter currents are regulated. It is obvious that the HBSMs just generate two voltage levels of zero and V_{cSM}. So, the STATCOM operation of the MMCs based on HBSMs are not able to be performed during faults. The MMCs based on the modified or combined SMs being capable of generating the bipolar voltages are able to operate in the tolerant control mode during faults, which are described in the following sections.

A. MMC Fault-Tolerant Control Based on Alternative Arm Conduction

1) Bipolar Output Voltage Generation of SMs: It is known that the CDSM, SCDSM, uFBSM, and CSSM are modified from the basic unit of HBSM to handle the fault-ride-through capability. At the normal condition, the HBSMs in the CDSM and SCDSM are operated as typically separated HBSMs, where the additional IGBTs, T_5 and T_s, are continuously conducting. Similarly, the uFBSM and CSSM also generate zero and positive voltage levels only without the negative value.

In the CDSM, SCDSM, uFBSM, and CSSM, the additional diodes are utilized to create the reverse-biased voltage as

TABLE I
SWITCHING STATES OF CDSM DURING FAULTS

Switches	T_1	T_2	T_3	T_4	T_5	D_6	D_7	i_{sm}	v_{sm}
Switching states	1	0	0	1	0	1	1	>0	V_{cSM}
	0	1	0	1	0	0	1	>0	0
	0	1	1	0	0	1	1	>0	$-V_{cSM}$

TABLE II
SWITCHING STATES OF SCDSM DURING FAULTS

Switches	T_{11}	T_{12}	T_{21}	T_{22}	T_s	D_{cl}	i_{sm}	v_{sm}
Switching states	0	1	1	0	0	1	>0	$-2V_{cSM}$
	0	1	0	1	0	1	>0	$-V_{cSM}$
	0	1	1	0	1	0	>0	0
	1	0	1	0	1	0	>0	V_{cSM}
	1	0	0	1	1	0	>0	$2V_{cSM}$

TABLE III
SWITCHING STATES OF UFBSM AND CSSM AT FAULT

Switches	T_{21}	T_{22}	T_1/T_{11}	T_2/T_{12}	T_4/T_s	D_3/D_c	i_{sm}	v_{sm}
Switching states	0	1	1	0	1	0	>0	V_{cSM}
	0	1	0	1	1	0	>0	0
	0	1	0	1	0	1	>0	$-V_{cSM}$

switching OFF all the IGBTs to block the fault currents in the MMCs. In addition, these SMs can produce the bipolar output voltage levels, $v_{\rm sm}$, with a certain current direction by proper switching states, which are utilized in the converter arms to control the phase currents. It is noted that for reducing the device count of the MMC, the SCDSMs, uFBSMs, and CSSMs are combined with the basic units, HBSMs, to configure the MMCs. Meanwhile, the CDSMs are wholly utilized to build the MMC, since the CDSM is just able to produce the output voltages of $-V_{c\rm SM}$, 0, $V_{c\rm SM}$, even though the CDSM contains two capacitors. A common characteristic of the above SMs is that they are able to produce bipolar output voltages only if the SM current, $i_{\rm sm}$, is positive, which corresponds to the negative arm currents, $i_{{\rm up}x}$ and $i_{{\rm low}x}$.

At dc-cable faults, by proper switching states with turning OFF the T_5 continuously, the CDSM can be operated as an FBSM when two capacitor voltages are the same, which then are controlled to produce bipolar output voltages with positive, zero, and negative values. The positive state, $v_{\rm sm}=V_{c\rm SM}$, is created by turning ON T_1 and T_4, where the current path is through T_4, either D_7 or D_6 or both of them, and T_1. It is similar for the bypass and negative states, $v_{\rm sm}=0$ or $-V_{c\rm SM}$, respectively. Fig. 7(a) associated with Table I explains the switching states of the CDSM during the faults. Table II lists the switching states of the SCDSM under the fault condition, which can generate five output voltage levels as the SM current is positive like shown in Fig. 7(b). For producing the negative and zero voltages, the T_s of the SCDSM is turned OFF, the D_{cl} conducts the arm current. Inversely, the T_s is switched ON and conducts the arm current to generate the positive voltages of $2V_{c\rm SM}$ and $V_{c\rm SM}$. The operation of the uFBSM and CSSM is similar, which can produce three voltage levels. Fig. 7(c) and (d) associated with Table III demonstrate the operation of the uFBSM and CSSM during the fault conditions.

2) Cascade-Multilevel Converter Operation of MMC Under Faults: Fig. 8 shows a diagram of the MMC, which can be configured by the hybrid of HBSMs with one type of the modified

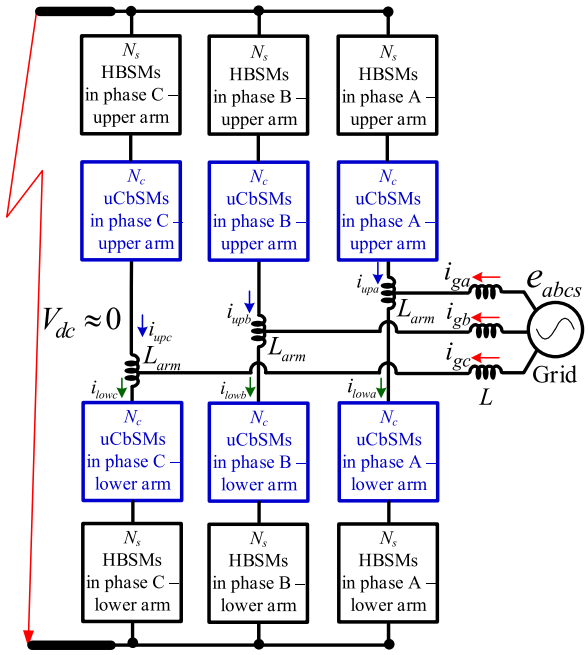

Fig. 8. Scheme of MMC with a hybrid of HBSMs and uCbSMs during pole-to-pole short circuits.

TABLE IV
RELATIONSHIP OF THE DC-LINE AND PHASE CURRENTS

Sectors \ Currents	i_{ga}	i_{gb}	i_{gc}	i_{dc}
I	>0	<0	>0	$-i_{gb}$
II	>0	<0	<0	i_{ga}
III	>0	>0	<0	$-i_{gc}$
IV	<0	>0	<0	i_{gb}
V	<0	>0	>0	$-i_{ga}$
VI	<0	<0	>0	i_{gc}

SM circuits such as CDSM, SCDSM, uFBSM, and CSSS. Each converter arm consists of N_s HBSMs and N_c modified SMs, where N_s and N_c are selected depending on the applications and the users. For the MMC based on the CDSM, no HBSM is used and the MMC contains only the CDSMs.

Assuming that the dc cable impedance and fault resistance are negligible, by alternating conduction of the arms determined by the current direction, the MMCs are reconstructed as a three-phase star-connection cascade-multilevel converter (CMC) [91]–[93]. A common characteristic of the CDSM, SCDSM, uFBSM, and CSSS, which is commonly called as uCbSM (unidirectional current bipolar SM) in this paper, is that they can produce bipolar output voltages when the arm current indicated in Fig. 8 is negative, so the principle of the CMC operation for these MMCs is the same. Due to regulating the phase currents, instead of based on the arm current directions, the phase current directions are utilized for selecting the arm conducting or blocking. Generally from Fig. 8, when the grid phase current is nonnegative, its upper arm is conducting, while blocking the lower arm. Inversely, the lower arm is in conduction mode to generate the desired phase voltage, while the upper arm is deactivated when its corresponding phase current is negative. Based on the phase current direction, the relationship of the dc-link current and the phase currents is listed in Table IV,

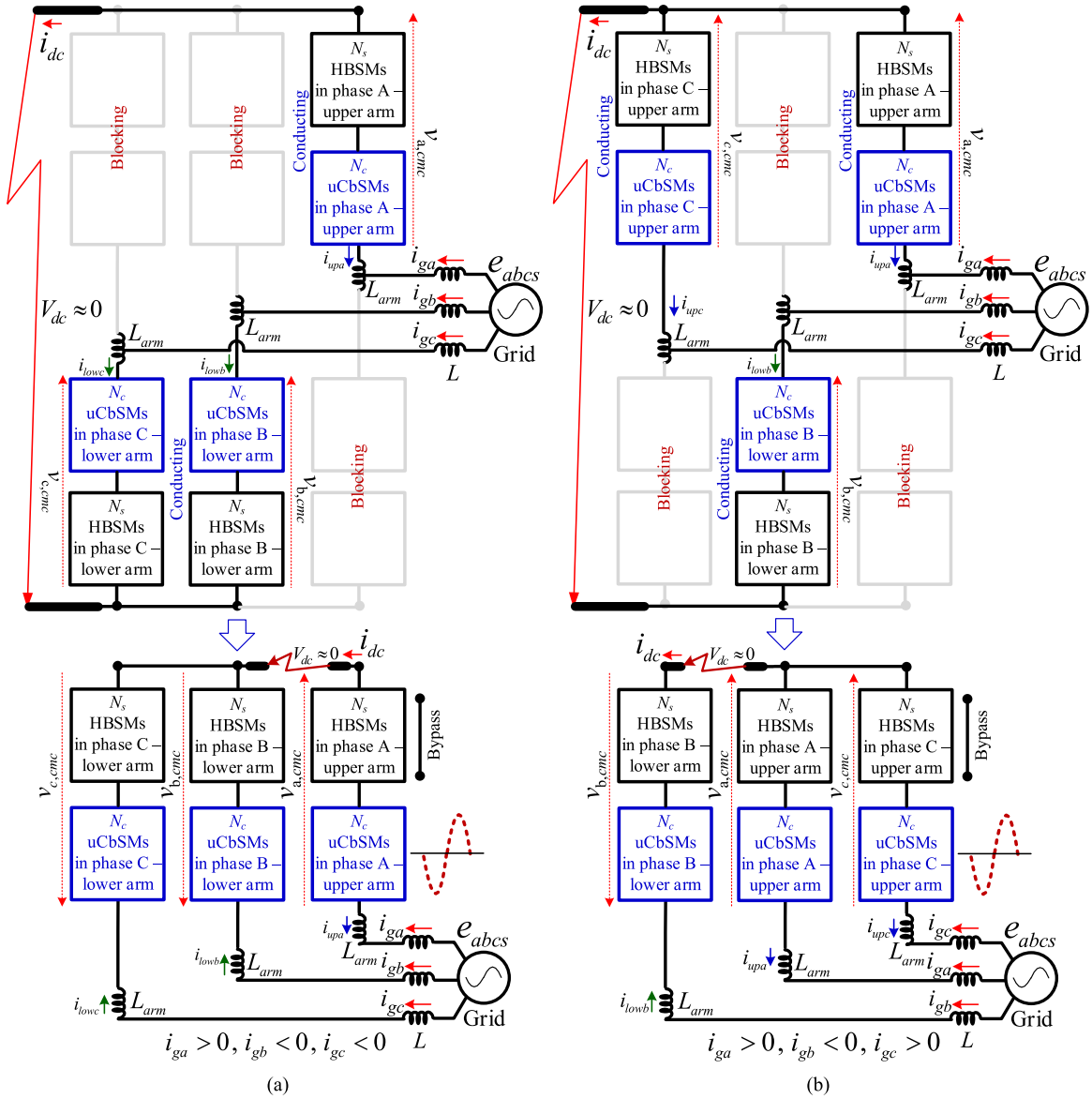

Fig. 9. Diagrams of equivalent circuits of MMC under fault for different current directions.

where the dc-line current is always equal to one of the three-phase currents within one-sixth of the fundamental cycle. It is worth noting that during the short-circuit conditions, the voltage between two terminals of the HVDC link is negligible. For this condition, Fig. 9(a) and (b) show the equivalent circuit diagrams of the MMC operating as the CMC for the cases of $(i_{ga} > 0,\ i_{gb} < 0,\ i_{gc} < 0)$ and $(i_{ga} > 0,\ i_{gb} < 0,\ i_{gc} > 0)$, respectively, where the $i_{\rm dc}$ is equal to the i_{ga} and $-i_{gb}$, respectively. The equivalent circuits of the MMCs for the other cases of phase current directions are derived similarly. For the CMC operation, the IGBTs of HBSMs and uCbSMs are all switched OFF for blocking the arms, while for the conducting arms, the HBSMs are by-passed by turning ON the lower IGBTs T_{22} and the bipolar output voltages are generated by switching the uCbSMs.

With the cascaded multilevel converter operation as depicted in Fig. 9, the level number of the output voltages of the converter is $2N_c + 1$ and the maximum magnitude of the fundamental phase voltage, $V_{\rm max}$, generated is calculated as follows [94], [95]:

$$V_{\rm max} = 0.816\, N_c V_{c\rm SM}. \tag{22}$$

To achieve the full controllability of the STATCOM operation during faults, the magnitude of the fundamental phase voltage should be high enough compared to the grid voltage, where the operation condition is selected as follows [65]:

$$V_{\rm max} \geq 1.1 E_{\rm mag} \text{ or } N_c V_{c\rm SM} \geq 1.35\ E_{\rm mag}. \tag{23}$$

It is seen from (15) and (23) that the STATCOM operation mode of the the CDSM-based MMC, where $N_c = 0.5\,$N, can be fully controlled under the following condition:

$$E_{\rm mag} \leq 0.37\, V_{\rm dc}. \tag{24}$$

This can be concluded that in this case the modulation index of the CDSM-based MMC is about 0.74 in the normal operation. Meanwhile, the voltage condition for the other MMCs based on either SCDSMs, uFBSMs, or CSSMs can obtain a maximum modulation index at 0.8 in normal condition and the full range of the STATCOM during faults when the conditions of (15) and (23) are satisfied and

$$N_c \geq 0.54 \text{ N}. \tag{25}$$

To obtain a proper STATCOM operation with alternative arm conduction, when the conducting arms generate the bipolar output voltages, the other arms should be fully blocked with sufficient reverse-biased voltages for the antiparallel diodes. Let us consider a case of the upper arms of the phase *x* and *y* conducting and their lower arms blocked with neglecting the arm inductor voltage drops, the voltage equation in the same leg can be obtained as follows:

$$v_{\text{up}x}(t) + v_{\text{low}x}(t) = 0 \tag{26}$$

where the voltage of the blocked lower arm is expressed as follows:

$$v_{\text{low}x}(t) = \begin{cases} v_{D+} + N_c V_{c\text{SM}} & \text{if } i_{\text{low}x} \geq 0 \\ v_{D-} - N_c V_{c\text{SM}} & \text{if } i_{\text{low}x} < 0 \end{cases} \tag{27}$$

where v_{D+} and v_{D-} are the forward voltages dropping on the positive and negative diodes of the uCbSMs, respectively. For the CDSM, the positive diodes consist of D_1, D_4, and D_5, while the negative diodes are D_2, D_3, D_6, and D_7. Similarly, D_{11}, D_s, and D_{22} are the positive diodes in the SCDSM, while D_{12}, D_{21}, and D_{cl} are the negative diodes. It is the same for the uFBSM and CSSM. From (26) and (27), the forward voltages of the positive and negative diodes can be rewritten as follows:

$$\begin{cases} v_{D+} = -N_c V_{c\text{SM}} - v_{\text{up}x}(t) \\ v_{D-} = -N_c V_{c\text{SM}} + v_{\text{up}x}(t). \end{cases} \tag{28}$$

According to Kirchoff's law for the loop of upper and lower arms from two different legs with the phase-to-phase grid voltage, the following relation is obtained:

$$e_{xy} = -v_{\text{up}x}(t) - v_{\text{low}y}(t). \tag{29}$$

Then, the diode forward voltages are rewritten as follows:

$$\begin{cases} v_{D+} = -e_{xy} - v_{\text{up}x}(t) - N_c V_{c\text{SM}} \\ v_{D-} = e_{xy} + v_{\text{up}x}(t) - N_c V_{c\text{SM}}. \end{cases} \tag{30}$$

It is noted that under the cascade multilevel converter operation, $e_{xs} \approx -v_{\text{up}x}(t)$, so (30) becomes the following:

$$\begin{cases} v_{D+} = e_{ys} - N_c V_{c\text{SM}} \\ v_{D-} = -e_{ys} - N_c V_{c\text{SM}}. \end{cases} \tag{31}$$

It is seen from (23), (26), and (31) that the forward voltages of the positive and negative diodes are always negative, which means that the condition for blocking one arm while conducting the other arm is satisfied.

For the other cases with the lower arm conducting and upper arm blocked, the positive and negative diodes in the blocked arms are fully blocked with nonpositive reverse-biased voltages, where a derivation can be applied in the same way as in (26)–(31). With the lower arm conduction, it is noted that $e_{xs} \approx v_{\text{low}x}(t)$.

3) Control of MMCs Under STATCOM Operation: As described in the previous section, the MMC is reconfigured with a star connection as the CMC for the fault-controlled operation. The phases of the CMC are constituted by either the upper arms or lower arms of the corresponding MMC legs, which depends on the phase current direction as indicated in Fig. 9. In this operation, the phase voltages and currents can be expressed with a relation to those of the MMC as follows:

$$v_{x,\,\text{cmc}}(t) = \begin{cases} -v_{\text{up}x}(t) & \text{if} \quad i_{gx} \geq 0 \\ v_{\text{low}x}(t) & \text{if} \quad i_{gx} < 0 \end{cases} \tag{32}$$

$$v_{gx}(t) = \begin{cases} -i_{\text{up}x}(t) & \text{if} \quad i_{gx} \geq 0 \\ i_{\text{low}x}(t) & \text{if} \quad i_{gx} < 0 \end{cases} \tag{33}$$

where $v_{x,\text{cmc}}(t)$ is the *x*-phase voltage of the CMC.

The mathematical model of the CMC under fault conditions in the *abc* frame can be expressed as follows:

$$e_{xs} = (L + L_{\text{arm}})\frac{di_{gx}}{dt} + v_{x,\text{cmc}} + v_N \tag{34}$$

where v_N is the voltage between the source neutral point and the common point of the CMC, which is the same as the fault point in the dc side. In the case of the balanced grid voltages, the balanced currents in the three phases of the converter are desired to be injected into the grid and the v_N is mostly zero and negligible. From (34), the mathematical model of the CMC can be converted into the *dq* frame, where the *q*-axis component of the grid voltage, e_{qe}, is aligned with the grid voltage vector and the *d*-axis component, e_{de}, is equal to zero. The inner current controllers are employed to regulate the i_{dqe} of the CMC [96]–[99], where the *q*-axis component of the converter current, i_{qe}, is used to adjust the converter real power and the *d*-axis component, i_{de}, is the reactive current component for regulating the reactive power exchanging between the CMC and grid. In this operation mode, since the dc voltage is collapsed to mostly zero, no real power from the dc side is injecting into the grid through the MMC. So, the reactive power capability of the MMC can be set up to 1 p.u. to compensate for the grid.

Even with a permanent or temporary short-circuit faults, the voltages of the individual SM capacitors and arms are all required to be balanced, which assist to achieve a satisfactory performance of the STATCOM operation and a fast recovery to the normal condition for the MMC after the fault clearance. It is noted that the voltage balancing control method based on the circulating current cannot be employed in this operation mode since the CMC does not produce any circulating current [100]–[106]. A method based on regulating the real power current component to balance the average voltages of all SM capacitors was presented in [39], where the voltages of the individual arms were not balanced. Similarly, the current component representing the real power is utilized to adjust the energy of the SM capacitors and between the arms [51], where the rms values of the capacitor voltages instead of using the

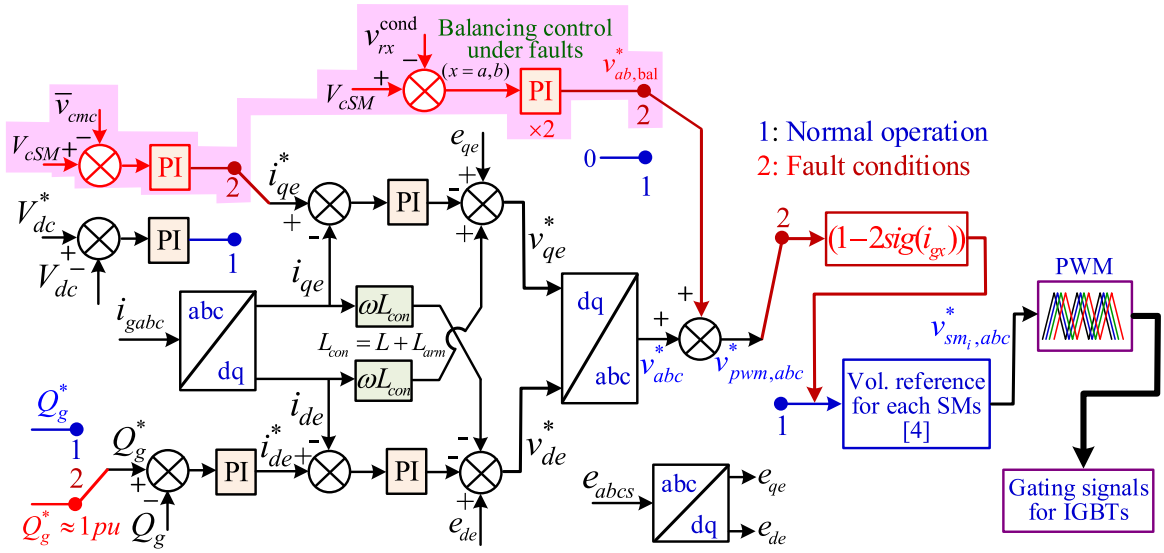

Fig. 10. Control block diagram of MMC under fault conditions.

energy as presented in [52] are utilized for the control variables. In this paper, an SM-capacitor voltage balancing control method is applied, where the average values of SM capacitor voltages obtained through the BSFs (band-stop filters) instead of capacitor energy are directly regulated. The q-axis current component is also regulated to adjust the real power exchange between the grid and the CMC, which helps keeping the SM capacitor voltages unchanged and compensate the losses by the fault resistance and converter, while the voltages of the individual arms are directly controlled to maintain at their nominal value.

Under the STATCOM operation of the MMCs using the hybrid scheme of the uCbSMs and HBSMs, the HBSMs are bypassed, where the SM capacitors are floating without charged and discharged action. So, only the capacitors of the uCbSMs are taking part in the operation, which are considered for the energy and voltage balancing. The average voltages of the uCbSMs capacitors in each arm are obtained as follows:

$$\bar{v}_{rx}^{c} = \frac{1}{N_c}\sum_{i=1}^{N_c} \mathrm{BSFs}\left(v_{c_i,x}^{r}\right) \quad (x = a, b, c \text{ and } r = \mathrm{up/low}) \tag{35}$$

where $\bar{v}_{rx}^{c}$ is the average value of upper or lower arm voltage in leg x, and $v_{c_i,x}^{r}$ is the ith-capacitor voltage of uCbSMs in the arm r of the leg x. $\mathrm{BSFs}(v_{c_i,x}^{r})$ is the voltages of $v_{c_i,x}^{r}$ filtered out by the BSFs at central frequencies of 60, 120, and 180 Hz.

With the alternative operation of the arms, the average capacitor voltage of the CMC, $\bar{v}_{\mathrm{cmc}}$, determined from three conducting arms simultaneously is calculated as follows:

$$\bar{v}_{\mathrm{cmc}} = \frac{1}{3}\sum_{x=a,b,c} v_{rx}^{\mathrm{cond}} \tag{36}$$

where v_{rx}^{cond} is the average value of the SM capacitor voltages in the conducting arm of the leg x, which is determined as follows:

$$v_{rx}^{\mathrm{cond}} = \left(\mathrm{sig}\left(i_{gx}\right)\bar{v}_{\mathrm{up}x}^{c} + \left(1 - \mathrm{sig}\left(i_{gx}\right)\right)\bar{v}_{\mathrm{low}x}^{c}\right) \tag{37}$$

where

$$\mathrm{sig}\left(i_{gx}\right) = \begin{cases} 1 & \text{if} \quad i_{gx} \geq 0 \\ 0 & \text{if} \quad i_{gx} < 0. \end{cases} \tag{38}$$

Fig. 10 shows an overall control block diagram of the MMC under both normal and dc-fault conditions, where the outer loops control the reactive power, Q_g, and the HVDC-link voltage, V_{dc}, at the normal operation and the average voltage of all SM capacitors, $\bar{v}_{\mathrm{cmc}}$, under the fault conditions. These controllers produce the current references, i_{dqe}^{*}, for the inner current control loops for the dq-axis components of the converter currents, where a vector current control strategy with the feed-forward and cross-decoupling terms is employed. In addition, the capacitor average voltages of the individual arms are also balanced at $V_{c\mathrm{SM}}$, which are regulated through the corresponding modulated phase voltages of cascaded-multilevel converter, $v_{sm_i,abc}^{*}$. Cooperating with the aforementioned average capacitor voltage control for $\bar{v}_{\mathrm{cmc}}$, only two controllers for the phases A and B are carried out for the individual arm voltage balancing, where the feedback arm voltages are determined from (35) and (37). The modulated voltage references $(v_{\mathrm{pwm},abc}^{*})$ are the summation of the outputs of the current controllers, (v_{abc}^{*}), and SM-capacitor voltage balancing controllers, $(v_{ab,\mathrm{bal}}^{*})$. Since the output voltages generated by the upper and lower arms of the CMC are opposite as depicted in Fig. 9, so the modulated voltage references $(v_{\mathrm{pwm},abc}^{*})$ for the upper arms need to be inversed determined from the sign of the phase currents as shown in Fig. 10. The voltage references $(v_{sm_i,abc}^{*})$ for the uCbSMs are determined according to the switching states as analyzed in Fig. 7 and Tables I-III. The carrier-phase- or level-shift-pulsewidth modulation (CP/LS-PWM) technique is employed to generate the gating signals for the SMs of the CMC [85], [108]–[112].

B. Fault-Tolerant Control of AAC and Hybrid-Based MMC

Fig. 11 shows the circuit diagram of the hybrid SM-based MMC and the AAC, where the hybrid-based MMC is config-

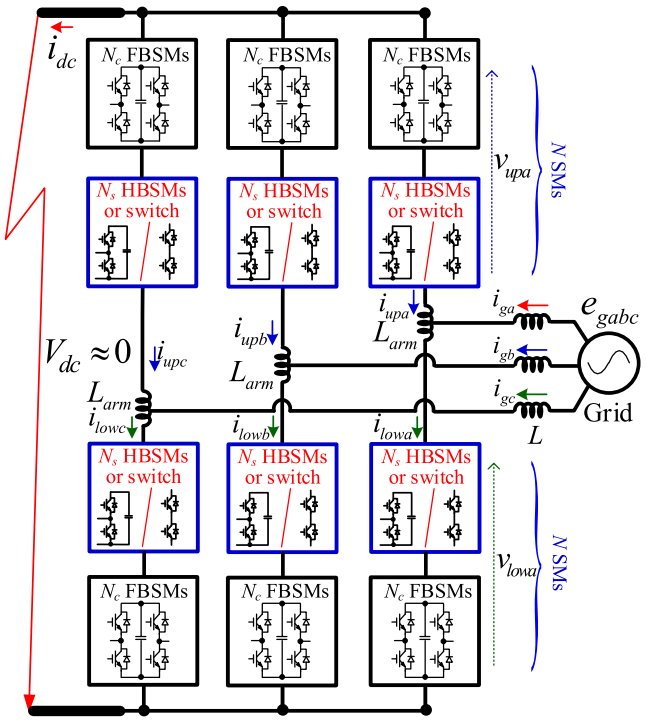

Fig. 11. Configuration of AAC and hybrid-based MMC with short circuit conditions.

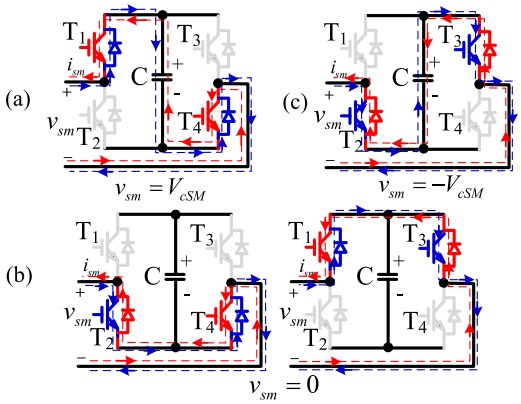

Fig. 12. Equivalent circuits and current paths of the FBSM for different voltage levels. (a) Positive. (b) Bypassed. (c) Negative.

ured by N_c FBSMs and N_s HBSMs per arm and the AAC arm consists of N_c FBSMs and direct switch [13], [33]. At normal operation, the FBSMs in the hybrid-based MMCs are operated as the HBSMs for producing zero and $V_{c\mathrm{SM}}$-voltage level, while the negative voltage level is not required. Due to an alternating conduction of the arms in the AAC, the FBSMs in the AAC are required to produce bipolar output voltages of $V_{c\mathrm{SM}}$, 0, $-V_{c\mathrm{SM}}$. Under the fault condition, the HBSMs in the hybrid SM-based MMC are bypassed by turning ON the lower switch of the HBSM, while the FBSMs in both the AAC and the MMC are operated in bipolar output voltage mode to control the grid currents. Fig. 12 shows the equivalent circuits and current paths of the FBSMs for different output voltage levels regardless the direction of the arm current and the switching states of the FBSM are listed in Table V.

TABLE V
SWITCHING STATES OF FBSM AT FAULT

Switches	T_1	T_2	T_3	T_4	i_{sm}	v_{sm}
Switching states	1	0	0	1	Any	V_{cSM}
	0	1	0	1	Any	0
	1	0	1	0		
	0	1	1	0	Any	$-V_{cSM}$

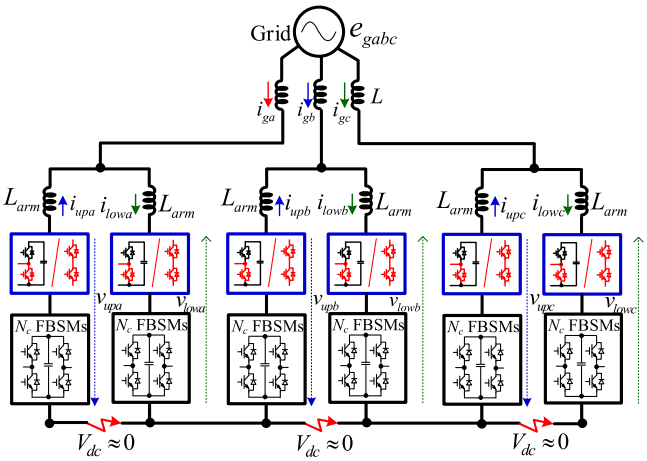

Fig. 13. Equivalent circuits of the AAC and hybrid SM-based MMC under P2P short circuit.

When the P2P short circuit occurs, the HVDC-link voltage is collapsed mostly to zero. The hybrid-based MMC and the AAC can be restructured as a CMC, where the FBSMs are utilized to produce the output voltage in bipolar for the grid current regulation, while the HBSMs in the MMC and the direct switches of the AAC are bypassed. As indicated in Fig. 12, the FBSMs can produce the bipolar output voltage with an independence of arm current direction, so the upper and lower arms can operate simultaneously in parallel connection. So, the reactive current compensation capacity of the cascaded-multilevel converter is increased twice compared to their rating, which is an advanced feature of the AAC and the hybrid-based MMC compared with the MMCs based on other SM circuits such as CDSMs, SCDSMs, uFBSMs, and CSSSs. Due to the increase of reactive current component higher than the rating, which may cause a high voltage drop on the inductor, so the current rating and inductance of ac input filter inductors in the converter should be properly selected. Fig. 13 shows an equivalent circuit diagram of the AAC/hybrid-based MMC under short-circuit faults. Similarly to the MMCs based on the uCbSMs, with the cascaded multilevel converter operation, the level number of the output voltages of the CMC is $2N_c + 1$ and the maximum magnitude of the fundamental phase voltage is described as in (31). Also, the FBSM number per arm in the hybrid SM-based MMC is required for the full reactive power regulation as presented in (34).

Similarly, from (19), (22), and (23), the number of FBSMs in each arm of the AAC to achieve the full range operation of the CMC is expressed as follows:

$$N_c \geq 0.858 \frac{V_{\mathrm{dc}}}{V_{c\mathrm{SM}}}. \tag{39}$$

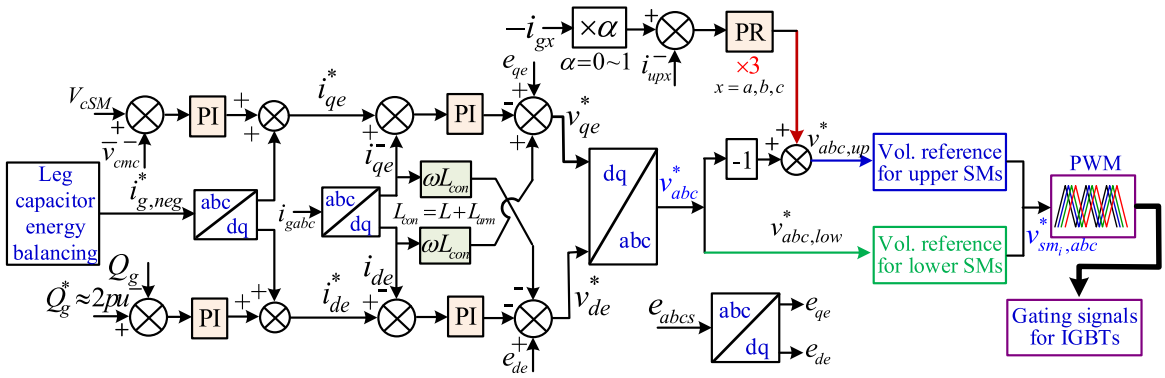

Fig. 14. Control block diagram of MMC and AAC under short-circuit conditions.

For controlling the grid-connected CMC under fault conditions, a vector current control strategy is also employed, where *d*–*q*-axis components of the converter currents are allocated to regulate the reactive/real powers, respectively, exchanged between the MMC and electric grid. Since the dc voltage is collapsed to mostly zero at the P2P short-circuit conditions, the MMC/AAC cannot transmit the real power between two sides. So, the MMC can be fully used for compensating the reactive current, where the reactive power can be provided to the grid up to 2 p.u. due to the parallel operation of the upper/lower converter arms in one phase [113], [114]. It is noted that due to the parallel connection of two arms, circulating current may exist in the two arms if the arm voltages are not equal to each other. In this case, the CMC cannot provide the reactive current up to 2 p.u. to the grid with a consideration of the current rating of the devices. So, the arm current controllers are required, which regulate the upper- and lower*-arm currents to be identical and being half of the corresponding phase current.

In addition, maintaining the voltages of the SM capacitors under the fault-tolerant operation is also essential for the CMC mode in order to obtain a satisfactory performance of the STATCOM operation and a fast recovery to the normal condition for the MMC/AAC after the fault clearance. The voltages of the SM capacitors can be maintained by balancing their energy, from which two methods for leg capacitor energy balancing for the hybrid SM-based MMC under dc short-circuit conditions were introduced in [52]. The first method is based on the voltage injection, where a common mode voltage is used to inject into the output terminal voltages of the CMC. Through the ac phase currents of the CMC, the injected voltages result in energy exchange among three legs, which assist to regulate the voltage of the SM capacitors in the three legs. The second method is utilizing the current injection, where a negative sequence component of the phase current is injected into the CMC. In accordance to the grid voltages, the injected currents produce the active power components in the three phases of the converter, by which the energies in the three phases are exchanged. These methods can also be applied for the AAC operating in the fault conditions.

A control block diagram of the hybrid-based MMC/AAC working as the CMC under fault conditions is shown in Fig. 14, where the CMC is also operating as a grid-connected converter and a PI-based vector control with the feed-forward and the cross-decoupling terms for the *dq*-axis grid current components is employed [96]–[99]. In this mode, the controller for keeping the average voltage of the SM capacitors of the converter, $\bar{v}_{\rm cmc}$, at the rated value, $V_{c\rm SM}$, is employed, whose output is the reference of the *q*-axis current component for regulating the real power exchange between dc and ac sides of the MMC/AAC. The reactive power of the converter is controlled by the *d*-axis current component, which can be regulated up to 2 p.u. In this case, each converter arm conducts half of the corresponding inversed phase current, where the arm current can be adjusted through the factor α as indicated in Fig. 14. The proportional resonant controllers at the line frequency are employed to regulate the upper arm currents, $i_{{\rm up}abc}$. The leg capacitor energy balancing control is also applied. Noting that the currents of the upper and lower arms can be controlled separately and differently, where only one of two arms can conduct the phase current ($\alpha = 0$ or $\alpha = 1$) or both of them conduct the phase current ($0 < \alpha < 1$) [33]. For modulating the reference voltages of the CMC, $v^{*}_{{\rm sm}_i,abc}$, the CP/LS-PWM techniques can be employed for generating the gating signals of the FBSMs of the CMC, where the voltage reference for the upper arm, $v^{*}_{abc,{\rm up}}$, is reversed from the controller output [4], [85].

V. Evaluation of MMCs

This section presents a comparison for different MMC configurations, which possess the dc-fault-ride-through capability. Six dominant converters analyzed in this paper are the MMCs configured by different SM circuits, such as the CDSMs, combinations of HBSMs and uFBSMs/CSSMs or SCDSMs, the hybrid-based MMCs, and the AAC. All the MMCs are designed to operate with the converter output voltage amplitude of about $0.4V_{\rm dc}$ and deliver the same rated power at $P_{\rm rate}$, while the HVDC-link voltage applied for the AAC is $0.628V_{\rm dc}$ for complying with the sweet spot operating point of the AAC and the HVDC-link voltage of the other MMCs is $V_{\rm dc}$. This comparison evaluates the dc-fault-ride-through performance in views of fault-current blocking time and capacity of reactive current compensation and semiconductor device count, which are summarized in Table VI. For the device count in Table VI, the voltage ratings of the IGBTs and diodes are identically selected as the SM capacitor voltage of $V_{\rm dc}/N$. Then, the submodule number in the MMC arm is determined, where the number of FBSMs, uFBSMs, CSSMs, and SCDSM is chosen as $N_c = 0.54\,\rm N$

TABLE VI
COMPARISON OF MMCS WITH DC-FAULT-RIDE-THROUGH CAPABILITY

Parameters \ MMCs		CDSMs	HBSMs-uFBSMs/CSSMs	SCDSMs	Hybrid SMs (HBSMs-FBSMs)	AAC
HVDC-link voltage		V_{dc}	V_{dc}	V_{dc}	V_{dc}	0.628 V_{dc}
Phase voltage amplitude		~ 0.4 V_{dc}	~ 0.4 V_{dc}	~ 0.4 V_{dc}	~ 0.4 V_{dc}	~ 0.4 V_{dc}
Ratings of devices		V_{cSM}=V_{dc}/N and I_{rat}				
Number of SMs per arm		N/2 CDSMs	0.46N HBSMs + 0.54N uFB/CSSMs	0.46N HBSMs+ 0.27N SCDSMs	0.46N HBSMs + 0.54N FBSMs	0.54N FBSMs
Number of levels		N + 1	N + 1	N + 1	N + 1	1.08N + 1
Additional devices per SM	IGBTs	1 for CDSM	1 for uFB/CSSM	2 for SCDSM	2 for FBSM	2 for FBSM
	Diodes	2 for CDSM	1 for uFB/CSSM	2 for SCDSM	0	0
Additional devices per arm	IGBTs	0.5N	0.54N	0.54N	1.08N	1.08N + 0.32N
	Diodes	N	0.54N	0.54N	0	0
Number of devices in total	IGBTs	15N	15.24N	15.24N	18.48N	14.88N
	Diodes	6N	3.24N	3.24N	0	0
Power delivery capability		P_{rate}	P_{rate}	P_{rate}	P_{rate}	P_{rate}
Fault current blocking	$V_{reversed}$	V_{dc}	1.08V_{dc}	1.08V_{dc}	1.08V_{dc}	1.08V_{dc}
	Performance	Satisfactory	Excellent	Excellent	Excellent	Excellent
STATCOM operation	Performance	Limited	Excellent	Excellent	Excellent	Excellent
	V_{max}	0.408 V_{dc}	0.44 V_{dc}	0.44 V_{dc}	0.44 V_{dc}	0.44 V_{dc}
	Capacity	1 pu	1 pu	1 pu	2 pu	2 pu

and the number of FBSMs in the AAC is selected as 0.539 N. With these designed structures, the reverse-biased voltages produced by these MMCs during the P2P short-circuit condition is 1.08 $V_{\rm dc}$ and their amplitude of the output phase voltage is about 0.44 $V_{\rm dc}$. Meanwhile, the reverse-biased voltage produced by the CDSM-based MMC is just $V_{\rm dc}$ and due to a parallel connection of two SM capacitors in the CDSM during fault, so the fault-blocking time of the CDSM-MMC is longer than the other MMCs as seen in (18). In addition, the maximum magnitude of the output fundamental phase voltage by the CDSM-based MMC during the STATCOM operation is just about 0.44 $V_{\rm dc}$. So, the controllability of the MMC with CDSMs is limited since its output voltage is not sufficient to control the converter phase current fully. Otherwise, the CDSM-based MMC is required to operate in a lower grid voltage (less than 0.4 $V_{\rm dc}$), which results in a low modulation index operation under normal condition. In view of reactive power compensation capability, the hybrid-based MMC and the AAC can compensate the reactive current to the grid twice their rating due to the parallel operation of the two converter arms per one leg, while the other MMCs based on uCbSMs are only able to inject the reactive current up to 1 p.u. due to the alternative operation of the two arms during the fault conditions.

It is seen in Table VI that the hybrid-based MMC requires the highest number of IGBTs, but no additional diodes are required. The numbers of IGBTs and diodes of the MMCs using the uFBSMs, CSSMs, and SCDSMs are the same, where the number of IGBTs is lower than in the case of the MMC based on FBSMs because a part of IGBT number in the FBSM-based MMC is replaced by the additional diodes. The number of additional diodes in the CDSM-based MMC is highest, while the IGBT number is slightly lower than those of the above MMCs. The AAC offers the lowest number of IGBTs without additional diodes compared with the other MMCs, while its fault-handling capability is also kept well with a double reactive current compensation comparing with its rating. However, the AAC requires the dc-link capacitors with very high voltage rating, while the other MMCs do not. Also, direct switches which utilize a high number of IGBTs connected in series are used. Due to the alternative operation of the converter arms, a remarkable sixth-order harmonic component of the dc current exists, which may require a large-sized reactor in the dc side.

It is worth noting that the additional IGBT and diode in the SCDSM as depicted in Fig. 2(g) can be realized by single semiconductor devices with $2V_{\rm dc}/N$-voltage rating instead of the series connection of two $V_{\rm dc}/N$-rated devices, which results in a lower number of separated semiconductor devices, hence for gating drivers, in the SCDSM than those in the FBSM, CDSM, uFBSM, and CSSM. It can be found from the datasheet of commercial IGBTs and diodes that the summation of conduction losses of two single devices is higher than that of a single device with double voltage rating [115]. Thus, the SCDSM-based MMC may offer advantages in terms of power loss, cost, and volume compared with the other MMCs.

Another issue for the studied MMC topology is that the additional IGBTs are continuously conducting the arm current, which may cause a higher power loss compared to other devices in the SM. This will have a negative impact on the loss distribution of the SMs and the converters. As reported in [116] that the director switches of the AAC with a continuous conduction are operated in the allowable range of the temperature. In the next section of simulation demonstration, the power losses, the performance of fault-current handling, and reactive power compensation capabilities of the studied MMCs and AAC will be illustrated.

VI. SIMULATION DEMONSTRATION

In this section, the performance and comparison among various MMCs in terms of power losses, fault-blocking time, and reactive power compensation capacity are evaluated. PSIM simulation tests for the conventional HBSM-based MMC and five MMCs structured by different SM circuits such as the CDSMs, SCDSMs, uFBSMs/CSSMs, hybrid scheme of HBSMs and FBSMs, and the AAC were carried out, which investigate the responses of these MMCs under both normal and fault conditions. Due to a high number of simulations for six different converters, in order to reduce the simulation running time, the

TABLE VII
PARAMETERS OF MMCS IN HVDC SYSTEM

Parameters	Values
Ratings	400 MW-300 kV for MMCs
	400 MW-172 kV for AAC
Grid voltage	33 kV / 60 Hz
Transformer (Y/Δ)	33/134.7 kV
Number of SMs per arm	8 HBSMs
	4 CDSMs
	2 SCDSMs + 4 HBSMs
	4 uFBSMs + 4 HBSMs
	4 FBSMs + 4 HBSMs
	4 FBSMs + Direct switch for AAC
SM capacitor	37.5 kV – 180 μF
Arm inductance	8 mH
DC-cable characteristics	0.082 Ω/km, 0.8 mH/km, 0.16 μF/km
DC-cable length	125 km
Short-circuit resistance	4.5 Ω
Carrier frequency	600 Hz

simulated HVDC system is simplified, which is configured by an MMC and a dc voltage source. Nine-level MMCs utilizing different SM structures with device-based model were implemented [117], [118], where the numbers of SMs in each converter arm for different MMCs and AAC and the parameters of the system are listed in Table VII. It is noted that the HVDC-link voltage for the AAC is different from those of the MMCs, from which their delivered power and current ratings are the same as those of the other ones.

A. Loss Evaluation

The C language interfacing with PSIM-based simulation programing is employed to calculate the power losses of the MMCs with the parameters in Table VI. The switches of the SMs in the MMCs are realized by the commercial ABB IGBT 5SNA 1600N170100 (1.7 kV and 1.6 kA) and 5SNA 1500E330305 (3.3 kV and 1.5 kA), where the converter power losses are calculated according to the device characteristics obtained from this datasheet [115]. The single switch of the SMs may require series and parallel connections of many 5SNA 1600N170100 or 5SNA 1500E330305 to comply with the voltage and current ratings of the SMs listed in Table VII. It is believed that even with the series and parallel connection of the single IGBTs to build the SMs, the power losses obtained are the same with the case of single IGBTs used for the SMs in the MMCs with a high number of SMs [5].

The total power loss of the MMCs are the summation of the conduction and switching losses of all IGBTs and diodes in the converter, which are calculated from the arm currents flowing through all switches, saturation forward voltages, and the ON/OFF energies of IGBTs and diodes and the switching gating signals to determine the conduction state of individual devices [5], [119–123]. The saturation forward voltages and the ON/OFF energies of the IGBTs and diodes are obtained as a function of the simulated arm current from the datasheet, where the arm currents are sensed in every simulation step of 5 μs. It is noted that for the simulation tests, the switches of the SMs in the MMCs are initialized ideally for decreasing the simulation time. Table VIII lists the power losses of the studied MMCs,

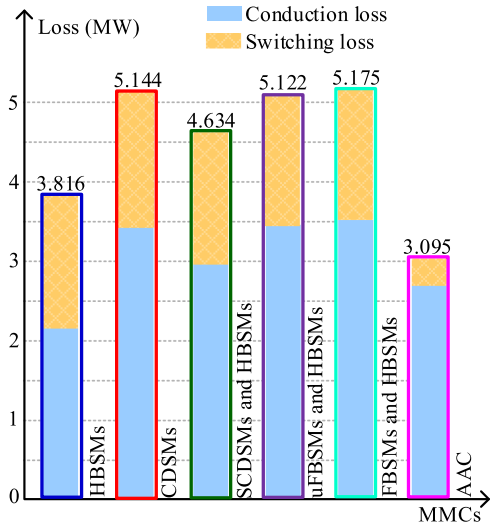

Fig. 15. Power loss comparison of five MMCs.

which are operating at the rating conditions. The power loss of the standard HBSM-based MMC is about 0.955%. It is seen that the AAC power loss is about 0.79%, which is lowest compared with the other MMCs. The reason is that the operation of the AAC is based on the alternating arm conduction and the number of IGBTs in the AAC is also lowest. The power losses of the MMCs based on the CDSMs and hybrid schemes of HBSMs and either FBSMs or uFBSMs/CSSMs are mostly similar, which are about 1.284%, 1.295%, and 1.280%, respectively. However, the power loss of the SCDSM-based MMC is about 1.156%, which is lower than those of the above MMCs. Fig. 15 shows a power loss comparison among various MMCs, which also indicates the conduction and switching losses of each MMC.

B. Fault-Blocking Time Investigation

In this section, the fault-current blocking time of the AAC and MMCs based on the four above SM topologies is investigated. The HVDC system based on the MMC is initially operating in a steady-state condition, which delivers the rated real power of about 400 MW to the dc side. A P2P short circuit occurs at the location of about 65 km from the dc terminal of the MMC at 0.25 s, where a short-circuit resistance of 4.5 Ω is applied. The equivalent inductance including the dc-cable inductance, input-filter, and arm inductances in these MMCs is about 250 mH. The sampling time for the fault detection in these simulation tests is 100 μs.

For investigating the fault response time, when the short-circuit condition is detected, all the IGBTs of the MMCs and the AAC are turned OFF instead of switching the converters to the fault-tolerant control mode. By turning OFF all the IGBTs of the converters, eight SM capacitors in two different legs are connected in series and create the reverse-biased voltages, which make the dc-cable currents to be decayed to zero and blocked within a certain time as illustrated in Fig. 16. Since the number of SM capacitors creating the reverse-biased voltage for blocking fault current is the same for all the MMCs and the AAC, the fault-current blocking times of these converters are similar. Fig. 16(a) shows the blocking time of the CDSM-

TABLE VIII
LOSS EVALUATION OF DIFFERENT MMCS

MMCs / Losses	HBSMs	CDSMs	SCDSMs and HBSMs	uFB/CSSMs and HBSMs	Hybrid SMs (HB-FB)	AAC
Operating power	399.8 MW	400.7 MW	400.8 MW	400.0 MW	399.5 MW	392.0 MW
Conduction loss	2.174 MW	3.467 MW	2.966 MW	3.468 MW	3.496 MW	2.733 MW
Switching loss	1.641 MW	1.677 MW	1.668 MW	1.654 MW	1.679 MW	0.362 MW
Total loss	3.816 MW	5.144 MW	4.634 MW	5.122 MW	5.175 MW	3.095 MW
	0.955%	1.284%	1.156%	1.281%	1.295%	0.790%
Fault-blocking time	Impossible	2.449 ms	2.370 ms	2.387 ms	2.283 ms	2.155 ms

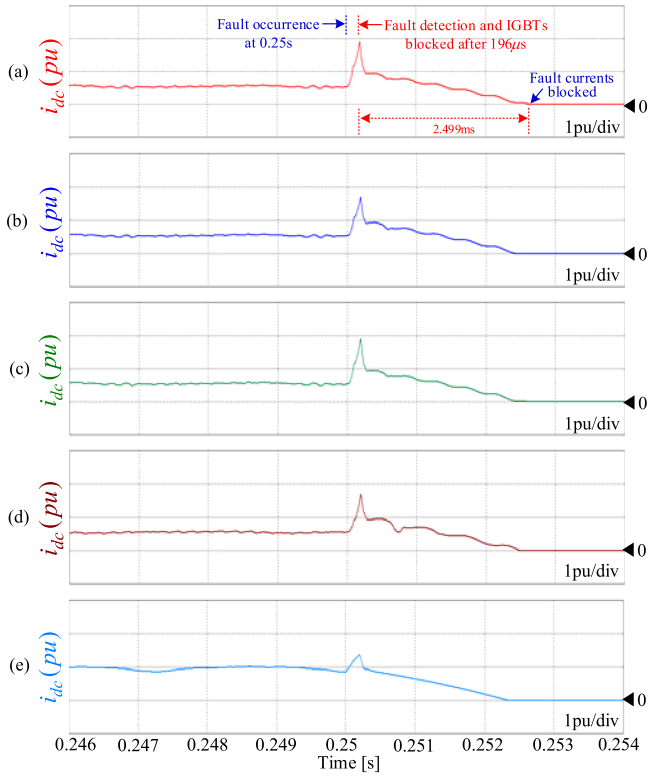

Fig. 16. DC-cable currents for current-blocking analysis in MMCs based on (a) CDSMs, (b) SCDSMs, (c) uFBSMs, (d) HBSM/FBSM-based hybrid scheme, and (e) AAC.

based MMC being about 2.449 ms, which is the highest time compared with the response of the other ones. The reason is that the equivalent capacitance connected in the fault-current path in the CDSM-based MMC is higher than those of the other converters. This matches with the analysis in Section III. The fault-blocking time of the AAC is about 2.155 ms as shown in Fig. 16(f), which is the lowest compared with the MMCs.

C. DC-Fault-Ride-Through With STATCOM Operation

1) MMCs Based on Alternating Arm Operation During Fault: The MMC using the hybrid scheme of uFBSMs and HBSMs representing for the uCbSM-based MMCs is investigated in this simulation, where the MMCs are able to operate as STATCOM with alternating arm conduction during P2P short-circuit conditions. The normal and fault-tolerant operations of the MMC are demonstrated in Fig. 17, where a P2P short-circuit fault occurs at 0.25 s, which lasts for 0.75 s and recovers at 1 s. At normal operation, the MMC is operating to deliver the real power of 0.8 p.u. and absorb 0.6 p.u.-reactive power to/from the grid. During fault condition, the MMC is operated in the tolerant-control mode to provide 0.95 p.u.-reactive power within $(0.25 \sim 0.75)$ s and 0.2 p.u. during $(0.75 \sim 1)$ s to the grid.

The HVDC-link voltage is shown in Fig. 17(a), which drops mostly to zero during the fault duration of $(0.25 \sim 1)$ s. Fig. 17(b) shows the dc-cable current, which is increased excessively when the fault occurs. Then, the fault-tolerant operation is activated, which keeps the fault currents in the allowable range. The three-phase currents of the MMC are shown in Fig. 17(c), which will be magnified in Figs. 18 and 19. Fig. 17(d) shows the *dq*-axis components of the converter currents, where the actual currents track their reference closely to show the well-performed current controllers in both normal and fault conditions. It is noted that at the fault operation, the *q*-axis current component is controlled to exchange the real power for maintaining the SM capacitor voltages only as shown in Fig. 17(d), which is mostly zero. Fig. 17(e) shows the real and reactive powers flowing through the MMC in normal and fault conditions, which are proportional to the corresponding current components in Fig. 17(d). Fig. 17(f)–(h) show the arm currents, SM capacitor voltages, and arm voltages, respectively, which will be magnified in Figs. 18 and 19 to show the converter control response in both normal and fault operation. From the above results, it is illustrated that the switching mode control of the MMC from the normal condition to the faulty operation and *vice versa* is performed smoothly, where the transient values of the voltages and currents are limited within the allowable ranges.

Fig. 18 demonstrates the performance of the uFBSM-based MMC in normal condition. Fig. 18(a) shows the three-phase currents of the MMC, which are pure sinusoidal and balanced at 1 p.u. The upper/lower arm currents of the phase A are shown in Fig. 18(b), which are opposite in the phase and have the same amplitude. It is seen in Fig. 18(c) that the capacitor voltages of the HBSMs and uFBSMs in the upper and lower arms are well maintained around the rating of 37.5 kV. Fig. 18(d) shows the upper/lower arm voltages of leg A, which are unipolar in positive side only and contain nine levels. Fig. 18(e) shows the output phase voltage of the MMC and its reference.

The control performance of the MMC operating as the CMC during the dc fault is illustrated in Fig. 19, which magnifies the waveforms from Fig. 17. Fig. 19(a) shows the dc-line current and the three-phase currents of the CMC, where the phase currents are balanced and pure sinusoidal. The dc-line current is always equal to one of the three phase currents within one-sixth of fundamental cycle depending on the direction of phase cur-

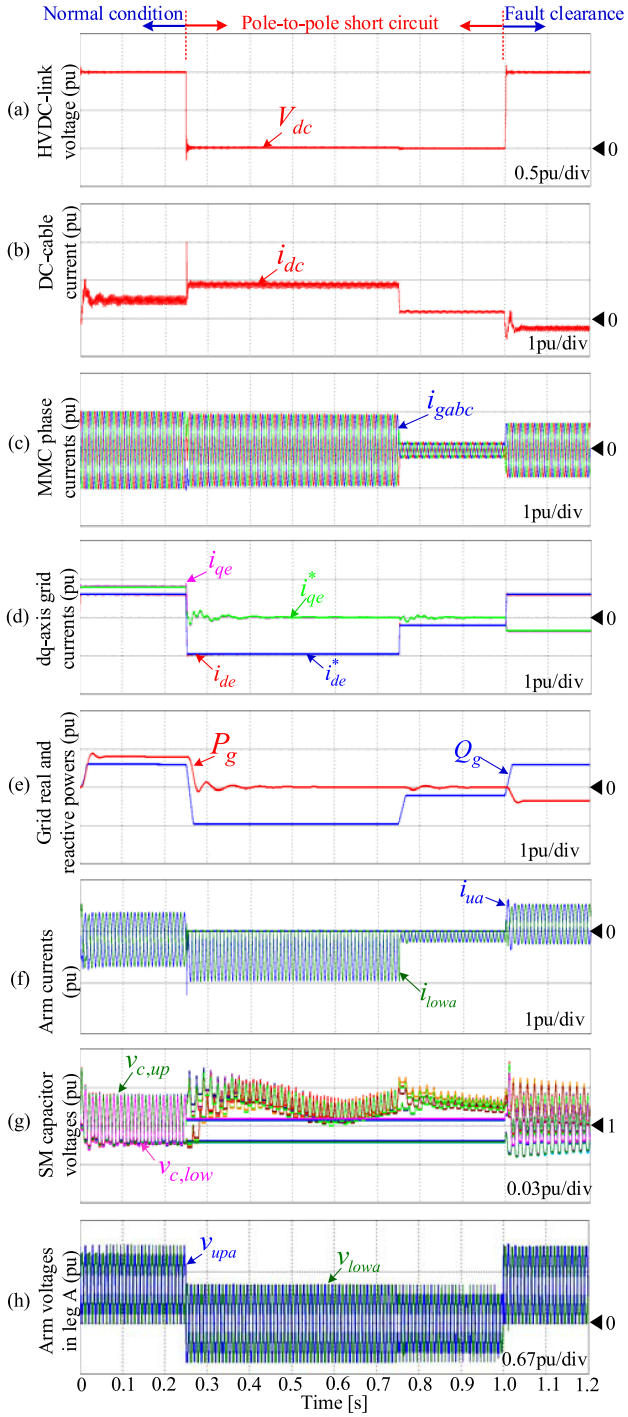

Fig. 17. Operation of the MMC based on hybrid scheme of HBSMs and uFBSMs in normal and fault-tolerant modes. (a) HVDC voltage. (b) DC-cable current. (c) MMC phase currents. (d) *dq*-axis currents. (e) MMC active and reactive powers. (f) Upper/lower arm currents. (g) SM capacitor voltages. (h) Upper/lower arm voltages.

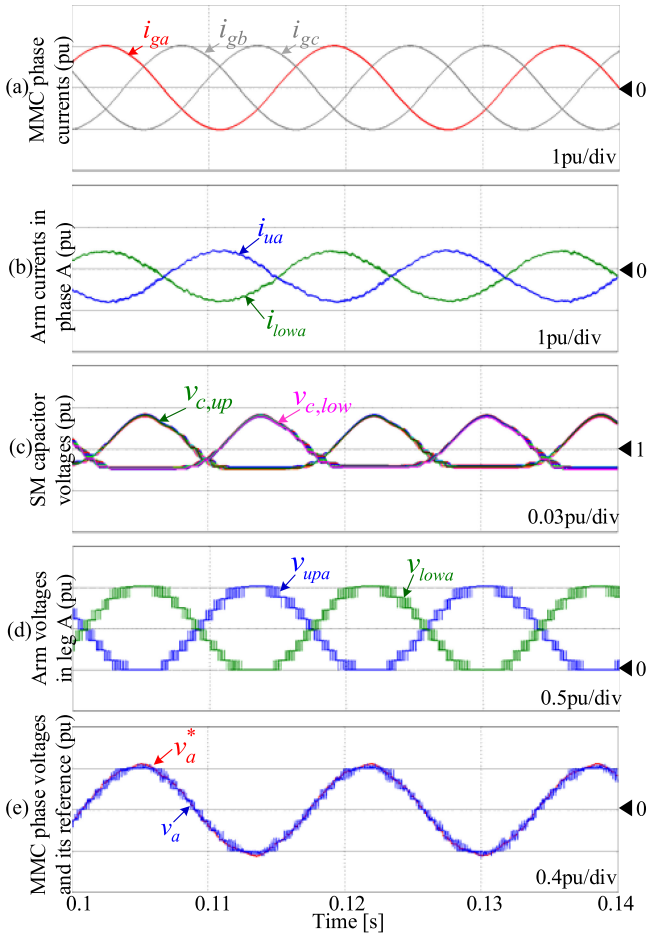

Fig. 18. MMC based on hybrid scheme of HBSMs and uFBSMs in normal operation. (a) Phase currents. (b) Arm currents. (c) SM capacitor voltages. (d) Arm voltages. (e) Terminal voltage and its reference (red).

rents as shown in Fig. 19(a). Fig. 19(b) shows the upper/lower arm currents of leg A. It is seen that when the phase current is positive, the upper arm is in the conduction mode and the lower arm is off. So, the upper arm conducts the phase current fully, which means that the phase current is the same as the upper arm current and the lower arm current is zero, which is demonstrated from Fig. 19(a) and (b). Inversely, when the phase current is negative, the phase current is the same as the lower arm current and the upper arm current is zero. Fig. 19(c) and (d) show the upper/lower arm SM capacitor voltages of the CMC, respectively, where the HBSM capacitor voltages in both conducting arms and blocked arms are kept unchanged since the HBSMs are bypassed and the capacitors are floating. In addition, the capacitor voltages of all SMs (HBSMs and uFBSMs) in the blocked arm are unchanged due to no current flow. Meanwhile, the capacitors of the uFBSMs in the conducting arms are charged in one-fourth of the fundamental cycle and discharged in the next one-fourth of the fundamental cycle, which depends on the corresponding arm voltages as shown in Fig. 19(e). It is seen in Fig. 19(e) that the upper/lower arm voltages of the MMC operating in the fault condition are bipolar. The arm voltages are also multilevel waveforms with a step change of SM capacitor voltage of 37.5 kV.

2) MMCs Based on the Hybrid Scheme of HBSMs and FBSMs During Fault: In this section, the performance of the MMCs based on the hybrid scheme of HBSMs and FBSMs is investigated, which represents for the hybrid-based MMCs and the AAC being capable of operating as STATCOM with two arms in the same leg connected in parallel during the P2P short-circuit fault. Fig. 20 shows the performance of the hybrid-SM-based MMC in normal and fault conditions, which correspond to those shown in Fig. 17 for the performance of the MMC based

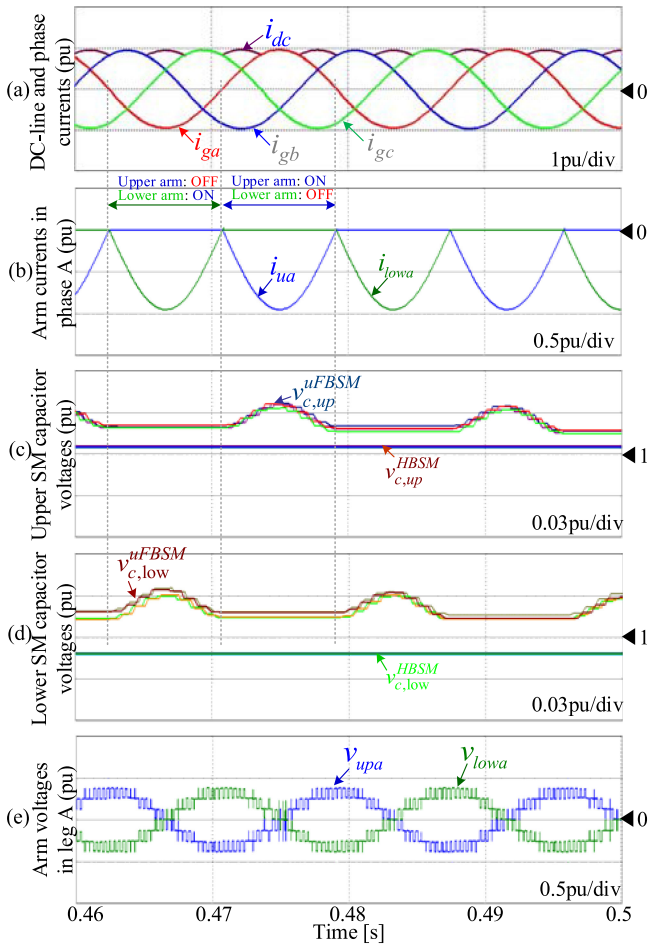

Fig. 19. Performance of fault-tolerant control of MMC based on hybrid scheme of HBSMs and uFBSMs. (a) DC-line and phase currents. (b) Upper and lower arm currents of leg A. (c) Upper SM capacitor voltages. (d) Lower SM capacitor voltages. (e) Upper/lower arm voltages.

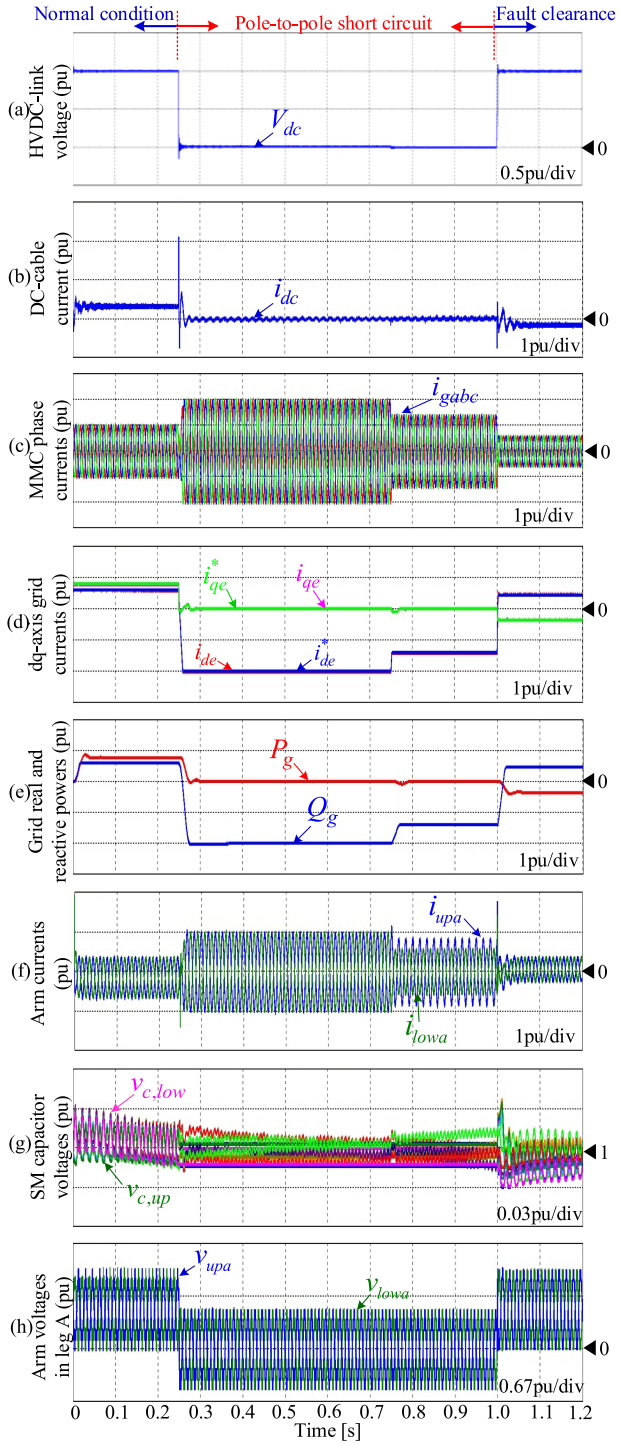

Fig. 20. Normal and fault-tolerant operations of the MMC based on hybrid scheme of HBSMs and FBSMs. (a) HVDC voltage. (b) DC-cable current. (c) Phase currents of MMC. (d) *dq*-axis currents. (e) MMC active and reactive powers. (f) Upper/lower arm currents. (g) SM capacitor voltages. (h) Upper/lower arm voltages.

on the uCbSMs. In the steady state, the hybrid-based MMC is also operating with the current rating for delivering 0.8 p.u.-real power and 0.6 p.u.-reactive power. During the fault, the currents flowing through the MMC are double up to 2 p.u. for providing 2 p.u.-reactive power to the grid from 0.25 to 0.75 s as shown in Fig. 20(c)–(e). In this operation mode, the arm current in each arm of the converter leg conducts the arm current of 1 p.u., which is symmetrical through zero as shown in Fig. 20(f). In addition, the *d*-axis current reference of the CMC is changed to 1.4 p.u., where the upper and lower arms conduct the phase current differently being 0.8 and 0.6 p.u., respectively, as shown in Fig. 20(f) for the duration of 0.75–1 s. Figs. 21–23 will magnify the waveforms in Fig. 20 to explain and analyze the performance of the hybrid-based MMC in the normal and fault condition, respectively.

The performance of the hybrid-based MMC is demonstrated in Fig. 21, where these waveforms correspond to those in Fig. 18 for the case of the uCbSM-based MMC operation. The results show that the operation of the hybrid-based MMC is similar to that of the uCbSM-based MMC, where the three-phase MMC currents also are balanced and sinusoidal as shown in Fig. 21(a) and the SM capacitor voltages are maintained closely to the rating as shown in Fig. 21(c). Fig. 21(d) shows the arm voltages of the hybrid-based MMC, which are unipolar and have nine-level waveforms similar to Fig. 18(d).

Fig. 22 shows the operation of the hybrid-based MMC during the P2P short-circuit fault, where the phase currents are regulated well as shown in Fig. 22(a). During the fault, both arms of

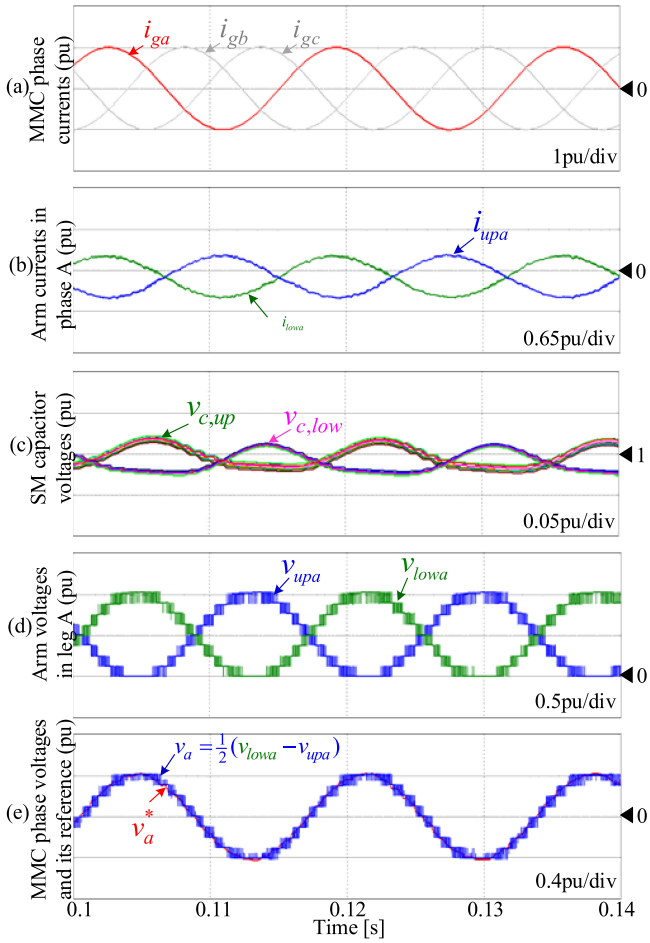

Fig. 21. Performance of MMC based on hybrid scheme of HBSMs and FBSMs in normal condition. (a) Phase currents. (b) Arm currents. (c) SM capacitor voltages. (d) Arm voltages. (e) Terminal voltage and its reference (red).

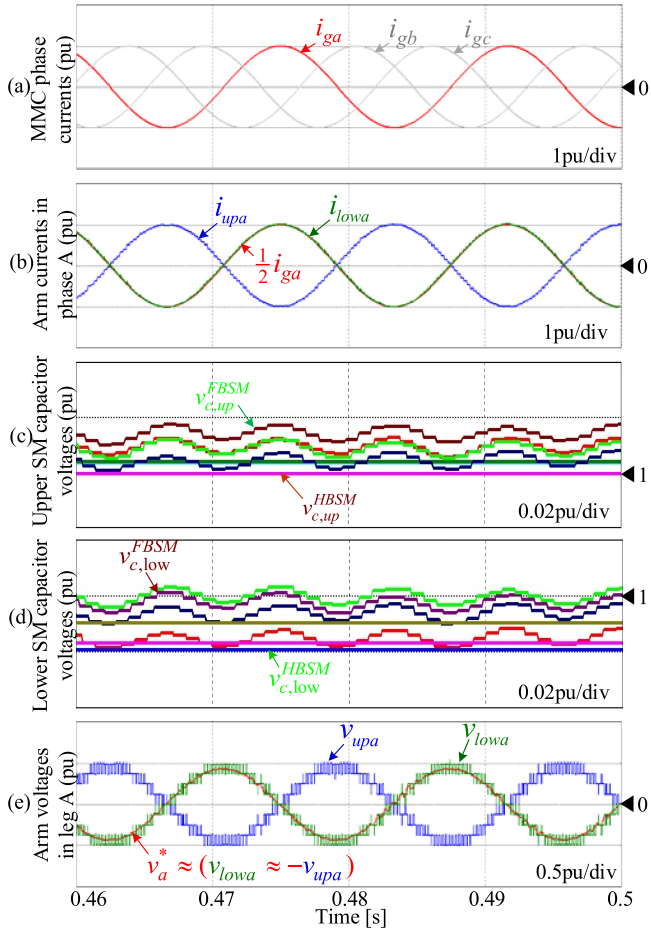

Fig. 22. Performance of fault-tolerant control of the MMC based on hybrid scheme of HBSMs and FBSMs. (a) Phase currents. (b) Upper/low arm currents of leg A. (c) Upper SM capacitor voltages. (d) Lower SM capacitor voltages. (e) Upper/lower arm voltages.

the converter leg are operated to adjust the corresponding arm currents as shown in Fig. 22(b), where it is seen that the arm currents are controlled to be half of the grid phase current. So, the phase current of the MMC can reach to 2 p.u. when each converter arm conducts the rated current as shown in Fig. 22(a) and (b). The upper and lower arm SM capacitor voltages are shown in Fig. 22(c) and (d), respectively, which are charged or discharged depending on the arm currents and still kept around its rating with a variation of about 3%. The arm voltages are produced in bipolar mode with a nine-level waveform as shown in Fig. 22(e), which are similar to the reference of the output terminal phase voltage.

Fig. 23 demonstrates the control performance of the hybrid-based MMC operating as the CMC, where the magnitudes of the upper and lower arm currents are controlled to be different. At 0.75 s, the phase current is changed from 2 to 1.4 p.u., by setting $\alpha = 0.57$ as indicated in Fig. 14, the upper arms conduct the current at 0.8 p.u. and the lower arms conduct the current at 0.6 p.u. as shown in Fig. 23(a). Fig. 23(b) and (c) show the upper/lower SM capacitor voltages, respectively, which are still kept close to their rating value. In addition, it can be seen in Fig. 23(b) and (c) that the ripples of the upper SM capacitor

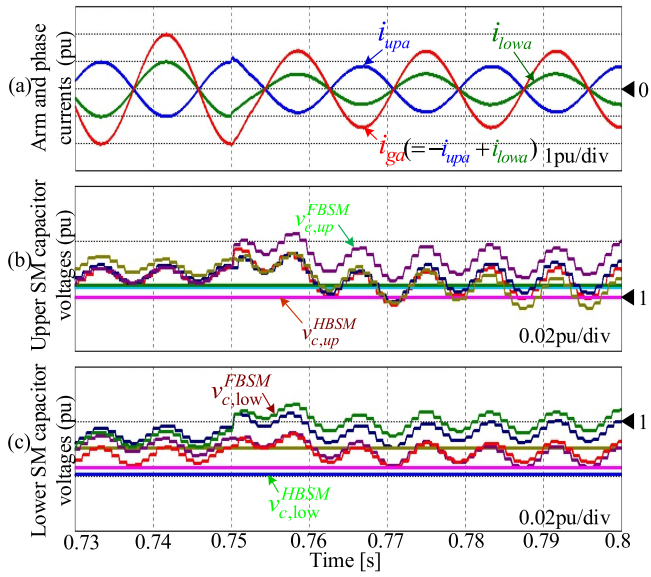

Fig. 23. Performance of the MMC based on hybrid scheme of HBSMs and FBSMs at changing arm current reference during fault-tolerant control. (a) Phase and arm currents. (b) Upper SM capacitor voltages. (c) Lower SM capacitor voltages.

voltages are slightly higher than those of the lower SM capacitor voltages, since the current amplitude flowing through the upper arm is higher than in the lower arm.

VII. Discussions

As highly required from the system operators for complying with the power quality and system stability in the modern power systems, the MMCs in the HVDC transmission systems have been remarkably developed in terms of structures and control algorithms to satisfy the requirements of the grid codes as well as improving the system efficiency, investment cost, and volume. So far, the standard MMC based on the HBSMs is a preferred choice for the applications in the HVDC system. However, the HBSM-based MMC will lose the operation and may be damaged by excessively high fault currents when the short-circuit faults occur in the dc side. The protection device of hybrid circuit breakers for the HVDC transmission systems has been developed by ABB Co., which is highly potential to be applied for limiting the fault currents and isolating the faults. The coordination operation of the HBSM-based MMCs and the hybrid CBs has been introduced. The AAC offers a high operation efficiency even higher than the HBSM-based MMC and provides a fault-handling capability with a double capacity of reactive power compensation to the electric grid during dc-side faults. However, due to alternating conduction of the arms in the same leg, the current in the dc side of the AAC contains a sixth-order harmonic ripple, which may require reactor filters in the dc side. In addition, the AAC is just operating with a specific relationship of the ac- and dc-side voltages to ensure an energy balance between the two sides.

All the modified SM topologies such as the CDSM, SCDSM, uFBSM, and FBSMs require additional devices, which lead to demerits in terms of power loss, cost, volume, assembling, and the cooling system. The SCDSM-based MMC gives lower power loss compared with the other ones, which however requires using separated additional devices of IGBTs and diodes and different semiconductor device types to obtain a reduced power loss. This causes challenges for the device assemble, cooling system, and power loss distribution on the devices. Although the power loss of the MMC based on the hybrid scheme of HBSMs and FBSMs is slightly higher than that of the SCDSM-based MMC, the hybrid-based MMC is considered as the most promising topology to comply with the requirements of fault-current blocking and reactive power compensation. The hybrid-based MMC can be assembled by the unified semiconductor devices of commercial dual IGBT modules and IGBT H-modules. In addition, the hybrid-based MMC provides additional capabilities for the loss distribution of the devices and SM capacitor voltage balancing and high capacity of reactive power compensation for stabilizing the grid. Thus, the hybrid configuration of MMCs based on the HBSMs and FBSMs will be the most preferred choice for the applications of the HVDC transmission systems.

Even though a huge number of studies and significant effects on the research of the MMCs have been demonstrated so far, unsolved issues and research direction for the MMCs below are still paying remarkable attention to the researchers in the new future. First, it is known that the number of the SM capacitors in the classical MMC and the aforementioned MMC configurations is large and the capacitors are normally the weakest and bulky components in the power electronic converters. Further research works, which focus on a reduction of the SM capacitances and SM capacitor voltage ripple at low frequencies, are essential. At the dc short-circuit faults, the unbalanced condition of the grid voltages will have effect on the operation of the MMC as the STATCOM, where controller algorithms and compensation strategies with providing the mitigation for negative sequence component and the oscillation on the SM capacitor voltages should be taken into account. In this case, sizing the SM capacitors is an important issue. In addition, with a high redundancy of the switching states in the MMCs based on the uCbSMs and FBSMs, new modulation techniques and control algorithms may break through the dimension of SM capacitors.

Next, the cost and complexity of the MMCs will be highly reduced with a reduction of the voltage sensors required for sensing the SM capacitor voltages. Even though few research works have introduced several methods to estimate such voltages, more deep research works are necessary to estimate the SM capacitor voltages consequently eliminating the number of the voltage sensors with a consideration of the reliability and stability of the system operation.

Third, thermal regulation for the semiconductor devices in the MMCs and especially in the MMCs with additional series IGBTs can help to lower the device damage possibility and enhance the lifetime of the switching devices. This also assists to reduce and simplify the cooling systems, which are normally not paid much attention from the researchers.

Finally, with many derived- and proposed-MMC topologies, it is believed that new configurations of the MMCs would be found out in the near future, which offer more merits compared to the existing ones in terms of cost, loss, volume, efficiency, and reliability in the steady-state operation as well as better performance in the dc fault-ride-through capability. Therefore, there are a plenty of space for the research in developing the converter topologies in view of switching, controllers, and grid synchronization schemes. In addition, new structures of the multilevel converters for achieving shunt and series compensation to enhance dynamic and fault-ride-through operations under both dc- and ac-side faults are still the research direction in the field of HVDC systems.

VIII. Conclusion

In this paper, the general overview and comprehensive understanding for the MMCs based on various SM circuits such as the CDSMs, the hybrid of HBSMs and SCDSMs, uFBSMs/CSSMs, FBSMs, and the AAC being capable of limiting the fault currents and providing the reactive power to the grid under dc-cable short-circuit conditions have been presented. The fault-current blocking principle and response of these MMCs under dc faults have been introduced and compared through the theoretical analysis and simulation studies. Two types of STATCOM operation based on arm-alternating conduction of the MMCs based on the

uCbSMs and arm-parallel connection of the hybrid-based MMC and the AAC are presented in detail, where the SM capacitor voltage balancing are taken into account. The simulation studies for the six MMCs based on different SMs have demonstrated and validated the analysis including the fault-current blocking performance, reactive power compensation capacities, and the converter power losses.

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