A Structurally Reconfigurable Resonant Dual-Active-Bridge Converter and Modulation Method to Achieve Full-Range Soft-Switching and Enhanced Light-Load Efficiency

Yiu Pang Chan, *Student Member, IEEE*, K. H. Loo, *Member, IEEE*, Muhammad Yaqoob, *Student Member, IEEE*, and Y. M. Lai, *Member, IEEE*

***Abstract*—This paper proposes a reconfigurable dual-active-bridge (DAB) converter that is capable of switching between two converter structures for enhancing its performances at different output power levels. For 50%–100% load, the converter operates in full-bridge mode and achieves soft-switching in all switches independently of the input-to-output voltage ratio. Below 50% load, the converter is reconfigured to operate in half-bridge mode for reduced circulating current and improved light-load efficiency while maintaining the desired soft-switching characteristic of full-bridge mode. The achievement of soft-switching is aided by the use of a tuned LCL resonant tank, which enables an accurate prediction of the phases of tank currents with respect to tank voltages, and therefore simplifies the realization of soft-switching. The effects of dead time are discussed and expressions for guiding the selection of appropriate dead time for ensuring soft-switching in practical implementation are derived. The proposed converter and the modulation scheme are experimentally verified with a 1.6-kW converter prototype, which demonstrates their merits in comparison with a nonreconfigurable, full-bridge DAB topology and conventional modulation schemes.**

***Index Terms*—Dual-active-bridge (DAB) converter, immittance network, reconfigurability, resonant converter, soft-switching.**

I. Introduction

THE use of renewable energy has become increasingly important due to the fast depletion of fossil fuels. However, the main drawback of renewable energy stems from the dynamic mismatches between energy supply and demand due to the intermittent nature of renewable energy sources. These mismatches can be effectively compensated by energy storages, which act as energy sources when there is shortage of renewable energy and vice versa [1]–[3]. To enable the connection of energy storages such as batteries and super-capacitors to the power grid,

Manuscript received March 30, 2018; revised June 23, 2018; accepted July 26, 2018. Date of publication August 2, 2018; date of current version March 29, 2019. This work was supported by The Hong Kong Polytechnic University Central Research under Grant G-YBR1. Recommended for publication by Associate Editor D. G. Lamar. *(Corresponding author: Yiu Pang Chan.)*

The authors are with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Hong Kong (e-mail:

various aspects such as lower device stress and more flexible power control [19]–[23].

From the conventional DAB converter using a single inductor as energy-transfer element evolved a number of resonant DAB converter topologies using second- or higher-order resonant tanks for energy transfer [24]–[26]. In comparison with the conventional topology, resonant DAB topologies offer the advantages of extended soft-switching range and reduced RMS current, hence reduced conduction loss and better transformer utilization. Specifically, DAB converters based on tuned LCL or CLC networks are attractive due to the in-phase (or anti-phase for reverse power flow) relationship between the high-frequency ac voltage and current at each terminal of the resonant tank [27]–[29]. For these resonant DAB converters, the external phase shift is kept constant at $\pm\pi/2$ and DPS modulation is used for realizing power control. Although circulating power is eliminated and conduction loss is significantly reduced, their switches suffer from hard switching at all operating power levels except at 50% duty cycle. A linear state-space model for a DAB converter with tuned $CLLC$ network was proposed for improving the soft-switching range of the converter [30]. However, higher order voltage and current harmonics cannot be effectively suppressed by $CLLC$ network, particularly in low-power operation. In addition, the effect of introducing dead time to gate drive signals is critical to the analysis and accurate prediction of soft-switching conditions, and must be carefully considered. Failure to do so will cause the shrinkage of soft-switching range and degradation in switching performance.

In this paper, a DAB converter system comprising a reconfigurable DAB converter and an enhanced DPS modulation scheme is proposed. In conjunction with the use of a tuned LCL immittance network, the proposed DAB converter system is capable of achieving full-range soft-switching operation independently of the input-to-output voltage ratio. Besides, by switching between full-bridge and half-bridge configurations, the proposed DAB converter can operate with 50% input voltage under light-load condition, leading to reduced circulating power and conduction loss. The overall efficiency is enhanced due to reduction in both switching and conduction losses. The idea of reconfigurability between full-bridge and half-bridge operations for enhancing light-load efficiency has been demonstrated for conventional DAB converter in [31]. However, without full-range soft-switching, the DAB converter still suffers from switching loss and all problems that follow from it such as degradation in device reliability and higher heat dissipation, and thus more expensive thermal design.

The main drawback associated with the proposed reconfigurable DAB converter is the need for additional active devices (two MOSFETs and two diodes) and passive components (one resonant inductor and one resonant capacitor), which leads to an increase in volume and cost. Furthermore, the proposed modulation scheme is applicable to resonant tanks with immittance characteristics only [34]. Nevertheless, as is discussed further in this paper, the increase in volume and size is well compensated by the increased degrees of freedom in power control of a reconfigurable DAB converter, with which full-range soft-switching is attained and "flatness" in efficiency is achieved over a wide load range. By means of full-range soft-switching, the reliability of the switching devices can be improved and devices with lower voltage rating, and hence lower cost and lower on-state resistance, can be selected. These devices also have less heat dissipation and therefore smaller heat sinks can be used.

This paper is organized as follows. Section II analyses the converter's operation in both full-bridge and half-bridge modes, and proposes a new modulation scheme for realizing full-range soft-switching in all switches. Some practical considerations while implementing the proposed modulation scheme are discussed in Section III, followed by the design of converter prototype and experimental results in Section IV. Finally, concluding remarks are given in Section V.

II. Converter Analysis

A. Full-Bridge Operation

Fig. 1 shows the proposed reconfigurable dc–dc DAB converter capable of operating in both full-bridge and half-bridge modes. It consists of a tuned inductor(L_{rx})-capacitor(C_r)-inductor(L_{ry}) (abbreviated as LCL) resonant tank, and 10 switches S_1, S_2, S_{3a}, S_{3b}, S_{4a}, S_{4b}, and Q_1–Q_4, where S_{3a} and S_{4b} are kept constantly ON for full-bridge operation and the remaining switches are controlled to commutate at the switching frequency f_s with 50% duty cycle. Under this configuration, both primary and secondary bridges work as full bridges. By introducing an internal phase shift between the two legs of the primary H-bridge (i.e., between S_1 and S_{4a} and between S_2 and S_{3b}), a high-frequency three-level ($+V_{\rm DC1}$, 0, $-V_{\rm DC1}$) ac voltage $v_x(t)$ is generated. Similarly, a high-frequency three-level ($+nV_{\rm DC2}$, 0, $-nV_{\rm DC2}$) ac voltage $v_y(t)$ is generated by the secondary H-bridge, which lags $v_x(t)$ by a phase shift of ϕ.

Assuming that d_1 and d_2 are the duty cycles of $v_x(t)$ and $v_y(t)$, respectively, the voltages $v_x(t)$ and $v_y(t)$ are given by their Fourier series expansions as follows:

$$v_x(t) = \frac{4V_{\rm DC1}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \frac{1}{k} \sin(k\omega_s t) \sin\left(\frac{kd_1}{2}\right) \tag{1}$$

$$v_y(t) = \frac{4nV_{\rm DC2}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \frac{1}{k} \sin(k\omega_s t - k\phi) \sin\left(\frac{kd_2}{2}\right) \tag{2}$$

where n is the turns ratio of the transformer and $\omega_s = 2\pi f_s$. Assuming that higher order voltage and current harmonics are removed by the LCL network, only the fundamental components of $v_x(t)$ and $v_y(t)$ are considered in power analysis, which are given in the phasor form by the following equations, respectively:

$$\mathbf{V_x} = |\mathbf{V_x}| \angle 0 = \frac{4V_{\rm DC1}}{\pi} \sin\left(\frac{d_1\pi}{2}\right) \angle 0 \tag{3}$$

$$\mathbf{V_y} = |\mathbf{V_y}| \angle -\phi = \frac{4nV_{\rm DC2}}{\pi} \sin\left(\frac{d_2\pi}{2}\right) \angle -\phi. \tag{4}$$

Due to the immittance characteristic of the LCL network, under the tuned condition given by (5), $|\mathbf{I_x}|$ is proportional to $|\mathbf{V_y}|$ and $|\mathbf{I_y}|$ is proportional to $|\mathbf{V_x}|$, as shown by (6) and (7); thus, voltage sources $\mathbf{V_x}$ and $\mathbf{V_y}$ are transformed into current

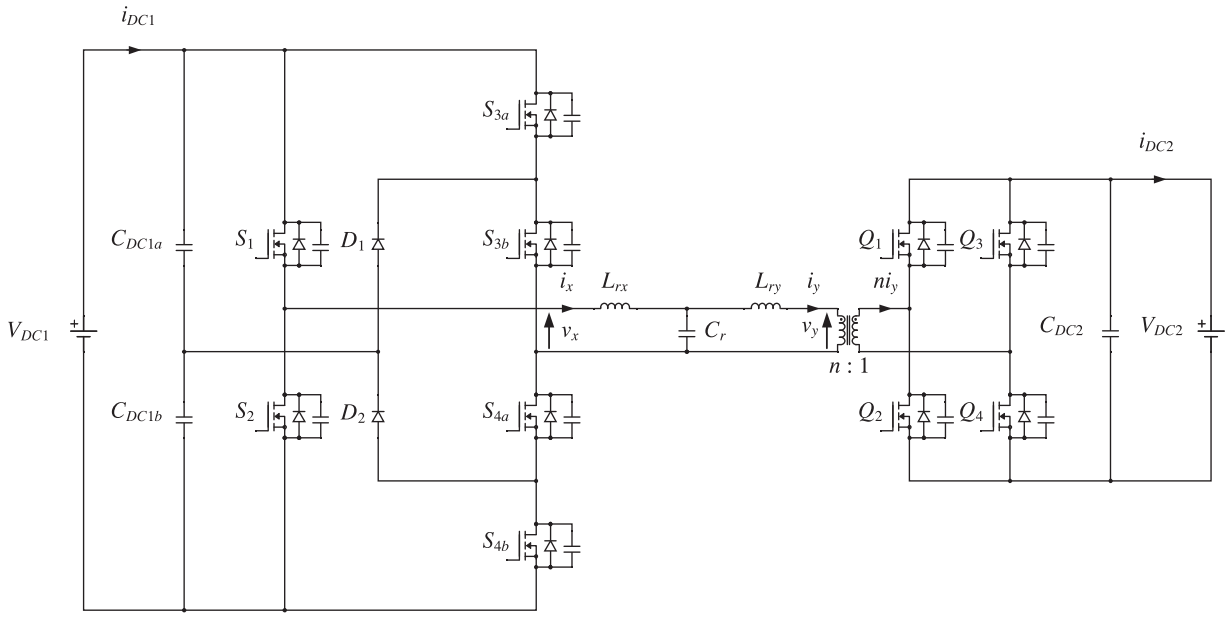

Fig. 1. Reconfigurable dc–dc DAB converter utilizing LCL immittance network.

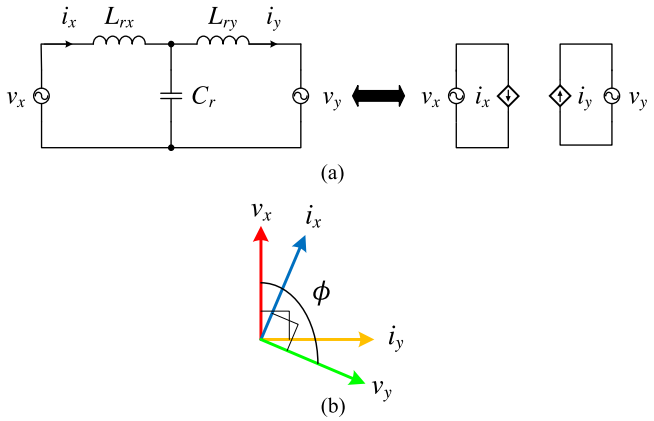

Fig. 2. (a) Simplified model of LCL network. (b) Voltage and current phasors of LCL network.

sources $\mathbf{I_y}$ and $\mathbf{I_x}$ via the tuned immittance network, and their relationships are depicted in Fig. 2

$$\omega_s = \frac{1}{\sqrt{L_{rx}C_r}} = \frac{1}{\sqrt{L_{ry}C_r}} = \frac{1}{\sqrt{L_rC_r}} \tag{5}$$

$$\mathbf{I_x} = \frac{|\mathbf{V_y}|}{\omega_s L_r}\angle\left(\frac{\pi}{2}-\phi\right) = \frac{4nV_{\mathrm{DC2}}}{\pi\omega_s L_r}\sin\left(\frac{d_2\pi}{2}\right)\angle\left(\frac{\pi}{2}-\phi\right) \tag{6}$$

$$\mathbf{I_y} = \frac{|\mathbf{V_x}|}{\omega_s L_r}\angle -\frac{\pi}{2} = \frac{4V_{\mathrm{DC1}}}{\pi\omega_s L_r}\sin\left(\frac{d_1\pi}{2}\right)\angle -\frac{\pi}{2}. \tag{7}$$

For a tuned LCL network, the fundamental components of $i_x(t)$ and $i_y(t)$ are given by the following equations in time domain:

$$i_x(t) = \frac{4nV_{\mathrm{DC2}}}{\pi\omega_s L_r}\sin\left(\frac{d_2\pi}{2}\right)\sin\left(\omega_s t+\frac{\pi}{2}-\phi\right) \tag{8}$$

$$i_y(t) = \frac{4V_{\mathrm{DC1}}}{\pi\omega_s L_r}\sin\left(\frac{d_1\pi}{2}\right)\sin\left(\omega_s t-\frac{\pi}{2}\right). \tag{9}$$

The theoretical conditions (without considering the effects of dead time) required for achieving soft-switching in all switches can be obtained by analyzing the signs of the inductor currents $i_x(t)$ and $i_y(t)$ at the switching instances of the switches. To achieve a more accurate prediction of the soft-switching conditions, the effects of including dead time in the gate drive signals of the switches are further analyzed in Section III and a corrective term is derived to compensate for the effects.

Fig. 3 shows the tank voltages $v_x(t)$ and $v_y(t)$, and currents $i_x(t)$ and $i_y(t)$ under three modulation schemes, namely, EPS, conventional DPS, and modified DPS proposed in this paper. The switching instances t_1–t_9 are derived and summarized in Table I to facilitate the derivation of soft-switching conditions. For simplicity and without the loss of generality, the initial time t_1 and the final time t_9 are set to 0 and T_s, respectively. For the primary-side switches S_1, S_2, S_{3b}, and S_{4a}, the achievement of soft-switching depends on the polarity of $i_x(t)$ at the switching instances t_1, t_4, t_5, and t_8. During the positive half-cycle of $v_x(t)$, S_1 and S_{3b} will turn on at zero voltage when $i_x(t_1)<0$ and $i_x(t_5)>0$, respectively. During the negative half cycle of $v_x(t)$, the roles of these switches are reciprocated. Therefore, S_2 and S_{4a} require $i_x(t_4)>0$ and $i_x(t_8)<0$, respectively, to turn ON at zero voltage. Similarly, for the secondary-side switches Q_1–Q_4, the achievement of soft-switching depends on the polarity of $ni_y(t)$ at the switching instances t_2, t_3, t_6, and t_7. Overall, the conditions for achieving soft-switching in the primary-side and secondary-side switches are given by (10) and (11), respectively. However, S_{3a} and S_{4b} are not commutating at the

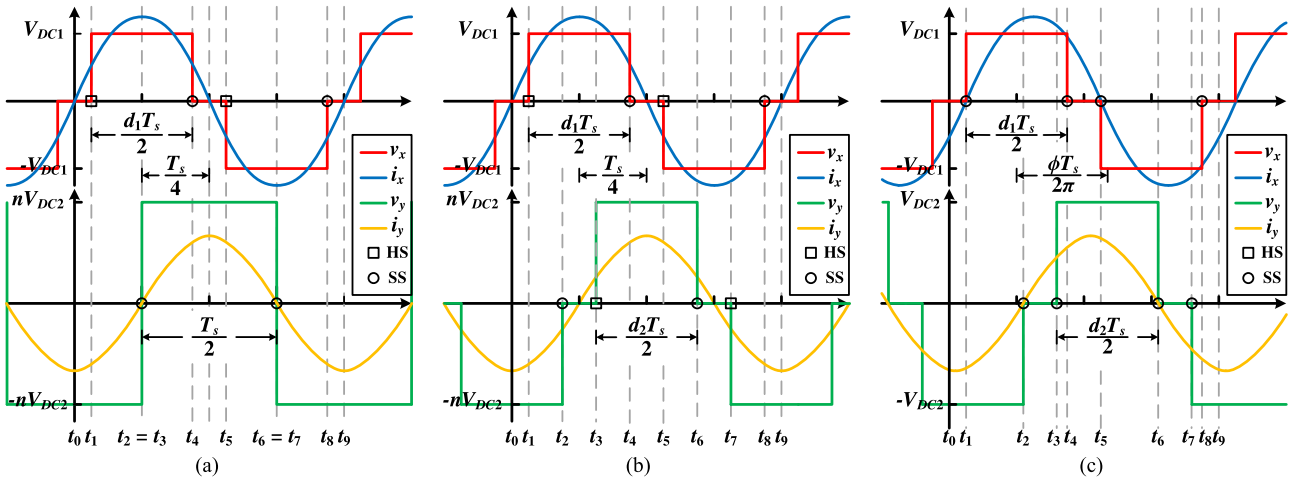

Fig. 3. Main waveforms of tank voltages and currents. (a) EPS modulation with fixed phase shift ($\phi = \pi/2$). (b) DPS modulation with fixed phase shift ($\phi = \pi/2$). (c) Enhanced DPS modulation with dynamically adjusted phase shift and primary bridge operating in full-bridge mode.

TABLE I
SWITCHING ACTIONS OF PRIMARY-SIDE AND SECONDARY-SIDE SWITCHES

Transition Time	Switching Actions
$t_0 = 0$	–
$t_1 = (1 - d_1)\frac{T_s}{4}$	S_2 turns off, S_1 turns on
$t_2 = \left(\frac{2d_2-1}{2} + \frac{\phi}{\pi}\right)\frac{T_s}{2}$	Q_3 turns off, Q_4 turns on
$t_3 = \left(\frac{1-d_2}{2} + \frac{\phi}{\pi}\right)\frac{T_s}{2}$	Q_2 turns off, Q_1 turns on
$t_4 = (1 + d_1)\frac{T_s}{4}$	S_{4a} turns off, S_{3b} turns on
$t_5 = (3 - d_1)\frac{T_s}{4}$	S_1 turns off, S_2 turns on
$t_6 = \left(\frac{1+d_2}{2} + \frac{\phi}{\pi}\right)\frac{T_s}{2}$	Q_4 turns off, Q_3 turns on
$t_7 = \left(\frac{3-d_2}{2} + \frac{\phi}{\pi}\right)\frac{T_s}{2}$	Q_1 turns off, Q_2 turns on
$t_8 = (3 + d_1)\frac{T_s}{4}$	S_{3b} turns off, S_{4a} turns on
$t_9 = T_s$	–

switching frequency but remain conducting during the entire switching cycle, which will not cause any switching loss

$$\phi \geq (2 - d_1)\frac{\pi}{2} \tag{10}$$

$$\phi \geq (2 - d_2)\frac{\pi}{2}. \tag{11}$$

Stemming from the immittance characteristics of the tuned LCL resonant tank, these conditions are independent of the input-to-output voltage ratio, which greatly simplifies the design and realization of soft-switching in the proposed DAB converter. It should be noted that the parts of the tank currents $i_x(t)$ and $i_y(t)$ contributing to circulating power increase with increasing phase shift ϕ for given d_1 and d_2. Therefore, ϕ should be limited to the minimum value required for achieving soft-switching in all switches, which occurs when d_1 and d_2 are set to be equal, i.e., $d_1 = d_2 = d$, and ϕ is modulated as a function of d according to (12). This new modulation scheme represents an improved version of the conventional DPS modulation due to its enhanced soft-switching characteristics; hence, it is termed as *enhanced DPS (EDPS) modulation*.

It can be seen from Fig. 3(c) that under EDPS modulation, the tank current $i_x(t)$ intersects with the tank voltage $v_x(t)$ at the switching instances t_1 and t_5 at zero current, leading to zero-current switching (ZCS) of S_1 and S_2. Over the entire switching cycle, it can be seen that no power is returned to the dc sources V_{DC1} and V_{DC2}; thus, zero circulating power is achieved by the proposed EDPS modulation scheme. A similar behavior is shown by the tank current $i_y(t)$, which intersects with the tank voltage $v_y(t)$ at the switching instances t_2 and t_6 leading to ZCS of Q_4 and Q_3

$$\phi = (2 - d)\frac{\pi}{2}. \tag{12}$$

Based on this modulation strategy, the DAB converter transfers the maximum power when $d = 1$ and $\phi = \pi/2$, and transfers no power when $d = 0$ and $\phi = \pi$. By substituting (12) into (6), the active power P transferred from V_{DC1} to V_{DC2} in full-bridge mode can be derived by evaluating the real part of $1/2\mathbf{V_x}\mathbf{I_x^*}$ or $1/2\mathbf{V_y}\mathbf{I_y^*}$ as follows:

$$\begin{aligned} P &= \frac{1}{2}\mathrm{Re}\left[\mathbf{V_x}\mathbf{I_x^*}\right] = \frac{1}{2}\mathrm{Re}\left[\mathbf{V_y}\mathbf{I_y^*}\right] \\ &= \frac{8nV_{\mathrm{DC1}}V_{\mathrm{DC2}}}{\pi^2\omega_s L_r}\sin^3\left(\frac{\pi d}{2}\right) \\ &= P_M \sin^3\left(\frac{\pi d}{2}\right). \end{aligned} \tag{13}$$

B. Half-Bridge Operation

When the DAB converter operates in half-bridge mode as shown in Fig. 4, S_{3a} and S_{4b} are turned OFF to disconnect the bridge leg from V_{DC1}. To generate a three-level ac voltage $v_x(t)$ having half amplitude, i.e., $(+V_{\mathrm{DC1}}/2,\ 0,\ -V_{\mathrm{DC1}}/2)$, the mid-point of the capacitor leg formed by $C_{\mathrm{DC1}a}$ and $C_{\mathrm{DC1}b}$ is connected via clamping diodes D_1 and D_2 to S_{3b} and S_{4a}. During the positive half cycle of $v_x(t)$ (i.e., $t = t_1$–t_4), S_1 and S_{4a} are

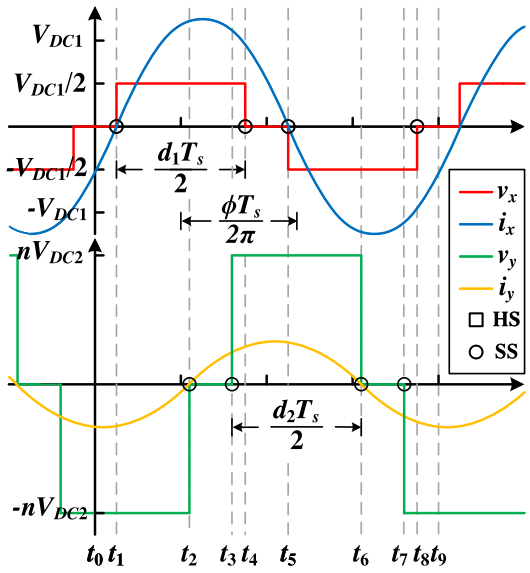

Fig. 4. Main waveforms of tank voltages and currents under EDPS modulation with DAB converter operating in half-bridge mode.

turned ON, which gives $v_x(t) = +V_{\mathrm{DC1}}/2$, during which $C_{\mathrm{DC1}a}$ and $C_{\mathrm{DC1}b}$ are discharged and charged by $i_x(t)/2$, respectively. At $t = t_4$, S_{4a} is turned OFF and S_{3b} is turned ON and the positive $i_x(t)$ flows through S_{3b} and the body diode of S_{3a}, while S_1 remains ON, resulting in a zero voltage level $v_x(t) = 0$.

S_2 changes to ON-state at $t = t_5$, which initiates the negative half cycle of $v_x(t)$ (i.e., $t = t_5 - t_8$). During this period, S_2 and S_{3b} are turned ON, which gives $v_x(t) = -V_{\mathrm{DC1}}/2$, and $C_{\mathrm{DC1}a}$ and $C_{\mathrm{DC1}b}$ are charged and discharged by $i_x(t)/2$, respectively. This state continues until S_{3b} is turned OFF and S_{4a} is turned ON at $t = t_8$, and the negative $i_x(t)$ circulates between S_2, S_{4a}, and the body diode of S_{4b}, resulting in a zero voltage level $v_x(t) = 0$. As only the primary bridge will undergo reconfiguration from full-bridge to half-bridge structure, the operation of the secondary H-bridge remains unchanged. By introducing an internal phase shift between two bridge legs, a three-level ac voltage $v_y(t)$ ($+V_{\mathrm{DC2}}$, 0, $-V_{\mathrm{DC2}}$) is generated and controlled to lag $v_x(t)$ by a phase shift of ϕ. As the soft-switching condition given by (11) is independent of the input-to-output voltage ratio $nV_{\mathrm{DC2}}/V_{\mathrm{DC1}}$, the halving of the amplitude of $v_x(t)$ does not affect the soft-switching characteristics of the reconfigured DAB converter operating in half-bridge mode.

Since the amplitude of $v_x(t)$ is reduced by 50%, it follows that the DAB converter operating in half-bridge mode can transfer at the maximum 50% of the maximum power transferable while operating in full-bridge mode. Thus, the active power transferred in this mode is given by

$$P = \frac{1}{2} P_M \sin^3\left(\frac{\pi d}{2}\right). \tag{14}$$

C. Comparison Between Full-Bridge and Half-Bridge Operations and Other Modulation Schemes

For $P \le P_M/2$, although both full-bridge and half-bridge modes can be used to output the same power, they will give rise

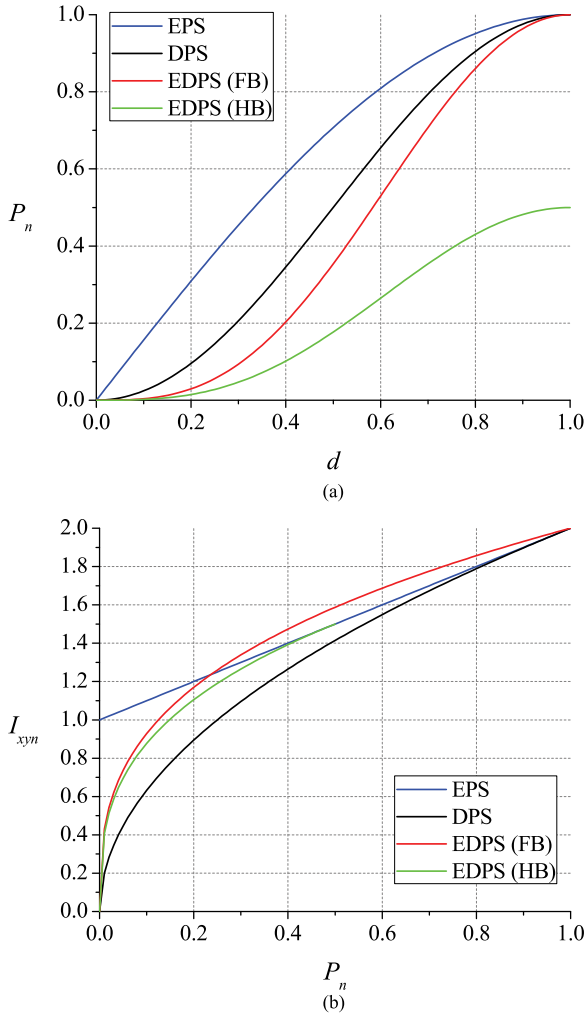

Fig. 5. (a) Normalized output power P_n versus duty cycle d. (b) Effective tank current I_{xyn} versus normalized output power P_n.

to different operating values of duty cycle d and phase shift ϕ. Assuming that d_{FB} and d_{HB} are the duty cycles required to output a given power under full-bridge and half-bridge modes, respectively, it can be verified from (15) that $d_{\mathrm{FB}} < d_{\mathrm{HB}}$, and from (12), this implies that $\phi_{\mathrm{FB}} > \phi_{\mathrm{HB}}$ and a higher circulating current will be generated when a DAB converter operates in full-bridge mode in this output power range. Therefore, for $0 < P \le P_M/2$, half-bridge operation is preferred as it leads to lower circulating current and conduction loss.

This clearly highlights the advantage of the proposed DAB converter, which is designed to be *reconfigurable* between half-bridge and full-bridge structures to maintain a high efficiency in both low-power and high-power operations. In summary, the proposed DAB converter will operate in half-bridge mode for $0 < P \le P_M/2$, and switches to full-bridge mode for $P_M/2 < P \le P_M$.

$$\sin\left(\frac{\pi d_{\mathrm{FB}}}{2}\right) = \frac{1}{\sqrt[3]{2}} \sin\left(\frac{\pi d_{\mathrm{HB}}}{2}\right) \tag{15}$$

To benchmark the performance of the proposed EDPS modulation scheme, comparisons are made with two other conven-

TABLE II
COMPARISON OF THREE MODULATION SCHEMES

Modulation Scheme	EPS	DPS	EDPS
Normalized output power	$P_n = \sin\left(\frac{\pi d}{2}\right)$	$P_n = \sin^2\left(\frac{\pi d}{2}\right)$	$P_n = \sin^3\left(\frac{\pi d}{2}\right)$ (FB) $P_n = \frac{1}{2}\sin^3\left(\frac{\pi d}{2}\right)$ (HB)
Normalized rms tank currents	$I_{xn} = 1$ $I_{yn} = P_n$	$I_{xn} = \sqrt{P_n}$ $I_{yn} = \sqrt{P_n}$	$I_{xn} = \sqrt[3]{P_n}$(FB) $I_{yn} = \sqrt[3]{P_n}$(FB) $I_{xn} = \sqrt[3]{2P_n}$(HB) $I_{yn} = \frac{\sqrt[3]{2P_n}}{2}$(HB)
Control parameters (forward power flow)	$d_1 = d$, $d_2 = 1$, $\phi = \frac{\pi}{2}$	$d_1 = d_2 = d$, $\phi = \frac{\pi}{2}$	$d_1 = d_2 = d$, $\phi = (2-d)\frac{\pi}{2}$
Control parameters (reverse power flow)	$d_1 = d$, $d_2 = 1$, $\phi = -\frac{\pi}{2}$	$d_1 = d_2 = d$, $\phi = -\frac{\pi}{2}$	$d_1 = d_2 = d$, $\phi = -(2-d)\frac{\pi}{2}$
Number of switches undergoing soft-switching	6	4	8
Number of switches undergoing hard-switching	2	4	0

tional modulation schemes, namely, EPS and DPS, in terms of soft-switching characteristic and the magnitude of rms tank current. As discussed in Section II-A, when applied to LCL immittance tank, the conventional EPS and DPS modulation schemes utilize a fixed external phase shift of $\phi = \pm\pi/2$ and variable duty cycle(s) for power control, whereas the proposed modulation scheme varies with both internal and external phase shifts according to (12) to achieve soft-switching in all switches. Compared with EDPS modulation, only the sixth and fourth switches are soft-switched under EPS and DPS modulation schemes, which implies that a lower switching loss can be achieved with EDPS modulation scheme, particularly under high switching frequency as will be experimentally verified later in Section IV.

Fig. 5(a) shows the normalized output power $P_n = P/P_M$ achieved with different modulation schemes as a function of the duty cycle d of $v_x(t)$ [and $v_y(t)$ for DPS and EDPS]. It can be shown that the output power of DAB converter with LCL immittance tank varies with $\sin(\pi d/2)$, $\sin^2(\pi d/2)$, and $\sin^3(\pi d/2)$ under EPS, DPS, and EDPS modulations, respectively. Hence, the problem of having to generate small duty cycles at low output power can be avoided by the EDPS modulation scheme. For example, when operating at 10% of the maximum output power, a duty cycle of $d = 0.0638$ is required for EPS modulation, whereas the same power can be achieved with a much larger duty cycle of $d = 0.3073$ for EDPS modulation in full-bridge mode and $d = 0.3977$ in half-bridge mode. As a result, the range of duty-cycle variation can be significantly reduced under EDPS modulation. In addition, as the harmonics in the LCL tank voltages and currents will increase with decreasing duty cycle, EDPS modulation will give rise to less distortion of the tank voltages and currents and thus more accurate prediction of the output power and soft-switching conditions derived based on fundamental component analysis.

The rms tank currents I_x and I_y can be obtained from (8) and (9) by dividing the peak values of $i_x(t)$ and $i_y(t)$ by $\sqrt{2}$. By further normalizing I_x and I_y using the base values defined by (16) and (17), normalized tank currents I_{xn} and I_{yn} are obtained, which are functions of duty cycle, and hence of normalized output power P_n, only, as given in Table II. To facilitate comparison between different modulation schemes, it is necessary to define an effective tank current that will reflect the total contribution of the tank currents to conduction loss. Here, an effective tank current I_{xyn} is defined by (18) as the summation of I_{xn} and I_{yn}. Fig. 5(b) plots the effective tank current I_{xyn} as a function of the normalized output power P_n under different modulation schemes

$$I_{x(\text{base})} = \frac{4nV_{DC2}}{\sqrt{2}\pi\omega_s L_r} \Rightarrow I_{xn} = \sin\left(\frac{d_2\pi}{2}\right) \tag{16}$$

$$I_{y(\text{base})} = \frac{4V_{DC1}}{\sqrt{2}\pi\omega_s L_r} \Rightarrow I_{yn} = \sin\left(\frac{d_1\pi}{2}\right) \tag{17}$$

$$I_{xyn} = I_{xn} + I_{yn}. \tag{18}$$

It can be seen from Fig. 5(b) that DPS modulation results in the lowest effective tank current over the entire range of output power. Under EPS modulation, one of the tank currents I_{xn} remains consistently high (i.e., $d_2 = 1$) while I_{yn} is modulated for power control. The consequence is a higher effective tank current, and hence a higher conduction loss, incurred by EPS modulation under light-load condition. As output power increases, the effective tank current under EPS modulation approaches that of DPS modulation. In comparison with both EPS and DPS modulations, full-range soft-switching is achieved un-

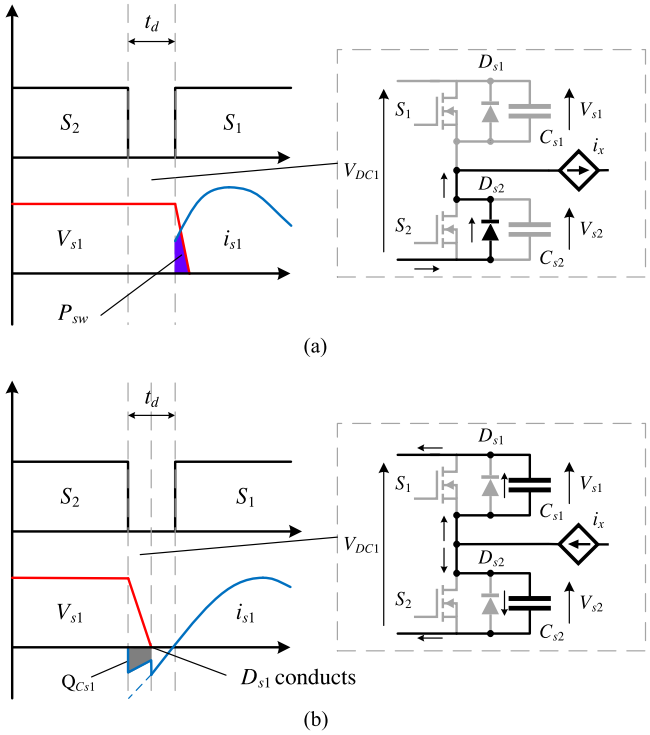

Fig. 6. (a) Hard-switching. (b) Soft-switching.

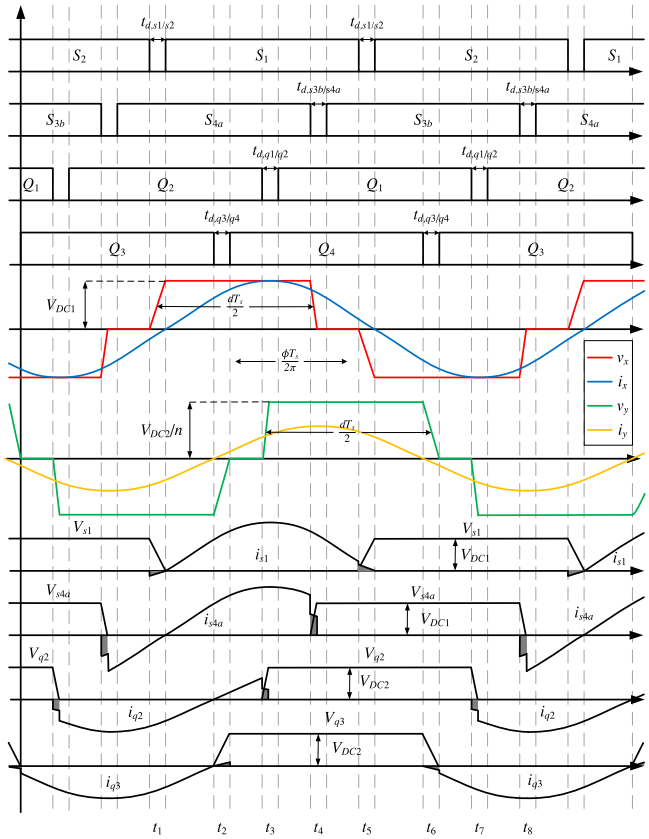

Fig. 7. Operating waveforms of gate drive signals, tank voltages/currents, and transistor voltages/currents including the effect of dead time.

der EDPS modulation at the expense of increased circulating current, and hence a higher effective tank current.

For output power below $P_M/2$, this drawback can be compensated by operating the DAB converter in half-bridge mode, which, as discussed previously, features a lower circulating current while ensuring soft-switching of all switches. As can be seen from Fig. 5(b), the effective tank current under EDPS modulation in half-bridge mode is constantly lower than that under EPS modulation. This justifies the advantage of reconfiguring the DAB converter from full-bridge mode to half-bridge mode for output power below $P_M/2$. For output power above $P_M/2$, it will be verified experimentally that the higher circulating current incurred by EDPS modulation in full-bridge mode does not necessarily lead to a lower converter's efficiency compared with DPS modulation due to the more severe switching loss encountered in the latter case.

III. Practical Considerations on the Selection of Dead Time and Additional External Phase Shift

Fig. 6 depicts the two possible switching scenarios in a bridge leg. To achieve soft-switching, the drain-source capacitance of the switch being turned OFF (i.e., the "outgoing" switch S_2) should be charged to the dc bus voltage V_{DC1}, while that of the other switch (i.e., the "incoming" switch S_1) should be discharged fully within the dead time t_d, which is defined as the time between the turn-OFFgate signal of S_2 and the turn-ON gate signal of S_1. If S_1 is turned ON before its drain-source voltage V_{s1} decreases to zero, hard-switching occurs that leads to switching loss P_{sw} and lowers the converter's efficiency.

To avoid hard-switching, a sufficiently negative tank current $i_x(t)$ must be available to charge C_{s2} and to discharge C_{s1} during the dead time. This can be realized by adding an extra phase lag $\Delta\phi$ to the theoretical value calculated from (12). As depicted in Fig. 6(b), setting $\Delta\phi = (t_d/2)\,2\pi/T_s$, where T_s is the switching frequency, will cause the zero crossing of the tank current $i_x(t)$ to occur at the turn-ON instance of S_1 so that $i_x(t)$ will remain negative during the dead time. If C_{s1} is discharged fully before the end of the dead time, as shown in the same figure, the body diode of S_1 (i.e., D_{s1}) will begin to conduct and the negative tank current $i_x(t)$ will flow in the bridge leg in the form of circulating current, leading to conduction loss. Therefore, setting the dead time to be unnecessarily long is not recommended. Ideally, S_1 should be turned ON as soon as C_{s1} is discharged fully, i.e., as soon as V_{s1} decreases to zero. As the discharge time of C_{s1} is a function of the tank current's magnitude during the dead time interval, the minimum dead time $t_{d(\min)}$ is defined as the time required for C_{s1} to discharge fully at the minimum load.

The switching transition described above occurs at $t = t_1$ in Fig. 7. Assume that S_1 and S_2 are identical and have the same drain-source capacitance, i.e., $C_{s1} = C_{s2}$, the following inequality must be satisfied to achieve zero-voltage turn-ON of S_1 [32]–[33]:

$$2C_{s1}\left(V_{\mathrm{DC1}}\right)V_{\mathrm{DC1}} \le \int_{t_1-t_d/2}^{t_1+t_d/2} |i_x(t)|\,\mathrm{d}t. \qquad (19)$$

TABLE III
SPECIFICATIONS OF CONVERTER PROTOTYPE

Parameter	Symbol	Design Value	Experimental Value
Primary voltage	V_{DC1}	400 V	
Secondary voltage	V_{DC2}	200 V	
Switching frequency	f_s	80 kHz	
Turns ratio	n	2	1.997
Maximum output power	P_M	1.6 kW	1.57 kW
Resonant capacitance	C_r	24.54 nF	24.40 nF
Resonant inductance	L_{rx}	161.3 μH	166.5 μH
	L_{ry}		167.0 μH
Switches	S_1-S_{4b}	UJC06505K	
	Q_1-Q_4		

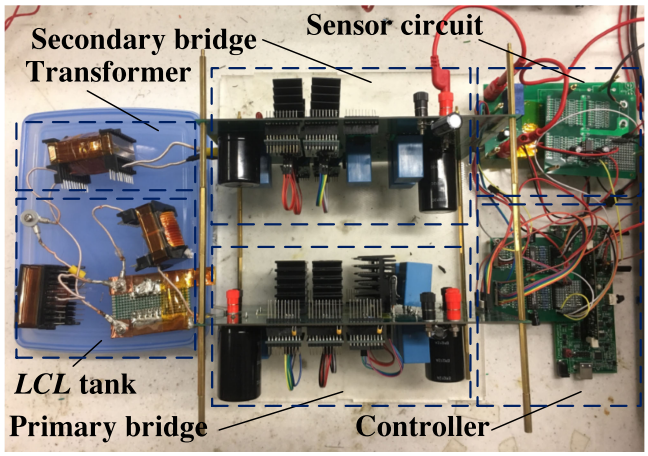

Fig. 8. Prototype of the proposed DAB converter.

By using (8) and (16), the integral term in (19), and hence the required minimum dead time $t_{d(\min)}$, can be derived as

$$\int_{t_1-t_d/2}^{t_1+t_d/2} |i_x(t)|\,\mathrm{d}t = \frac{\sqrt{2}I_{xn}I_{x(\text{base})}}{\omega_s}\left[1-\cos\left(\frac{2\pi t_d}{T_s}\right)\right] \tag{20}$$

$$t_{d(\min)} = \frac{T_s}{2\pi}\cos^{-1}\left[1-\frac{\sqrt{2}\omega_s C_{s1}\left(V_{\text{DC1}}\right)V_{\text{DC1}}}{I_{xn}I_{x(\text{base})}}\right]. \tag{21}$$

Equation (21) can be used to determine the minimum dead time required for ensuring soft-switching in S_1 (at $t = t_1$), S_2 (at $t = t_5$), Q_4 (at $t = t_2$), and Q_3 (at $t = t_6$). For other switching transitions at $t = t_3, t_4, t_7$, and t_8, the tank current has a significantly larger magnitude and will require a time less than $t_{d(\min)}$ to charge fully and discharge the drain-source capacitance of the outgoing and incoming switches, respectively. Thus, it is assumed that soft-switching is always achieved for these cases.

IV. DESIGN OF CONVERTER PROTOTYPE AND EXPERIMENTAL RESULTS

In this section, a converter prototype is designed with the specifications listed in Table III and as shown in Fig. 8. The components of the LCL tank are designed based on the maximum output power $P_M = 1.6$ kW.

Resonant inductance L_r is given as follows:

$$L_r = \frac{8nV_{\text{DC1}}V_{\text{DC2}}}{\pi^2\omega_s P_M} = 161.3\,\mu\text{H}.$$

Resonant capacitance C_r is given as follows:

$$C_r = \frac{1}{\omega_s^2 L_r} = 24.54\text{ nF}.$$

SiC MOSFETs UJC06505K are used in both primary and secondary bridges, which have a drain-source capacitance of $C_{s1} = 80$ pF at 400 V. In full-bridge mode, the minimum load power is 800 W (i.e., 50% load), which gives $I_{x(\text{base})} = 4.44$ and $I_{xn} = \sqrt[3]{0.5} = 0.794$. Using (21), the required minimum dead time is $t_{d(\min)} = 226$ ns. In half-bridge mode, the minimum load power is fixed at 80 W (i.e., 5% load) below which the required minimum dead time will be unrealistically long. At 80 W, $I_{x(\text{base})} = 4.44$ and $I_{xn} = \sqrt[3]{2 \times 0.05} = 0.464$, which gives $t_{d(\min)} = 296$ ns. Based on the calculated $t_{d(\min)}$, an extra phase lag of $\Delta\phi = t_{d(\min)} \times 2\pi/T_s$ is added to the theoretical phase shift calculated from (12).

The designed DAB converter with the specifications above is simulated in PSIM. The simulated tank voltage and current waveforms corresponding to three modulations schemes, i.e., EPS, DPS, and EDPS, are shown in Fig. 9(a)–(c) for 70% load condition. For comparison, the corresponding experimental waveforms are shown in Fig. 10(a)–(c). Figs. 9(a) and 10(a) show the case of EPS modulation with $d_1 = 0.494$, $d_2 = 1$, and $\phi = 90°$, with which the tank voltage and current at each port are in phase with each other, i.e., $v_x(t)$ in phase with $i_x(t)$ and $v_y(t)$ in phase with $i_y(t)$. Figs. 9(b) and 10(b) show the case of DPS modulation with $d_1 = d_2 = 0.631$ and $\phi = 90°$, and the voltage and current at the respective end of the LCL tank are in phase with each other as in the case of EPS modulation. Figs. 9(c) and 10(c) show the case of EDPS modulation operating in full-bridge mode with $d_1 = d_2 = 0.696$ and $\phi = 2.048$, which causes $v_x(t)$ to lead $v_y(t)$ by 117.4°, and $i_x(t)$ and $v_y(t)$ to lag $v_x(t)$ and $i_y(t)$, respectively, by 27.4°. In all cases, the simulated waveforms agree closely with the measured waveforms.

To illustrate the case of the DAB converter working in half-bridge mode, the measured tank voltage and current waveforms corresponding to half-bridge operation at 40% load condition were captured and shown in Fig. 11(a). In comparison with the operation in full-bridge mode [cf. Fig. 11(b)], it can be clearly seen that the duty cycles of the tank voltages increase in half-bridge mode, which translates to a lower circulating current and lower distortion of the tank currents, as explained previously in Section II-C. This highlights the advantage of switching to half-bridge configuration under light-load condition. For example, in full-bridge mode, $d_1 = d_2 = 0.527$, and $v_x(t)$ leads $v_y(t)$ by 132.5°, which causes $i_x(t)$ and $v_y(t)$ to lag $v_x(t)$ and $i_y(t)$, respectively, by 42.5°. When the same output power is delivered by the converter operating in half-bridge mode, the duty cycles of the tank voltages increase to $d_1 = d_2 = 0.757$, and the phase shift between $v_x(t)$ and $v_y(t)$ decreases to 111.8°. Under this condition, the phase difference between $i_x(t)$ and $v_x(t)$ and that between $i_y(t)$ and $v_y(t)$ both decrease to 21.8°. Therefore, for a

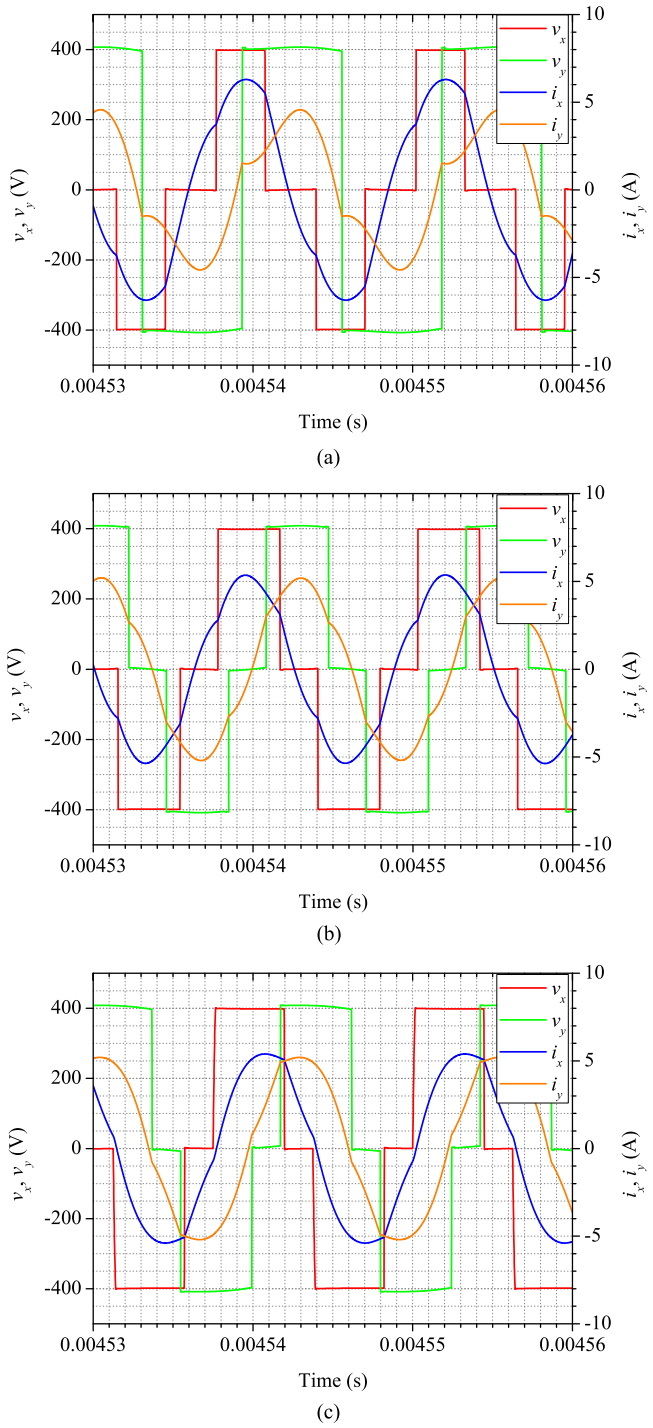

Fig. 9. Simulated tank voltage and currents at 70% forward power transfer. (a) EPS modulation with $\phi = 90°$. (b) DPS modulation with $\phi = 90°$. (c) Enhanced DPS modulation with $\phi = 117.4°$ and primary bridge operating in full-bridge mode.

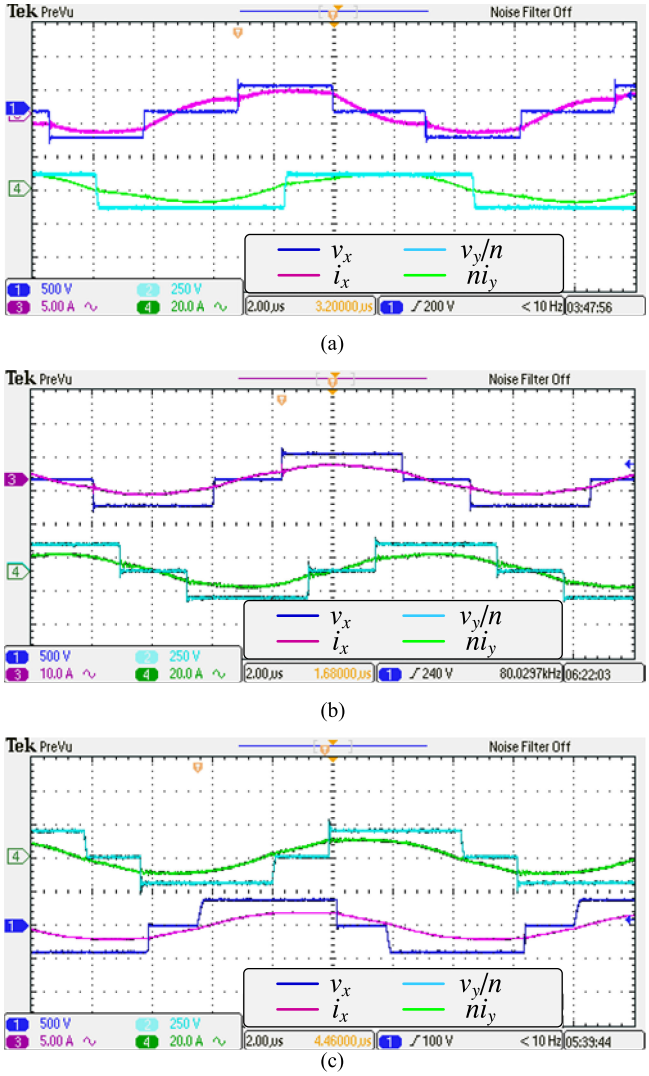

Fig. 10. Measured tank voltage/current and primary-reflected tank voltage/current at 70% forward power transfer. (a) EPS modulation with $\phi = 90°$. (b) DPS modulation with $\phi = 90°$. (c) Enhanced DPS modulation with $\phi = 117.4°$ and primary bridge operating in full-bridge mode.

given output power under light-load condition, half-bridge operation is expected to perform better than full-bridge operation by resulting in a lower rms tank current and conduction loss, which is advantageous to the enhancement of light-load efficiency.

It is interesting to note from Fig. 11(a) that in half-bridge mode the converter exhibits "overshoot" at the rising edges of the tank voltage $v_x(t)$. This phenomenon can be explained as follows. During the positive half cycle shortly before S_1 is turned ON, a negative tank current $i_x(t) < 0$ flows through S_{4a} and the body diodes of S_1 and S_{4b}, clamping $v_x(t)$ at the dc input voltage V_{DC1}. After S_1 is turned ON, a positive tank current $i_x(t) > 0$ initially flows through S_1, S_{4a}, and the body diode of S_{4b} until it has fully recovered its reverse-blocking state and forces the tank current to flow through D_2 to $C_{\mathrm{DC1}b}$, which reduces $v_x(t)$ to $V_{\mathrm{DC1}}/2$. For the negative half cycle, a similar process occurs due to the finite reverse-recovery time of the body diode of S_{3a}.

Fig. 12 shows the measured waveforms at the switching instances of S_1, S_{4a}, Q_1, and Q_4 under different modulation schemes. Since S_2, S_{3b}, Q_2, and Q_4 are complementary to S_1, S_{4a}, Q_1, and Q_4, their waveforms are not shown here. Fig. 12(a) shows that both S_1 and S_2 undergo hard-switching under EPS modulation as these switches are turned ON when their drain-source voltages are still high. Under DPS modulation, the

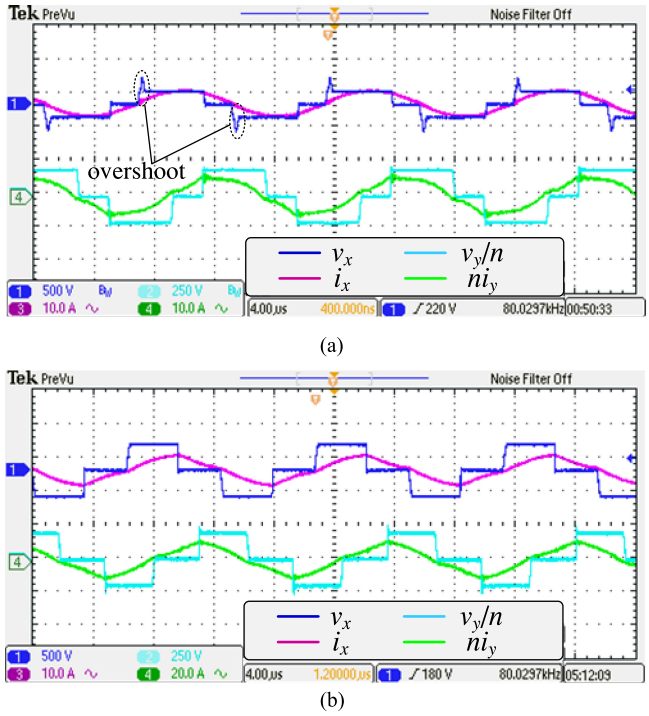

Fig. 11. Measured tank voltage/current and primary-reflected tank voltage/current at 40% forward power transfer. (a) Enhanced DPS modulation with $\phi = 111.8^\circ$ and primary bridge operating in half-bridge mode. (b) Enhanced DPS modulation with $\phi = 132.5^\circ$ and primary bridge operating in full-bridge mode.

number of switches that undergo hard-switching has increased to four (S_1, S_2, Q_3, Q_4) as both primary and secondary bridges are modulated. In contrast, soft-switching is achieved in all switches under EDPS modulation in both full-bridge and half-bridge modes as shown in Fig. 12(c) and (d). This is achieved with the aid of a tuned LCL tank, which naturally aligns the zero crossings of $i_x(t)$ and $i_y(t)$ with the rising edges of $v_x(t)$ and falling edges of $v_y(t)$, respectively, when a phase difference of $\phi = (2-d)\pi/2$ is introduced between $v_x(t)$ and $v_y(t)$. As the alignment is independent of the input-to-output voltage ratio, the realization of soft-switching is greatly simplified.

Fig. 13(a)–(b) depict the closed-loop design of the reconfigurable DAB converter and the flowchart for selection of operation mode. In our experimental setup, the DAB converter is used to interface two dc voltage sources V_{DC1} and V_{DC2}, hence the control objective is to regulate the secondary-side dc current i_{DC2} at a given reference value I_{ref}. As the duty cycle of the bridge voltages is represented by the compensator's output, it is used to determine the operation mode of the converter. When $d_{\text{ref}} > 2/\pi \sin^{-1}\left(1/\sqrt[3]{2}\right)$, which corresponds to $P_M/2 < P \leq P_M$, the DAB converter will operate in full-bridge mode and $d_{\text{FB}} = d_{\text{ref}}$ will be used directly to control the converter. Otherwise, the DAB converter will operate in half-bridge mode with $d_{\text{HB}} = 2/\pi \sin^{-1}\left[\sqrt[3]{2}\sin\left(\pi d_{\text{ref}}/2\right)\right]$, which corresponds to $0 < P \leq P_M/2$. Experimental results depicting the transient response of a closed-loop reconfigurable DAB converter under step load changes from 2.5 to 5.5 A and from 5.5 A back to 2.5 A are shown in Fig. 14(a)–(b), while the transition

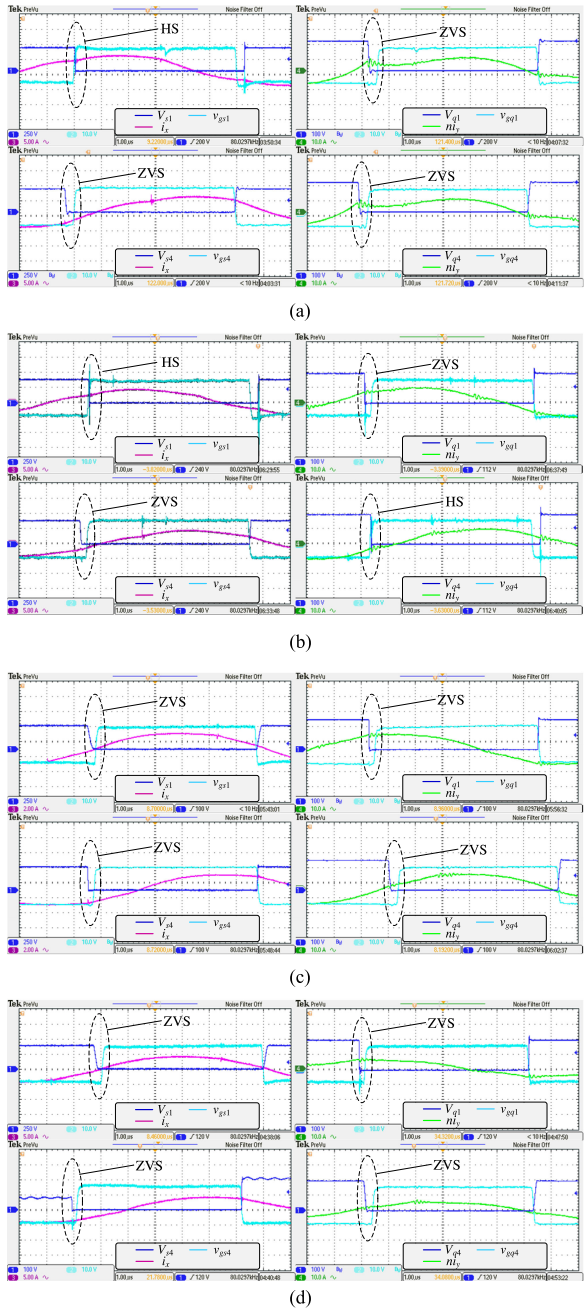

Fig. 12. Measured gate drive signals and drain-source voltages of S_1, S_{4a}, Q_1, and Q_4, tank current $i_x(t)$, and primary-reflected tank current $ni_y(t)$. (a) EPS modulation. (b) DPS modulation. (c) EDPS modulation in full-bridge mode. (d) EDPS modulation in half-bridge mode. Cases (a)–(c) correspond to 70% forward power transfer and case (d) corresponds to 35% forward power transfer.

from half-bridge to full-bridge operation modes is shown in Fig. 14(c), which shows that the transition completes stably in about four switching cycles.

Fig. 15 plots the efficiency of the DAB converter as a function of output power under different modulation schemes, i.e., EDPS modulation with two additional MOSFETs, DPS, and EPS modulations without two additional MOSFETs. It can be seen that despite the higher circulating current incurred by the proposed EDPS modulation scheme, it results in a higher efficiency than

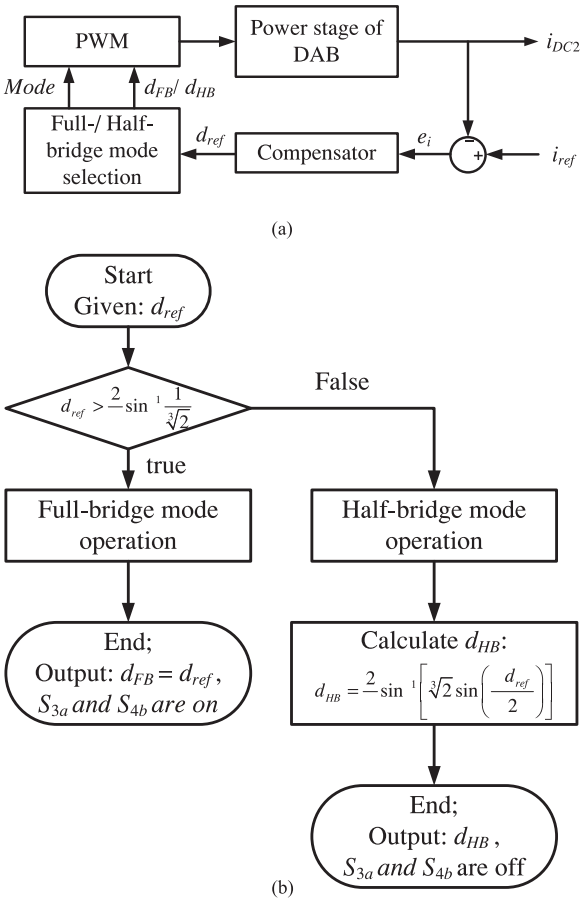

Fig. 13. (a) Closed-form implementation of the proposed EDPS modulation scheme. (b) Flowchart for selection of operation mode and calculation of effective duty cycle.

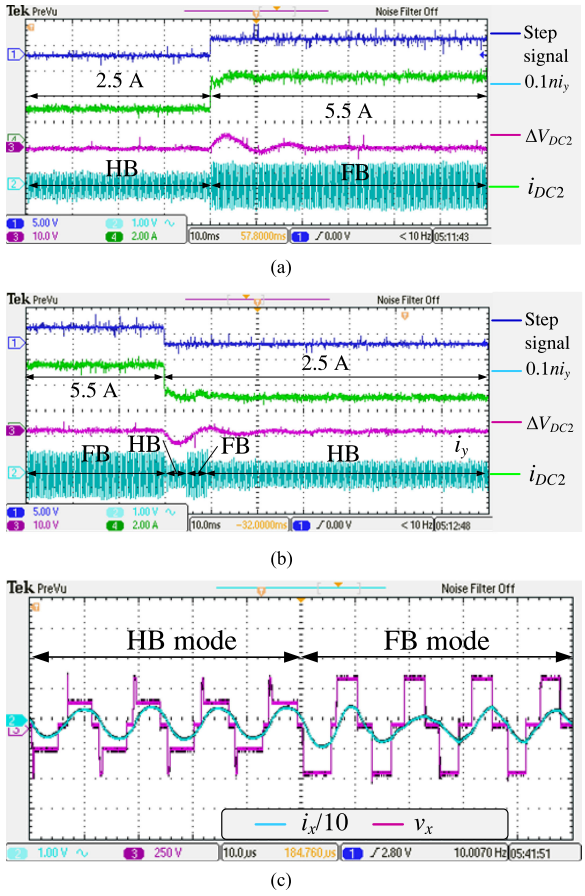

Fig. 14. Closed-loop transient response of the reconfigurable DAB converter implemented with EDPS modulation scheme. (a) Under step load changes from 2.5 to 5.5 A. (b) From 5.5 A to 2.5 A. (c) Transition from half-bridge to full-bridge operation.

both EPS and DPS modulation over a wide range of output power due to its soft-switching characteristic. For EPS modulation, the converter's efficiency decreases rapidly with decreasing output power as the secondary bridge is unmodulated and the tank current $i_x(t)$ remains constant at its maximum value.

Despite producing the lowest tank current among the three modulation schemes [cf. Fig. 5(b)], DPS modulation suffers from high switching loss at high output power due to hard-switching; hence, the overall result is a lower efficiency compared to that of EDPS modulation. As output power decreases, the difference between DPS and EDPS diminishes as EDPS modulation suffers from increased circulating current (due to operation at larger phase shift) while under DPS modulation the magnitude of switching loss decreases at low output power (as MOSFETs will switch at lower current), causing the converter's efficiency under both modulation schemes to close to each other at low output power.

To enhance light-load efficiency, it is proposed that the DAB converter should operate in half-bridge mode for reducing circulating current and conduction loss. This is verified by the measured converter's efficiency in Fig. 15, which shows that EDPS modulation in half-bridge mode produces the highest efficiency for output power below 800 W or $P_M/2$. Therefore, by switching the DAB converter between two structures,

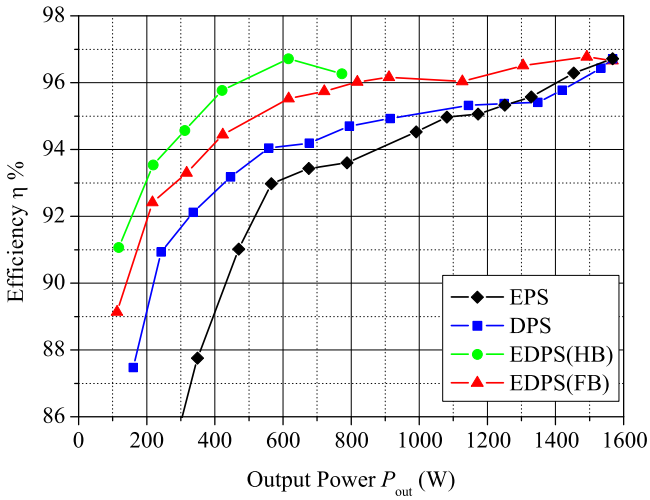

Fig. 15. Measured converter's efficiency under three modulation schemes.

i.e., half-bridge mode for $P \leq P_M/2$ and full-bridge mode for $P_M/2 < P \leq P_M$, it will ensure that the converter constantly operates with the maximum efficiency, or follows the "envelope" of maximum efficiency, over the entire output power range.

V. Conclusion

In conclusion, a DAB converter with reconfigurable structure and modulation method to achieve full-range soft-switching are proposed in this paper. By switching from full-bridge to half-bridge configuration under light-load condition, the DAB converter will operate with reduced circulating current, lower conduction loss, and hence higher efficiency. The paper is a demonstration of the advantage of introducing reconfigurability into DAB converter as a means to enhance its efficiency over a wide range of load conditions, and a similar concept can be extended to other types of converters. The small deviations of the tank currents i_x and i_y from pure sinusoidal ones due to the presence of higher order harmonics are found to have influences on the accuracy of the prediction of soft-switching conditions. These issues will be subjects for future research. The use of higher order resonant tanks for reducing the effects of higher order harmonics [34] or including these harmonics in the computation of soft-switching conditions are some possible solutions that are worth exploring.

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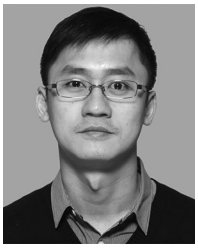
Yiu Pang Chan (S'17) received the B.Sc.(Hons.) degree in engineering physics in 2015 from The Hong Kong Polytechnic University, Hong Kong, where he is currently working toward the Ph.D. degree in the area of power electronics.

His research interests include high-frequency bidirectional isolated dc/dc and ac/dc converters.



K. H. Loo (S'97–M'99) received the B.Eng.(Hons.) and Ph.D. degrees from the University of Sheffield, Sheffield, U.K., in 1999 and 2002, respectively, both in electronics engineering.

From 2002 to 2004, he was a Postdoctoral Fellow with the Japan Society for the Promotion of Science, Ehime University, Matsuyama, Japan. In 2006, he started working as an Instructor with the Faculty of Engineering, Hong Kong Polytechnic University, Hong Kong as an Instructor, where he is currently an Associate Professor with the Department of Electronic and Information Engineering. His research interest focuses on power electronics for renewable energy systems.

Dr. Loo is an Associate Editor for the IEEE TRANSACTIONS ON ENERGY CONVERSION since 2013.

Muhammad Yaqoob (S'16) received the B.Eng. degree in electronics engineering from the National University of Sciences and Technology, Islamabad, Pakistan, in 2012, and the M.Sc. degree in electric power system and its automation from the North China Electric Power University, Beijing, China, in 2014. He is currently working toward the Ph.D. degree in the area of power electronics at The Hong Kong Polytechnic University, Hong Kong.

His current research interests include high frequency bidirectional isolated dc/dc converters and advanced soft-switching techniques.

Mr. Yaqoob is a Reviewer for the IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS, IEEE TRANSACTIONS ON CONTROL SYSTEMS TECHNOLOGY, *IET High Voltage,* and *IET Power Electronics*.

Y. M. Lai (M'92–SM'11) received the B.Eng. degree in electrical engineering from the University of Western Australia, Perth, Australia, in 1983, the M.Eng.Sc. degree in electrical engineering from the University of Sydney, Sydney, Australia, in 1986, and the Ph.D. degree in power electronics from Brunel University, London, U.K., in 1997.

He was an Associate Professor with Hong Kong Polytechnic University, Hong Kong. His research interests include computer-aided design of power electronics and nonlinear dynamics.