A Smart IGBT Gate Driver IC With Temperature Compensated Collector Current Sensing

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***Abstract*—Conventional insulated gate bipolar transistor (IGBT) current sensing and protection techniques usually employ discrete sensors, such as lossy shunt resistors, and may involve accessing the high-voltage collector load of the IGBT. This would normally present difficulties for integration. This paper presents an IGBT gate driver IC with a collector current sensing circuit and an on-chip CPU for local data processing. This IC is prototyped using a TSMC 0.18 μm 40 V BCD Gen-2 process. The collector current sensing technique is based on the unique Miller plateau relationship between the gate current and collector current (I_C and I_G) for a particular gate resistance (R_G). It allows a cycle-by-cycle measurement of I_C during both turn-ON and turn-OFF transients without any extra discrete components. The temperature variation is compensated internally by the on-chip CPU using polynomial curve fitting. This technique only monitors the low-voltage signal at the gate terminal, without the need to handle any high-voltage signal on the collector/load side. Measurements using a double pulse test setup show an accuracy of $\pm$0.5 A over the current ranges of 1–30 A for turn-ON and 1–50 A for turn-OFF from 25 to 75 °C.**

***Index Terms*—Insulated gate bipolar transistors (IGBTs), IGBT current sensing, IGBT gate driver IC.**

I. Introduction

INSULATED gate bipolar transistor (IGBT) is widely used in a variety of power switching applications due to its superior electrical characteristics and easy-to-drive feature by virtue of its merged MOS-bipolar structure [1]. The basic IGBT power modules usually only include multiple IGBTs and free wheeling diodes (FWDs). They can be driven by external gate drivers or controller boards [2]. In order to provide self-protection and load monitoring capabilities to the IGBTs, the concept of intelligent power module (IPM) was introduced in the late 1980s

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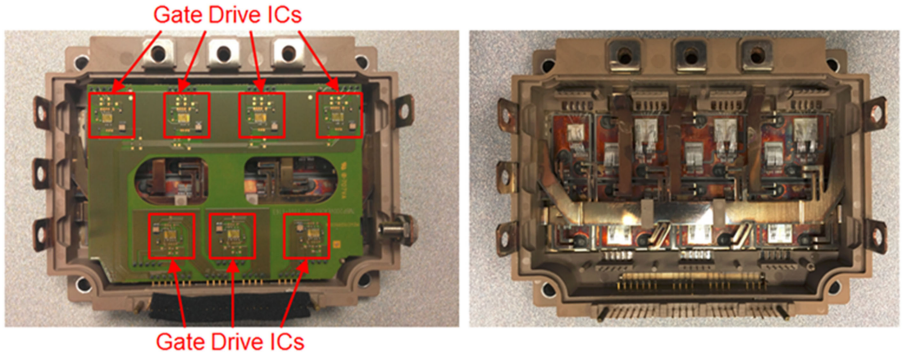


Fig. 1. Fuji Electric 7MBP200VEA060-50 IPM module. (a) Driver and control circuit board. (b) IGBTs and FWDs on the bottom.

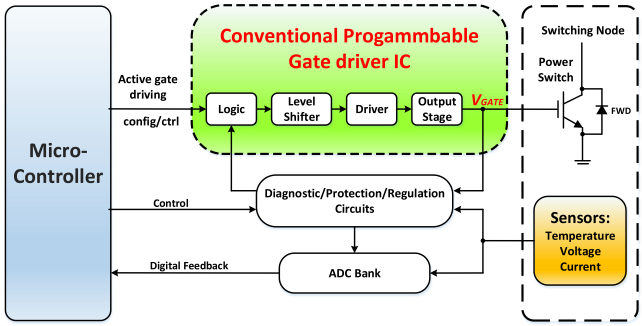


Fig. 2. Functional block diagram of a conventional programmable gate driver IC.

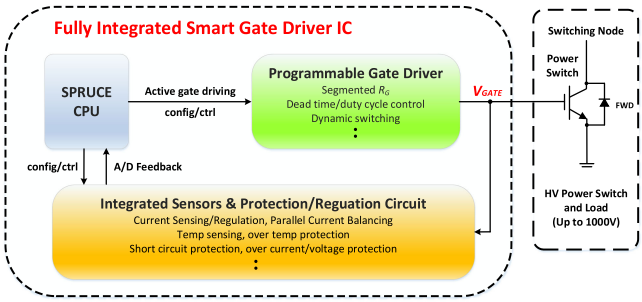


Fig. 3. Functional block diagram of the proposed smart gate driver IC with integrated CPU, programmable gate driver, and sensor circuits.

that rely on the monitoring of only the gate characteristics are also fully integrated. There is no need for any extra discrete components, nor to access signals on the high-voltage side of the power switch and the load.

The smart gate driver IC, presented in this paper, includes a programmable gate driver, an on-chip CPU and an integrated current sensor. The programmable gate driver is highly configurable with the on-chip CPU control. The CPU is a simple stack-based microcontroller named Stack PRocessor Unit for Controlling Energy (SPRUCE), which was proposed in [23]. This embedded processor in the gate driver IC can provide reconfigurable control algorithm for many types of closed-loop control functions for the IPMs. The integrated sensor in this design is also temperature compensated, and it only monitors the gate current during the Miller plateau region to predict the collector current of the IGBTs.

This paper focuses on the discussion of the proposed current sensing technique and its incorporation into a smart gate driver IC. The paper is organized as follows. The conventional current sensing methods are reviewed in Section II. The proposed collector current sensing method using gate current is presented in Section III. Section IV provides the details of the driver IC design. Section V discusses the experimental setup and the measurement results. This is followed by a discussion on the thermal behavior and the mathematical curve fitting for the temperature compensation. Section VI concludes the paper.

II. Conventional Current Sensing Methods

Current sensing has always been critical for protection and regulation in modern high-voltage and high-current power systems. Different current sensing techniques have been reviewed in [24]–[26]. There are resistive current sensors, such as series/shunt resistors, or magnetic/inductive sensors, such as Rogowski coils, current transformers, and Hall effect sensor. Efforts have been made to integrate the above-mentioned sensors to various industrial power systems to monitor the output currents [27]–[30]. However, all of these sensors introduce extra discrete components and may increase the volume, the complexity, and the cost of the power system significantly.

For current sensing in IGBT modules, the shunt resistor sensors remain the most popular due to their low cost and small size. As shown in Fig. 4(a), a low-value ohmic shunt resistor is inserted between the emitter of the IGBT and ground. The voltage drop across the resistor can be used for monitoring and protection [26], [27], [31]. The power losses across this resistor can be high and the system cost and size can increase drastically, especially if very high currents are being switched and heat-sinking is required.

A more popular way to sense IGBT current is to embed a sensing device in the IGBT, similar to the sense field effect transistor (FET) used for power MOSFET [32], [33]. The small sense current I_S is directly proportional to the main collector current I_C and can be measured though a sense resistor, as shown in Fig. 4(b). The current sensing ratio is dependent on the area ratio of the emitters, IGBT junction temperature, sense

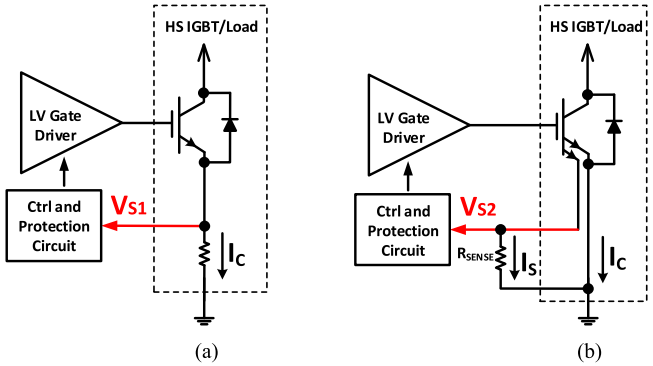


Fig. 4. Traditional IGBT collector current sensing methods using (a) an external resistor or (b) an embedded sense transistor.

resistor resistance, collector current I_C, and also V_{CE} [32], [34]–[36]. Therefore, this current sensing method is widely adopted in IPMs for short-circuit protection only. However, it lacks the accuracy required for current regulation. A low sense resistor value would lead to a weak signal in a potential noisy environment, substantially reducing the measurement accuracy. A high sense resistor value may cause V_{S1} and V_{S2} (in Fig. 4) to exceed the maximum supply voltage of the low-voltage control and protection circuit, and possibly destroying the IC.

III. Proposed Current Sensing Technique

Recently, various innovative ideas of using the IGBT gate current, gate voltage, or gate charge to predict or monitor the IGBT condition or behavior have been proposed and verified. This trend is driven by the need to fully integrate the sensors and protection circuits into the gate driver IC, as illustrated in Fig. 3. At the same time, the handling of low-voltage gate signals only ensures the feasibility for full integration. The techniques for short-circuit detection by analyzing the gate voltage pattern or gate charge characteristics were presented in [37]–[39]. A novel way to measure the imbalance of the currents in paralleled IGBTs using gate charge was proposed in [40]. The gate signals could also be analyzed for IGBT health monitoring [41], [42] and even junction temperature extraction [43]–[45].

The idea of using the IGBT gate current to predict the collector current was initially proposed and demonstrated experimentally by the author Chen *et al.* [46]. A discrete version of the automatic collector current sensing using gate current was presented in [47]. This paper is an extension of previous work with full integration of all the current sensing circuitry into one gate drive IC [48].

A. Physical Background of the Proposed Technique

The proposed collector current sensing method utilizes the Miller effect in the IGBT (also in power MOSFETs), as shown in the typical switching waveforms in Fig. 5. Both the gate-emitter voltage (V_{GE}) and gate current (I_G) exhibit a Miller plateau during turn-ON and turn-OFF, due to the charging and discharging of the gate collector capacitor (C_{GC}). The voltage at the V_{GE} plateau is largely dependent on the value of I_C [49]. Therefore, I_C can be obtained by measuring the plateau value of

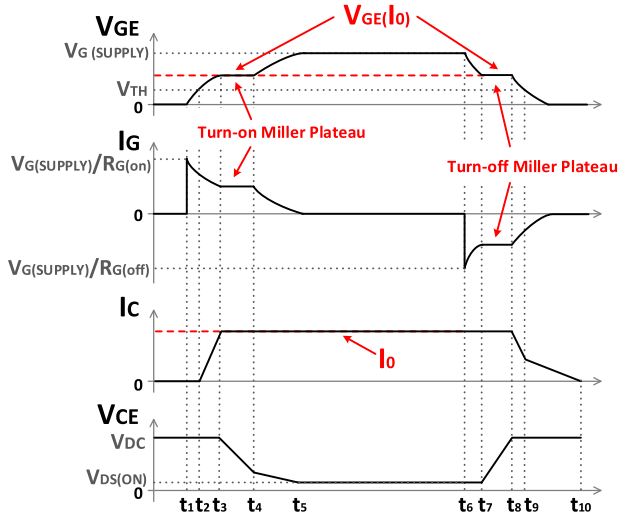


Fig. 5. Typical IGBT switching waveforms.

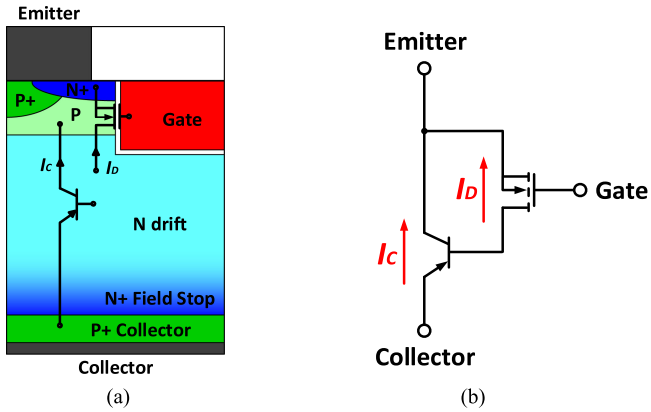


Fig. 6. (a) Cross section of a typical trench gate field-stop IGBT. (b) Simplified IGBT model.

V_{GE} or by measuring I_G. In practice, it is not convenient to measure V_{GE} directly as the emitter of the IGBT may be connected to the ground via substantial amount of parasitic inductance from the circuit wiring. Therefore, the proposed measurement technique is to measure I_G to indirectly deduce I_C.

To understand the physical relationship between I_G and I_C, the following analysis is carried out using a simple IGBT model. Fig. 6(a) shows the cross section of a typical trench gate field-stop IGBT, which is the most popular IGBT structure with short turn-OFF time and low on-state voltage drop [50]. Fig. 6(b) shows the simplified model for the IGBT, which is a MOSFET driving a wide–based p-n-p transistor. The physical locations of the MOSFET and the p-n-p transistor in the trench gate field-stop IGBT is shown in Fig. 6(a). In this IGBT, the electron current (I_n) flowing through the MOSFET serves as the base drive current for the p-n-p transistor; therefore, the hole current (I_p) flowing through the p-n-p transistor is [51]

$$I_p = \beta_{\mathrm{PNP}} I_n = \left(\frac{\alpha_{\mathrm{PNP}}}{1-\alpha_{\mathrm{PNP}}}\right) I_n \tag{1}$$

where β_{PNP} denotes the common emitter current gain of the p-n-p transistor and α_{PNP} is the common base current gain. The

emitter current of the IGBT I_E can be obtained by adding the electron and hole currents as

$$I_E = I_n + I_p = \frac{I_n}{1-\alpha_{\mathrm{PNP}}}. \tag{2}$$

Due to the high input impedance of the MOS gate structure, the gate current I_G is zero in the steady state. Even during switching, the charging and discharging gate currents are much smaller than the emitter current. Therefore, I_E is approximately equal to the collector current I_C. The electron current I_n is in fact the drain current of the MOSFET. Therefore, I_C and I_D can be related as shown below

$$I_C = \frac{I_D}{1-\alpha_{\mathrm{PNP}}}. \tag{3}$$

Suppose a voltage source switching between V_{DRIVE} and ground is applied to the IGBT. During the turn-ON process, the gate current I_G of the IGBT (also the MOSFET) can be expressed as

$$I_G = \frac{V_{\mathrm{DRIVE}} - V_{\mathrm{GE}}}{R_{G(\mathrm{ON})}} \tag{4}$$

and drain current of the MOSFET (I_D) can be expressed as

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{\mathrm{GE}} - V_{\mathrm{TH}})^2 \tag{5}$$

considering that

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{\mathrm{GE}} - V_{\mathrm{TH}}). \tag{6}$$

Thus, I_D can be simplified as

$$I_D = \frac{g_m (V_{\mathrm{GE}} - V_{\mathrm{TH}})}{2}. \tag{7}$$

Combining (4) and (7), we get

$$I_G = \frac{V_{\mathrm{DRIVE}} - V_{\mathrm{TH}} - \frac{2I_D}{g_m}}{R_{G(\mathrm{ON})}}. \tag{8}$$

Substituting (3) into (8), the relationship between I_C and I_G can be expressed as

$$I_C = -\frac{R_{G(\mathrm{ON})} g_m}{2(1-\alpha_{\mathrm{PNP}})} I_G + \frac{g_m (V_{\mathrm{DRIVE}} - V_{\mathrm{TH}})}{2(1-\alpha_{\mathrm{PNP}})} \tag{9}$$

where g_m is the transconductance of the MOSFET. It is related to the transconductance of the IGBT G_m by [52]

$$G_m = \frac{g_m}{1-\alpha_{\mathrm{PNP}}}. \tag{10}$$

During the turn-ON transient I_C can be determined by

$$I_C = -\frac{R_{G(\mathrm{ON})} G_m}{2} I_G + \frac{G_m (V_{\mathrm{DRIVE}} - V_{\mathrm{TH}})}{2}. \tag{11}$$

A similar derivation for I_C can also be applied to the turn-OFF process

$$I_C = -\frac{R_{G(\mathrm{OFF})} G_m}{2} I_G + \frac{G_m V_{\mathrm{TH}}}{2} \tag{12}$$

where $R_{G(\mathrm{ON})}$ and $R_{G(\mathrm{OFF})}$ are the turn-ON and turn-OFF gate resistance. V_{TH} is the threshold voltage of the IGBT. R_G, V_{DRIVE}, and V_{TH} are usually constants. G_m of the IGBT can be found from the I_C versus V_{GE} transfer curves in the device data sheet. Therefore, there is indeed a relationship between the gate current I_G and collector current I_C. This is a unique relationship for a particular IGBT structure and is only affected by temperature and process variations. The temperature compensation method will be introduced in Section V. However, this relationship is only valid in the Miller plateau region, where the device is in a saturation mode. In practical applications, where on-the-fly computing should be minimized, it is easy to model this relationship by a simple lookup table or curve fitting.

B. Experimental Verification of the Proposed Technique

Simple experiments have been carried out to demonstrate the relationship between I_G and I_C. Fig. 7 shows the measured I_G waveforms for different I_C conditions during turn-ON and turn-OFF at $V_{\mathrm{DD}} = 250$ V (V_{DD} is the load side supply voltage) when a discrete IGBT (Infineon IGBT Model IGB30N60H3) is switched. It is clear that the I_G plateau region changes with the I_C with a reasonable sensitivity.

The Miller plateau values for I_G during turn-ON and turn-OFF are extracted and plotted against I_C for difference V_{DD} from 25 to 250 V, as shown in Fig. 8. The measurement results remain consistent regardless of V_{DD} levels for both turn-ON and turn-OFF transients. The reason behind this is well explained in [53]. Increasing V_{DD} (or V_{CE} of the IGBT) will only increase the V_{GE} or I_G plateau length without changing the plateau level. Therefore, the proposed technique is quite robust considering the possible fluctuations of V_{DD} or V_{CE} in real applications.

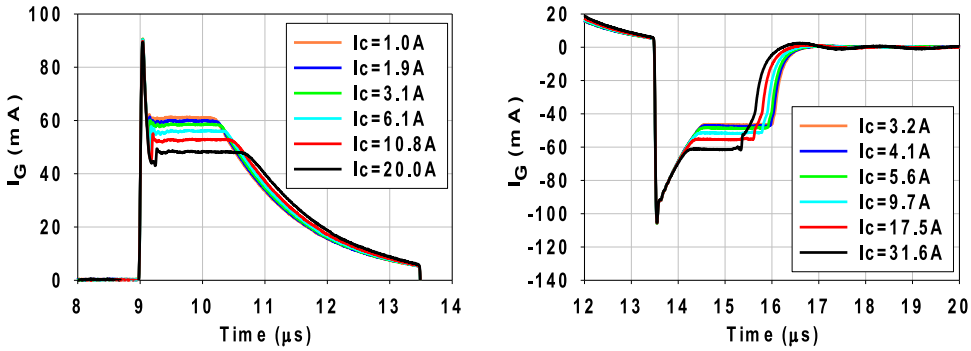
IV. Circuit Design and Implementation

A. Design Overview

The block diagram of the proposed gate driver chip is shown in Fig. 9. It includes a segmented IGBT gate driver, a SPRUCE unit, and the proposed collector current sensing circuit. There are three voltage domains in the gate driver IC: 1.8 V for the CPU core and gate driver logic control; 3.3 V for the CPU I/O and the current sensing circuit block; and up to 20 V for the gate driver output stage. All the current sensing function could be realized within the low-voltage gate driver chip block. No sensing circuit needs to access the IGBT's high-voltage load side which could easily be a few hundreds of volts.

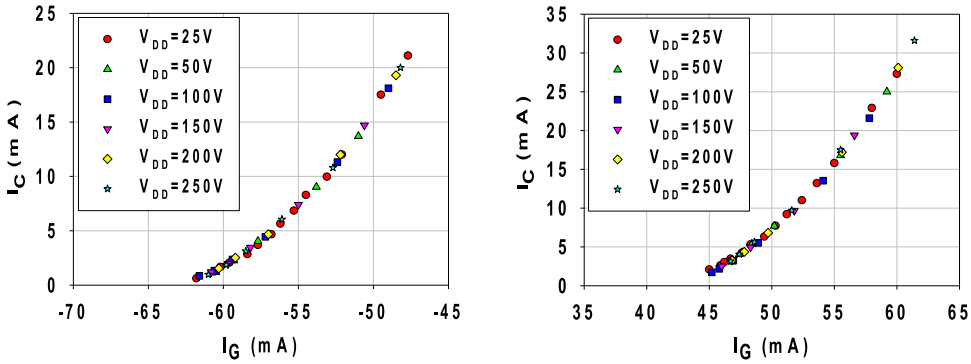
The gate driver uses a voltage driven topology, containing a chain of inverters with selectable output driver segments [54]. There are eight output segments for pull up and pull down strength variation, which ranges from 0.35 to 41.9 Ω. This output stage has been implemented and characterized previously [55]. The designed gate resistance value and the actual measured values are listed in Table I. In this case, no external discrete gate resistance is needed for the IGBT. The driver is highly configurable using the intelligent SPRUCE control, which includes output segments selection, PWM control, and dynamic switching. The gate driver's performance can be easily optimized.

The block level diagram for the SPRUCE unit and its peripheral digital modules are illustrated in Fig. 10. Included in this module are a SPRUCE core, a serial peripheral interface



(a) (b)

Fig. 7. Measured I_G waveforms for different I_C with $V_{DD} = 250$ V during (a) turn-ON and (b) turn-OFF for an Infineon IGB30N60H3 IGBT.



(a) (b)

Fig. 8. (a) Measured I_C versus I_G (turn-ON plateau values). (b) Measured I_C versus I_G (turn-OFF plateau values) [47].

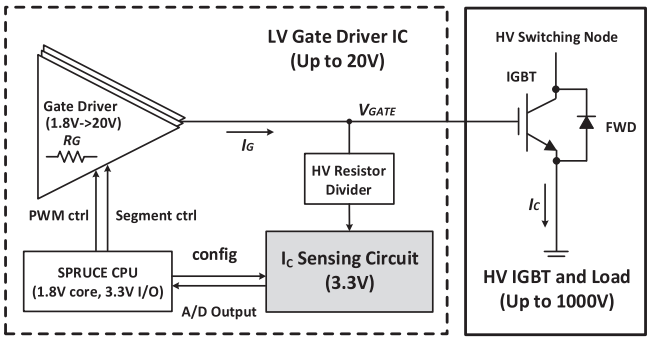


Fig. 9. Block diagram of the proposed gate driver IC with current sensing.

TABLE I
GATE DRIVER OUTPUT RESISTANCE

No. of Active Segments	Designed R_{OUT} (Ω)	Measured R_{OUT} (Ω)
0	41.9	41.6
1	21.0	21.6
2	10.5	11.1
3	5.26	5.77
4	2.81	3.17
5	1.41	1.71
6	0.70	0.88
7	0.35	0.46

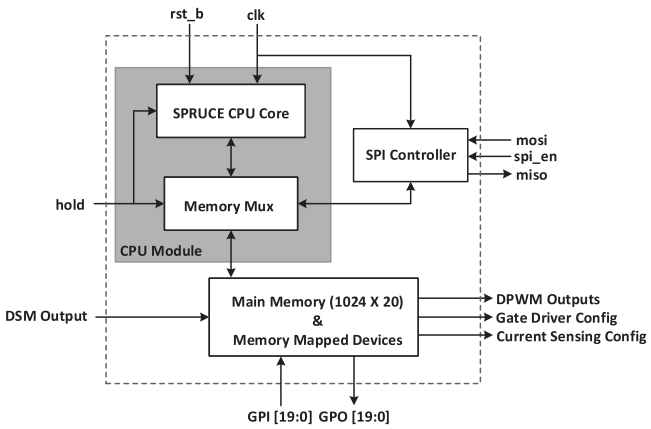


Fig. 10. Block level diagram for the SPRUCE unit and its peripheral digital modules on the gate driver IC.

(SPI) controller, and a main memory composed of 1024 × 20 b of memory. Several memory mapped modules are controlled by the SPRUCE unit. They are the digital pulsewidth modulator, the gate driver and current sensing circuitry configuration bits, 20 general purpose input) registers and 20 general purpose output registers for I/O interfaces, and a 100 b shift register to temporarily store the DSM outputs for digital processing. All these modules are premapped into dedicated memory locations and can be easily configured and accessed by the CPU.

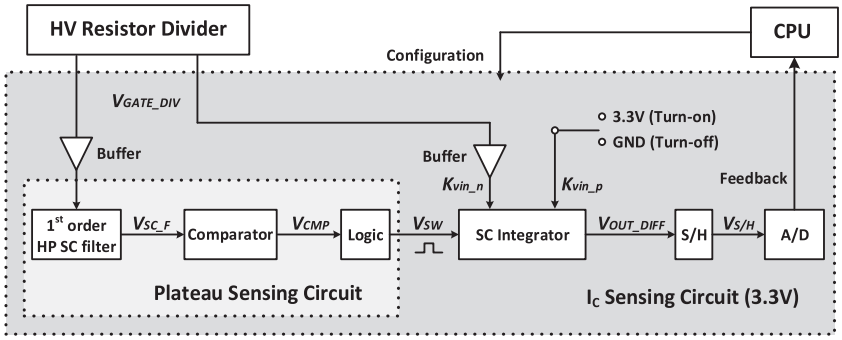


Fig. 11. Block diagram of the I_C sensing circuit.

The SPRUCE unit is a simple stack machine with minimum instruction set and registers [23]. The memory Multiplexer (MUX) in Fig. 10 shows how the SPI controller can provide external access to the memory space. Also, the behavior of SPRUCE can be monitored for testing purposes.

The block diagram of the I_C sensing circuit is shown in Fig. 11. First, a high-voltage resistor divider network scales the $V_{\rm GE}$ to below 3.3 V in order to be compatible with the signal processing circuit. A plateau sensing circuit block is then used to produce timing pulses that indicate the turn-ON and turn-OFF of the plateau. These pulses serve as the triggering signals for the switched capacitor (SC) integrator, which accumulates the voltage difference across R_G (represented by the voltage across the input and output of the gate driver with selectable output segments) inside the plateau. The sample and hold (S/H) circuit maintains the integrator output until the next cycle. This provides enough time for the delta sigma modulator (DSM) to perform 100× oversampling. The output from the 1-b DSM is fed back to the on-chip SPRUCE unit. It performs digital filtering before producing the actual ADC output.

B. Circuit Implementation

1) Plateau Sensing: The plateau sensing circuit consists of a SC filter, a comparator, and a logic block. The SC filter implements a typical first-order high-pass filter with the loading capacitor C_P made relatively large and the sampling switch made relatively small. This forms a bandpass filter with frequency response peaks around 3 MHz (switching frequency is 15 MHz), as shown in Fig. 12. When the scaled IGBT gate signal is applied to the filter at $K_{\text{vin\_}p}$ while $K_{\text{vin\_}n}$ is grounded, the output waveform will be series of weak analog double pulses where the time in between correspond to the Miller plateau region during turn-ON and turn-OFF, as illustrated in Fig. 13. The filter output is fully differential with common mode voltage of 1.6 V, where the positive output $(V_{\text{SC\_}F\,(\text{turn\_on})})$ is for turn-ON plateau sensing and negative output $(V_{\text{SC\_}F\,(\text{turn\_off})})$ is used for turn-OFF plateau sensing.

After the SC filter stage, a comparator with a reference voltage set at 1.8 V is used to reshape the SC filter output. The resultant waveform $V_{\text{CMP(turn\_on)}}$ is a single pulse while $V_{\text{CMP(turn\_off)}}$ is a double pulse, as illustrated in Fig. 14. This is due to the fact that the charging process after the turn-ON plateau is slow, causing the second analog pulse of the filter output having small amplitude. The reference voltage for the comparator is purposely set a bit higher (1.8 V compared to the common mode voltage of 1.6 V); this is to make the comparator immune to the potential ringing noise from EMI during the turn-ON plateau. The comparator output only gives the starting range for the plateau sensing. The exact integration time for both turn-ON and turn-OFF transients is determined from experimental data and realized using the fixed PWM block.

Therefore, it should be noted that only the first pulse for the comparator output is important, as shown in Fig. 14. The subsequent logic circuit will generate a pulse with its rising edge corresponding to the falling edge of the first pulse, which is roughly the desired starting point of the Miller plateau.

The exact start and end point of the plateau sensing output is then determined by the fixed PWM block. The circuit implementation and sample waveforms are illustrated in Fig. 15. This block is composed of a chain of D flip-flops and two MUXs for the selection of the exact rising and falling time. The MUX is implemented to provide programmability for different IGBT modules and can be configured by the SPRUCE unit. This block makes sure that the output is always an integer multiple of the master clock and the obtained pulse is always well within the Miller plateau region. In this case, five clock cycles are selected for both turn-ON and turn-OFF with the clock frequency of 3.75 MHz. The fixed time integration method could greatly improve the accuracy of this technique. Since the integration time is now immune to any EMI noise that would potentially impact the comparator output and cause the integration time to vary. The exact integration time could be chosen to be as long as possible but shorter than the minimum Miller plateau length, which can be determined at a lower $V_{\rm CE}$ value as explained at the end of Section III.

2) Plateau Value Integration and Digitization: The SC filter employs a parasitic-insensitive and delayed topology, as shown in Fig. 16(a). Capacitance of C_2 is six times larger than C_1, which means that the output decreases by six times for each cycle. The same switching frequency of 15 MHz is used with the fixed integration time of 1.33 μs, which translates to 20 cycles. Therefore, the transfer function of the integrator for one cycle can be expressed as

$$V_{\text{out\_diff}} = (V_{\text{in\_diff}} - V_{\text{ref\_diff}}) \times 20/6. \tag{13}$$

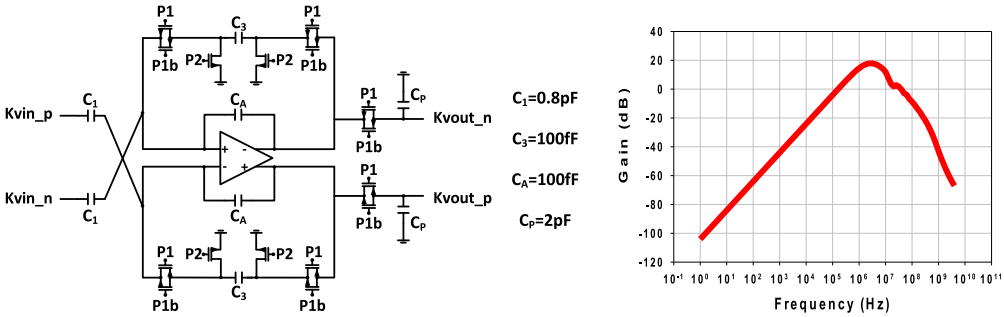


Fig. 12. SC filter schematic (left) and its frequency response using Spectre PSS analysis (right).

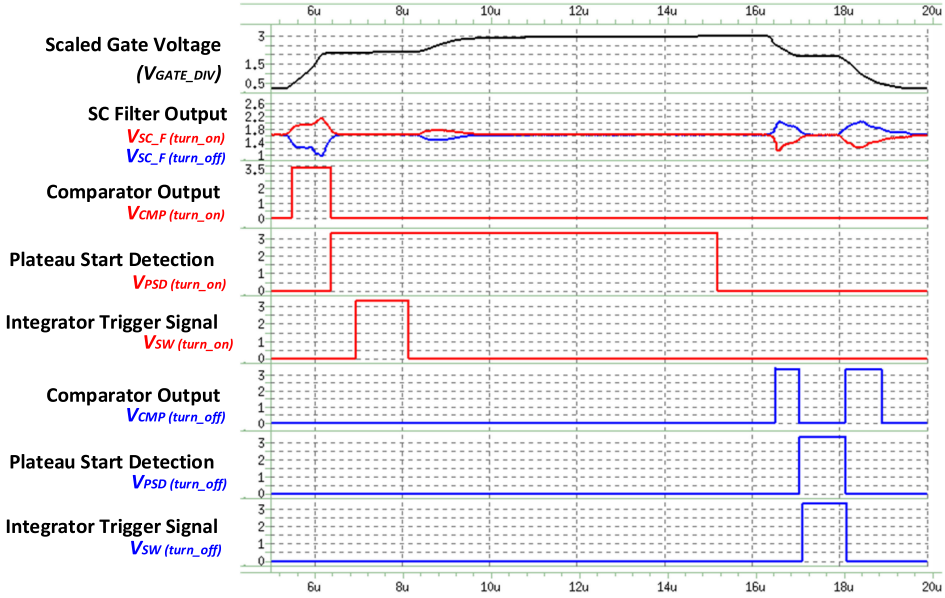


Fig. 13. Simulation results showing the turn-ON and turn-OFF plateau sensing signals. (The variables listed in these waveforms are mapped to the same variables labeled in Fig. 11.)

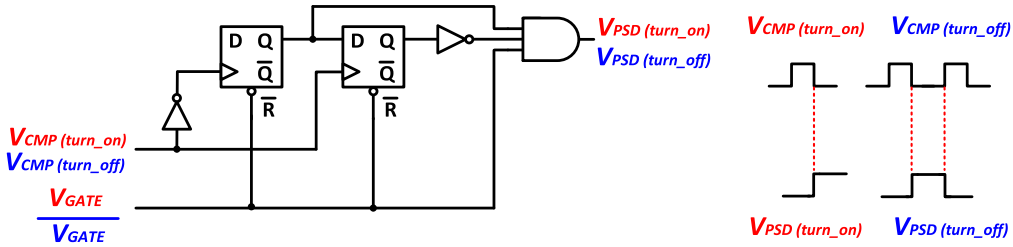


Fig. 14. Simple logic circuit for turn-ON and turn-OFF plateau start detection.

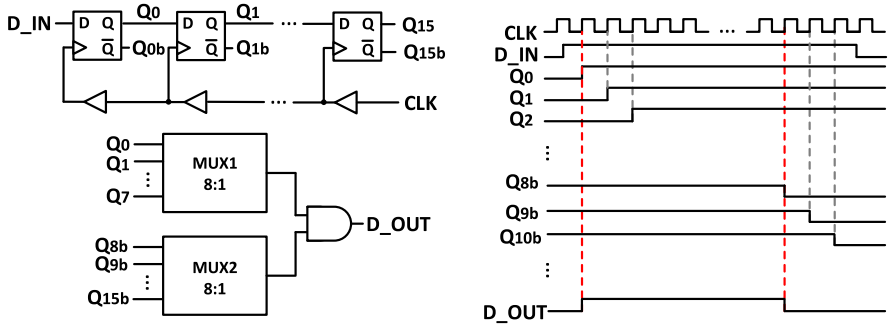


Fig. 15. Circuit implementation for the fixed PWM.

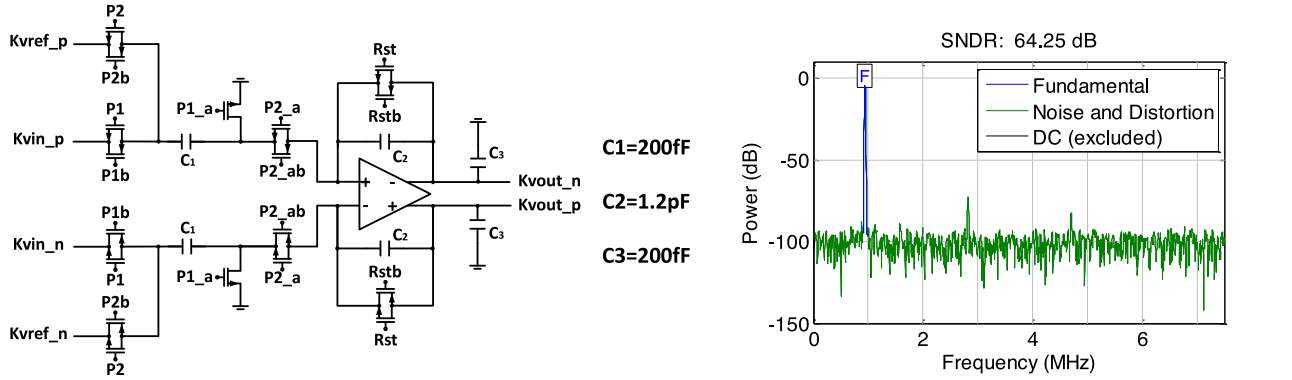


Fig. 16. SC integrator schematic (left) and the simulated FFT result for worst case SNDR condition at turn-ON (right).

This subtraction and amplify stage could increase the sensitivity of the gate current to the collector current relationship, and reduce the accuracy requirement for the ADC. At the same time, the output of the integrator is carefully controlled to be within the desired input range for the ADC.

During the turn-ON Miller plateau, the integrator accumulates the voltage difference between 3.3 V and the scaled gate voltage (common mode voltage is around 2 V). During the turn-OFF Miller plateau, it accumulates the voltage difference between the scaled gate voltage and ground (common mode voltage is around 1 V). Given the input signal around 1 MHz with 2 V peak-to-peak for the FFT simulation, the worst case signal–to-noise plus distortion ratio (SNDR) happens during turn-ON, which has an SNDR of 64.3 dB.

After the integrator stage, there is an S/H block with a clock-feedthrough cancelation topology. The sampling switch is triggered shortly after the V_{SW} signal (the integrator triggering signal) to ensure that the correct integrated output is sampled and held till the next cycle. The output then serves as the input to the subsequent DSM stage.

The reason for choosing a delta sigma ADC to digitize the output is that the input signal is relatively slow (20 kHz for a typical IGBT module), allowing a high over sampling ratio (OSR). In addition, the DSM has simple architectures and good tolerance to analog component inaccuracy but requires additional digital processing, which could be handled by the on-chip SPRUCE unit.

In our previous discrete implementation [47], the testing result is only up to 30 A. For the integrated design, in order to ensure an accuracy of ± 1 A over a current range of 50 A, the estimated resolution requirement of the ADC is around 10–20 mV. With a supply voltage of $V_{DD} = 3.3$ V, this translates to an effective number of bits (ENOB) for the ADC to be between 8 b ($3.3/256 \approx 12.89$ mV) and 9 b ($3.3/256 \approx 6.45$ mV). In order to leave some margin for the design and make the gate drive IC more adaptive for other IGBT devices, the target ENOB for the ADC is 10 b ($3.3/1024 \approx 3.22$ mV).

For design simplicity, linearity, and easier interfacing with the CPU, a 1-b quantization implemented with one comparator is chosen. In order to obtain a 10-b ENOB (SNR = 6.02 ENOB+1.76, equivalent to 62 dB) with a 1-b quantizer, a MOD 2 topology and an OSR of 100 are chosen for a theoretical 86 dB peak SQNR [56], taking into account of thermal noise, layout mismatch, and process variations. The Delta Sigma Tool box by Schreier and Temes is used to synthesize, simulate, and construct the topology of the DSM [57]. Fig. 17 shows the second-order modulator structure with the coefficients after dynamic scaling. The circuit is implemented using a two-stage SC integrator with the capacitors sized according to the coefficients.

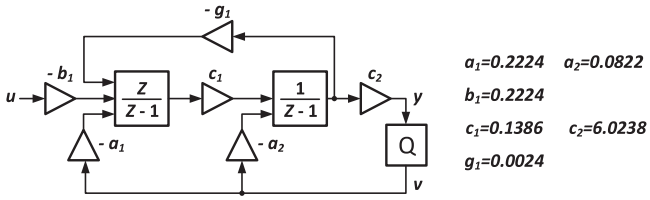


Fig. 17. Designed MOD2 $\Delta\Sigma$ ADC modulator.

TABLE II
SPECIFICATION FOR THE ADC

Parameter	Value
V_{DD}	3.3 V
Quantization	1 bit
Technology	0.18um HV
Architecture	2nd Order
OSR	100
Input Signal Frequency	20 kHz
Clock Frequency	10 MHz
Input / Output Common Mode Voltage	1.65 V
Full Input Range	±1.2 V
Peak Input Amplitude	-2.5 dBFS
DAC Reference Voltages	0.8 V, 2.5 V
Simulated SNDR for the DSM	77.9 db
Simulated SNDR for the ADC	61.28 db
Power Consumption	71.4 mW

The specifications for the ADC are listed in Table II. Considering an input frequency of $f_B = 20$ kHz, the minimum sampling frequency is $2 \times \text{OSR} \times f_B = 4$ MHz. Therefore, a 10-MHz clock is chosen to allow margins for digital processing. The full input range is ± 1.2 V. The simulated SNDR for the DSM is 77.9 dB with -2.5 dBFS and 12.5 kHz input.

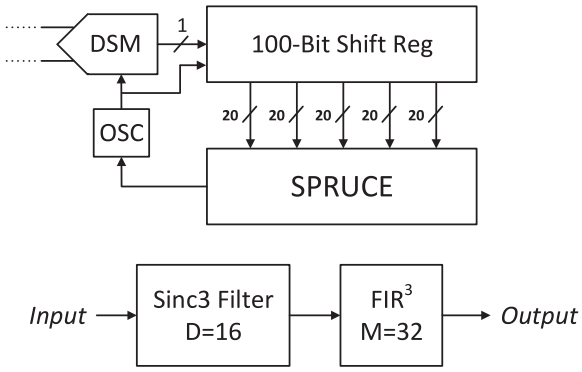


Fig. 18. Interface between the ADC and SPRUCE (upper) third-order CIC decimation filter architecture (lower).

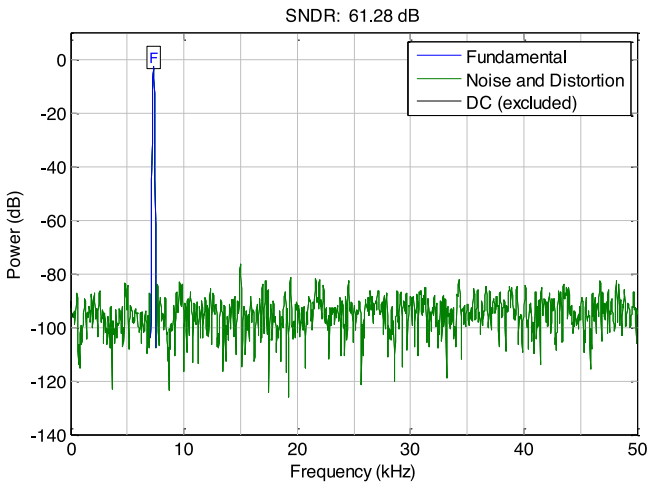


Fig. 19. Simulated static linearity of the DSM ADC.

The 1-b output of the DSM block is clocked into a 100-b shift register, as illustrated in Fig. 18. The shift register is memory mapped to 5 words (length is 20 each) in the main memory. The DSM could be started and stopped via the GPO controlled oscillator. It is triggered after the plateau region when the integrator finishes integrating and the sample hold block settles. The DSM is allowed to run free for a short time to allow initial settling with the last 100 b of data stored in the shift registers. These 100 b of data will go through a SPRUCE implemented third-order cascaded integrator-comb (CIC) filter and an FIR filter for noise suppression.

The final FFT plot for the ADC after the decimation filter is illustrated in Fig. 19. The sampling data are divided into 100 points per group and fed into the designed decimation filter. With 4096 ADC output codes, the obtained SNDR is 61.3 dB. This translates to an ENOB of 9.9 b. This is slightly below the design target (10 b) but the resolution is more than enough for this application.

The SPRUCE unit in this application provides intelligent on-chip digital processing. However, it was not a good idea to implement the digital filtering using the SPRUCE unit. This is because only one stack is available for all the basic operations. Meanwhile a large amount of arithmetic operations are needed for the digital filter. Therefore, the implemented digital filter is extremely slow. The measured processing time for the digital filter is around 2 ms, this means that the current readout cannot be obtained within one switching cycle. A simple solution is to synthesize a stand-alone digital filter block using Verilog. ModelSim simulations have been carried out for the same filter, as shown in Fig. 18. With a clock frequency of 100 MHz, the digital processing time is well within 5 μs. Considering the switching frequency of the IGBT is 20 kHz, the current reading could certainly be achieved within one cycle.

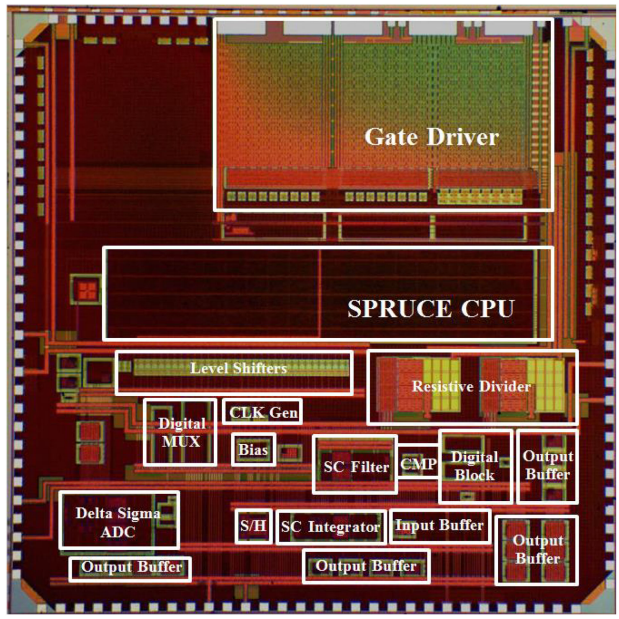


Fig. 20. Micrograph of the gate driver IC, fabricated using TSMC's 0.18 μm BCD Gen-2 process (chip area 5 mm $\times$ 5 mm).

V. Experimental Verification

A. Experimental Setup

The proposed smart gate driver IC is fabricated using the TSMC's 0.18 μm 40 V BCD Gen-2 process. The chip is fitted into a 5 mm $\times$ 5 mm pad frame, which is common in multiproject wafer implementation. Based on the bond wire connection plan, the top level circuit block placement is as shown in the micrograph of the chip in Fig. 20. The SPRUCE unit is placed in the center of the chip to facilitate easy control access to the upper gate drivers (with selectable segmented output stage and PWM control) and the lower IC sensing circuit (with configurations, ADC, and decimation filter, etc.). The output buffers (including digital output buffers and analog output buffers) surrounded the IC sensing circuit are connected to the output pins for an output probing purpose.

The fabricated gate driver IC is packaged and mounted on a custom printed circuit board plugged directly on top of a modified Fuji Electric 7MBP200VEA060-50 IGBT module, with the original driver board removed [as shown in Fig. 1(b)]. A double pulse test was carried out to test the current sensing function. The measurements are performed at the rising and falling edges

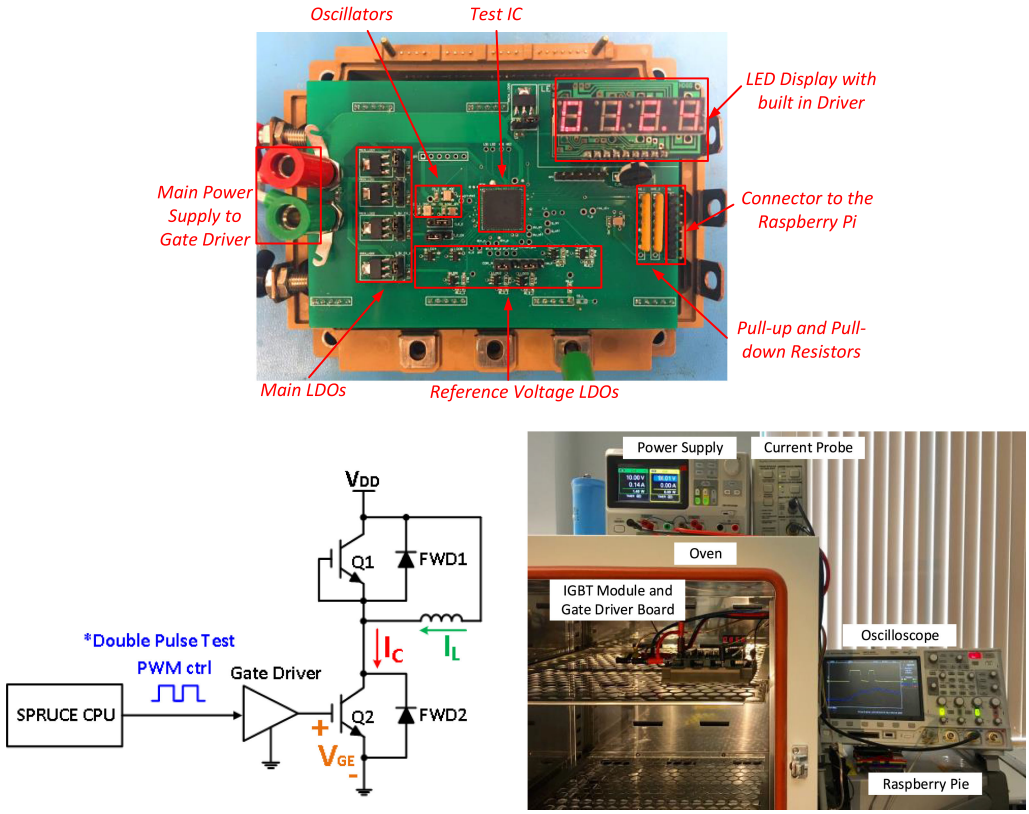


Fig. 21. Experimental setup for the gate driver IC with real time IC display (top). The double pulse test bench schematic (lower left) experimental test setup for the gate driver IC (lower right).

of the second gate pulse. The test bench schematic and hardware setup are shown in Fig. 21. The IGBT module and driver board are put in a climate chamber for the temperature sensitivity test. The Raspberry Pi is used to do initial programming of the SPRUCE unit. During the testing, the load side voltage is increased step by step in order to increase the load current. The resulting load current I_C and corresponding ADC readouts were recorded.

The basic timing diagram of the testing procedure at IGBT turning ON is illustrated in Fig. 22. First, the SPRUCE unit sets all the configuration bits for the I_C sensing circuitry. This is followed by the double pulse test. The turn-ON Miller plateau sensing circuit generates a pulse that is inside the Miller plateau region and with a fixed pulsewidth of 1.33 μs. After the plateau sensing, the integrator integrates the voltage difference between $V_{\rm DD}$ and $V_{\rm GE}$ during $V_{\rm SW}$. After the second pulse, the SPRUCE unit takes the DSM output and performs digital filtering, and puts the output results to the LED display.

B. Measurement Results and Discussion

The basic functionality results for this IC are shown from Fig. 23 to Fig. 25. These measurement results were briefly reported in [48]. Fig. 23 shows the outputs of the HV resistive divider and the SC filter. Fig. 24 shows the outputs waveforms for the Miller plateau sensing at turn-ON and turn-OFF transients. Fig. 25 shows the SC integrator outputs at turn-ON and turn-OFF.

Fig. 26 shows the ADC output codes as a function of I_C for turn-ON and turn-OFF transients at different ambient temperatures from 25 to 75 °C. The slow repetition rate is used in these double pulse tests to avoid self-heating of the IGBTs. The experiments are carried out using three different IGBTs at different ambient temperatures (at 35, 55, and 75 °C), as shown in Fig. 27. The results exhibit a small device to device variation. However, it clearly shows that the proposed technique is sensitive to temperature variations.

Referring to (11) and (12), both G_m and $V_{\rm th}$ are thermal sensitive parameters [58]. Therefore, the Miller plateau voltage value, which corresponds to certain I_C, would change with the temperature. Furthermore, R_G, which was realized using power MOSFETs, segments are also subjected to the temperature change, this may also impact the driving strength of the IGBT and hence the Miller plateau voltage to a certain extent.

Fig. 28 depicts the extracted gate voltage in the Miller plateau versus I_C for turn-ON and turn-OFF transients at different ambient temperatures. It demonstrates that the gate Miller plateau voltage changes with the temperature for a given I_C value. This is the main reason for the variations of the ADC readouts versus I_C with the temperature. It is also verified that the relationship of the integrator outputs (Interpreted from the ADC readouts) and the Miller plateau voltages match (13) quite well for both turn-ON and turn-OFF transients.

For the I_C sensing circuitry, the main circuit blocks are mostly SC circuits (filter, integrator, and also DSM ADC) that are

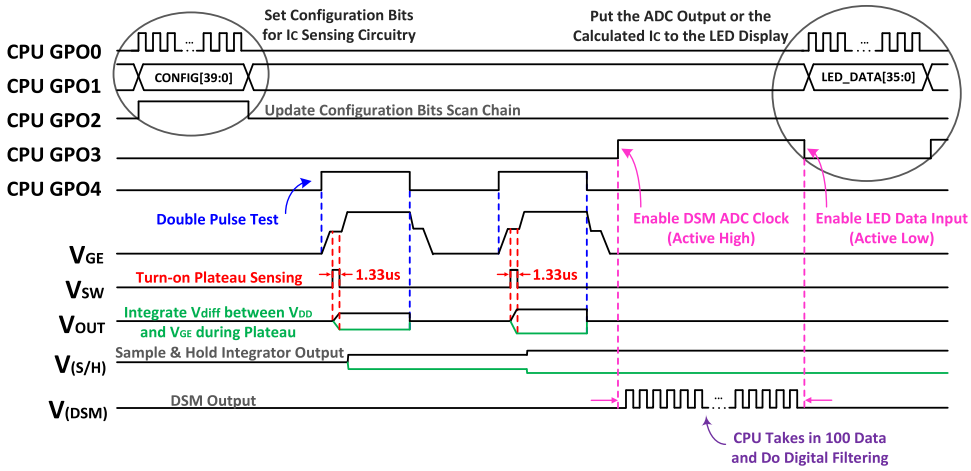


Fig. 22. Timing diagram for the sensing of I_C during turn-ON.

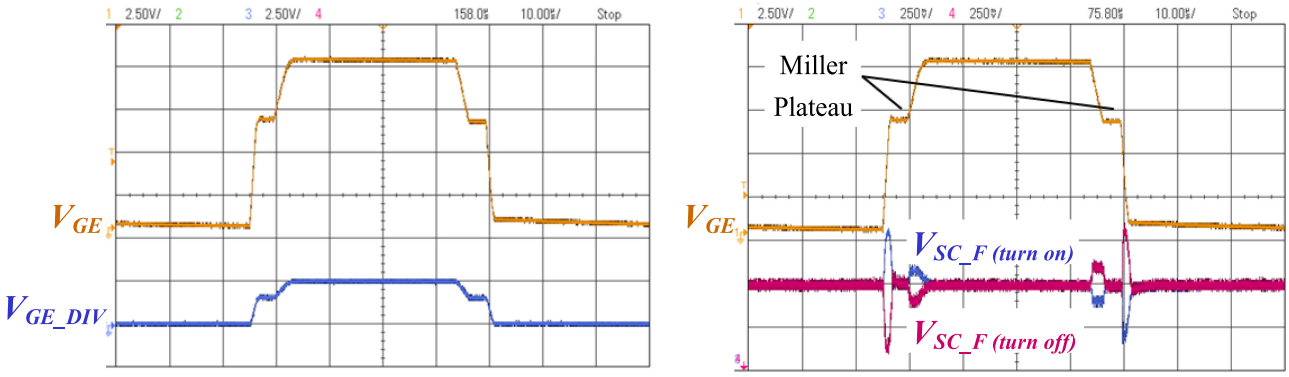


Fig. 23. Measured waveforms for V_{GE} and the HV resistive divider output V_{GE_DIV} (left) and measured waveforms for V_{GE} and the SC filter output V_{SC_F} (right) [V_{GE} : 2.5 V/div, V_{GE_DIV} : 2.5 V/div, V_{SC_F} : 0.25 V/div].

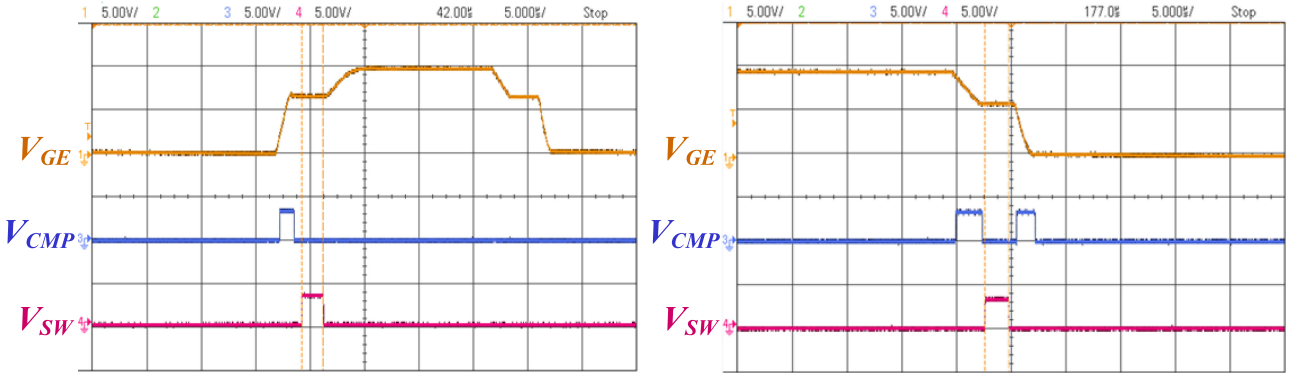


Fig. 24. Measured waveforms for V_{GE}, the comparator output V_{CMP}, and the logic output V_{SW} for turn-ON transient (left) and turn-OFF transient (right) [V_{GE} : 5 V/div, V_{CMP} : 5 V/div, V_{SW} : 5 V/div].

insensitive to the temperature change. Simulation results show that for a given Miller plateau voltage, the ADC outputs would change by less than 2% when the temperature changes from 25 to 75 °C.

Considering the fact that the IGBT is usually operating under high temperature conditions, temperature compensation is necessary for the proposed current measurement technique. A third-order polynomial curve fitting is carried out using MATLAB for I_C versus ADC output codes and the ambient temperature, as depicted in Figs. 29 and 30. The polynomial fit residues (the difference between the actual I_C value and the predicted I_C value based on the ADC codes and temperature

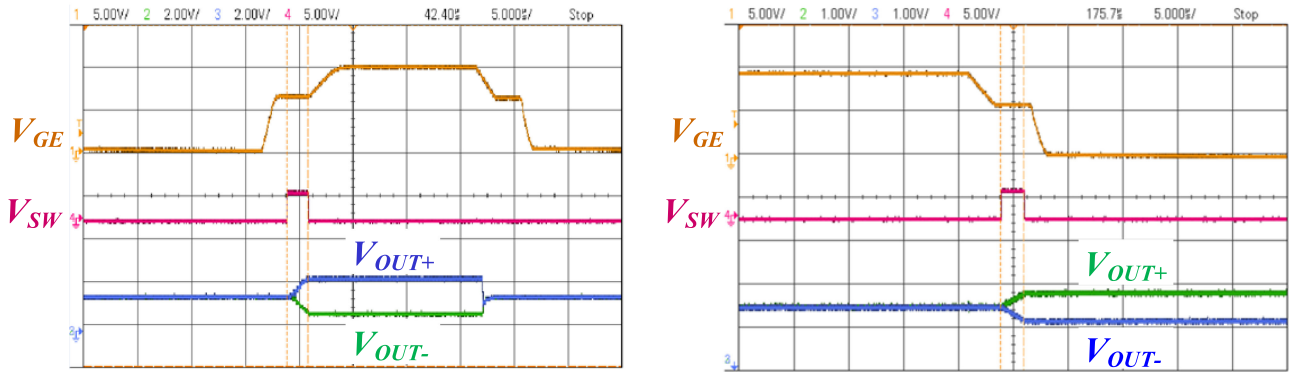


Fig. 25. Waveforms for V_{GE}, V_{SW}, and SC integrator outputs, V_{OUT+} and V_{OUT-} for turn-ON transient (left) and turn-OFF transient (right) [V_{GE} : 5 V/div, V_{SW} : 5 V/div, V_{OUT+}, and V_{OUT-} : 2 V/div].

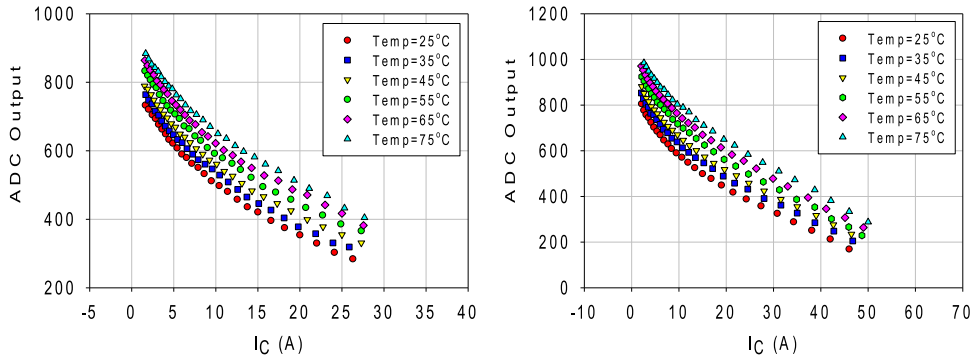


Fig. 26. Measured ADC output codes versus I_C at different ambient temperatures during turn-ON (left) and turn-OFF (right).

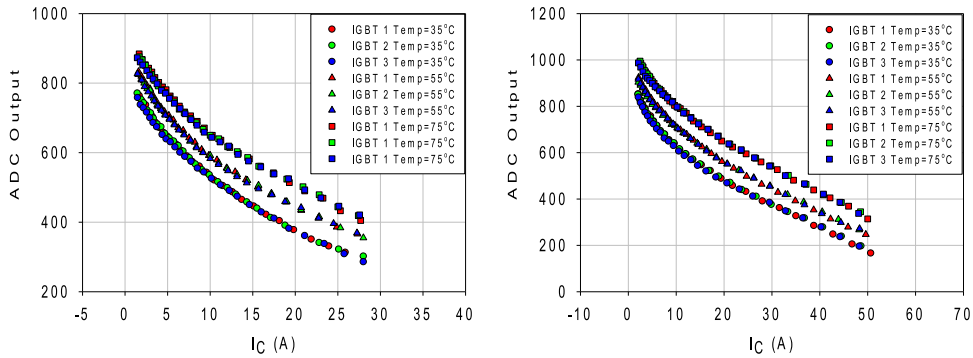


Fig. 27. Measured ADC output codes versus I_C at different ambient temperatures during turn-ON (left) and turn-OFF (right) for three different IGBTs.

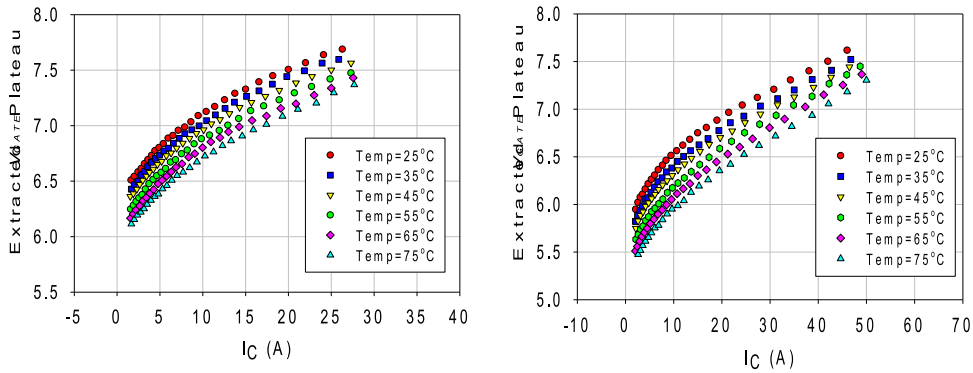


Fig. 28. Extracted gate plateau voltage versus I_C at different ambient temperatures during turn-ON (left) and turn-OFF (right).

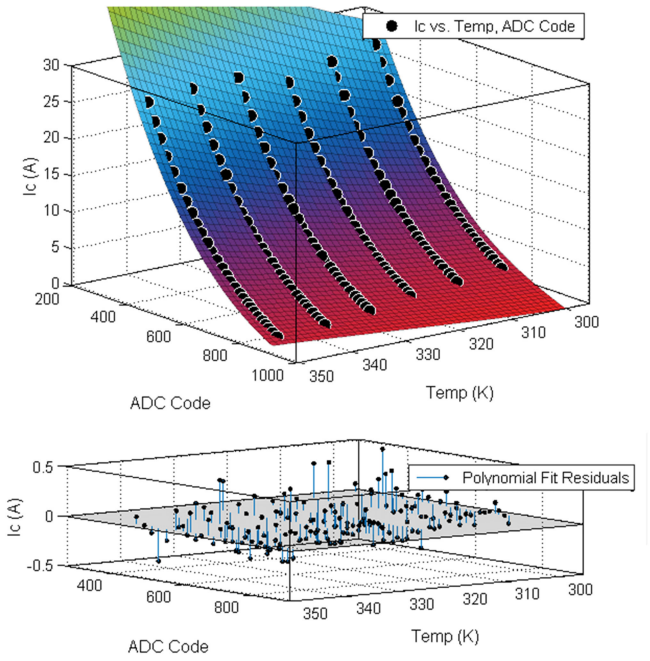


Fig. 29. Plot of I_c versus ADC output codes and temperature, and the third-order polynomial fit (top) for turn-ON transients. The polynomial fit residues plot (bottom).

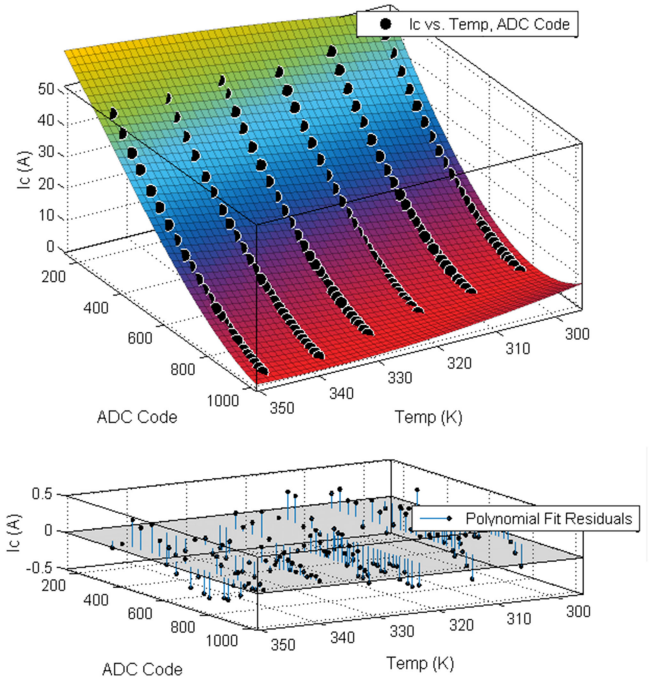


Fig. 30. Plot of I_c versus ADC output codes and temperature, and the third-order polynomial fit (top) for turn-OFF transients. The polynomial fit residues plot (bottom).

using the polynomial equations) across the full testing range are within ± 0.5 A.

Furthermore, the on-chip SPRUCE unit can implement the third-order curve fitting based on the digitized readouts from any temperature sensor. Therefore, the temperature effect can be compensated internally.

TABLE III
SMART GATE DRIVE IC PERFORMANCE SUMMARY

Parameters		**Values**	**Units**
Technology		0.18	μm
V_{DD}		3.3	V
Chip Size	Total	5×5	mm×mm
	CPU	0.8×3.6	mm×mm
	Gate Driver	1.2×2.7	mm×mm
	I_C Sensing Circuitry	1.5×4	mm×mm
Power Consumption	SPRUCE (CPU)	23	mW
	Gate Driver	320	mW
	I_C Sensing Circuitry	113	mW
IGBT Switching Frequency		20	kHz
I_C Sensing Testing Current Range		0-50	A
I_C Sensing Testing Temperature Range		25-75	°C
I_C Sensing Accuracy		$\pm$0.5A	A

VI. CONCLUSION

This paper presents a smart IGBT gate driver IC with integrated collector current sensor and on-chip CPU for digital processing. The proposed current sensing method utilizes the low-voltage gate signal to indirectly predict the collector current. Table III summarizes the measured performance of the proposed smart gate driver IC for IGBTs. With the on-chip temperature compensation, an accuracy of ± 0.5 A is achieved within the current range of 1–30 A for turn-ON and 1–50 A for turn-OFF from 25 to 75 °C.

The current measurement technique is applicable across different types of IGBTs and even power MOSFETs as long as there are the presence of Miller plateaus during turn-ON and turn-OFF transients. However, different devices may have different relationships between the Miller plateau voltages and the load currents, and also different thermal sensitivity. Curve fitting needs to be customized for each type of devices. In addition, certain devices bearing bad chip to chip variations may degrade the accuracy of the measurement.

Future work could focus on how to further improve the accuracy of the proposed current sensing method, such as employing a more accurate ADC, and getting the real junction temperature of the IGBT to refine the thermal modeling. The current testing range could also be extended and the effect of EMI exerting on the measurement results when the current level becomes exceedingly high could be examined. Other areas for the future work could be the applications for the proposed current sensing methods, such as the closed-loop current regulation and zero current crossing detection. In order to achieve these functions, the digital filter should be redesigned, and it should be ensured that the current readout can be obtained within each IGBT switching cycle.

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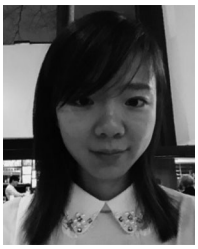

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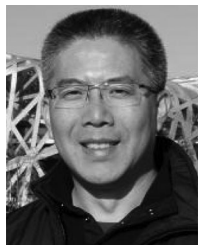

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