A Self-Tuned Class-E Power Oscillator

Mohammad Mahdi Ahmadi, *Member, IEEE*, and Maryam Salehi-Sirzar

***Abstract*—The efficiency and output power of a high-Q Class-E power amplifier (PA) are very sensitive to the values of the circuit components. Any mismatch between the nominal Class-E frequency and the input clock frequency could result in considerable degradation in the efficiency and much change in the output power. In this paper, we present a new self-oscillating Class-E PA, or so-called Class-E power oscillator (PO), whose feedback network is mainly constructed of a low-Q *RC* circuit. As a result, the phase response of the feedback network is almost flat around the operating frequency, and if the nominal Class-E frequency of the load network changes due to variations in the component values, the phase shift in the feedback network does not change considerably, and therefore, the Class-E operation of the circuit is substantially maintained. We also present a complete design procedure for the proposed Class-E PO. We have built and tested a sample Class-E PO based on the proposed circuit. At $V_{DD} = 4.5$ V, the measured oscillation frequency, output power, and efficiency of the circuit are 800 kHz, 0.96 W, and 89%, respectively. Simulation and measurement results confirmed that the efficiency and output power of the proposed Class-E PO have small sensitivities to the variations in the component values; therefore, we call the proposed circuit a self-tuned Class-E PO.**

***Index Terms*—Circuit tuning, feedback, power amplifier (PA), power oscillator (PO), RC circuits, self-oscillating, self-tuned.**

I. Introduction

CLASS-E power amplifiers (PAs) are widely used in numerous applications, including dc–ac inverters, dc–dc converters, wireless communication, and wireless power transfer systems. Fig. 1 shows the basic topology of a Class-E PA, which was first introduced by the Sokals in 1975 [1]. This circuit consists of a single transistor M_1, an RF choke L_1, a load resistor R_L, and a load network consisting of C_1, C_2, and L_2. An input clock signal periodically turns M_1 ON and OFF at the clock frequency, which is also called the switching frequency. The inductance of L_1 is usually very large at the switching frequency such that it behaves like a constant dc current source. The load network filters out the second- and higher-order harmonics of the drain signal and delivers a near sinusoidal waveform to R_L.

Class-E PAs, if tuned properly, can achieve efficiencies in the range of 80%–100% [2]. In a nominally tuned Class-E PA, the values of the load network components are chosen such that the drain voltage of the transistor satisfies the zero-voltage switching (ZVS) and zero-voltage-derivative switching (ZVDS) conditions. Only one switching frequency exists that can maintain the Class-E PA at its nominal operating conditions. This frequency, so-called Class-E frequency or f_e, is between the series and parallel resonance frequencies of the load network given by [3]

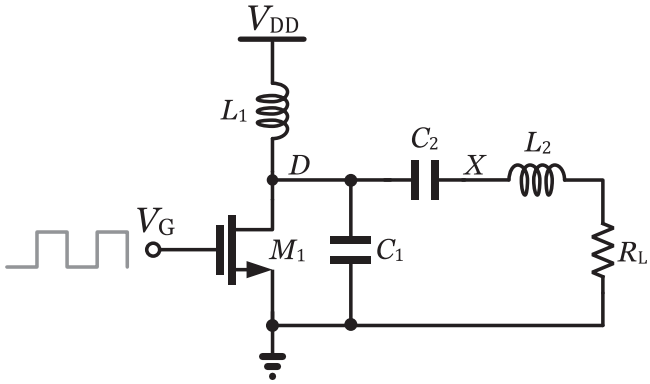

Fig. 1. Basic structure of a Class-E PA.

$$f_{o1} = \frac{1}{2\pi\sqrt{L_2 C_2}} \tag{1}$$

$$f_{o2} = \frac{1}{2\pi\sqrt{L_2 \frac{C_1 C_2}{C_1 + C_2}}}. \tag{2}$$

If a mismatch exists between the switching frequency and the Class-E frequency f_e, the power loss in the transistor could considerably increase and degrade the efficiency. If the loaded q-factor of the PA, Q_L, is large, the power loss in the transistor could be substantial, potentially damaging the transistor. Even if the switching frequency is well-controlled with a crystal oscillator, the mismatch between the switching frequency and f_e can quite naturally arise from the changes in the component values. For example, the inductance of L_2 can change due to the coil warping, or the proximity of L_2 to other strong electromagnetic fields or ferro-magnetic objects [4]. Therefore, it is crucial to keep the PA in, or close to, its optimal operating condition.

To resolve the aforementioned issue, a solution is to adjust the switching frequency based on a feedback obtained from a signal in the load network. Several circuits have been proposed in the literature to implement this idea [4]–[16]. These circuits actually convert the Class-E PA to a self-oscillating PA, or as is named in [16], a Class-E power oscillator (PO). Most of the proposed self-oscillating Class-E PAs are for wireless power transfer applications and require complicated frequency tuning circuits. The circuit proposed in [16] is a general-purpose PO,

Manuscript received May 21, 2018; accepted June 29, 2018. Date of publication July 24, 2018; date of current version March 29, 2019. Recommended for publication by Associate Editor M. E. Andersen. *(Corresponding author: Mohammad Mahdi Ahmadi.)*

The authors are with the Department of Biomedical Engineering, Amirkabir University of Technology, Tehran 15875-4413, Iran (e-mail:

for which several design procedures have been proposed in the literature [17]–[21].

In this paper, we propose a new general-purpose Class-E PO, which has a simpler feedback network than the conventional Class-E PO proposed in [16]. The proposed feedback network consists of only resistors and a capacitor, and since the feedback network does not have a self-resonance frequency, both the switching frequency and the Class-E frequency are defined by the inductor L_2 and capacitors C_1 and C_2 in the load network; therefore, these frequencies track each other better, and as a result, the output power and the efficiency of the proposed PO show negligible sensitivities to the changes in the component values. This important feature allows for larger tolerances and variation windows for the load network components. We also present a fully analytical design procedure for the proposed circuit. The procedure allows an engineer to quickly calculate the component values using a hand-held calculator or computer software, such as MATLAB.

II. Working Principle

In this section, we explain the working principle of our proposed Class-E PO using the same circuit specifications described in [17]. In Section III, we present an analytical design procedure for the proposed circuit.

The specifications of the Class-E PO described in this paper, taken from [17], are as follows.

1) The output power delivered to the load $P_o = 1\,\text{W}$.
2) The supply voltage $V_{DD} = 4.5\,\text{V}$.
3) The operating frequency $f_e = 800\,\text{kHz}$.
4) The load resistance $R_o = 50\,\Omega$.
5) The loaded q-factor $Q_L = 13$.

Assuming a large value for L_1 and a duty ratio of $D = 0.5$ for the gate drive signal V_G, we can use the following formulas, described by Sokal in [2], to find the values of C_1, C_2, L_2, and R_L for the circuit shown in Fig. 1:

$$R_L = 0.5768\frac{V_{DD}^2}{P_O}\left(1.001245 - \frac{0.452}{Q_L} - \frac{0.4}{Q_L^2}\right) = 11.26\,\Omega \tag{3}$$

$$L_2 = \frac{Q_L R_L}{\omega_e} = 29.12\,\mu\text{H} \tag{4}$$

$$C_1 = \frac{1}{\omega_e R_L}\left(\frac{8}{\pi(\pi^2+4)}\left(0.999 + \frac{0.914}{Q_L} - \frac{1.03}{Q_L^2}\right) + \frac{0.6}{Q_L(L_1/L_2)}\right) = 3.45\,\text{nF} \tag{5}$$

$$C_2 = \frac{1}{\omega_e R_L}\left(\left(\frac{1}{Q_L - 0.105}\right)\left(1.001 + \frac{1.015}{Q_L - 1.788}\right) - \frac{0.2}{Q_L(L_1/L_2)}\right) = 1.49\,\text{nF} \tag{6}$$

where $\omega_e = 2\pi f_e$ is the nominal Class-E frequency in terms of radians per second. The calculated value for R_L using (3) is the optimal value resulting in nominal Class-E operation for $P_o = 1\,\text{W}$, $V_{DD} = 4.5\,\text{V}$, and $Q_L = 13$. If this value is different from the actual load resistance R_o, we can use well-known matching circuits [3], [22]–[23] to transform R_o to R_L. As a result, for the sake of simplicity, we shall keep $R_L = 11.26\,\Omega$ in this section. In Section III, we briefly describe a couple of matching circuits that can convert $R_o = 50\,\Omega$ to $R_L = 11.26\,\Omega$.

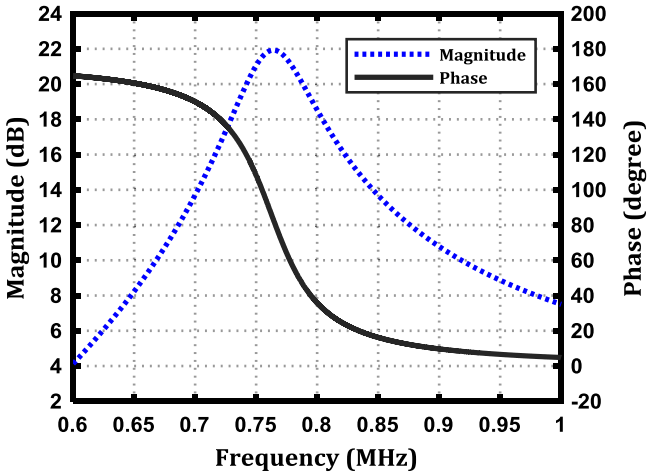

Fig. 2. Transfer function $V_X(s)/V_D(s)$ of the $C_2 - L_2 - R_L$ branch of the circuit shown in Fig. 1.

It is shown in [3] and [24] that, if a Class-E PA is nominally tuned, the phase shift between the fundamental components of the gate signal V_G and the drain signal V_D equals +196.6°. Because V_D lags V_G, in this paper, we prefer to say that the phase shift from the gate to the drain of M_1 is –163.4°. The series $C_2 - L_2 - R_L$ branch is a narrow-band filter that filters out the second- and higher-order harmonics of V_D, and delivers a near sinusoidal waveform to R_L.

Fig. 2 shows an ac simulation on the $C_2 - L_2 - R_L$ branch of the Class-E PA shown in Fig. 1. The phase shift from D to the resonance node X, starts from +90° at dc (not shown in the figure) and moves toward +180° before reaching the resonance frequency of the $C_2 - L_2 - R_L$ branch, which is $f_{o1} = 764\,\text{kHz}$. As it is clear in Fig. 2, in the vicinity of f_{o1}, the phase shift moves from around +180° to around 0°, reaching to 0° at infinity. For the example that we are dealing with, the phase shift is almost 83° at $f_{o1} = 764\,\text{kHz}$ and +36.5° at the Class-E frequency of $f_e = 800\,\text{kHz}$. Since the phase shift from G to D is –163.4°, the phase shift from G to X is about –126.9°.

In order to convert the Class-E PA to a Class-E PO, we can add a feedback network that returns a portion of the signal at node X to node G with an appropriate phase shift and amplitude. In order to satisfy the oscillation criteria, the phase shift in the entire oscillation loop should be –360°; therefore, the feedback network must provide a phase shift of $-233.1^\circ(= -360^\circ + 126.9^\circ)$. A passive feedback network that can provide such amount of phase shift is fairly complicated and needs at least three frequency poles in its transfer function.

If we put L_2 at the left of C_2, as it is shown in Fig. 3, the requirement for the feedback network is facilitated. Fig. 4 shows an ac simulation on the $L_2 - C_2 - R_L$ branch of the circuit shown in Fig. 3. In Fig. 3, the phase shift from D to X, starts from +0° at dc and around the resonance frequency of $f_{o1} = 764\,\text{kHz}$, it sharply drops to about –180°. It then goes back up to –90° at infinity (not shown in Fig. 4). For our example,

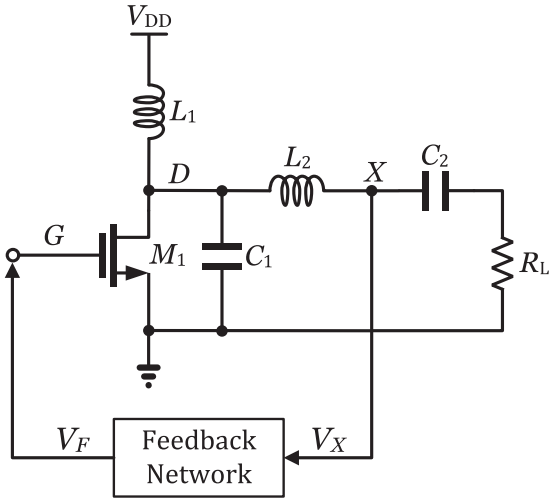

Fig. 3. Basic structure of a Class-E PO.

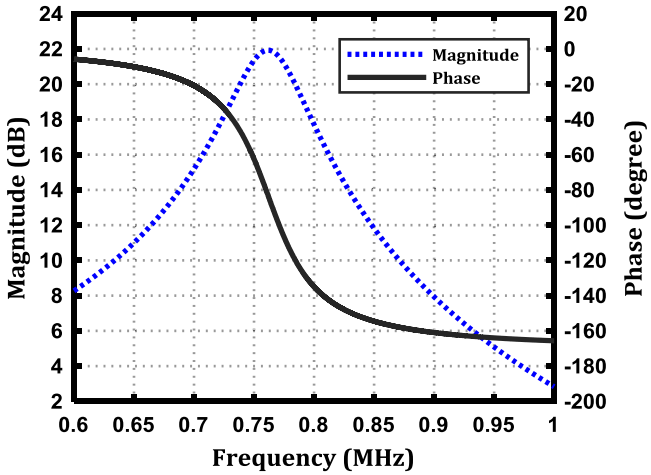

Fig. 4. Transfer function $V_X(s)/V_D(s)$ of the $L_2 - C_2 - R_L$ branch of the circuit shown in Fig. 3.

the phase shift is almost –83° at $f_{o1} = 764$ kHz and –134° at $f_e = 800$ kHz. In other words, since the phase shift from G to D is –163.4°, the phase shift from G to X is about –297.4°, which means that the feedback network must only provide a phase shift of about –62.6° to satisfy the oscillation criteria. Fortunately, this amount of phase shift can be easily obtained using a simple series RC circuit.

A simple RC network, as shown in Fig. 5(a), is sufficient to convert the Class-E PA to a Class-E PO. However, the signal amplitude at node X is often large and could damage M_1. Therefore, the feedback network, in addition to providing sufficient phase shift, should attenuate the signal. This can be achieved with the RC network shown in Fig. 5(b). Adding another resistor to the feedback network of Fig. 5(b), as is shown in Fig. 5(c), can provide enough flexibility to adjust the phase shift, the dc level, and the amplitude of the signal driving M_1. Adjusting the dc level of V_F helps defining the duty cycle of the gate drive signal.

Fig. 6 shows a complete circuit implementation of the proposed Class-E PO. The gate driver is not necessarily part of the circuit and can be removed for many designs. In order for

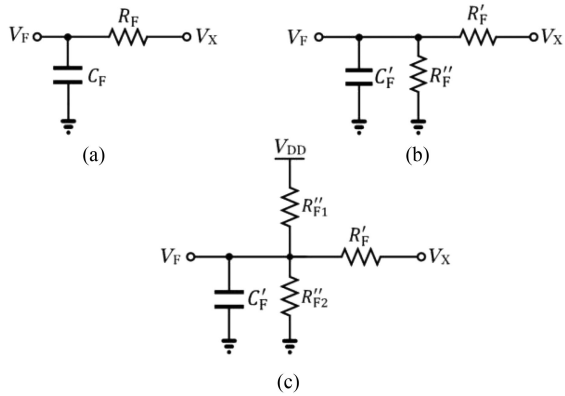

Fig. 5. Three RC circuits that can be used as the feedback network of the Class-E PO shown in Fig. 3. (a) Simple RC circuit that can only satisfy the phase shift requirement on the feedback network. (b) RC circuit that can satisfy the phase shift and the voltage amplitude requirements. (c) RC circuit that can satisfy phase shift, voltage amplitude, and dc level requirements.

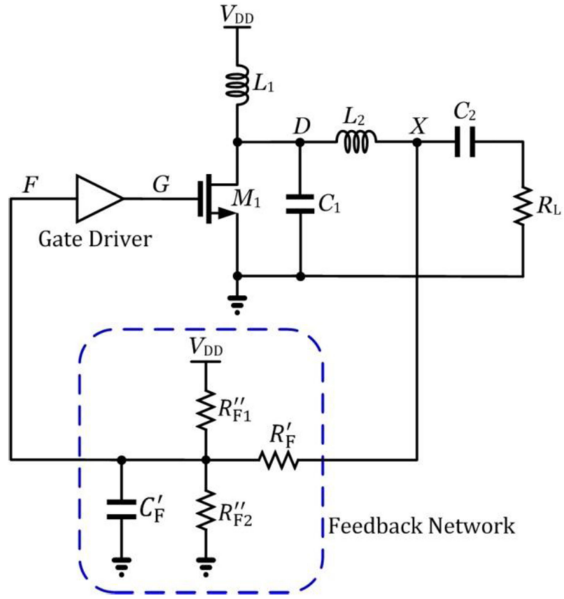

Fig. 6. Circuit implementation of our proposed Class-E PO.

the Class-E PO to work properly, a couple of issues should be taken care of: first, the loading effect of M_1 (or the gate driver) on the feedback network, and second, the loading effect of the feedback network on the load network.

If the gate capacitance of M_1 is less than the calculated capacitance for the feedback network, i.e., C_F in Fig. 5(a), or C'_F in Figs. 5(b) and (c), we can easily account for that by subtracting the value of the gate capacitance from the calculated value for C_F (or C'_F). However, if the gate capacitance of M_1 is larger than the calculated C_F, we can use a gate driver to minimize the loading effect, and then, account for the input capacitance and delay of the gate driver while calculating the phase shift of the feedback network. In either case, using a gate driver is beneficial because, first it buffers the nonlinear gate capacitance of M_1, which is difficult to model and account for in the calculations, and second, it converts the sinusoidal waveform outputted from the feedback network to a pulsatile waveform and minimizes the transistor loss during the switching times.

To account for the loading effect of the feedback network on the load network, we can model the feedback network with a parallel RC section placed between the node X and ground. At the same time, we can convert the series $C_2 - R_L$ branch to its equivalent parallel circuit. We can then account for the loading effect of the feedback network on the load network while choosing the values of R_L and C_2. This procedure is more clearly explained in Section III.

III. Design Procedure

A. Design Procedure With Ideal Circuit Components

In this section, we present the design procedure of the circuit shown in Fig. 6 for the case that all the circuit components are ideal, i.e., we assume that the transistor is an ideal switch and the rest of circuit components do not have any parasitic element. In Section III-E, we incorporate the effects of component imperfections in the design procedure.

In order to find the phase shift that the feedback network has to provide, first we need to find the phase shift in the load network from node D to node X. Consider the Class-E PO shown in Fig. 3. The voltage transfer function from node D to node X is given by

$$H(s) = \frac{V_X(s)}{V_D(s)} = \frac{R_L C_2 s + 1}{L_2 C_2 s^2 + R_L C_2 s + 1}. \quad (7)$$

Let us define the phase of $H(s)$ at the Class-E frequency f_e by φ_X. We can calculate φ_X by substituting $j\omega$ for s in (7) and then using

$$\begin{aligned}\varphi_X &= \tan^{-1}\left(R_L C_2 \omega_e\right) - \tan^{-1}\left(\frac{R_L C_2 \omega_e}{1 - L_2 C_2 {\omega_e}^2}\right) \\ &= \tan^{-1}\left(R_L C_2 \omega_e\right) - \tan^{-1}\left(\frac{1}{\frac{1}{R_L C_2 \omega_e} - \frac{L_2 \omega_e}{R_L}}\right). \quad (8)\end{aligned}$$

We define $Q_{C2} = 1/R_L C_2 \omega_e$. Since f_e is larger than the resonance frequency of the series $C_2 - L_2$ branch, i.e., f_{o1}, the series $C_2 - L_2$ branch is inductive at f_e and Q_{C2} is smaller than Q_L. Hence, $Q_{C2} - Q_L$ is negative. From the circuit example that we described in Section II, we know that we should end up having φ_X in the third quadrant of the unit circle; therefore, φ_X can be obtained by

$$\varphi_X = \tan^{-1}\left(\frac{1}{Q_{C2}}\right) + \tan^{-1}\left(\frac{1}{Q_L - Q_{C2}}\right) - 180^\circ. \quad (9)$$

We know that the phase shift in the whole network should be $-360°$. We also know that, in a tuned Class-E PA with $D = 0.5$, the phase shift from node G to node D is –163.4° [3], [24]. Therefore, after calculating φ_X using (9), we can obtain the phase shift that the feedback network has to provide, defined here by φ_F, using

$$\varphi_F = -360 - \varphi_X - (-163.4). \quad (10)$$

Since (3) to (6) are not 100% accurate [2], if the values of R_L, L_2, and C_2 that are directly resulted from (3), (4), and (6) are used in (8) to (10), we could see large errors in the calculated φ_F. Therefore, we suggest simulating the Class-E PA using the values calculated from (3) to (6) and fine-tuning the PA to find the optimum values for C_1, C_2, L_2, and R_L, and then using (8) to (10) to find φ_F. Table I provides φ_F for some typical values of Q_L and L_1/L_2.

TABLE I
Required Phase Shift, φ_F, in the Feedback Network for Different Q_L Values and L_1/L_2 Ratios

Q_L \ L_1/L_2	100	20	10	5	3	1
5	-69.6	-70.1	-70.6	-71.0	-72.1	-77.4
10	-60.2	-62.9	-63.1	-63.5	-65.8	-66.4
20	-59.8	-60.3	-60.3	-60.5	-60.6	-62.9
50	-57.8	-57.9	-58.1	-58.4	-58.7	-60.3
100	-55.9	-56.6	-56.6	-56.6	-57.9	-58.3

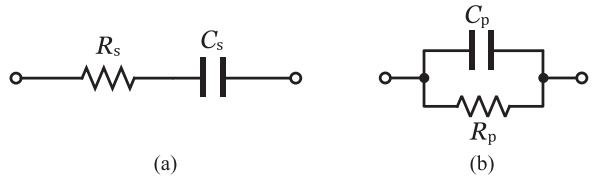

Fig. 7. (a) Series RC network. (b) Parallel RC network.

As shown in Table I, the phase shift that the feedback network has to provide, i.e., φ_F, ranges from –55.9° to –77.4°. Therefore, a single-pole *RC* network can easily satisfy the phase shift requirement. Now we can develop a design procedure for the feedback network.

Before moving forward with the design procedure, we review the series-to-parallel conversion of an RC circuit as we use it multiple times in the design procedure. The theory of impedance transformation states that the series $R_s - C_s$ branch shown in Fig. 7(a) is equivalent to the parallel $R_p - C_p$ section shown in Fig. 7(b) around the operating frequency of ω, if the following relationships hold [22]:

$$C_p = C_s \times \frac{Q^2}{1 + Q^2} \quad (11)$$

$$R_p = R_s \times \left(1 + Q^2\right) \quad (12)$$

where Q represents the q-factor of the parallel and series circuits at the operating frequency of ω

$$Q = \frac{1}{R_s C_s \omega} = R_p C_p \omega. \quad (13)$$

Using this technique, we can simplify the feedback networks shown in Fig. 5 and convert them to a parallel RC section, $R_{Fp} - C_{Fp}$, as is shown in Fig. 8. The series $C_2 - R_L$ branch in Fig. 3 can also be converted to the parallel $C_{2p} - R_{Lp}$ section, as is shown in Fig. 8. We can then subtract the admittance of the $R_{Fp} - C_{Fp}$ section from the admittance of the $C_{2p} - R_{Lp}$ section and, from the remaining $R'_{Lp} - C'_{2p}$ section, construct the load and matching networks.

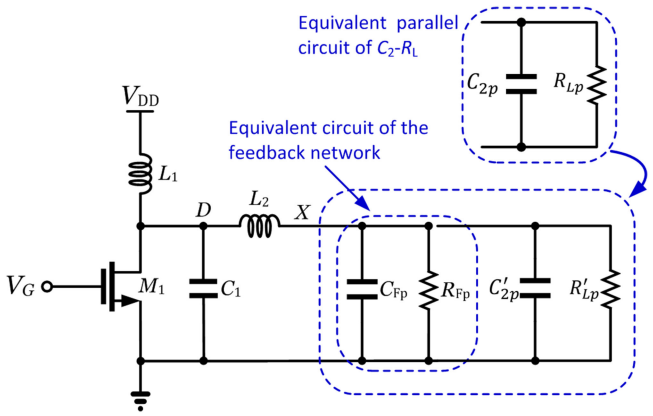

Fig. 8. Equivalent parallel *RC* circuit of the feedback network and $C_2 - R_L$ branch seen by the Class-E PO.

In Fig. 8, we can see that R_{Fp} is in parallel with R'_{Lp}. Therefore, a portion of the power, which was supposed to be delivered to the output load, is now wasted in R_{Fp}, i.e., the feedback network. Therefore, we should account for this power loss at the onset of our design procedure. To minimize the power loss in the feedback network, we should choose R_{Fp} considerably larger than R'_{Lp}. Let us define K_R with

$$K_R = \frac{R_{Fp}}{R'_{Lp}}. \tag{14}$$

If, for example, we choose $K_R = 10$, almost 10%, or to be precise, $100/(K_R + 1) = 9.1\%$, of the drawn power from V_{DD} will be dissipated in the feedback network. Obviously, the larger the ratio of R_{Fp} over R'_{Lp} we choose, the larger efficiency we can obtain; however, as we will see later in this section, increasing the value of R_{Fp} will reduce the calculated value for the feedback network capacitor (C_F or C'_F shown in Fig. 5). Therefore, we should choose a value for R_{Fp} that will not result in a prohibitively small values for C_F or C'_F.

Assuming that we are acquiesced with 5% power loss in the feedback network (or $K_R = 20$), we start the design of the basic Class-E PA with 5% more output power, i.e., $P_o = 1.05$ W. We also assume that $D = 0.5$. Since we do not know the value of L_1 *a priori*, we assume a reasonably large value for the ratio of L_1/L_2, e.g., 40. Using (3) to (6), we obtain the values of R_L, C_1, C_2, and L_2 as 10.73 Ω, 3.65 nF, 1.56 nF, and 27.74 μH, respectively. Then, we choose L_1 to be 900 μH to make the ratio of L_1 over L_2 fairly large. We then construct a Class-E PA and fine-tune the values of C_1 and C_2 using the procedure explained in [2]. During the fine-tuning process, we realized that the value of C_2 should be adjusted from 1.56 to 1.57 nF for the circuit to be nominally tuned.

Using (9) and (10), or using Table I, we find φ_F to be –61.6°. Using series-to-parallel conversion, we then convert the series $C_2 - R_L$ branch to the parallel RC branch consisting of $R_{Lp} = 1.51\,\text{k}\Omega$ and $C_{2p} = 1.558$ nF. Looking at Fig. 8, we realize that $R_{Lp} = R'_{Lp}||R_{Fp}$ and $C_{2p} = C'_{2p}||C_{Fp}$. We choose to have only 5% power loss in the feedback network; therefore, we divide R_{Lp} into two parallel resistors such that R_{Fp} is 20 times of R'_{Lp}. This results in $R_{Fp} = (K_R + 1)R_{Lp} = 31.71\,\text{k}\Omega$ and $R'_{Lp} = ((K_R + 1)/K_R)R_{Lp} = 1.59\,\text{k}\Omega$.

In order to construct the feedback network, we should convert the parallel $R_{Fp} - C_{Fp}$ section to its equivalent series branch $R_F - C_F$, which in fact, would construct the feedback network shown in Fig. 5(a).

We know that, in order for the Class-E PO to be nominally tuned, the phase shift in the series $R_F - C_F$ branch should be equal to φ_F. The transfer function of the series $R_F - C_F$ branch, shown in Fig. 5(a), can be expressed by

$$H_F\,(j\omega) = \frac{V_F\,(j\omega)}{V_X\,(j\omega)} = \frac{1}{1 + R_F C_F j\omega}. \tag{15}$$

The phase of $H_F(j\omega)$ at $\omega = \omega_e$ is

$$\varphi_F = -\tan^{-1}\left(R_F C_F \omega_e\right). \tag{16}$$

Let us define the q-factor of the series $R_F - C_F$ circuit by Q_F. Q_F is also the q-factor of the parallel $R_{Fp} - C_{Fp}$ section; therefore, we have

$$Q_F = \frac{1}{R_F C_F \omega_e} = R_{Fp} C_{Fp} \omega_e. \tag{17}$$

Combining (16) and (17), we can calculate Q_F using

$$Q_F = \frac{1}{R_F C_F \omega_e} = -\frac{1}{\tan\left(\varphi_F\right)} = 0.54. \tag{18}$$

Substituting (18) in (17), we can calculate the value of C_{Fp} as follows:

$$C_{Fp} = \frac{-1}{\tan\left(\varphi_F\right) R_{Fp} \omega_e} = 3.4\ \text{pF}. \tag{19}$$

We can then calculate the value of C'_{2p}, shown in Fig. 8, using

$$C'_{2p} = C_{2p} - C_{Fp} = 1558 - 3.4 \cong 1555\,\text{pF}. \tag{20}$$

To construct the simplest feedback network, which is the one shown in Fig. 5(a), we can simply convert the parallel $R_{Fp} - C_{Fp}$ section to its equivalent series circuit. R_F can be calculated using

$$R_F = \frac{R_{Fp}}{1 + Q_F^2} = 24.6\,\text{k}\Omega. \tag{21}$$

Using (18) and considering that $1 + \tan^{-2}(\varphi_F) = 1/\sin^2(\varphi_F)$, we can simplify (21) to

$$R_F = R_{Fp} \sin^2\left(\varphi_F\right). \tag{22}$$

Considering (18), the value of C_F can now be calculated as

$$C_F = \frac{-\tan(\varphi_F)}{\omega_e R_F} = 15\,\text{pF}. \tag{23}$$

Combining (22) and (23), C_F can also be directly calculated from R_{Fp} using

$$C_F = \frac{-2}{\omega_e R_{Fp} \sin\left(2\varphi_F\right)} = 15\,\text{pF}. \tag{24}$$

Looking at (24), we realize that if we increase the value of R_{Fp}, the value of C_F will decrease. This means that, if we increase the ratio of R_{Fp} over R'_{Lp} to minimize the power loss in the feedback network, C_F decreases and we might end up to a situation that C_F becomes smaller than the gate capacitance of M_1 in which case, the feedback network of Fig. 5(a)

is not realizable, unless we use a gate driver to buffer the gate capacitance.

If one wants to use the feedback network shown in Fig. 5(a) to implement a Class-E PO, the design of the feedback network is now complete. However, as explained in Section II, the feedback network of Fig. 5(a) does not provide any flexibility to adjust the amplitude or the dc level of the gate drive signal. Therefore, we can resort to the networks shown in Fig. 5(b) or 5(c). We first explain the design procedure for the feedback network shown in Fig. 5(b); from there, we explain the procedure for the network shown in Fig. 5(c).

The feedback network of Fig. 5(b) allows us to adjust either the amplitude, or the dc level of the gate drive signal, but not both. We design it for the case that we want to adjust the amplitude of the gate drive signal.

Let V_X and V_F be signal amplitudes at input and output nodes of the feedback network, respectively. We usually choose V_F to be, at least, half the supply voltage; however, to achieve very small MOSFET on-resistance, larger values are preferred. Let us choose $V_F = 3.0\,\mathrm{V}$. As it is proved in Appendix A, V_X can be calculated using

$$V_X = \sqrt{\frac{2P_O}{R_L}} \times \sqrt{R_L^2 + \left(\frac{1}{C_2\omega_e}\right)^2} = 56.51\,\mathrm{V}. \tag{25}$$

Let us assume that

$$R'_F = \alpha R''_F \tag{26}$$

where α is the ratio of R'_F over R''_F in Fig. 5(b). From (46), proved in Appendix A, we can calculate the value of α using

$$\alpha = \frac{V_X}{V_F}\cos(\varphi_F) - 1 = 7.96. \tag{27}$$

The input impedance, Z_F, of the feedback network of Fig. 5(b) can be calculated using

$$Z_F = R'_F + \frac{R''_F}{1 + R''_F C'_F \omega j} = \frac{R'_F + R''_F + R'_F R''_F C'_F \omega j}{1 + R''_F C'_F \omega j} \tag{28}$$

and the input admittance Y_F can be expressed by

$$Y_F = \frac{1}{Z_F} = \frac{1 + R''_F C'_F \omega j}{R'_F + R''_F + R'_F R''_F C'_F \omega j}. \tag{29}$$

Substituting R'_F from (26) in (29), we can calculate the real part of Y_F as

$$\mathrm{Re}\{Y_F\} = \frac{1}{R''_F} \times \frac{\alpha + \sin^2(\varphi_F)}{\alpha(\alpha+1)}. \tag{30}$$

The real part of Y_F represents a conductance which actually should be equal to the inverse of R_{Fp}. In other words, we have

$$\frac{1}{R_{Fp}} = \frac{1}{R''_F} \times \frac{\alpha + \sin^2(\varphi_F)}{\alpha(\alpha+1)}. \tag{31}$$

Therefore, we can calculate the value of R''_F from

$$R''_F = R_{Fp} \times \frac{\alpha + \sin^2(\varphi_F)}{\alpha(\alpha+1)} = 3.88\ \mathrm{k\Omega}. \tag{32}$$

Using (26), we can calculate the value of R'_F to be 30.9 kΩ.

To calculate the value of C'_F, we consider that both feedback networks of Fig. 5(a) and 5(b) should provide the same amount of phase shift. Hence, the RC time-constant of both networks should be the same, or

$$R_F C_F = (R'_F || R''_F)\ C'_F \rightarrow R_F C_F \omega_e = \left(\frac{\alpha}{\alpha+1}\right) R''_F C'_F \omega_e. \tag{33}$$

Therefore, we can find the value of C'_F as

$$C'_F = \frac{R_F C_F \omega_e}{(R'_F || R''_F)\omega_e} = \frac{-\tan(\varphi_F)}{(R'_F || R''_F)\omega_e} = 107\,\mathrm{pF}. \tag{34}$$

The design of the feedback network of Fig. 5(b) is now complete. We should only calculate the equivalent parallel capacitance of this feedback network, i.e., C_{Fp}, shown in Fig. 8, from which, we can take into account the capacitive loading of the feedback network on the load network. It is proved in Appendix B that C_{Fp} can be calculated using

$$C_{Fp} = \frac{Q_{F2}^2}{1 + Q_{F2}^2} \times \frac{\alpha^2 + (\alpha+1)^2 \tan^2(\varphi_F)}{(\alpha+1)^2 \tan^2(\varphi_F)} C'_F \tag{35}$$

where Q_{F2} is defined in Appendix B and is proved that can be calculated using

$$Q_{F2} = -\frac{\tan(\varphi_F)}{\alpha + (1+\alpha)\tan^2(\varphi_F)}. \tag{36}$$

Using (35), C_{Fp} is calculated to be 0.3 pF, and using (20), C'_{2p} is calculated to be 1558 pF.

If we want to define both the amplitude and the dc level of the gate drive signal, we should choose the feedback network shown in Fig. 5(c). We can find the values of R''_{F1} and R''_{F2} in Fig. 5(c) using the following equations:

$$R''_{F1} || R''_{F2} = R''_F \tag{37}$$

$$V_{F,\mathrm{dc}} = \frac{R''_{F2}}{R''_{F2} + (R''_{F1} || R'_F)} \times V_{DD} \tag{38}$$

where $V_{F,\mathrm{dc}}$ is the dc level of the gate drive signal.

We usually set $V_{F,\mathrm{dc}}$ slightly larger than the threshold voltage of M_1 to achieve a duty cycle of 50% and also initiate the oscillation after the supply is turned ON. As it will be explained in Section IV, because the gate capacitance of M_1 is nonlinear and voltage dependent, it is almost impossible to achieve a duty cycle of 50% without using a gate driver. Therefore, we recommend using a gate driver for M_1 and setting $V_{F,\mathrm{dc}}$ larger than the switching threshold voltage of the gate drive. If we assume that $V_{F,\mathrm{dc}}$ should be 2.25 V, or half the supply voltage, the values of R''_{F1} and R''_{F2} are calculated to be 8.9 and 6.9 kΩ, respectively.

B. Load Impedance Matching

Most often, the calculated value for R_L for nominal Class-E operation is different from the actual load resistance R_o. In these cases, we can use impedance matching techniques to make the actual resistance seen by the Class-E load network equal to R_L. For example, if $R_o > R_L$, or in other words, $R_o < R'_{Lp}$, we can use the capacitive transformer circuit shown in Fig. 9(d), or the

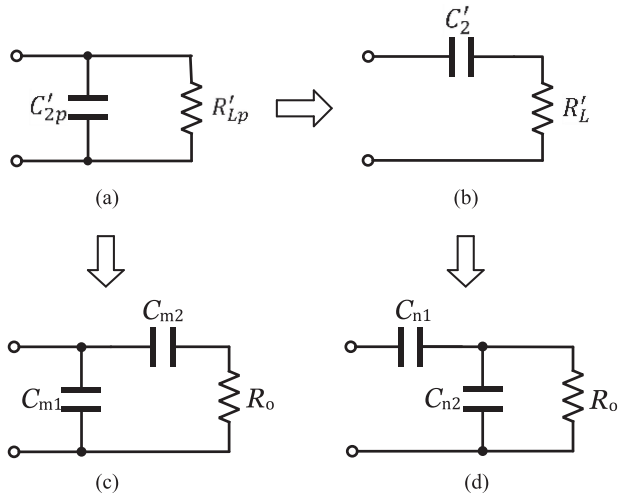

Fig. 9. Impedance transformation procedures. (a) Parallel $C'_{2p} - R'_{Lp}$ section. (b) Series equivalent circuit of the parallel $C'_{2p} - R'_{Lp}$ section shown in (a). (c) Using an L-match circuit to convert $R_o = 50\,\Omega$ to $R'_{Lp} = 1.59\,\text{k}\Omega$. (d) Using capacitive transformation to convert $R_o = 50\,\Omega$ to $R'_L = 10.2\,\Omega$.

TABLE II
VALUES CALCULATED AND SIMULATED FOR THE PROPOSED CLASS-E PO WITH IDEAL CIRCUIT COMPONENTS

Component	L_1 (mH)	L_2 (μH)	C_1 (nF)	C'_2 (nF)	R'_L (Ω)	R'_{F1} $(k\Omega)$	R''_{F1} $(k\Omega)$	R''_{F2} $(k\Omega)$	C'_F (pF)
Calculated	0.9	27.74	3.65	1.568	10.2	30.9	8.9	6.9	107
Simulated	0.9	27.74	3.56	1.568	10.2	30.9	8.9	6.9	107

L-match circuit shown in Fig. 9(c) to arrive to the actual load resistance $R_o = 50\ \Omega$.

For now, we just convert the parallel $C'_{2p} - R'_{Lp}$ section to its equivalent series $C'_2 - R'_L$ branch to make our designed Class-E PO similar to a standard Class-E PA. The final calculated values for the Class-E PO with feedback circuit shown in Fig. 5(c) are given in Table II.

C. Fine-Tuning the Class-E PO

In Section III-A, even though we assumed that all the components are ideal, the values calculated by the formulas provided in that section might result in slightly suboptimal waveforms. A couple of issues contribute to this issue. First of all, (3) to (6) are not completely accurate. Second and more importantly, (3) to (6) are for the duty ratio of $D = 0.5$. We set $V_{F,\text{dc}}$ slightly larger than the threshold voltage of the transistor (or the gate driver) to obtain a duty ratio of 0.5, but because the q-factor of the load network is not infinity, the voltage signal at the resonance node X and at the output node of the feedback network are not ideal sinusoids and have harmonics; therefore, the positive and negative half-cycles of the gate drive signal does not have exactly the same duration. As a consequence, the values of the components should be slightly adjusted to bring the drain waveform to its nominal Class-E condition.

To provide insight on how the drain waveform of the PO changes with the variation in the component values, we have first simulated the Class-E PO designed in Section III-A and fine-tuned the values of the components. The final values, resulted from simulation, are given in Table II. As it is clear, only the value of C_1 has to change by less than 2.5% to make the PO fully tuned. Then, we simulated the designed PO with $\pm 10\%$ changes in each of the major components affecting the circuit performance, and plotted the drain waveforms. For example, Fig. 10(a) shows the drain waveforms for the cases that C_1 is nominal ($\Delta C_1 = 0$), 10% larger ($\Delta C_1 = +0.1C_1$), and 10% smaller ($\Delta C_1 = -0.1C_1$). We have increased and decreased R''_{F1} and R''_{F2} together and with the same proportion in order not to change the duty cycle of the gate drive signal.

Looking at the waveforms shown in Fig. 10, we can make the following conclusions.

1) L_2 has the largest effect on the frequency of operation [shown in Fig. 10(c)], and in fact, $f_e \propto L_2^{-0.5}$. In addition, increasing L_2 moves the trough, i.e., the zero-slope point, of the waveform downwards and to the right.
2) The effect of C_2, shown in Fig. 10(b), on the frequency is almost as large as the effect of L_2. Increasing C_2 moves the trough of the waveform downwards and to the right.
3) Increasing C_1, as is shown in Fig. 10(a), moves the trough of the waveform upwards and to the right. Increasing C_1 slightly reduces f_e.
4) Increasing R_L, as is shown in Fig. 10(d), moves the trough of the waveform upwards.
5) Increasing C'_F, as is shown in Fig. 10(e), slightly moves the trough of the waveform upwards and to the left.
6) Similarly to increasing C'_F, increasing R''_{F1} and R''_{F2} together and with the same proportion, as is shown in Fig. 10(f), moves the trough of the waveform upwards and to the left.

Since we do not usually want to change the oscillation frequency or the output power, we recommend fine-tuning the Class-E PO by adjusting the values C_1 and C'_F.

D. Comparison With a Standard Class-E PA

To compare the effects of component variations on the output power, efficiency, and drain waveform of the proposed Class-E PO with those of a standard Class-E PA designed for the same specifications, we designed a Class-E PA for the same specifications listed in Section II. The values of C_1, C_2, L_2, and R_L obtained from (3) to (6) for the standard Class-E PA are 3.65 nF, 1.57 nF, 27.74 μH, and 10.73 Ω, respectively.

We simulated the proposed Class-E PO and the Class-E PA and measured the output power and efficiency of the circuits for nominal, 10% increased and 10% decreased values of each component. Fig. 11 illustrates the drain waveforms for each comparison. For instance, Fig. 11(a) shows the comparison when C_1 changes. Five drain waveforms are plotted in Fig. 11(a): the black curve is for the nominal case which is the same for both PA and PO; one waveform is for the case that C_1 of the PA increases by 10%, one is for the case that C_1 of the PO increases by 10%, one is for the case that C_1 of the PA decreases by 10%, and finally one is for the case that C_1 of the PO decreases by 10%. The percent changes of the output power and the efficiency of both PA and PO are written on each plot.

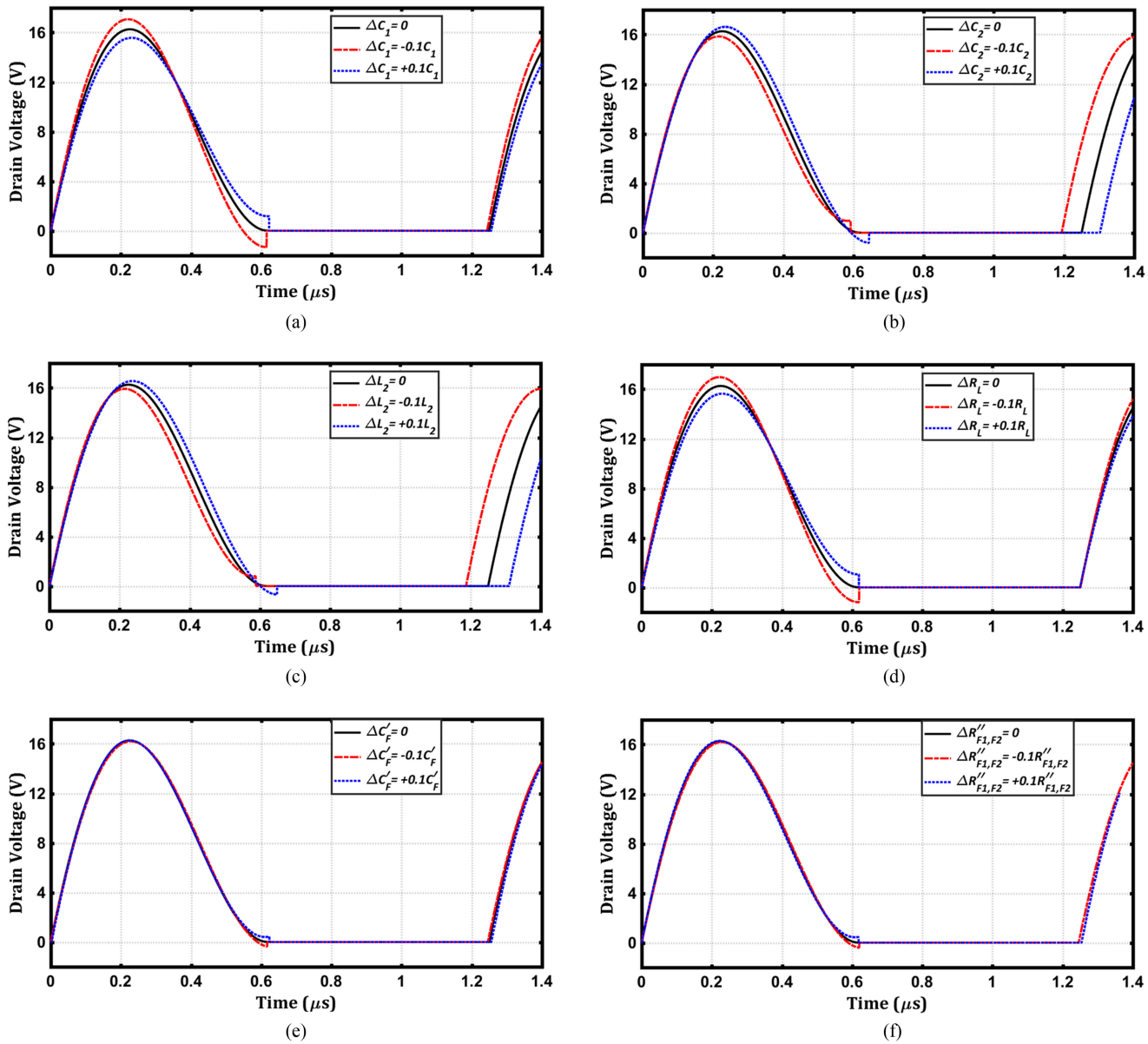

Fig. 10. Drain waveforms for $\pm 10\%$ variations in (a) C_1, (b) C_2, (c) L_2, (d) R_L, (e) C'_F, and (f) $R''_{F1,F2}$.

Looking at Fig. 11(a), we can observe that 10% variation in C_1 would cause almost 5% change in the output power in both PA and PO. The variation in the output power of the PO is about 1% larger than that of the PA. The percent changes in efficiency are less than 0.3% in all cases for both PO and PO. Therefore, we can conclude that the output power of the PA is slightly more robust against the variations in C_1.

Similar statements can be made for the variation in R_L. As is illustrated in Fig. 11(d), the output power of the PA has changed slightly less than that of the PO. The percent changes in efficiency are less than 1% for both PO and PA.

The merits of the proposed Class-E PO become clear when we compare the effects of variations in C_2 and L_2. The output power and the efficiency are most sensitive to the values of these two components. As is illustrated in Fig. 11(c), when L_2 increases by 10%, the output power of the PA decreases by 70% (or more than three times), while it decreases by only 6.3% in the PO. Also when L_2 decreases by 10%, the output power of the PA increases by 46%, while it increases by only 6.8% in the PO. Efficiency of the Class PA is also very sensitive to the values of C_2 and L_2, while the efficiency of the PO shows little sensitivity to the changes in all component values. For example, as illustrated in Fig. 11(b) when C_2 decreases by 10%, the efficiency of the PA decreases by about 23%, while it changes by less than 1% in the PO.

We should clarify that the percent variations that we have reported in this section are for the Class-E PO and PA designed with the specifications listed in Section II, and as the Q of the circuit increases, the PA becomes more sensitive to the component values and the advantages of the proposed Class-E PO become more pronounced.

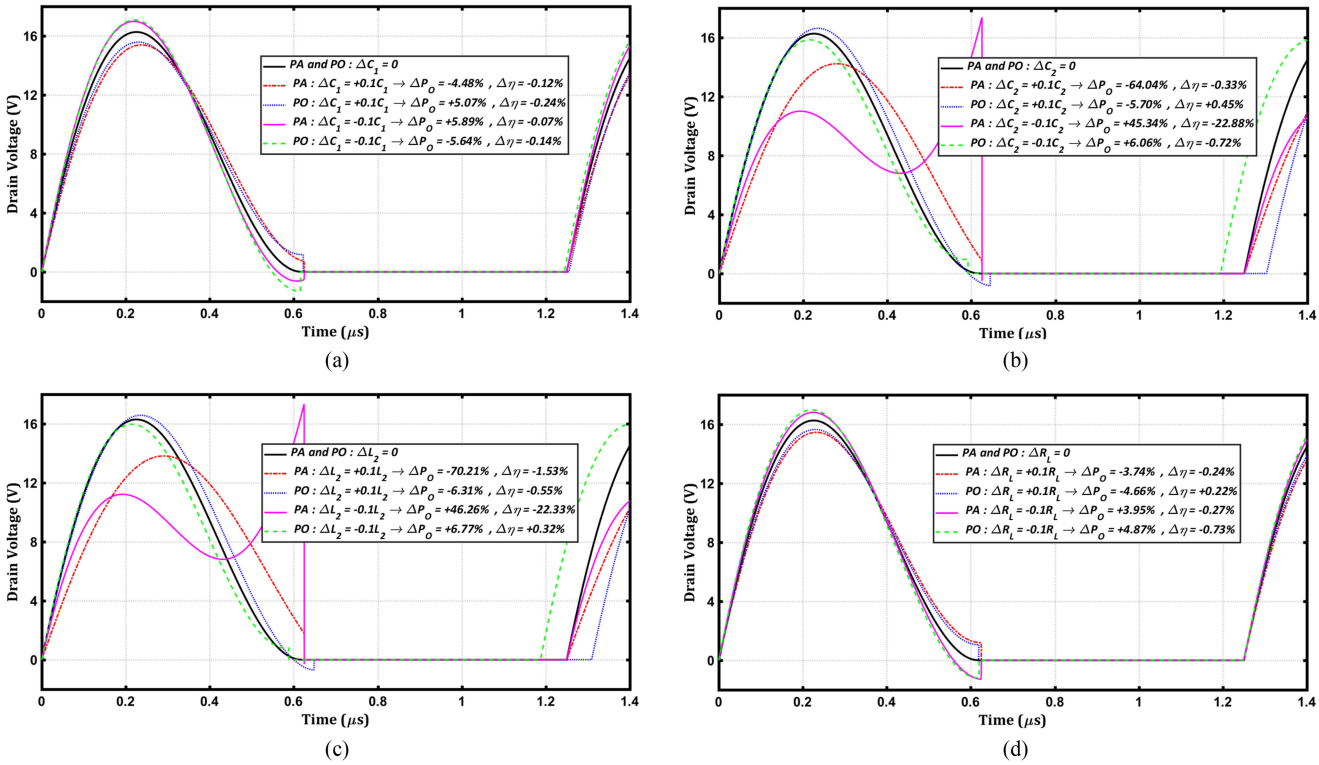

Fig. 11. Comparing the variations in the output power, efficiency, and drain waveform of the proposed Class-E PO with those of a Class-E PA designed for the same specifications. The values of (a) C_1, (b) C_2, (c) L_2, and (d) R_L have changed by $\pm 10\%$.

E. Design Procedure Considering the Imperfections in the Components

In Section III-A, we assumed that all the circuit components are ideal, and accordingly, we developed a design procedure for the proposed Class-E PA. In reality, no ideal circuit component exists and we should modify our design procedure to incorporate the effects of circuit imperfections that considerably degrade the efficiency and the signal phase shift as it travels through the feedback loop.

The main components of power loss include the transistor on-resistance, $R_{\rm on}$, the power loss for charging and discharging the transistor gate capacitance, the power consumption of the gate driver, the power loss in the ESR of L_1, L_2, and the capacitors, and finally the losses associated with the nonzero fall time of the drain current when the transistor is turning OFF. Another component of the power loss is the one dissipated in the feedback network; however, the ac power loss in the feedback network is already taken into account in the design procedure, and the dc power loss in the resistive divider of the feedback network is fairly small due to the large values of R'_F, R''_{F1}, and R''_{F2}.

The aforementioned losses are not known at the start of the design procedure. Therefore, we have to assume a realistic value for the efficiency η in the first round of calculations and then, we can choose the components, which considerably degrade the power efficiency, i.e., the transistor, the gate driver, and the inductors L_1 and L_2. In the second round of calculations, we know the approximate power loss in these components using either calculation, simulation or measurement and we can reiterate the design procedure and fine-tune the component values.

The transistor should be chosen based on the following criteria [2].

1) Its typical threshold voltage must be much less than V_{DD} so that the gate driver can easily turn it ON.
2) Its drain-source breakdown voltage, BV_{DSS}, should be higher than $3.56\,V_{DD}$.
3) Its $R_{\rm on}$ should be much smaller than R_L. $R_{\rm on}$ degrades the efficiency by about $(1.365\,R_{\rm on}/R_L) \times 100$ percent [2].
4) The turn-on transition time of the transistor should be less than 30% of the clock period and the turn-off should be less than 20% of the clock period [2].
5) The drain capacitance of the transistor should be less than the calculated C_1.
6) Its maximum allowed power dissipation should be more than the desired output power. When the Class-E operation of the circuit is established, the power dissipated in the transistor is much less than the output power; but, during the start-up, the circuit is not yet tuned and the power loss in the transistor can be high enough to damage the transistor.

Based on the criteria for the transistor, we chose FQT13n06 MOSFET manufactured by ON Semiconductor for our design example. FQT13n06 has a maximum drain capacitance of 120 pF, and a typical $R_{\rm on}$ of 0.1 Ω. Therefore, we expect

to have a degradation of about $1.3\%\,(=1.365\,R_{\rm on}/R_L\times 100)$ due to $R_{\rm on}$.

ESRs of L_1 and L_2 are other sources of power loss in the circuit. Since we have chosen the value of L_1 much larger than the value of L_2, the current in L_1 is fairly constant and its ac component is very small. Therefore, we can ignore the magnetic loss in L_1 and only consider the power loss due to the dc resistance of L_1. We have chosen an RF choke with an inductance of 900 μH and a dc resistance of 0.01 Ω. The dc resistance of L_1 introduces a power loss of about 0.5 mW and an efficiency degradation of about 0.05%, which is negligible.

In contrast to the current of L_1, the current in L_2 is a high-frequency ac current. At high frequencies, the effective ESR of L_2, i.e., R_{L2}, increases by a large extent due to skin effect and magnetic loss in the inductor's core. Therefore, choosing L_2 needs considerable attention. A good strategy to minimize R_{L2} is to use air core inductor with litz wire to increase the effective wire cross section at high frequencies. We constructed L_2 using litz wire, and measured its inductance and resistance at 800 kHz using a GW 8101G LCR meter. We measured the inductance and resistance to be 25.6 μH and $R_{L2}=0.5\,\Omega$, respectively. The degradation in the efficiency due to R_{L2} is about $R_{L2}/R_L\times 100$, or 4.7% which is very large compared to other losses. R_{L2} also introduces a negligible change in the calculated φ_X, which can be neglected.

The gate driver should be chosen based on the following criteria.

1) It should have a small propagation delay compared to the delay of the feedback network. Usually an inverting gate driver has a smaller delay compared to a noninverting one, but due to the phase shift requirement on the feedback network, a noninverting gate drive should be used in the proposed circuit.
2) Its input capacitance should be smaller than the calculated capacitance for the feedback network, i.e., C_F'.

An important parameter of the gate driver is its propagation delay. If we represent the propagation delay of the gate driver by t_d, the phase shift φ_d caused by the gate driver can then be expressed by

$$\varphi_d=-\omega\times t_d. \tag{39}$$

To take φ_d into account, the passive part of the feedback network should provide a phase shift of $\varphi_F-\varphi_d$.

We used a 74AC244 digital buffer as the gate driver. The power consumption of this buffer is 200 μW, which is fairly negligible compared to other losses. This buffer has a switching threshold voltage of 2.25 V, an input capacitance of 4.5 pF, and a typical delay of 5 ns. According to (39), this delay amounts to a phase shift of -1.44° at 800 kHz. Therefore, after finding the required phase shift in the feedback network, we should subtract -1.44° from that and design the feedback network for the remaining amount.

Another component of the power loss is the one dissipated due to the charging and discharging of the transistor gate capacitance. The gate capacitance of FQT13n06, based on its datasheet, is typically about 270 pF. However, the input capacitance of a MOSFET is very nonlinear (voltage-dependent). Relatively speaking, the input capacitance is small when the MOSFET is OFF. It increases considerably when the transistor becomes ON and is in saturation. It drops again, when the transistor is fully ON and is in the triode region [25]. Consequently, when the amplitude of the gate signal is so large that the transistor periodically switches ON and OFF, it is not possible to simply model the input capacitance with a linear (ideal) capacitor. Even if we want to have a rough value of the input capacitance, we should simulate the transistor with real large signals and in a circuit similar to the actual one. Therefore, to measure the power loss due to the charging and discharging the gate capacitance, we designed a very simple Class-E PA for the specifications stated in Section II and drove the transistor with an 800-kHz 4.5-V pulse signal. We measured the power required to charge and discharge the input capacitance to be about 8 mW. Therefore, we expect an efficiency degradation of about 0.8% due to the gate capacitance.

TABLE III
MAJOR SOURCES OF POWER LOSS IN THE PROPOSED CLASS-E PO AND THEIR SHARE IN DEGRADING EFFICIENCY

Source of power loss	Degradation in η (%)
AC Power Loss in Feedback	5
ESR of L_2	4.7
R_{ON} of transistor	1.3
Gate charge and discharge	0.8

The major components of power loss are summarized in Table III. Overall, we estimate to have about 12% degradation in efficiency due to the feedback network, the ESRs of L_1 and L_2, $R_{\rm on}$ of the transistor and charging and discharging of the gate capacitance. It should be noted that the dc power loss in the feedback network and the power dissipated in the gate capacitance and the gate driver are not supplied through L_1, Therefore, the design procedure, i.e., calculating R_L using (3), should be started with a P_o that includes the output power and the power loss in $R_{\rm on}$ and L_2, as well as the ac power loss in the feedback network. In other words, we should start the design procedure with $P_o=1.11$ W.

We started the aforementioned design procedure with $P_o=1.11$ W. Then, we simulated the PO using LT-SPICE XVII [26] and realized that the circuit is not nominally tuned. The source of the issue was that the duty cycle of the gate drive signal was slightly larger than 50%. The reason, as explained in Section III-C, was the limited q-factor of the load network. We fine-tuned the values of C_1 and C_F' to achieve the ZVS and ZVDS conditions, but we ended up having about 7% more output power than the expected value. The cause of the issue was again the larger than expected duty cycle of the gate drive signal. Therefore, we reiterated the design procedure, but this time, with 7% less power, or $P_o=1.04$ W. After simulating the PO and fine-tuning the values of C_1 and C_F', the output power was 0.99 W and the efficiency was 89%.

After designing the basic structure of Class-E PO shown in Fig. 6, we designed the impedance matching network shown in Fig. 9(c) to arrive to $R_L=50\,\Omega$. The finally calculated values of the circuit components are shown in the "Calculation" column

TABLE IV
VALUES OF CIRCUIT COMPONENTS IN FIG. 6 RESULTED FROM CALCULATION, SIMULATION AND EXPERIMENTAL TUNING. INSTEAD OF THE R_2–C_L BRANCH IN FIG. 6, THE MATCHING NETWORK, SHOWN IN FIG. 9(C) IS USED.

Parameter	Calculation	Simulation	Experiment
$C_1(nF)$	3.6	3.3	3.4
$C_{n1}(nF)$	1.85	1.85	2.02
$C_{n2}(nF)$	8.0	8.0	8.6
$C'_F(pF)$	104	98	62
$R_L(\Omega)$	50	50	50
$R'_{F1}(k\Omega)$	31	31	30
$R''_{F1}(k\Omega)$	8.38	8.38	8.02
$R''_{F2}(k\Omega)$	6.59	6.59	6.32
$L_1(mH)$	0.9	0.9	0.9
$L_2(\mu H)$	28	28	25.6
$f_e(kHz)$	800	800	800
$P_o(W)$	1	0.99	0.96
$\eta(\%)$	88	89	89

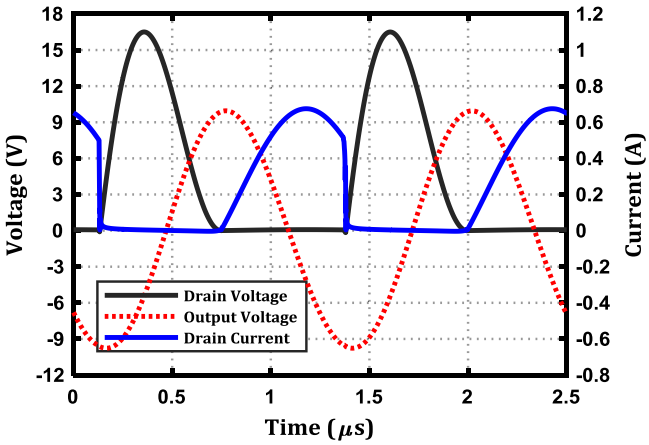

Fig. 12. Simulation result of the proposed Class-E PO with actual components.

of Table IV. The values of the components, after fine-tuning in simulation, are given in the "Simulation" column of Table IV. It is clear that our design procedure results in a circuit that is very close to being fully tuned. The simulated waveforms of the drain voltage, drain current, and output voltage are depicted in Fig. 12.

It is worth mentioning that the calculated C'_F in (34) is much larger than the input capacitance of the gate driver that we have chosen in this work. Therefore, we could go back to (14) and choose a larger value for K_R. This would minimize the ac power loss in the feedback network and increase the efficiency of the circuit. But, it is not our aim to develop a Class-E PO that outperforms all previous Class-E POs in efficiency; here, we only want to prove the concept, describe the design procedure of the new circuit, and verify it through simulation and experimental results. Therefore, we kept $K_R = 20$.

In summary, we suggest that the designer start the design with a reasonable estimate of the power loss in the circuit (for example 10%). Then, he should calculate the values of C_1, C_2, L_2, and R_L using (3)–(6), and based on those values, choose an

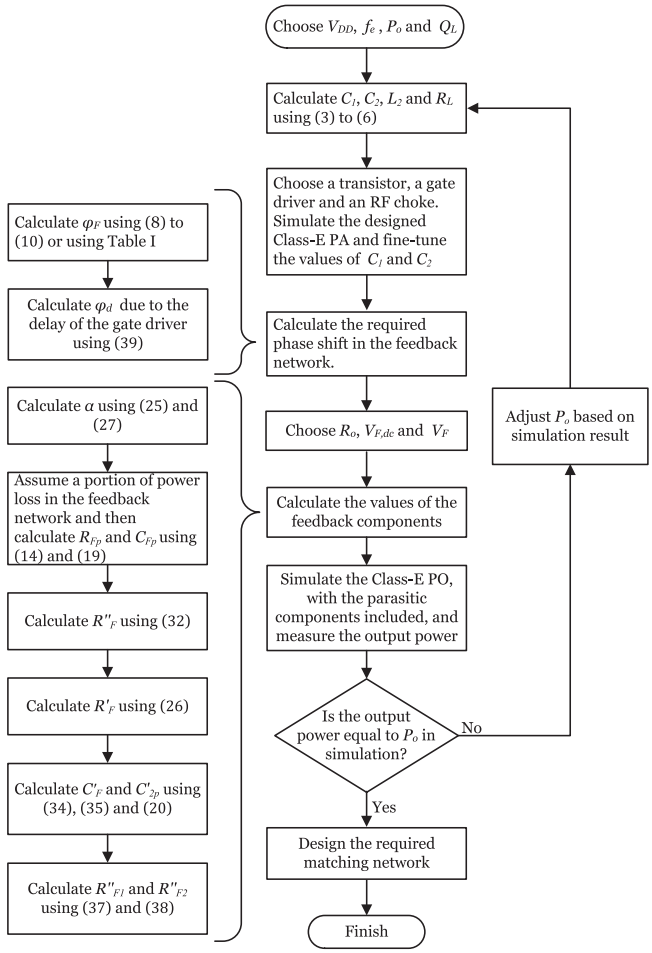

Fig. 13. Flowchart of the design procedure.

appropriate transistor, gate driver, and RF choke. He should simulate the resulting Class-E PA with the selected components and their parasitic elements, and fine-tune the PA in simulation. This step is required because the values of C_1 and C_2 should be adjusted based on the chosen transistor, gate driver, and RF choke. The designer should then continue the rest of the described design procedure to convert the Class-E PA to a Class-E PO. Fig. 13 shows a flowchart summarizing the design procedure.

IV. COMPARISON WITH CONVENTIONAL CLASS-E PO

Fig. 14 illustrates the schematic of the conventional Class-E PO [16], [17]. Similar structures to the one proposed in [16] and [17] have been used to convert other classes of PAs to POs [27]–[28]. In this section, we compare our proposed Class-E PO with the conventional one proposed in [16] and [17].

In the circuit shown in Fig. 14, the feedback network mainly consists of C_{n1}, C_{n2}, L_F and the transistor's gate capacitance, C_g. In this circuit, the feedback signal is obtained from the voltage across R_L, which is an attenuated version of the signal at node X. This signal is further attenuated by the capacitive voltage divider consisting of C_{n1} and C_{n2}. Therefore, in the feedback

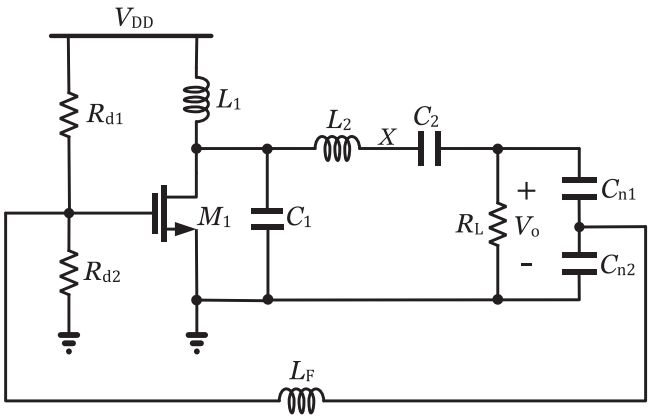

Fig. 14. Schematic of the conventional Class-E PO [17].

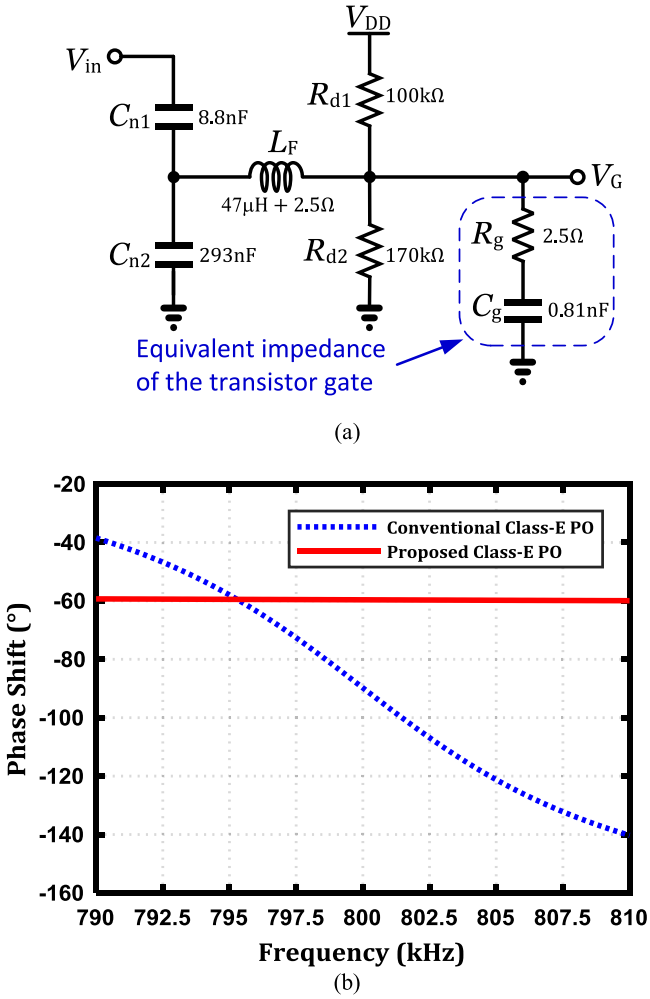

Fig. 15. (a) Feedback network of the conventional Class-E PO presented in [17]. (b) Phase response of the conventional and proposed feedback networks.

network, L_F is added to generate a high-Q RLC circuit that can amplify the attenuated feedback signal so that it can drive the transistor. The high-Q RLC circuit consisting of C_{n1}, C_{n2}, L_F, and C_g, has a steep slope in its phase response. Fig. 15(a) depicts the feedback network of the Class-E oscillator designed in [17] and Fig. 15(b) shows the phase shifts provided by this circuit (dotted line) and the phase shift of the proposed PO in this paper (solid line). As it is clear in Fig. 15(b), when the input frequency of the conventional feedback network changes from 790 to 810 kHz, its phase shift changes from –40° to –140°, while the phase shift of the proposed circuit is almost fixed at –60° with less than 0.5° change. This is an important advantage of the proposed circuit because, for example, if L_2 increases by only 2%, the Class-E frequency of the load network decreases by about 1%, or it goes from 800 to 792 kHz. So now, the phase shift provided by the proposed feedback circuit is still about –60° and the proposed PO stays close to its nominal Class-E operation, while the phase shift provided by the conventional feedback circuit changes from –90° to –45° and greatly disturbs the Class-E operation of the circuit. Moreover the exact values of L_F and C_g play important roles in the proper operation of the conventional Class-E PO. If either L_F or C_g slightly changes, the phase shift of the conventional feedback network changes considerably and the PO either becomes mistuned or stops oscillating. This fact is also indicated in [17] where it is mentioned that L_F and C_g are the most influential elements on the operating frequency. We see several issues with this feature of the circuit.

1) An important reason for using a Class-E PO, instead of a Class-E PA, is that in a Class-E PA the frequency of the gate drive signal is defined by an external oscillator and is independently controlled from the Class-E frequency of the load network. These two frequencies should ideally be equal. In fact, the purpose of tuning a Class-E PA is to make these two frequencies exactly equal. If, for a reason, any of these frequencies deviates from its desired value, we will see large degradations in the efficiency or the output power as illustrated in Section III-D. Therefore, we resort to feedback theory to convert a Class-E PA to a Class-E PO to minimize this problem. In the conventional Class-E PO shown in Fig. 14, both the load network and the feedback network are high-Q resonant RLC circuits, which have steep slopes in their input-to-output phase responses. The transfer function of these RLC circuits should be well-matched in order to sustain a phase shift of 360° around the PO loop. Any change in the values of the components of either the feedback or the load network can cause large degradation in the output power or the efficiency, albeit, these degradations are less than those for a conventional Class-E PA.
2) Since the gate capacitance, C_g, plays a crucial role in the proper operation of the conventional Class-E PO, it is important to know its precise value before starting the design procedure. C_g consists of two portions; a portion due to the gate-source capacitance C_{gs}, and a portion due to the gate-drain capacitance C_{gd}. C_{gs} is a very nonlinear voltage-dependent capacitor. Also, C_{gd} experiences different Miller multiplication factors as the transistor turns ON and OFF. Therefore, we cannot simply model the gate capacitance with a simple linear capacitor [29], [30].
3) Even if we assume C_g is a linear capacitor, its value greatly changes from transistor to transistor. This means that for each design and each product, the input impedance of the

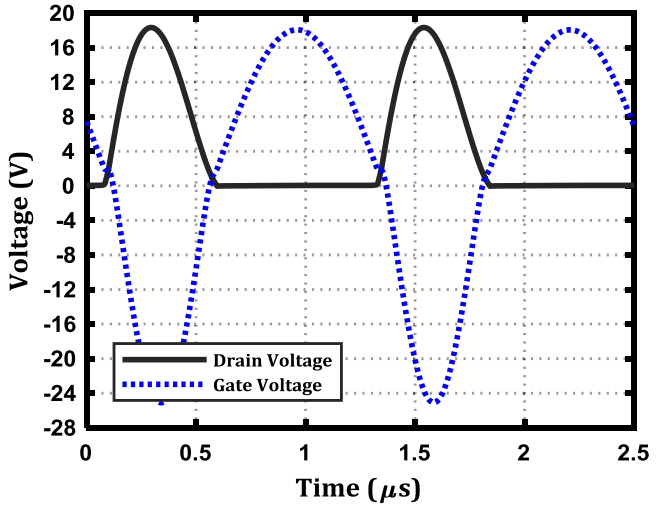

Fig. 16. Drain waveform of conventional Class-E PO [17] designed with a FQT13N06L MOSFET.

TABLE V
VALUES RESULTED FROM CALCULATION AND SIMULATION FOR THE CIRCUIT OF FIG. 14

Component	L_1 (mH)	C_1 (nF)	L_2 (μH)	C_2 (nF)	R_L (Ω)	C_{n1} (nF)	C_{n2} (nF)	L_f (μH)	R_{d1} $(k\Omega)$	R_{d2} $(k\Omega)$
Calculated	0.9	3.29	28.7	1.79	50	7.87	320	75.4	100	65
Simulated	0.9	2.5	28.7	1.79	50	7.87	320	70	100	65

transistor should be measured and then, based on that, the feedback network should be designed and tuned. This is difficult and time-consuming.

To compare the performance of the proposed Class-E PO with that of the conventional one, we designed the conventional Class-E PO for the same specification mentioned in Section II and with the same transistor that we used in our own circuit, i.e., FQT13n06. Using simulation, we measured the gate impedance of FQT13n06 to be $1.4 - j379\ \Omega$, which means a 1.4-Ω resistor in series with an 525 pF capacitor. We then followed the design procedure described in [17] to design the circuit shown in Fig. 14 for the specifications listed in Section II.

In our calculations and simulations, we chose an ESR of 2.5 Ω for L_F (as in [17]) and an ESR of 0.5 Ω for L_2. We simulated the designed PO with the calculated values, but the PO was far from being nominally tuned and satisfying the ZVS and ZVDS conditions. After much effort, the best drain waveform that we could achieve is shown in Fig. 16. The values resulted from calculation and the ones achieved after fine-tuning in simulation are given in Table V. The drain waveform shown in Fig. 16 fulfills the ZVS condition, but not the ZVDS condition. In addition, even though we designed the PO for the duty cycle of 50%, the actual duty cycle of the gate signal is about 60%. We believe this is the main cause of the circuit not satisfying ZVDS condition and that is due to the large nonlinearity in the gate capacitance.

As it is clear, in Fig. 16, when the gate signal goes over the V_{th} of the transistor, it slows down because when the transistor turns ON, its gate capacitance considerably increases. Therefore, even though we set the dc level of the gate drive signal slightly larger than V_{th} to have a duty cycle of 50%, the duty cycle is much larger than 50%. To adjust the duty cycle back to 50%, we should reduce the dc level of the gate signal by decreasing the ratio of R_{d2}/R_{d1}. However, this causes that the dc level become smaller than V_{th}, which itself causes that the PO does not autonomously start oscillation and if we kick-start the oscillation by an external circuit, the oscillation could easily die out. Therefore, conflicting requirements exist on the dc level of the gate signal. Therefore, to minimize the issues regarding the nonlinearity and modeling of the gate capacitance, we suggest using a gate driver for the conventional PO as well.

We should clarify that using a gate driver for the conventional circuit only removes the nonlinearity issues due to the gate capacitance and also simplifies the design procedure, but the main problem of the circuit, which is the large sensitivity of the feedback phase shift to the values of the components, still exists.

To evaluate the influence of component tolerances on the performance of the proposed and the conventional circuits, we increased the values of the components that have major effects on the operation of the circuits and simulated both circuits. Table VI shows the percent changes in the oscillation frequency, output power, and the efficiency of both circuits when the value of some components increases by 5%.

TABLE VI
COMPARING THE INFLUENCE OF THE COMPONENT VALUES ON THE PERFORMANCE OF THE CONVENTIONAL AND THE PROPOSED CLASS-E POS

	$\left(\frac{\Delta P_o}{P_o}\right)\times 100$		$\left(\frac{\Delta \eta}{\eta}\right)\times 100$		$\left(\frac{\Delta f_e}{f_e}\right)\times 100$	
Circuit Type	Conv.	Prop.	Conv.	Prop.	Conv.	Prop.
$\Delta C_2 = +5\%$	-21.5		+0. 1		-1.0	
$\Delta L_2 = +5\%$	-26.3	-4.71	+0.26	+0.22	-1.26	-2.25
$\Delta C_{n1} = +5\%$	-11.0	-3.77	-0.55	+0.56	+0.26	-1.75
$\Delta C'_F = +5\%$ or $\Delta C_g = +4.2\%$	+38.5	+3.77	0.0	0.0	-1.3	-1.25
$\Delta L_f = +3.7\%$	+35.0		0.0		-1.28	
$\Delta R'_F = +5\%$		0.0		+0.22		0.0

The major issue that we observed with the conventional circuit is that, in some cases, if the change in the component value is large, the oscillator does not oscillate, even if we try to kick-start it. For example, if the value of L_F increases by more than 3.7% or if the gate capacitance increases by more than 4.2%, the oscillator does not oscillate or does not have sustainable oscillation. Therefore, in Table VI, we increased C_g by only 4.2% and L_F by 3.7% and then compared the result with those with 5% increase in C'_F or R'_F of the proposed circuit.

Putting the problem of sustainable oscillation aside, efficiencies of both circuits are fairly insensitive to the changes in the component values. However, the variations in the output power of the conventional circuit could be as high as 38.5%, while it is less than 5% in the proposed circuit.

We believe that the advantages of the proposed circuit is due to the fact that the feedback network in the proposed circuit is a low-Q RC circuit, whose phase response, as shown in Fig. 15(b),

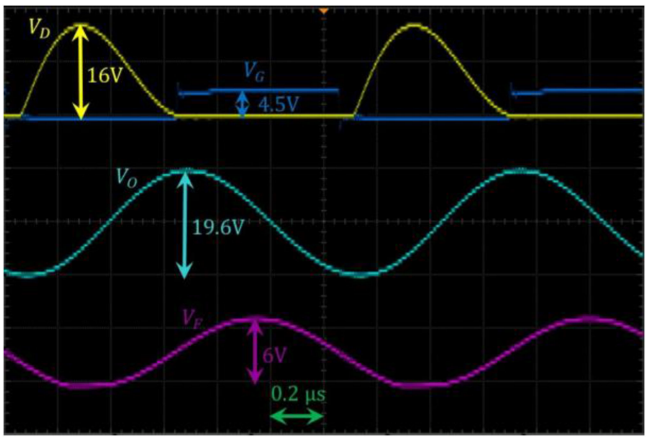

Fig. 17. Experimental waveforms of the Class-E PO.

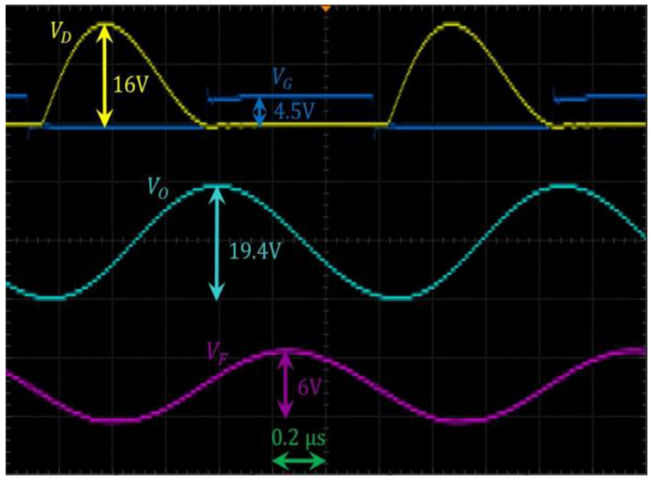

Fig. 18. Experimental waveforms of the Class-E PO when the value of C_{n1} increases by 10%.

is almost flat around the Class-E frequency and if the Class-E frequency changes for whatever reason, the change in the phase shift provided by the feedback network would be very small and the proposed PO stays close to its nominal Class-E operation. In addition, because the proposed feedback network is not a resonant circuit, it does not have a specific resonance frequency interfering with the Class-E frequency of the load network.

As shown in this section and also in Section III-D, the output power and the efficiency of the proposed Class-E PO have negligible sensitivities to the variations in component values. In fact, if a component value changes, the oscillation frequency of the PO moves toward the new nominal Class-E frequency of the load network; therefore, we call this circuit a self-tuned Class-E PO.

V. Experimental Result

To confirm the circuit operation, the designed and simulated Class-E PO in Section III-E was built and tested. The calculated values of the components and their corresponding values in simulation and in measurement are given in Table IV. Experimental parameters are also shown in Table IV, alongside the simulation results. Experimental waveforms of the drain voltage V_D, the load voltage V_O, the input voltage to the gate driver V_F, and the gate drive signal V_G are shown in Fig. 17, which shows that the drain voltage V_D has satisfied ZVS and ZVDS conditions at the turn-ON time.

The frequency and the amplitude of the output signal were measured to be 800 kHz and 9.8 V, respectively. This corresponds to an output power of 0.960 W ($R_L = 50\,\Omega$). The measured efficiency of the PO was 89%.

We increased the value of C_{n1} by 10% to evaluate the self-tuning capability of the PO. Fig. 18 shows V_D, V_O, V_F, and V_G after 10% increase in C_{n1}. Clearly, the V_D still achieves the ZVS and ZVDS conditions at the turn-ON time. The new frequency, output power, and efficiency are 773 kHz, 940 mW, and 89%, respectively, indicating that the PO has adjusted its frequency of operation to maintain its Class-E operation and its high efficiency.

Table VII compares the performance of the proposed Class-E PO with other published Class-E POs designed for similar specifications and in almost the same frequency range. The measured efficiency of the proposed PO is on par or better than the previously published works. As mentioned in Section III-E, we could easily increase the efficiency of the proposed PO by at least 2%, had we chosen a larger K_R to dissipate less ac power in the feedback network, but our aim in this paper is to only prove the concept of a Class-E PO with a low-Q RC feedback network. It is worth mentioning that the main advantage of the proposed Class-E PO over the existing ones is that its output power has much smaller sensitivity to the component variations, a fact that cannot be seen in Table VII.

TABLE VII
Performance Comparison of Published Class-E POs

Parameter	This work	[17]	[18]	[21]	[21]	[28]
f_e (MHz)	0.8	0.8	1.95	2.02	1.97	0.8
P_o (W)	0.96	0.95	4.82	6.8	2.8	0.91
η (%)	89	82	89	90.7	89.7	86.2
R_L (Ω)	50	50	10	10	9.9	49.4
V_{DD}(V)	4.5	4.5	12	12	12	6
Q_L	13	13	10	10	3	12
Transistor	FQT 13n06	MTP 3055E	IRF 530	IRF 530	IRF 530	IRFR 120Z
Class	E	E	E	E	E	E/F_3

VI. Conclusion

In this paper, we presented a new Class-E PO whose feedback network is constructed of a low-Q RC network. As a result, the phase shift of the feedback network does not change much if the Class-E frequency of the PO changes due to the variations in the circuit components. Simulation and experimental evaluations verified that the performance of the proposed circuit is much less sensitive to the component tolerances. We also presented a design procedure for the new Class-E PO and then verified the design procedure with simulation and experimental measurements.

APPENDIX

A. Analytical Proof of (25) and (27)

Consider the Class-E PA shown in Fig. 3. The output power P_o delivered to R_L is an input parameter and is equal to

$$P_o = \frac{1}{2} R_L I_p^2 \tag{40}$$

where I_p is the magnitude of the sinusoidal current flowing into R_L. From there, we can find the magnitude of the sinusoidal voltage at node X as

$$V_X = \sqrt{\frac{2P_o}{R_L}} \times \sqrt{R_L^2 + \left(\frac{1}{C_2\omega}\right)^2}. \tag{41}$$

In Fig. 5(b), the transfer function of the feedback network can be expressed by

$$H'_F(j\omega) = \frac{R''_F}{R''_F + R'_F + R''_F R'_F C'_F(j\omega)}. \tag{42}$$

The phase shift in $H'_F(j\omega)$ can be calculated by

$$\varphi_F = -\tan^{-1}\left(\frac{R''_F R'_F C'_F \omega}{R''_F + R'_F}\right). \tag{43}$$

If we define the magnitude of the sinusoidal waveform at the output of the feedback network as V_F, we can write

$$\frac{V_F}{V_X} = \frac{R''_F}{\sqrt{\left(R''_F + R'_F\right)^2 + \left(R''_F R'_F C'_F \omega\right)^2}}. \tag{44}$$

Considering that $R'_F = \alpha R''_F$, we can simplify (43) and (44) to

$$\varphi_F = -\tan^{-1}\left(\frac{\alpha R''_F C'_F \omega}{1+\alpha}\right) \tag{45}$$

and

$$\frac{V_F}{V_X} = \frac{R''_F}{\sqrt{\left(R''_F + \alpha R''_F\right)^2 + \left(R''_F\left(\alpha R''_F\right) C'_F \omega\right)^2}} = \frac{1}{(1+\alpha)\times\sqrt{1+\tan^2(\varphi_F)}} = \frac{\cos(\varphi_F)}{(1+\alpha)} \tag{46}$$

respectively.

B. Analytical Proof of (35) and (36)

The q-factor of the parallel $C'_F - R''_F$ section in Fig. 5(b) can be expressed by

$$Q_{F1} = \omega C'_F R''_F. \tag{47}$$

Therefore, the values of the resistor and capacitor in the series equivalent circuit of the parallel $C'_F - R''_F$ can be calculated using

$$C'_{Fs} = \frac{1+Q_{F1}^2}{Q_{F1}^2} C'_F = \frac{1+\left(\omega C'_F R''_F\right)^2}{\left(\omega C'_F R''_F\right)^2} C'_F \tag{48}$$

and

$$R''_{Fs} = \frac{R''_F}{1+Q_{F1}^2} = \frac{R''_F}{1+\left(\omega C'_F R''_F\right)^2} \tag{49}$$

respectively. Using (26) and (45), (48) and (49) can be simplified to

$$C'_{Fs} = \frac{\alpha^2 + (\alpha+1)^2\tan^2(\varphi_F)}{(\alpha+1)^2\tan^2(\varphi_F)} C'_F \tag{50}$$

$$R''_{Fs} = \frac{\alpha^2}{\alpha^2 + (\alpha+1)^2\tan^2(\varphi_F)} R''_F. \tag{51}$$

Now, we calculate the parallel equivalent RC circuit of the series connection of $R''_{Fs} + R'_F$ and C'_{Fs}. The q-factor of this connection can be calculated using

$$Q_{F2} = \frac{1}{\omega C'_{Fs}\left(R''_{Fs} + R'_F\right)} \tag{52}$$

which, using (43), (50), and (51), can be simplified to

$$Q_{F2} = -\frac{\tan(\varphi_F)}{\alpha + (1+\alpha)\tan^2(\varphi_F)}. \tag{53}$$

Therefore, the parallel equivalent capacitance of C_{Fp} can be calculated using

$$C_{Fp} = \frac{Q_{F2}^2}{1+Q_{F2}^2} \times \frac{\alpha^2 + (\alpha+1)^2\tan^2(\varphi_F)}{(\alpha+1)^2\tan^2(\varphi_F)} C'_F. \tag{54}$$

ACKNOWLEDGMENT

The authors would like to thank Shirin Pezeshkpour for her assistance in revising the paper.

REFERENCES

[1] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. 10, no. 3, pp. 168–176, Jun. 1975.
[2] N. O. Sokal, "RF power amplifiers," *QEX*, pp. 1–20, 2001.
[3] M. K. Kazimierczuk, *Radio-Frequency Power Amplifiers*, 2nd ed. New York, NY, USA: Wiley, 2015.
[4] B. Ziaie, S. C. Rose, M. D. Nardin, and K. Najafi, "A self-oscillating detuning-insensitive class-E transmitter for implantable microsystems," *IEEE Trans. Biomed. Eng.*, vol. 48, no. 3, pp. 397–400, Mar. 2001.
[5] P. R. Troyk and M. A. K. Schwan, "Closed-loop class E transcutaneous power and data link for microimplants," *IEEE Trans. Biomed. Eng.*, vol. 39, no. 6, pp. 589–599, Jun. 1992.
[6] C. M. Zierhofer and E. S. Hochmair, "High-efficiency coupling-insensitive transcutaneous power and data transmission via an inductive link," *IEEE Trans. Biomed. Eng.*, vol. 37, no. 7, pp. 716–722, Jul. 1990.
[7] G. A. Kendir *et al.*, "An optimal design methodology for inductive power link with class-E amplifier," *IEEE Trans. Circuits Syst. I. Reg. Papers*, vol. 52, no. 5, pp. 857–866, May 2005.
[8] G. Vandevoorde and R. Puers, "Wireless energy transfer for stand-alone systems: A comparison between low and high power applicability," *Sens. Actuators A: Phys.*, vol. 92, no. 1, pp. 305–311, 2001.
[9] E. K. F. Lee, "A feedback controlled coil driver for transcutaneous power transmission," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, 2012, pp. 1–4.
[10] M. W. Baker and R. Sarpeshkar, "Feedback analysis and design of RF power links for low-power bionic systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 1, pp. 28–38, Mar. 2007.
[11] A. N. Laskovski and M. R. Yuce, "Class-E self-oscillation for the transmission of wireless power to implants," *Sens. Actuators A: Phys.*, vol. 171, no. 2, pp. 391–397, 2011.
[12] Guoxing Wang *et al.*, "A closed loop transcutaneous power transfer system for implantable devices with enhanced stability," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2004, vol. 4, pp. 17–20.

[13] R. Carta, J. Thon, G. Gosset, G. Cogels, D. Flandre, and R. Puers, "A self-tuning inductive powering system for biomedical implants," *Procedia Eng.*, vol. 25, pp. 1585–1588, 2011.
[14] A. Trigui, S. Hached, F. Mounaim, A. C. Ammari, and M. Sawan, "Inductive power transfer system with self-calibrated primary resonant frequency," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6078–6087, Nov. 2015.
[15] T. Yang, C. Zhao, and D. Chen, "Feedback analysis of transcutaneous energy transmission with a variable load parameter," *ETRI J.*, vol. 32, no. 4, pp. 548–554, 2010.
[16] J. Ebert and M. Kazimierczuk, "Class E high-efficiency tuned power oscillator," *IEEE J. Solid-State Circuits*, vol. SSC-16, no. 2. pp. 62–66, Apr. 1981.
[17] M. K. Kazimierczuk, V. G. Krizhanovski, J. V. Rassokhina, and D. V. Chernov, "Class-E MOSFET tuned power oscillator design procedure," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 6, pp. 1138–1147, Jun. 2005.
[18] H. Sekiya, T. Ezawa, and Y. Tanji, "Design procedure for class E switching circuits allowing implicit circuit equations," *IEEE Trans. Circuits Syst. I Reg. Papers*, vol. 55, no. 11, pp. 3688–3696, Dec. 2008.
[19] D. V Chernov, M. K. Kazimierczuk, and V. G. Krizhanovski, "Class-E MOSFET low-voltage power oscillator," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2002, vol. 5, pp. 509–512.
[20] H. Hase, H. Sekiya, J. Lu, and T. Yahagi, "Resonant DC/DC converter with class E oscillator," in *Proc. IEEE Int. Circuits Syst. Symp.*, 2005, pp. 720–723.
[21] H. Hase, H. Sekiya, J. Lu, and T. Yahagi, "Novel design procedure for MOSFET class E oscillator," *IEICE Trans. Fundam. Electron. Commun. Comput. Sci.*, vol. E87-A, no. 9, pp. 2241–2247, 2004.
[22] B. Razavi, "Basic concepts in RF design" in *RF Microelectronics*, 2nd ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 2011, pp. 62–67.
[23] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004.
[24] W. H. Cantrell, "Tuning analysis for the high-Q class-E power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 48, no. 12, pp. 2397–2402, Dec. 2000.
[25] B. Razavi, "Basic MOS device physics," in *Design of Analog CMOS*, 2nd ed. New York, NY, USA: McGraw-Hill, 2017, p. 30.
[26] LT, "LT-SPICE XVII," *Linear Technology*, 2017. [Online]. Available: http://www.linear.com/designtools/software/
[27] R. Miyahara, X. Wei, T. Nagashima, T. Kousaka, and H. Sekiya, "Design of class-E_M oscillator with second harmonic injection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 10, pp. 2456–2467, Oct. 2012.
[28] T. Inaba and H. Koizumi, "Class E/F_3 tuned power oscillator," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1420–1427, Feb. 2018.
[29] M. Hayati, A. Lotfi, M. K. Kazimierczuk, and H. Sekiya, "Analysis and design of class-E power amplifier with MOSFET parasitic linear and nonlinear capacitances at any duty ratio," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5222–5232, Nov. 2013.
[30] M. Hayati, A. Lotfi, M. K. Kazimierczuk, and H. Sekiya, "Generalized design considerations and analysis of class-E amplifier for sinusoidal and square input voltage waveforms," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 211–220, Jan. 2015.

Mohammad Mahdi Ahmadi (S'05–M'07) received the B.Sc. degree in biomedical engineering (Highest Hons.) from Shahid Beheshti University, Tehran, Iran, in 2000, the M.Sc. degree in electronic engineering from Sharif University of Technology, Tehran, in 2002, and the Ph.D. degree in electrical engineering from the University of Calgary, Calgary, Canada, in 2007.

His Ph.D. research was on developing a wireless implantable microsystem for continuous blood glucose monitoring. From 2007 to 2010, he was with Sound Design Technologies Ltd., Burlington, Canada (acquired by ON Semiconductor) where he designed ultra low-power and low-voltage analog integrated circuits for hearing aids. From 2010 to 2014, he was with Synopsys Inc., Toronto, Canada, where he designed high-speed circuits for multistandard multi-Gb/s wireline applications. In the summers of 2015 and 2017, he was with Rambus Inc., Sunnyvale, CA, USA, where he was involved with the design of equalizers for high-speed (up to 112 Gb/s) electrical links. Since 2014, he has been an Assistant Professor with the Department of Biomedical Engineering, Amirkabir University of Technology, Tehran. His current research interests include biomedical circuits and systems.

Dr. Ahmadi received awards at the 44th ISSCC/DAC and the third Analog Devices Student Circuit Design Contests. He was part of a team which received the 2010 EDN Innovation Award for developing the world's first full SoC for hearing aids.

Maryam Salehi-Sirzar received the B.Sc. degree in biomedical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2015 (with hons.).

Her research interests include medical instrumentation and circuit design for biomedical applications.