# A Non-Segmented PSpice Model of SiC MOSFET With Temperature-Dependent Parameters

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***Abstract*—A non-segmented PSpice model of silicon carbide metal-oxide semiconductor field effect transistor (SiC MOSFET) with temperature-dependent parameters is proposed in this paper, which can improve the model's convergence and temperature characteristics. The non-segmented equations and the parameter-extraction method for the proposed SiC MOSFET PSpice model are introduced first. Simulation and experiment results are given to verify the correctness of the model while considering the temperature-dependent parameters. The static characteristics of the model are verified by comparing the simulation curves with the static characteristic curves in the SiC MOSFET's datasheet, and its dynamic characteristics are verified by comparing the simulation results with experimental results under different ambient temperatures (25, 75, and 125 °C) based on a double-pulse test platform. Moreover, the proposed non-segmented model, the conventional segmented model, and the model from the manufacturer are adopted and simulated in a full-bridge inverter. The simulation results show better convergence of the proposed non-segmented model. Therefore, an accurate and practical simulation model of SiC MOSFET is provided for circuit design in this paper.**

***Index Terms*—Non-segmented PSpice model, silicon carbide metal-oxide semiconductor field effect transistor (SiC MOSFET), simulation convergence, temperature-dependent.**

## I. Introduction

With the improvement of the packaging technology and the manufacturing process of silicon carbide (SiC) wafers in recent years, SiC devices now can operate stably at a high blocking voltage, high switching frequency, and high temperature [1]–[3]. Commercial SiC devices are used increasingly in power electronics equipment and systems. This is especially true of SiC metal-oxide semiconductor field effect transistors

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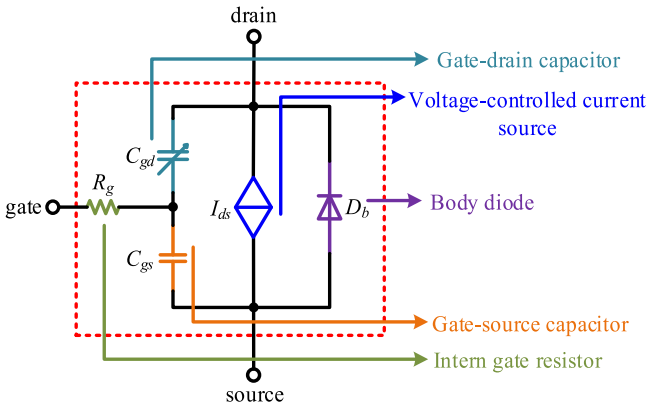


Fig. 1. Proposed non-segmented model of a SiC MOSFET.

MOSFET in this paper. In the proposed SiC MOSFET model, a non-segmented equation is used to describe the static characteristics of SiC MOSFET, which will not cause the discontinuity during circuit simulations; and the temperature characteristics of SiC MOSFET body diode are also considered, which makes the proposed SiC MOSFET model more accurate at different ambient temperatures. A SiC MOSFET of type C2M0045170D (1700V/72A) is chosen as the modeling object in this paper. In Section II, the modeling method of the proposed SiC MOSFET model is introduced in detail. In Section III, the model's accuracy is verified by simulation and experimental results. In Section IV, the proposed model is employed in a full-bridge inverter to show its good simulation convergence. Conclusions are drawn in Section V.

## II. Non-Segmented Model of SiC MOSFET With Temperature-Dependent Parameters

The proposed non-segmented model of a SiC MOSFET is shown in Fig. 1. This model includes voltage-controlled current source $I_{\rm ds}$, body diode $D_b$, gate-drain capacitor $C_{\rm gd}$, gate-source capacitor $C_{\rm gs}$, and internal gate resistor $R_g$.

### A. Voltage-Controlled Current Source $I_{ds}$

In this paper, a non-segmented equation is used to define the voltage-controlled current source $I_{\rm ds}$ to improve the simulation convergence. $I_{\rm ds}$ is used to describe the drain–source current of the SiC MOSFET, and $I_{\rm ds}$ includes $I_{\rm ds\_transfer}$ for the transfer characteristic and $I_{\rm ds\_output}$ for the output characteristic of the SiC MOSFET. According to the datasheet [16], the transfer characteristic curve is the $I_{\rm ds}-V_{\rm gs}$ curve, where $V_{\rm gs}$ is the gate-source voltage, and the output characteristic curve is the $I_{\rm ds}-V_{\rm ds}$ curve, where $V_{\rm ds}$ is the drain–source voltage. To fit the transfer characteristic, $I_{\rm ds\_transfer}$ can be obtained based on the Angelov model [17], as shown in (1); to fit the output characteristic, $I_{\rm ds\_output}$ can be obtained from (2). To fit the transfer and output characteristics at the same time, $I_{\rm ds}$ can be expressed as the combination of $I_{\rm ds\_transfer}$ and $I_{\rm ds\_output}$, as follows:

$$I_{\rm ds\_transfer}=k\cdot\left\{1+\tanh\left[a\cdot(V_{\rm gs}+c)+b\cdot(V_{\rm gs}+d)^2\right]\right\} \tag{1}$$

$$I_{\rm ds\_output}=p\cdot\frac{V_{\rm ds}}{1+q\cdot V_{\rm ds}} \tag{2}$$

$$\begin{aligned} I_{\rm ds}&=I_{\rm ds\_transfer}\cdot I_{\rm ds\_output}\\ &=k\cdot\left\{1+\tanh\left[a\cdot(V_{\rm gs}+c)+b\cdot(V_{\rm gs}+d)^2\right]\right\}\\ &\quad\cdot\frac{p\cdot V_{\rm ds}}{1+q\cdot V_{\rm ds}} \end{aligned} \tag{3}$$

where $k$, $a$, $b$, $c$, and $d$ are parameters of the transfer characteristic, and $p$ and $q$ are parameters of the output characteristic. In (1), the hyperbolic tangent function is used to fit the transconductance curve of the SiC MOSFET. The hyperbolic tangent function is continuously differentiable, which is conducive to the simulation convergence.

To better fit the output characteristic curves under different $V_{\rm gs}$, the parameters $p$ and $q$ are variable, which means that they vary with different $V_{\rm gs}$. Then, the expression of $I_{\rm ds}$ can be given as

$$\begin{aligned} I_{\rm ds}&=k\cdot\left\{1+\tanh\left[a\cdot(V_{\rm gs}+c)+b\cdot(V_{\rm gs}+d)^2\right]\right\}\\ &\quad\cdot\frac{p(V_{\rm gs})\cdot V_{\rm ds}}{1+q(V_{\rm gs})\cdot V_{\rm ds}}. \end{aligned} \tag{4}$$

In addition, the transfer and output characteristics change with the ambient temperature $T$, so the expression of $I_{\rm ds}$ should consider the influence of the temperature. Based on (4), $V_{\rm gs}$ and $V_{\rm ds}$ are replaced by temperature-dependent equations for $V_{\rm gs}\,(T)$ and $V_{\rm ds}\,(T)$, as follows:

$$\begin{cases} V_{\rm gs}(T)=[m_{\rm gs}(T)\cdot V_{\rm gs}+n_{\rm gs}(T)]\\ V_{\rm ds}(T)=[m_{\rm ds}(T)\cdot V_{\rm ds}+n_{\rm ds}(T)]. \end{cases} \tag{5}$$

Since the datasheet of SiC MOSFET only provides the transfer and output characteristics curves at –40, 25, and 150 °C, the quadratic functions are used to fit $m_{\rm gs}(T)$, $n_{\rm gs}(T)$, $m_{\rm ds}(T)$, and $n_{\rm ds}(T)$ in (5), as follows:

$$\begin{cases} m_{\rm gs}(T)=m_1\cdot(T-25)^2+m_2\cdot(T-25)+1\\ n_{\rm gs}(T)=n_1\cdot(T-25)^2+n_2\cdot(T-25)\\ m_{\rm ds}(T)=m_3\cdot(T-25)^2+m_4\cdot(T-25)+1\\ n_{\rm ds}(T)=n_3\cdot(T-25)^2+n_4\cdot(T-25) \end{cases} \tag{6}$$

where $m_1$–$m_4$ and $n_1$–$n_4$ are the parameters to be determined based on the temperature characteristic.

Then, the expression of $I_{\rm ds}$ with temperature-dependent parameters can be rewritten as (7)

$$\begin{aligned} I_{\rm ds}&=k\cdot\{1+\tanh[a\cdot(V_{\rm gs}(T)+c)+b\cdot(V_{\rm gs}(T)+d)^2]\}\\ &\quad\cdot\frac{p(V_{\rm gs}(T))\cdot V_{\rm ds}(T)}{1+q(V_{\rm gs}(T))\cdot V_{\rm ds}(T)}. \end{aligned} \tag{7}$$

### B. Body Diode $D_b$

The modeling of body diode $D_b$ is based on the PSpice diode model. The static characteristic and the junction capacitor $C_j$ are included in this PSpice diode model. Where $C_j$ can be considered as the drain–source capacitor $C_{\rm ds}$ of SiC MOSFET.

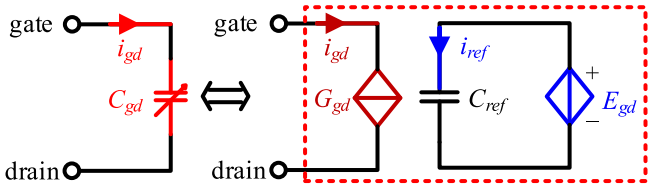


Fig. 2. Equivalent model of $C_{\rm gd}$.

According to the datasheet of the SiC MOSFET, the static characteristic of $D_b$ changes with the ambient temperature $T$, so the temperature characteristic should also be considered in the diode model.

In the PSpice diode model, different characteristics are decided by different model parameters [18]. The static characteristic is decided by the reverse saturation current $I_S$, the emission coefficient $N$, the parasitic resistance $R_S$, and the reverse breakdown voltage $V_{\rm BV}$, as follows:

$$I_{\rm sd} = I_S \cdot (e^{q\cdot(V_{\rm sd}-I_{\rm sd}\cdot R_S)/N\cdot k\cdot T} - 1) \tag{8}$$

where $I_{\rm sd}$ is the current of $D_b$, $V_{\rm sd}$ is the voltage across $D_b$, $q$ is the electron charge, and $k$ is the Boltzmann's constant.

In (8), the values of $I_S$ and $R_S$ change with $T$, and they are decided by the bandgap voltage $V_{\rm EG}$, temperature exponent $X_{TI}$, temperature coefficient (linear) $T_{RS1}$, and temperature coefficient (quadratic) $T_{RS2}$, as follows:

$$\begin{cases} I_S(T) = I_S \cdot e^{(T/25-1)\cdot V_{\rm EG}\cdot q/N\cdot k\cdot T} \cdot (T/25)^{X_{TI}/N} \\ R_S(T) = R_S \cdot [1 + T_{RS1}\cdot(T-25) + T_{RS2}\cdot(T-25)^2]. \end{cases} \tag{9}$$

$C_{\rm ds}$ is decided by the zero-bias p-n capacitance $C_{JO}$, the p-n gradient factor $M$, the p-n potential $V_J$, the forward-bias depletion capacitance coefficient $F_C$, and the transit time $T_T$, as follows: Eqn. (10) as shown bottom of this page.

### C. Gate-Drain Capacitor $C_{gd}$

According to the $C_{\rm gd}$–$V_{\rm gd}$ curves provided in the datasheet of the SiC MOSFET, $C_{\rm gd}$ depends on the gate-drain voltage $V_{\rm gd}$, so the normal linear capacitor model in PSpice cannot meet the accuracy requirement of $C_{\rm gd}$ [19]. In this paper, a voltage-controlled voltage source $E_{\rm gd}$, normal linear capacitor $C_{\rm ref}$, and current-controlled current source $G_{\rm gd}$ are used to model the voltage-controlled capacitor $C_{\rm gd}$, as shown in Fig. 2.

In Fig. 2, $E_{\rm gd}$ is used to provide the changed voltage, which is dependent on $V_{\rm gd}$. $C_{\rm ref}$ is used to realize the differential characteristic d$V_{\rm gd}$/d$t$ of $C_{\rm gd}$. Then, the current $i_{\rm ref}$ is dependent on $V_{\rm gd}$, as follows:

$$\begin{cases} E_{\rm gd} = f(V_{\rm gd}) \\ i_{\rm ref} = C_{\rm ref}\frac{dE_{\rm gd}}{dt} = C_{\rm ref}\frac{dE_{\rm gd}}{dV_{\rm gd}}\cdot\frac{dV_{\rm gd}}{dt}. \end{cases} \tag{11}$$

$G_{\rm gd}$ is used to get the voltage-controlled current $i_{\rm ref}$ and the equation for $G_{\rm gd}$ is

$$i_{\rm gd} = \frac{1}{C_{\rm ref}} i_{\rm ref}. \tag{12}$$

By substituting (11) into (12), the current $i_{\rm gd}$ can be expressed as

$$i_{\rm gd} = \frac{dE_{\rm gd}}{dV_{\rm gd}}\cdot\frac{dV_{\rm gd}}{dt}. \tag{13}$$

In addition, the current $i_{\rm gd}$ is the equivalent current through $C_{\rm gd}$, so it can be expressed as

$$i_{\rm gd} = C_{\rm gd}\cdot\frac{dV_{\rm gd}}{dt}. \tag{14}$$

Then, the relationship between $C_{\rm gd}$ and $E_{\rm gd}$ can be obtained from (13) and (14), which is shown as

$$E_{\rm gd} = \int C_{\rm gd} dV_{\rm gd}. \tag{15}$$

According to the $C_{\rm gd}$–$V_{\rm gd}$ curves, the equation of $C_{\rm gd}$–$V_{\rm gd}$ can be obtained, and the equation of $E_{\rm gd}$–$V_{\rm gd}$ can be obtained by (15), as follows:

$$\begin{cases} C_{\rm gd} = s_1\cdot\dfrac{1}{1+e^{\frac{s_2-V_{\rm gd}}{s_3}}} + s_4\cdot\dfrac{1}{1+e^{\frac{s_5-V_{\rm gd}}{s_6}}} + s_7 \\ E_{\rm gd} = s_1\cdot s_3\cdot\ln\left(1+e^{\frac{V_{\rm gd}-s_2}{s_3}}\right) + s_4\cdot s_6 \\ \qquad \cdot\ln\left(1+e^{\frac{V_{\rm gd}-s_5}{s_6}}\right) + s_7\cdot V_{\rm gd} \end{cases} \tag{16}$$

where $s_1$–$s_7$ are related parameters of the $C_{\rm gd}$–$V_{\rm gd}$ characteristic.

### D. Internal Gate Resistor $R_g$ and Gate-Source Capacitor $C_{gs}$

The internal gate resistor $R_g$ uses the normal PSpice resistor model, and the value is set as 1.3 Ω, in accordance with the datasheet [16].

According to the $C_{\rm gs}$–$V_{\rm gs}$ characteristic curves provided in the datasheet of the SiC MOSFET, the gate-source capacitance $C_{\rm gs}$ almost does not change with $V_{\rm gs}$, so the normal PSpice capacitor model is satisfactory. The value of the capacitor is set at 3700 pF according to the datasheet [16].

### E. Model Parameter Extraction

In this paper, the parameters of $I_{\rm ds}$–$V_{\rm ds}$, $I_{\rm ds}$–$V_{\rm gs}$, and $C_{\rm gd}$–$V_{\rm gd}$ characteristics are extracted by two software programs: GetData Graph Digitizer (GetData) and First Optimization (1stOpt) [15]. GetData is a program for digitizing graphs and plots, which can be used to obtain the original data from graphs or plots. Since $I_{\rm ds}$–$V_{\rm ds}$, $I_{\rm ds}$–$V_{\rm gs}$, and $C_{\rm gd}$–$V_{\rm gd}$ characteristic curves are provided in the datasheet of SiC MOSFET, the data of $I_{\rm ds}$–$V_{\rm ds}$, $I_{\rm ds}$–$V_{\rm gs}$,

$$C_{\rm ds} = \begin{cases} T_T\cdot dI_{\rm sd}/dV_{\rm sd} + C_{JO}\cdot(1+V_{\rm ds}/V_J)^{-M} & V_{\rm sd} \le F_C\cdot V_J \\ T_T\cdot dI_{\rm sd}/dV_{\rm sd} + C_{JO}\cdot(1-F_C)^{-(1+M)}\cdot[1-F_C\cdot(1+M)-M\cdot V_{\rm ds}/V_J], & V_{\rm sd} > F_C\cdot V_J \end{cases} \tag{10}$$

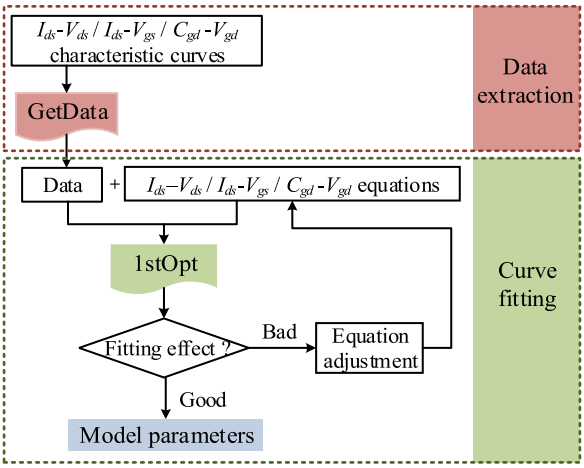


Fig. 3. Parameter-extraction method for SiC MOSFET model.

TABLE I
PARAMETERS OF $I_{\rm ds}$ AT 25 °C

| Parameters | $k$ | $a$ | $b$ | $c$ | $d$ |
|---|---|---|---|---|---|
| Values | 2.2321 | 0.3126 | -0.0083 | -10.2432 | -2.2259 |

TABLE II
TEMPERATURE-DEPENDENT PARAMETERS OF $I_{\rm ds}$

| Parameters | $m_1$ | $m_2$ | $m_3$ | $m_4$ |
|---|---|---|---|---|
| Values | 7.91e-6 | -1.45e-3 | -2.13e-5 | -1.22e-3 |
| Parameters | $n_1$ | $n_2$ | $n_3$ | $n_4$ |
| Values | -5.92e-5 | 3.97e-2 | 1.69e-5 | -2.81e-3 |

TABLE III
PARAMETERS OF $C_{\rm gd}$

| Parameters | $s_1$ | $s_2$ | $s_3$ | $s_4$ |
|---|---|---|---|---|
| Values | -523.1 | -0.775 | -0.198 | -460.1 |
| Parameters | $s_5$ | $s_6$ | $s_7$ | |
| Values | -7.97 | -2.54 | 997.1 | |

and $C_{\rm gd}$–$V_{\rm gd}$ curves can be obtained by GetData. 1stOpt is a mathematical optimization analysis program. Put the obtained data of $I_{\rm ds}$–$V_{\rm ds}$, $I_{\rm ds}$–$V_{\rm gs}$, and $C_{\rm gd}$–$V_{\rm gd}$ curves and the (4)–(7) and (16) into 1stOpt, the required parameters in (4)–(7) and (16) can be obtained by the unique global optimization algorithm of 1stOpt. According to the fitting effect, the above-mentioned parameters could be adjusted lightly to obtain the accurate SiC MOSFET model. The parameter-extraction method for the SiC MOSFET model is shown in Fig. 3.

After the parameter extraction, the equations of $p(V_{\rm gs})$ and $q(V_{\rm gs})$ in (4) can be obtained as

$$\begin{cases} p(V_{\rm gs}) = -34.9296 \cdot e^{0.01144 \cdot V_{\rm gs}} + 43.9896 \\ q(V_{\rm gs}) = 72.0433 \cdot e^{(-8.813\times10^{-5}) \cdot V_{\rm gs}} - 71.9656. \end{cases} \tag{17}$$

The parameters of $I_{\rm ds}$ at 25 °C are presented in Table I, and the temperature-dependent parameters of $I_{\rm ds}$ are presented in Table II. The parameters of $C_{\rm gd}$ are presented in Table III.

TABLE IV
PARAMETERS OF $D_b$

| Parameters | Description | Values |
|---|---|---|
| $I_S$ | Saturation current | 1.1256e-5 |
| $N$ | Emission coefficient | 9.095 |
| $R_S$ | Parasitic resistance | 0.018 |
| $V_{BV}$ | Reverse breakdown knee voltage | 1700 |
| $C_{JO}$ | Zero-bias $p$-$n$ capacitance | 2357p |
| $M$ | $p$-$n$ grading coefficient | 0.46495 |
| $V_J$ | $p$-$n$ potential | 3.82 |
| $F_C$ | Forward-bias depletion capacitance coefficient | 0.5 |
| $T_T$ | Transit time | 10n |
| $V_{EG}$ | Bandgap voltage (barrier height) | 0.7 |
| $X_{TI}$ | $I_S$ temperature exponent | 130 |
| $T_{RS1}$ | $R_S$ temperature coefficient (linear) | -5.423e-3 |
| $T_{RS2}$ | $R_S$ temperature coefficient (quadratic) | 2.842e-5 |

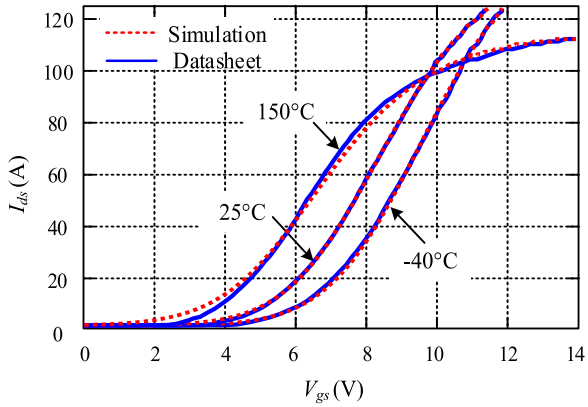


Fig. 4. Transfer characteristic comparison results between simulation (dashed) and datasheet (solid) at –40, 25, and 150 °C.

The parameters of $D_b$ can be extracted by Model Editor (PSpice modeling tool). The parameters of $D_b$ can be automatically extracted by inputting the data (extracted by GetData), which are shown in Table IV.

## III. VERIFICATION OF THE PROPOSED MODEL

The static and dynamic characteristics of the proposed non-segmented SiC MOSFET model with temperature-dependent parameters are verified by simulation and experiment in this section.

### A. Verification of Static Characteristic

The static characteristic is verified by comparing the PSpice simulation results obtained by the proposed model with the characteristic curves provided by the datasheet.

The simulation curves of transfer and output characteristics can be obtained by dc sweep analysis in PSpice for $V_{\rm gs}$ and $V_{\rm ds}$, respectively. The comparison results between the simulation and datasheet are shown in Figs. 4 and 5. The simulation curves are in good agreement with the datasheet curves.

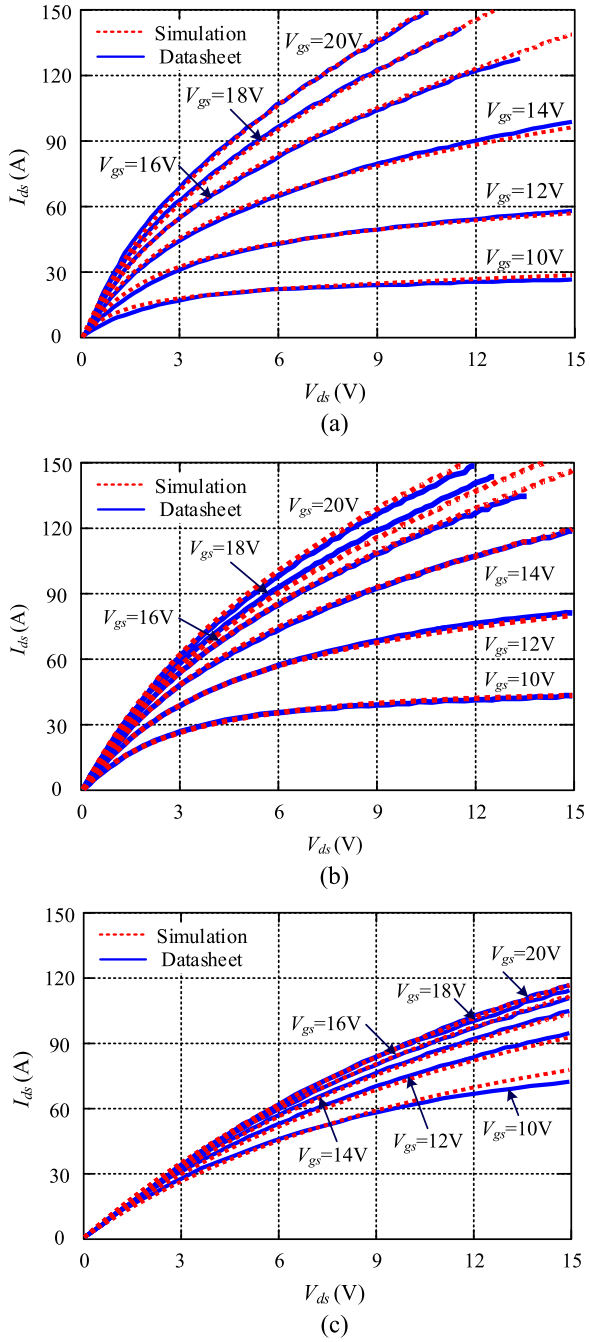


Fig. 5. Output characteristic comparison results between simulation (dashed) and datasheet (solid) at (a) –40 °C; (b) 25 °C; and (c) 150 °C.

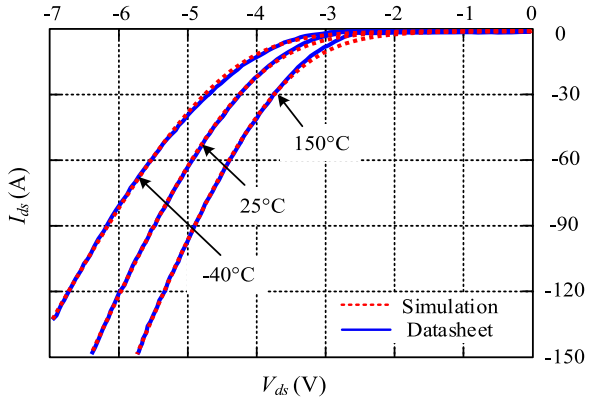


Fig. 6. Body diode static characteristic comparison results between simulation (dashed) and datasheet (solid) at –40, 25, and 150 °C.

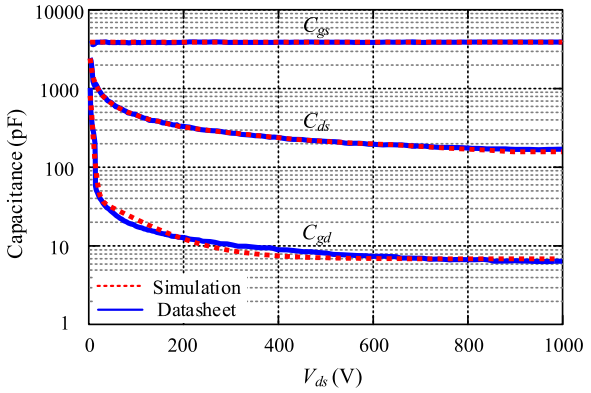


Fig. 7. Comparison between the simulation curves (dashed) of $C_{\rm gs}$, $C_{\rm ds}$, and $C_{\rm gd}$, and those curves (solid) on datasheet.

The simulation curves of the body diode static characteristic can be obtained by dc sweep analysis in PSpice for source–drain voltage $V_{\rm sd}$. The comparison results between the simulation and datasheet are shown in Fig. 6. The simulation curves are in good agreement with the datasheet curves.

The simulation curves of $C_{\rm gd}$ can be obtained based on (16) and the parameters in Table III. Inputting the extracted data of $C_{\rm ds}$–$V_{\rm ds}$ into Model Editor, the simulation curves of $C_{\rm ds}$ can be obtained automatically. Furthermore, $C_{\rm gs}$ is constant as mentioned before, so the simulation curves of $C_{\rm gs}$ are in a straight line. The comparison between the simulation curves of $C_{\rm gs}$, $C_{\rm ds}$, and $C_{\rm gd}$, and those curves on datasheet are shown in Fig. 7. The simulation curves are in good agreement with the datasheet curves.

### *B. Verification of Dynamic Characteristic*

To verify the dynamic characteristic of the proposed model under switching conditions, a double-pulse simulation platform and an experiment platform of the SiC MOSFET were built. The double-pulse circuit schematic is shown in Fig. 8.

The two switching devices of the double-pulse circuit use the selected type of SiC MOSFET, C2M0045170D. The digital isolator with the type Si8271 and the driver IC with the type IXDN609SI are adopted as the gate driver of $Q_2$. Actually, $Q_1$ is always turned OFF with negative gate-source voltage bias in double-pulse circuit, and only its body diode works as a freewheeling diode when $Q_2$ is turned OFF. Furthermore, to predict the voltage and current transient spikes, ringing, and shocks, the circuit stay inductors $L_{\sigma 1}$–$L_{\sigma 4}$ are also considered in the simulation; these can be extracted by Ansoft Q3D [20], [21]. The extracted stray inductances $L_{\sigma 1}$–$L_{\sigma 4}$ are shown in Table V.

The double-pulse experiment platform is shown in Fig. 9, and the instrument types and parameters used in the experiment platform are shown in Table VI.

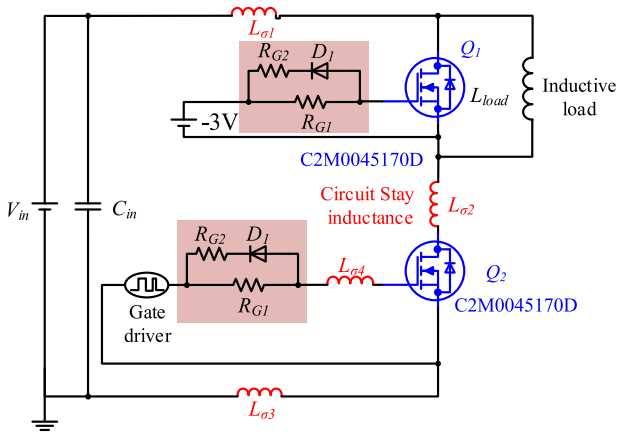


Fig. 8. Double-pulse circuit schematic.

TABLE V
STRAY INDUCTANCES OF DOUBLE-PULSE CIRCUIT

| Parameters | $L_{\sigma 1}$ | $L_{\sigma 2}$ | $L_{\sigma 3}$ | $L_{\sigma 4}$ |
|---|---|---|---|---|
| Values (nH) | 10 | 25 | 10 | 6 |

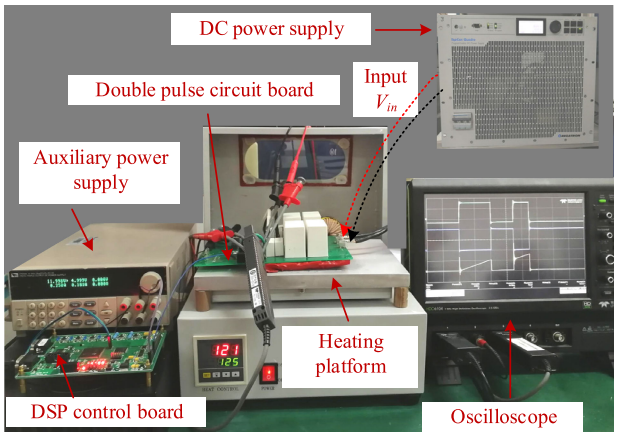


Fig. 9. Double-pulse circuit experiment platform.

TABLE VI
TYPES AND PARAMETERS OF EXPERIMENT INSTRUMENTS

| Instruments | Types | Parameters |
|---|---|---|
| DC power supply | TopCon Quadro | 0-1,000V |
| Auxiliary power supply | IT6322 | 0-30V×2, 0-5V×1 |
| Heating platform | MWJ-3020 | 0-350°C |
| Oscilloscope | HDO6104 | 1 GMHz |
| Voltage probe | P5200A | 50 MHz/1,300 V |
| Current probe | CP030A | 50 MHz/30 A |
| DSP control board | TMS320F28335 | |

Because the heating platform could only increase the ambient temperature, the double-pulse circuit is tested at 25, 75, and 125 °C. At 25 °C, the input voltage of the double-pulse circuit is 700 V; at 75 and 125 °C, the input voltage is reduced to 400 V for safety. The double-pulse circuit parameters used in simulation and experiment are shown in Table VII.

TABLE VII
DOUBLE-PULSE CIRCUIT PARAMETERS USED IN SIMULATION AND EXPERIMENT

| Parameters | Input Voltage $V_{in}$ (V) | Load Current (A) | |
|---|---|---|---|
| Values | 700 (25°C)<br>400 (75°C, 125°C) | 30.13 (25°C)<br>17.22 (75°C, 125°C) | |
| Parameters | Inductive Load $L_{load}$ (μH) | Gate Resistance $R_{G1}$ (Ω) | $R_{G2}$ (Ω) |
| Values | 355 | 15 | 20 |

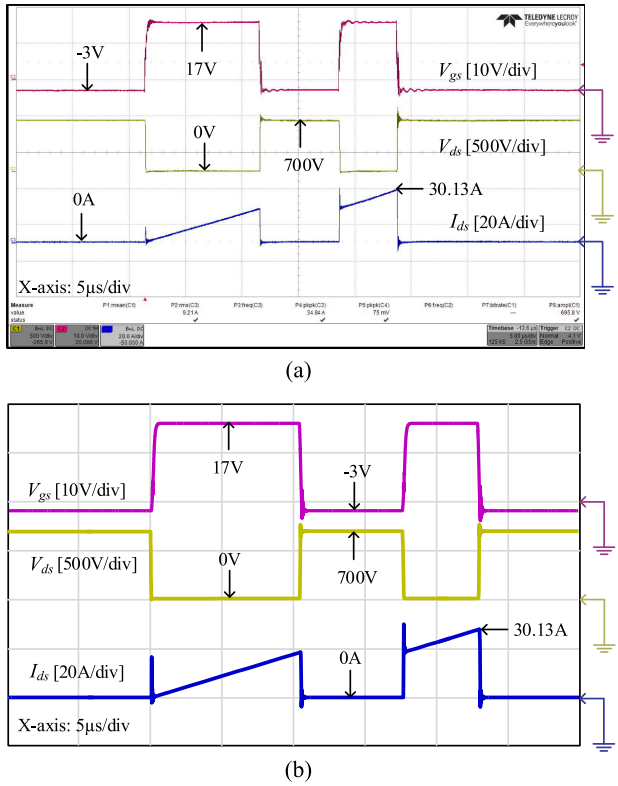


Fig. 10. Voltage and current waveforms of $Q_2$ at 25 °C. (a) Experiment. (b) Simulation.

The experiment and simulation waveforms of $Q_2$ at 25 °C are shown in Fig. 10.

To observe the reverse recovery characteristic of the body diode, the first turn-OFF transient and second turn-ON transient waveforms are compared between the simulation and experiment. The comparison results of voltage and current waveforms at 25, 75, and 125 °C are shown in Figs. 11, 12, and 13, respectively.

It can be seen that the voltage and current waveforms of the simulation and experiment are basically consistent at 25, 75, and 125 °C, but the stray parameters of the circuit cannot be fully considered, so there are still some differences between the simulation and experiment.

Furthermore, to verify the accuracy of the proposed model more intuitively, the rise and fall times of the voltage and current are compared between the simulation and experiment. The

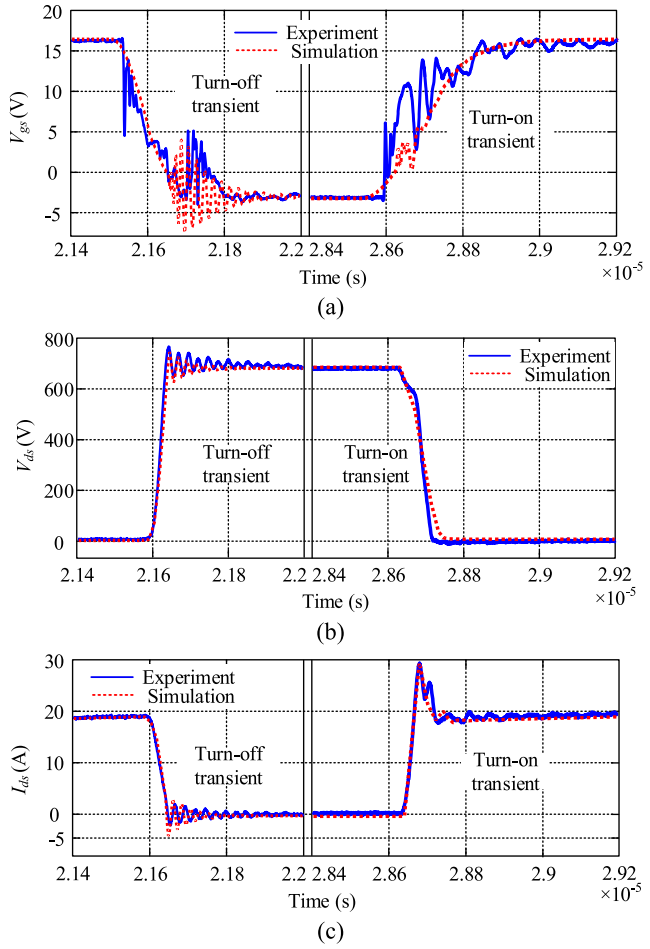


Fig. 11. Comparison results between simulation (dashed) and experiment (solid) at 25 °C. (a) $V_{\rm gs}$. (b) $V_{\rm ds}$. (c) $I_{\rm ds}$.

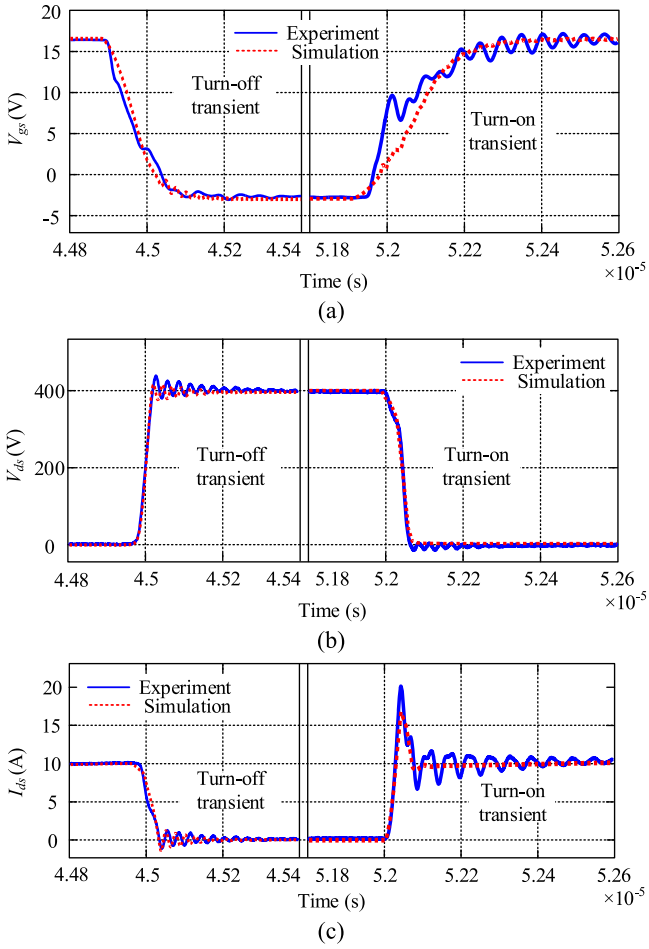


Fig. 12. Comparison results between simulation (dashed) and experiment (solid) at 75 °C. (a) $V_{\rm gs}$. (b) $V_{\rm ds}$. (c) $I_{\rm ds}$.

rise time $t_{rv}$ ($t_{ri}$) represents the time from 10% $V_{\rm ds}$ (10% $I_{\rm ds}$) to 90% $V_{\rm ds}$ (90% $I_{\rm ds}$) for the first time, and the fall time $t_{fv}$ ($t_{fi}$) represents the time from 90% $V_{\rm ds}$ (90% $I_{\rm ds}$) to 10% $V_{\rm ds}$ (10% $I_{\rm ds}$) for the first time. The comparison results between the simulation and experiment are shown in Tables VIII, IX, and X, respectively.

At 25, 75, and 125 °C, the errors of the rise time and fall time are all very low. Due to the differences in $V_{\rm gs}$ at 25 °C between the simulation and experiment, the errors of the rise time and fall time at 25 °C are larger than at 75 and 125 °C. The comparison results prove the accuracy of the proposed non-segmented SiC MOSFET model with temperature-dependent parameters, so the proposed non-segmented model can be used to simulate the dynamic characteristics of a SiC MOSFET under different ambient temperatures.

## IV. Simulation Convergence Verification of Proposed Model

To verify the simulation convergence of the proposed non-segmented SiC MOSFET model for the C2M0045170D, the proposed non-segmented model, the conventional segmented model [12], and the model from the manufacturer official website [22] are compared by putting them into the same full-bridge inverter circuit, as shown in Fig. 14.

In Fig. 14, the drive signals $V_{g1}$–$V_{g4}$ of $S_1$–$S_4$ are generated by unipolar sinusoidal pulsewidth modulation (SPWM), as shown in Fig. 15. The modulation wave $V_m$ is a sine wave with 0.75 V/50 Hz, and the carrier $V_c$ is a triangle wave with 1 V and 4 kHz in this paper. The simulation circuit parameters are presented in Table XI.

The simulation results of the inverter are shown in Fig. 16. Fig. 16(a) shows that the full-bridge inverter can be simulated well with the proposed non-segmented model, and the waveforms of the bridge arm midpoints voltage $V_b$ and output voltage $V_o$ are both correct. However, this inverter with the conventional segmented model and the model from the manufacturer cannot work normally due to the convergence problem, as shown in Fig. 16(b) and (c).

To further compare the simulation convergence of these three models, the full-bridge inverter is simplified by removing the inductor $L$ and capacitor $C$ in Fig. 14, as shown in Fig. 17, and the simulation accuracy is reduced by increasing the maximum simulation step size in PSpice.

Then, the simplified inverter is simulated again with these three models. The simulation waveforms are shown in Fig. 18.

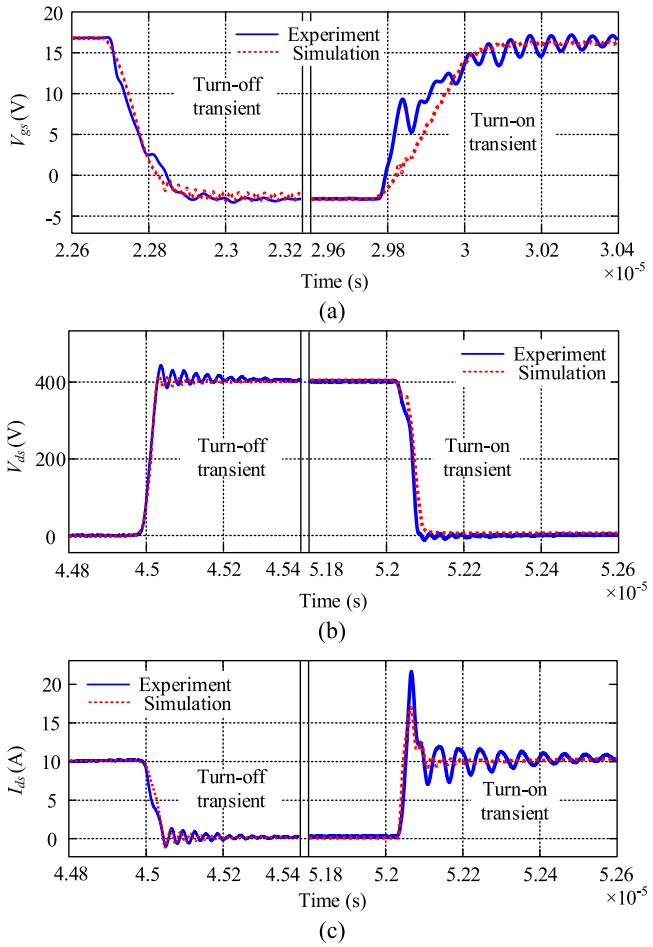


Fig. 13. Comparison results between simulation (dashed) and experiment (solid) at 125 °C. (a) $V_{gs}$. (b) $V_{ds}$. (c) $I_{ds}$.

TABLE VIII
COMPARISON RESULTS OF RISE TIME AND FALL TIME AT 25 °C

| Parameters | Voltage rise time $t_{rv}$ | Current rise time $t_{ri}$ | Voltage fall time $t_{fv}$ | Current fall time $t_{fi}$ |
|---|---|---|---|---|
| **Experiment (ns)** | 27.797 | 23.125 | 59.6 | 37.2 |
| **Simulation (ns)** | 33.02 | 19.91 | 79.18 | 37.00 |
| **Error (%)** | 18.79 | 13.9 | 32.85 | 0.53 |

TABLE IX
COMPARISON RESULTS OF RISE TIME AND FALL TIME AT 75 °C

| Parameters | Voltage rise time $t_{rv}$ | Current rise time $t_{ri}$ | Voltage fall time $t_{fv}$ | Current fall time $t_{fi}$ |
|---|---|---|---|---|
| **Experiment (ns)** | 30.528 | 16.258 | 44.998 | 43.003 |
| **Simulation (ns)** | 27.391 | 14.222 | 42.24 | 45.123 |
| **Error (%)** | 10.27 | 12.52 | 6.13 | 4.93 |

Fig. 18 shows that the simulation waveform of the output voltage $V_o$ with the proposed non-segmented model is correct. With the conventional segmented model, the simulation waveform of $V_o$ is seriously distorted; and with the model from the manufacturer official website, the inverter in Fig. 17 still cannot run normally due to the convergence problem. The comparison results verify the good simulation convergence of the proposed non-segmented SiC MOSFET model in this paper.

TABLE X
COMPARISON RESULTS OF RISE TIME AND FALL TIME AT 125 °C

| Parameters | Voltage rise time $t_{rv}$ | Current rise time $t_{ri}$ | Voltage fall time $t_{fv}$ | Current fall time $t_{fi}$ |
|---|---|---|---|---|
| **Experiment (ns)** | 30.628 | 13.899 | 39.982 | 41.594 |
| **Simulation (ns)** | 29.645 | 14.408 | 39.233 | 37.93 |
| **Error (%)** | 3.21 | 3.66 | 1.87 | 8.81 |

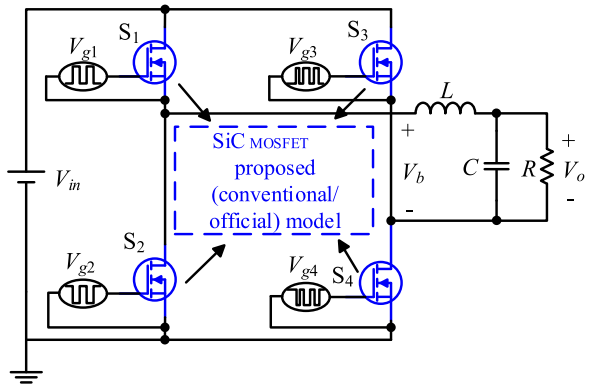


Fig. 14. Full-bridge inverter.

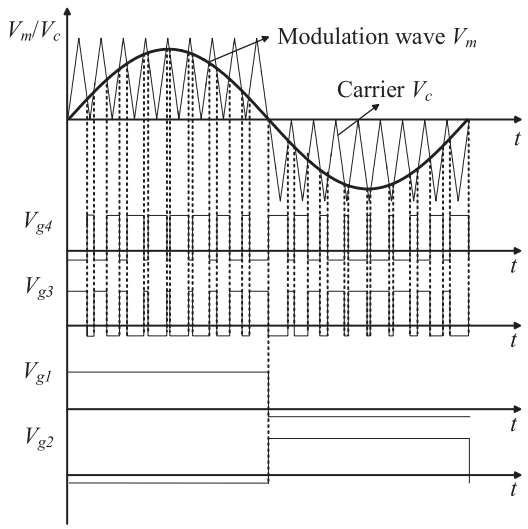


Fig. 15. Dive signals for $S_1$–$S_4$ under unipolar SPWM.

TABLE XI
SIMULATION PARAMETERS OF FULL-BRIDGE INVERTER

| Parameters | Input voltage $V_{in}$ (V) | Inductance $L$ (mH) | Capacitance $C$ (μF) |
|---|---|---|---|
| **Values** | 311 | 2 | 230 |
| **Parameters** | Resistance $R$ (Ω) | Drive signals $V_{g1}$-$V_{g4}$ (V) | Output voltage frequency $f$ (Hz) |
| **Values** | 5.3 | -5/20 | 50 |

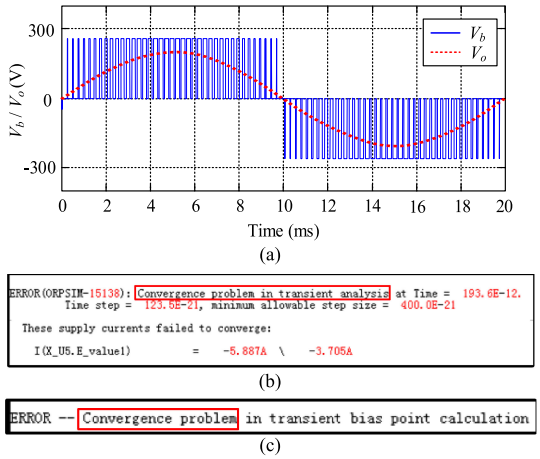


Fig. 16. Simulation results of the full-bridge inverter. (a) With the proposed non-segmented model. (b) With the conventional segmented model. (c) With the model from the manufacture.

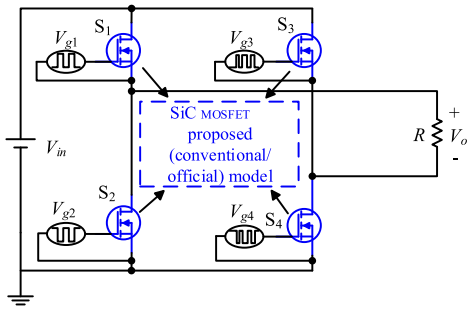


Fig. 17. Topology of the simplified full-bridge inverter.

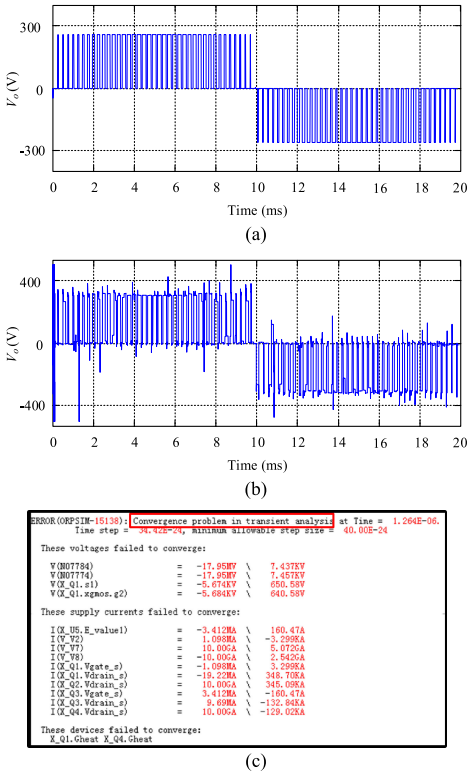


Fig. 18. Simulation results of the simplified full-bridge inverter. (a) With the proposed non-segmented model. (b) With the conventional segmented model. (c) With the model from the manufacturer.

## V. Conclusion

In this paper, a non-segmented PSpice model of a SiC MOSFET with temperature-dependent parameters is proposed. The static characteristic of the proposed non-segmented model is well verified based on the datasheet, and the dynamic characteristic at different ambient temperatures (25, 75, and 125 °C) is verified based on a double-pulse experiment platform. Furthermore, the proposed model of a SiC MOSFET is applied to a real power electronics circuit simulation, and the good simulation convergence of the proposed non-segmented model is also proved by the simulation results of a full-bridge inverter compared to the conventional segmented model and the model from the manufacturer. Therefore, the proposed non-segmented PSpice model of SiC MOSFET with temperature-dependent parameters can be used for practical circuit simulation, making the design and analysis of power converters with SiC MOSFETs more convenient and efficient.

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