A New Grid-Connected DC/AC Inverter With Soft Switching and Low Current Ripple

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***Abstract*—This paper presents a new dc/ac inverter for low-power applications (i.e., high-voltage, low-current applications), which offers soft switching of the power semiconductors and low output current ripple. In the proposed power circuitry, a novel ripple steering approach is used that can provide soft switching for the power semiconductors and significantly attenuate the high-frequency current ripple of the inverter. The proposed ripple steering technique utilizes the switching frequency and the duty cycle in order to perform the aforementioned tasks. Basically, the ripple steering technique steers the energy of the ripple to the output capacitances of the power semiconductors in order to provide the soft-switching condition. Theoretical analysis, simulation results, and experimental results verify the feasibility of the proposed technique and demonstrate the superior performance of the proposed inverter.**

***Index Terms*—DC/AC converters, grid-connected converters, inductor current ripple, pulsewidth modulation (PWM), voltage source inverters (VSIs), zero voltage switching (ZVS).**

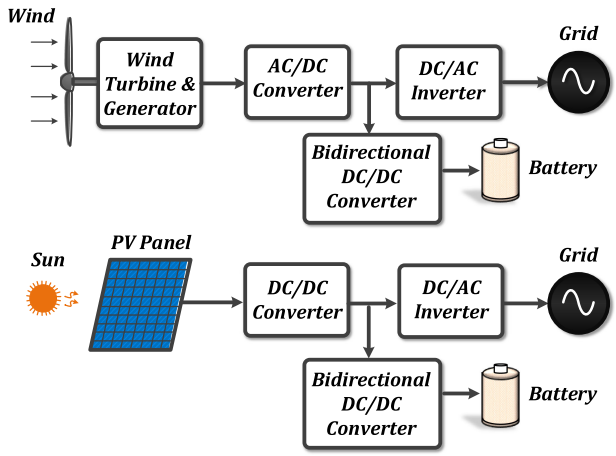

Fig. 1. Block diagram of renewable energy power conditioning system.

I. Introduction

THE limited supply of fossil fuel-based energies and growing global concerns about the imminence of climate change are leading causes as to why wind and solar are the fastest growing sources of energy worldwide. Solar and wind energy is harvested using solar panels and wind turbines, respectively [1], [2]. In solar and wind energy harvesting systems, power electronic converters are very efficient ways to integrate solar and wind energy into the power system [3], [4].

In wind and solar energy conversion systems, two-stage power conditioning systems are usually used. Fig. 1 shows typical two-stage power conditioning systems for wind and solar applications. According to Fig. 1, a dc/ac inverter is the interface to the grid [5], [6]. The main focus of this paper is on the design and implementation of a high-efficiency dc/ac inverter for these applications. DC/AC inverters are responsible for regulating the dc-bus voltage and shaping the output current to a nearly sinusoidal waveform synchronous with the utility grid [7]–[11]. Conventionally, full-bridge voltage source inverters (VSIs) are used to implement the dc/ac inverter for these applications. Even though VSIs are extensively used in many industrial products they suffer from some technical difficulties. One of the main difficulties with VSIs is the fact that they usually operate under hard switching where neither the voltage nor the current of the power semiconductors is zero during the switching transitions. The power semiconductors of the dc/ac converters are usually switched under very high voltage/current. Thus, switching losses of the power semiconductors in such inverters significantly contribute to the overall losses of the power conditioning system. In particular, the reverse-recovery losses of the power semiconductors' body diodes are inevitable for such power circuit topologies [12]. Because of the hard switching, the switching frequency of dc/ac converters is very limited (usually in the range of 5–20 kHz) in industrial products. Due to the strict regulatory standards (e.g., IEEE 1547, UL1741, etc.) on the amount of harmonics that can be present at the output of dc/ac inverters, a high quality current needs to be produced by grid-connected dc/ac inverters. To this end, dc/ac inverters usually require large filters at their outputs. Herein lies another difficulty with the currently used dc/ac inverters. Operating with low switching frequencies makes the output filter very bulky and creates a high amount of current ripple at the inverter's output inductor and in turn increased core losses. This current ripple not only increases the core losses of the inductor, but also increases the inductor's high-frequency copper losses. Thus, the impact

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of this current ripple on the power losses is twofold (i.e., core losses and high-frequency copper losses) [13]–[15]. In addition to the aforementioned drawbacks, the high frequency ripples and harmonics create a significant amount of EMI noise that may affect the operation of the control system and highly degrades the reliability of dc/ac inverters [16]–[18].

Various power circuit topologies have been proposed in order to improve the performance of dc/ac inverters in the literature [19]–[27]. In [28], a soft-switched dc/ac inverter is presented. In the proposed inverter, a high-frequency resonant network is added to the conventional hard-switching inverter in order to provide soft-switching condition. In addition, Bellar *et al.* [28] classify some types of soft-switched inverters with resonant networks based on both the location of the resonant network (e.g., at the load side, bridge side, or dc-bus side) and the type of employed resonant circuits (i.e., series or parallel). The main difficulty with the methods which utilize resonant circuits at the dc bus is that the auxiliary switch usually carries the main current. This increases the conduction losses. Furthermore, the auxiliary circuit usually contains several switches to provide soft-switching condition for power semiconductors that makes the circuitry complicated and costly. In [29], a soft-switching inverter with one dc-link switch is proposed which is in series with a coupled inductor. Although the number of switches is reduced in comparison to [28], the leakage inductance of the coupled inductor may cause very high voltage/current stresses on the switch. In [30]–[32], power circuits with coupled inductors are presented. In these circuit topologies, coupled inductors resonate with the dc-bus capacitor and the resonant energy is injected into the dc bus through magnetic coupling. The size of the coupled magnetics can be minimized since the magnetizing current can be reset in every switching cycle. However, the proposed topologies still suffer from having an extra active auxiliary circuit. In summary, existing techniques require many extra active/passive components. In particular, extra active circuits highly deteriorate the reliability of the system due to the additional complexity and cost imposed by the active components. Also, the effectiveness of these techniques is questionable. Smith and Smedley [33] present a control method to achieve zero voltage switching (ZVS) for dc/ac inverters without using extra auxiliary circuitry. The disadvantage of the method introduced in [33] is that low current ripple cannot be achieved.

Some studies have shown that soft switching in dc/ac inverters may add more losses and sacrifice the simplicity, robustness, and cost of inverters and, consequently, greatly offset their advantages. Because of this, most industrial products still use the conventional hard-switching inverters with large filters in order to ensure a reliable operation of dc/ac inverters. Even though the system's performance is highly compromised with hard-switching and bulky filters, industrial decision makers prefer to use a reliable well-known solution for dc/ac inverters [33].

In this paper, a soft switching topology along with a novel ripple steering technique is proposed to substantially improve the performance of dc/ac converters. The proposed technique effectively attenuates the current ripple at the output of the inverter by steering the ripple from the output filter to the capacitances of the power semiconductors in order to provide the ZVS condition. Reduced output current ripple results in substantially lower power losses of the output filter and improving the power quality of the inverter. The proposed soft commutation along with the ripple steering technique is implemented using digital control system. The control system is responsible for providing ZVS condition and performing the ripple steering technique. The proposed inverter is well suited for low power applications (e.g., solar microinverters), where switching losses greatly contribute to the overall losses and efficiency degradation (i.e., switching losses are dominant compared to the conduction losses). For high current applications, where the conduction losses are dominant, the proposed approach may not provide very efficient operation. However, for high-voltage low-current applications such as solar microinverters, the proposed approach can significantly improve the performance.

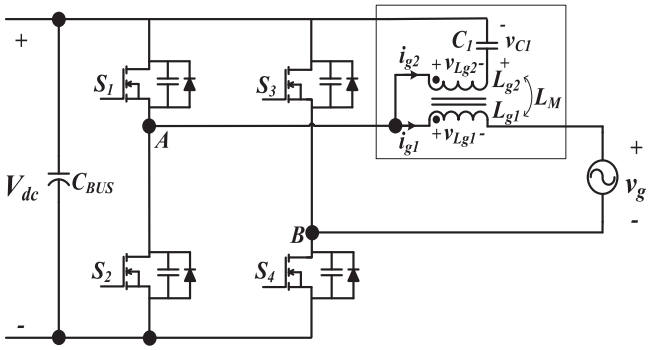


Fig. 2. Circuit diagram of the proposed soft-switched dc/ac inverter.

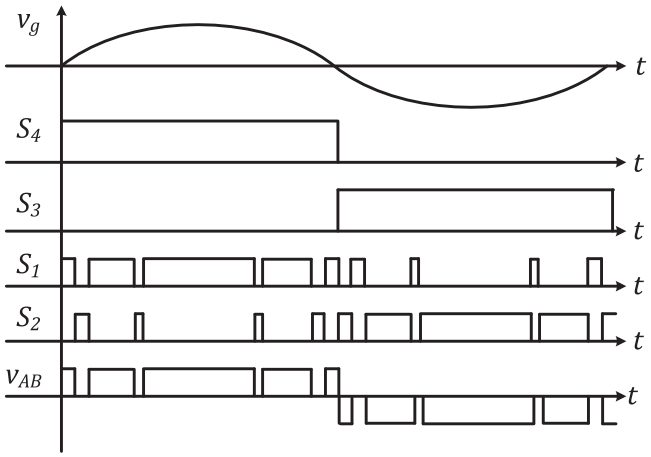


Fig. 3. Conceptual switching waveforms of the proposed inverter.

II. Proposed Soft-Switched DC/AC Inverter

In this section, the proposed soft-switched inverter is described. The main objective of the proposed approach is to introduce a power circuit, which can provide soft-switching without adding complex auxiliary circuits to the inverter. Fig. 2 shows the circuit diagram of the proposed inverter. According to Fig. 2, the dc/ac inverter includes a dc-bus capacitor, a full-bridge inverter, and an integrated magnetics. In the proposed circuitry, the energy of the output inductor's current ripple is utilized to provide soft-switching for the power semiconductors. Basically, the integrated magnetics steers the energy of the current ripple to the output capacitances of the power semicon-

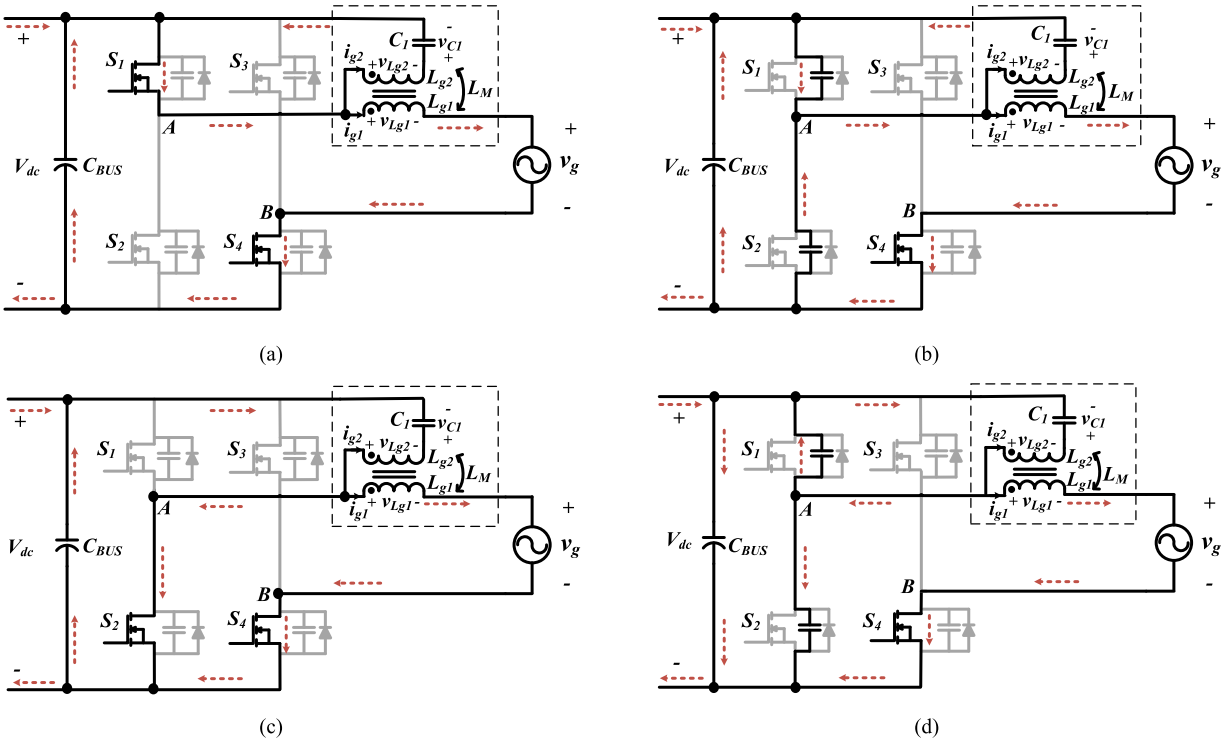


Fig. 4. Equivalent circuits of the proposed dc/ac inverter. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

ductors by charging one output capacitor and discharging the other one during switching transitions. Therefore, the semiconductors are switched ON at zero voltage. This eliminates the switching losses at turn-ON and also removes the reverse recovery losses of the body diodes of the power semiconductors. The proposed ripple steering technique is performed through properly controlling the duty cycle and the switching frequency in the digital control system. In order to clarify the operating principles of the proposed circuitry, various modes of operation will be described. The conceptual switching waveforms of the proposed inverter are sketched in Fig. 3. According to this figure, one of the legs (i.e., S_1 and S_2) is switched with high frequency, and the other leg (i.e., S_3 and S_4) is switched with the line frequency (e.g., 60 Hz).

In order to simplify the analysis, the following assumptions are considered.

1) All components are assumed to be ideal.
2) The inverter is in the steady-state condition.
3) The grid voltage v_g is primarily sinusoidal and approximately constant in each switching cycle.

The operating principles of the inverter will only be described for the positive half cycle (i.e., $V_g > 0$, S_3 is OFF, and S_4 is ON). Due to the symmetry, similar procedure can be applied to derive various modes of operation for the negative half cycle. In the positive half cycle, there are four modes of operation. Fig. 4 illustrates the equivalent circuits for each modes and Fig. 5 shows the key waveforms of the inverter for different time intervals. In the following, different modes of operation will be described.

1) *Mode I ($t_0 \le t < t_1$):* Fig. 4(a) shows the equivalent circuit during Mode I. In this mode, power semiconductor S_1 turns ON under ZVS condition (since its current is negative at t_0). The mathematical equation for the coupled inductor is given by

$$v_{L_{g_1}} = L_{g_1}\frac{di_{g_1}}{dt} + L_M\frac{di_{g_2}}{dt} \tag{1}$$

$$v_{L_{g_2}} = L_M\frac{di_{g_1}}{dt} + L_{g_2}\frac{di_{g_2}}{dt} \tag{2}$$

where the voltages across each inductor in Mode I are given by

$$v_{L_{g_1}} = V_{dc} - v_g \tag{3}$$

$$v_{L_{g_2}} = -v_{C1}. \tag{4}$$

In order to satisfy the volt-second balance for the coupled inductor, the low frequency component of v_{C1} must be equal to $v_g - V_{\rm dc}$ (during steady-state condition). Thus, the voltage across the capacitor C_1 can be decomposed into a low-frequency term, $v_g - V_{\rm dc}$ and a high-frequency term, $\hat{v}_{C1}$ as follows:

$$v_{C1} = v_g - V_{\rm dc} + \hat{v}_{C1}. \tag{5}$$

Equations (1)–(5) can be used to calculate the current ripples of the coupled inductors. The current ripples are given by

$$\frac{di_{g_1}}{dt} = \frac{V_{\rm dc} - v_g}{L_{g_1}}\eta - \frac{\hat{v}_{C1}}{L_{g_1}}\lambda_1 \tag{6}$$

$$\frac{di_{g_2}}{dt} = \frac{V_{\rm dc} - v_g}{L_{g_2}}\zeta - \frac{\hat{v}_{C1}}{L_{g_2}}\lambda_2 \tag{7}$$

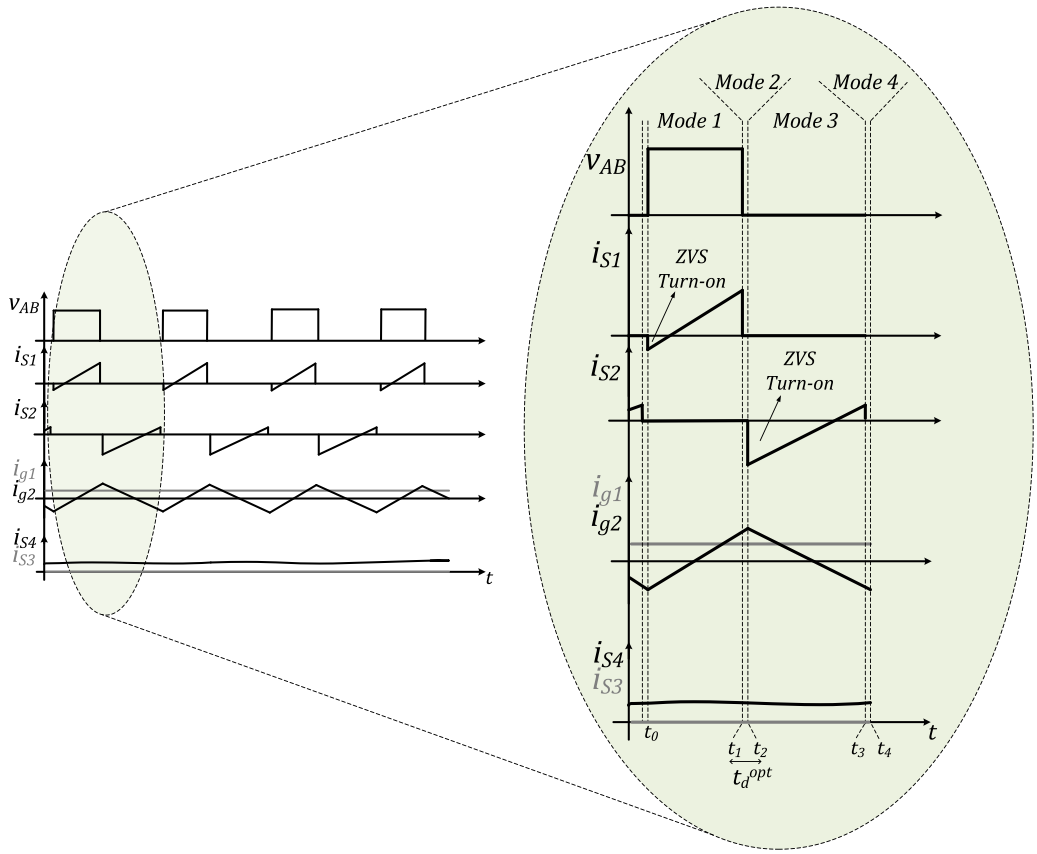


Fig. 5. Key waveforms of the inverter.

where

$$\eta = \frac{1 - L_M/L_{g_2}}{1 - k^2},\quad \lambda_1 = \frac{L_M/L_{g_2}}{1 - k^2},\quad \zeta = \frac{1 - L_M/L_{g_1}}{1 - k^2},$$

$$\lambda_2 = \frac{1}{1 - k^2},\quad k = \frac{L_M}{\sqrt{L_{g_1} L_{g_2}}}.$$

2) *Mode II ($t_1 \le t < t_2$):* This mode starts with turning the power semiconductor S_1 OFF. The reactive current provided by the coupled inductor charges the junction capacitance of MOSFET S_1 (C_{S_1}) and discharges the junction capacitance of MOSFET S_2 (C_{S_2}) and provides the ZVS condition for turning the power semiconductor S_2 ON. Since this time interval is relatively short, currents are approximately constant. This interval continues until C_{S_2} (output capacitance of S_2) is fully discharged and $i_{g_2}(t)$ reaches its maximum peak. Fig. 4(b) shows the equivalent circuit during this time interval. The current through the capacitances and the voltage across the capacitances of S_1 and S_2 are given by

$$I_{C_{S_1}} = -I_{C_{S_2}} = \frac{i_{g_1}(t_1) + i_{g_2}(t_1)}{2} \tag{8}$$

$$v_{C_{S_1}}(t) = \frac{1}{C_S}\int_{t_1}^{t} I_{C_{S_1}} d\tau \tag{9}$$

$$v_{C_{S_2}}(t) = \frac{1}{C_S}\int_{t_1}^{t} I_{C_{S_2}} d\tau + V_{\rm dc}. \tag{10}$$

Since the currents are approximately constant, the voltages across the capacitances at the end of this mode are given by

$$v_{C_{S_1}}(t_2) = \frac{1}{2C_S}\Big(i_{g_1}(t_1) + i_{g_2}(t_1)\Big)(t_2 - t_1) \tag{11}$$

$$v_{C_{S_2}}(t_2) = V_{\rm dc} - \frac{1}{2C_S}\Big(i_{g_1}(t_1) + i_{g_2}(t_1)\Big)(t_2 - t_1). \tag{12}$$

The aforementioned equations determine the optimal dead time of the gate pulses for S_1 and S_2. If the dead time is set such that the respective power semiconductor turns ON when its capacitor is completely discharged, the body diodes will not turn ON. Thus, the optimal operation is achieved. Otherwise, the body diode naturally turns ON and the current needs to commutate from the body diode to the MOSFET's channel when the power semiconductor turns ON. Thus, the optimal dead time is calculated using (11) or (12) as follows:

$$t_d^{\rm opt} = \frac{2C_S V_{\rm dc}}{i_{g_1}(t_1) + i_{g_2}(t_1)}. \tag{13}$$

3) *Mode III ($t_2 \le t < t_3$):* This mode starts when the power semiconductor S_2 turns ON under ZVS condition. Fig. 4(c) shows the equivalent circuit during this time interval. The

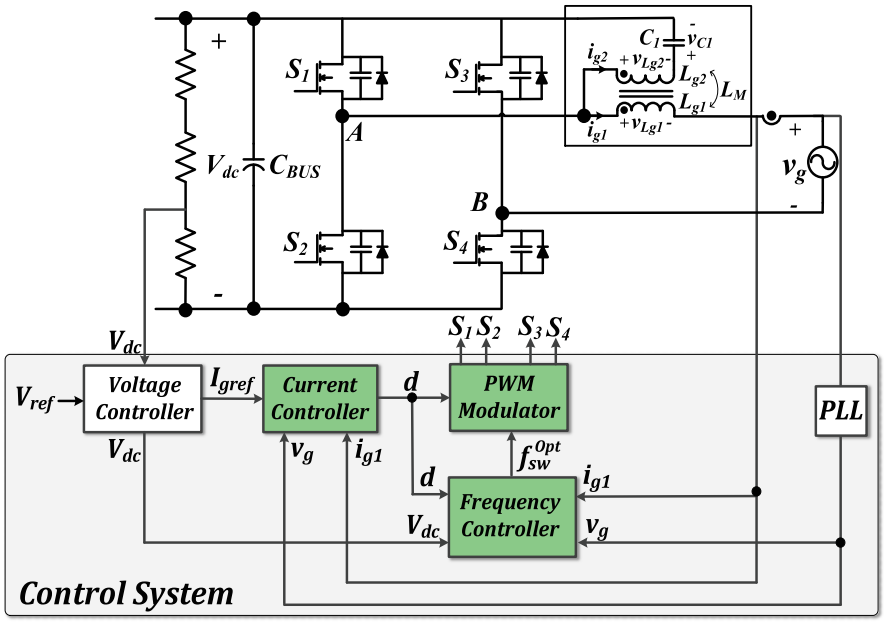


Fig. 6. Block diagram of the closed-loop control system.

current ripples through the coupled inductors are given by

$$\frac{di_{g_1}}{dt} = \frac{-v_g}{L_{g_1}}\eta + \frac{\hat{v}_{C1}}{L_{g_1}}\lambda_1 \tag{14}$$

$$\frac{di_{g_2}}{dt} = \frac{-v_g}{L_{g_2}}\zeta - \frac{\hat{v}_{C1}}{L_{g_2}}\lambda_2. \tag{15}$$

4) *Mode IV ($t_3 \leq t < t_4$):* This mode starts when the power semiconductor S_2 is turned OFF and the reactive current provided by the coupled inductor charges C_{S_2} and discharges C_{S_1}. This interval continues until C_{S_1} is fully discharged and the ZVS condition is provided for S_1. Equations for this Mode are very similar to Mode II. Fig. 4(d) shows the equivalent circuit during this time interval.

Equations (6) and (14) determine the output current ripple of the inverter. Ideally, the output current ripple should be as low as possible in order to have high power quality. In Section IV, the design of different parameters (e.g., η, ζ, etc.) will be discussed in order to have minimum output current ripple.

III. Control Approach of the Proposed Inverter

The control system of the proposed dc/ac inverter plays a crucial role in providing the ZVS condition for power semiconductors and attenuating the current ripple at the output of the inverter. The control system performs the optimal ripple steering from the output inductor to the output capacitances of the power semiconductors using the switching frequency and duty cycle. Fig. 6 shows the block diagram of the proposed control system for the dc/ac inverter. According to Fig. 6, the control system utilizes both the duty cycle and switching frequency in order to regulate the dc-bus voltage, shape the output current to a sinusoidal waveform synchronous with the grid voltage, and perform ripple steering. The duty cycle is used to regulate the dc-bus voltage and shape the output current and the switching frequency is responsible for ripple steering. Fortunately, the duty cycle control loop and the frequency control loop are decoupled. Thus, they will not create oscillatory behavior and instability for the dc/ac inverter.

The control system includes a voltage controller, a current controller, a frequency controller, a PWM modulator, and a phase-locked loop (PLL). The voltage controller is responsible for regulating the dc-bus voltage and it produces the reference value for the amplitude of the output current. The design and implementation of the voltage controller and the PLL have been described in the literature [6], [34], [35], [36], [37]. Thus, these blocks will not be described in this paper. There are some subtleties related to the design of the current controller and the pulsewidth modulator (PWM) in the closed-loop control system. These subtleties stem from the fact that one of the leg is switched based on the line voltage (i.e., grid voltage). In particular when S_4 is ON during the positive cycle, S_1 acts as the high side switch of the equivalent buck converter and its duty cycle determines the inverter's gain, whereas during the negative cycle, the roles of S_1 and S_2 are switched. Thus, the duty cycle of S_2 determines the inverter's gain. This creates discontinuity in the duty cycle if the conventional current controller and the PWM scheme are used. This discontinuity creates disturbances and current spikes at the zero crossings of the output current, where the roles of S_1 and S_2 are switched. The discontinuity of the control signal and current spikes at the zero crossings are illustrated in Fig. 7. Since the control direction is switched at the zero crossing points, the controller needs time to catch up and correct the direction to perform proper tracking. The discontinuity in the control signal (i.e., duty cycle) can be rectified by using the closed-loop control system shown in Fig. 8.

The proposed control system employs a current controller, which takes the absolute value of the grid voltage (the output voltage of the PLL) and the absolute value of the grid current in order to eliminate the discontinuity in the control signal and provide a stable operation. According to Fig. 8, the output grid voltage from PLL and the grid current are multiplied by the sign of the grid voltage in the modified current controller and,

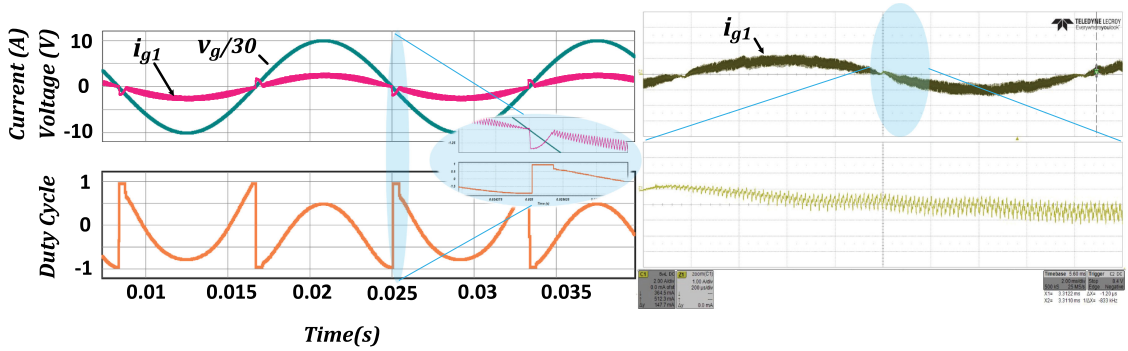


Fig. 7. Performance of the conventional closed-loop control system.

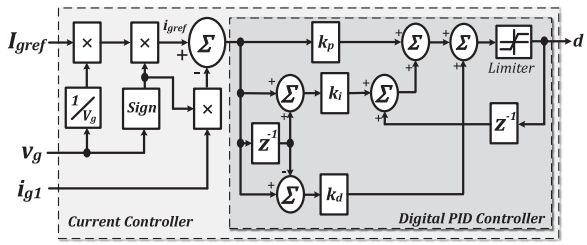


Fig. 8. Modified closed-loop current control system.

therefore, the direction of the duty cycle is preserved during the zero crossings of the voltage and a high quality current is produced at the output of the inverter. If the inverter works at nonunity power factor, the current controller continue working properly and the generated high-frequency current will follow the profile of the grid current since the phase shift of the grid current is provided by PLL.

Fig. 9 shows the performance of the modified current controller. According to this figure, the transitions are smooth at zero crossings due to the continuity of the control input (i.e., duty cycle). By comparing Figs. 7 and 9, it is clear that the duty cycle is discontinuous for the conventional current controller and it is continuous for the proposed current controller.

The direction of the control input (i.e., duty cycle) is switched during the transitions between the positive half cycle and negative half cycle. This can also be observed from the mathematical model of the proposed converter. According to Fig. 6, the dynamical equations of the system are given by

$$\Sigma_{\text{Inv}}: \begin{cases} \dfrac{di_{g_1}}{dt} = \dfrac{1}{\mu L_{g_1}}\left(V_{\text{dc}} S_{\text{inv}}^{\text{HF}} - v_g - V_{\text{dc}} - V_{\text{dc}} S_{\text{inv}}^{\text{LF}}\right) \\ \qquad\qquad -\dfrac{1}{\mu L_{g_1}}\dfrac{L_M}{L_{g_2}}\left(V_{\text{dc}} S_{\text{inv}}^{\text{HF}} - V_{\text{dc}} - v_{C_1}\right) \\ \dfrac{di_{g_2}}{dt} = \dfrac{1}{\mu L_{g_2}}\left(V_{\text{dc}} S_{\text{inv}}^{\text{HF}} - V_{\text{dc}} - v_{C_1}\right) \\ \qquad\qquad -\dfrac{1}{\mu L_{g_2}}\dfrac{L_M}{L_{g_2}}\left(V_{\text{dc}} S_{\text{inv}}^{\text{HF}} - v_g - V_{\text{dc}} - V_{\text{dc}} S_{\text{inv}}^{LF}\right) \\ \dfrac{di_{v_{C1}}}{dt} = \dfrac{1}{C_1} i_{g_2} \end{cases} \tag{16}$$

where $\mu = 1 - k^2$ and the high-frequency switching function $S_{\text{inv}}^{\text{HF}}$ and the low-frequency switching function $S_{\text{inv}}^{\text{LF}}$ are defined as

$$S_{\text{inv}}^{\text{HF}} \begin{cases} 1, & S_1 : \text{ON} \\ 0, & S_2 : \text{OFF} \end{cases}, \quad S_{\text{inv}}^{\text{LF}} \begin{cases} 1, & v_g \geq 0 \\ 0, & v_g < 0. \end{cases}$$

The low-frequency switching function $S_{\text{inv}}^{\text{LF}}$ is zero during the negative cycle and is unity during the positive cycle. According to the first equation of (16), this transition changes the sign of the right-hand side expression for $\dfrac{di_{g_1}}{dt}$. Thus, this transition changes the direction of the control that has to be modified in order to get a smooth transition. This modification is performed by having the absolute value of the current as shown in Fig. 8. Also, the modulator needs to be modified to avoid changes in the control direction. Fig. 10 shows the block diagram of the proposed modified modulator. According to Fig. 10, the gate pulses for power semiconductors S_1 and S_2 are switched at the zero crossings of the grid voltage. This is performed by using digital signals Cyc+ and Cyc− , which represent the positive and negative half cycles, respectively, (for positive cycles Cyc+ $= 1$ and Cyc− $= 0$, and for negative cycles Cyc+ $= 0$ and Cyc− $= 1$). The proposed modulator receives the duty cycle value and the optimal frequency value to produce gate pulses for the power semiconductors. The optimal switching frequency value is determined to control the current flowing through the coupled inductors. The switching frequency is controlled in a specific way such that the soft-switching condition for S_1 and S_2 is provided. Basically, the frequency controller calculates the optimum value of the switching frequency based on the duty cycle generated by the modified current controller, the dc-bus voltage, and the grid voltage and current.

The peak value of the current flowing through L_{g_2} in the positive cycle is given by

$$I_p = \frac{(V_{\text{dc}} - v_g - \hat{v}_{C1})d}{2L_{g_2} f_{\text{sw}}}. \tag{17}$$

In order to guarantee ZVS, I_P must be greater than the output current

$$I_p = I_{\text{ZVS}} + i_{g_1} - \left(\frac{V_{\text{dc}} - v_g}{2L_{g_1}}\eta - \frac{\hat{v}_{C1}}{2L_{g_1}}\lambda_1\right)\frac{d}{f_{\text{sw}}} \tag{18}$$

where

$$I_{\text{ZVS}} = 2C_S \frac{V_{\text{dc}}}{t_d}. \tag{19}$$

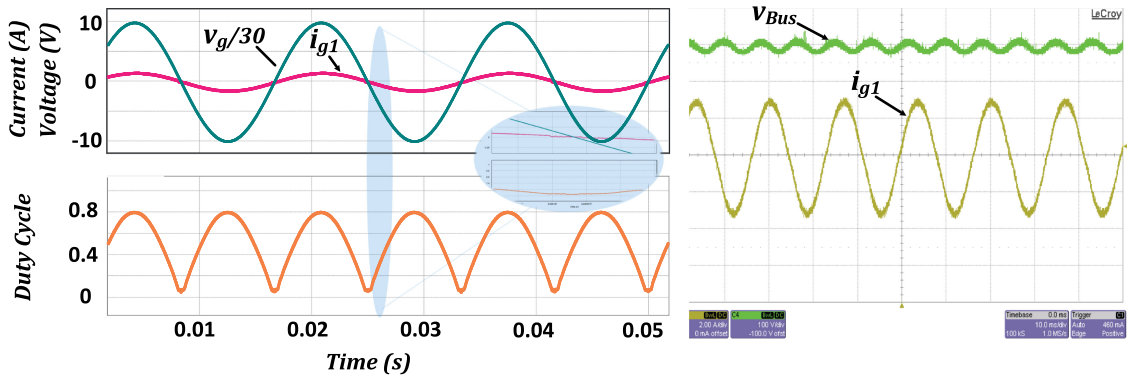


Fig. 9. Performance of the proposed closed-loop control system.

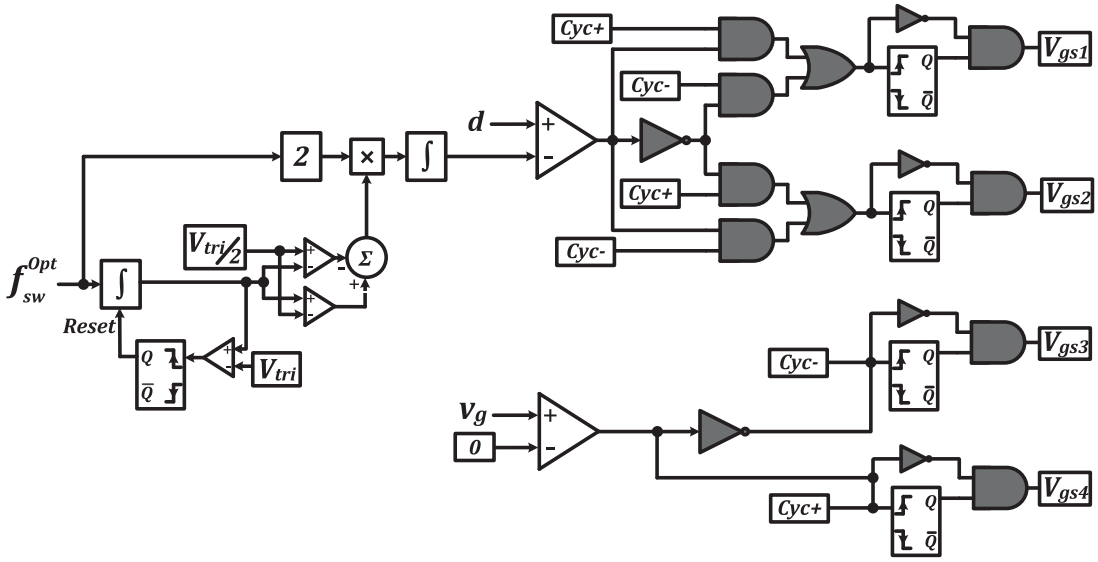


Fig. 10. Block diagram of the PWM modulator.

Equations (17)–(19) can be used to determine the optimum switching frequency as follows:

$$f_{sw}^{\text{opt}} = \frac{(V_{\text{dc}} - v_g)\left(1 + \frac{L_{g_2}}{L_{g_1}}\eta\right) - \hat{v}_{C1}\left(1 + \frac{L_{g_2}}{L_{g_1}}\lambda_1\right)}{2L_{g_2}\left(2C_S\frac{V_{\text{dc}}}{t_d} + i_{g_1}\right)}d. \quad (20)$$

IV. Integrated Magnetic Design

In this section, the design of the integrated magnetics for the proposed ZVS inverter is described in detail. One of the main objectives of the proposed integrated magnetics is to attenuate the current ripple at the output of the inverter in order to inject a high quality current into the utility grid. According to the analysis given in Section II, the current ripple is determined by the self-inductances and the mutual inductance of the coupled inductors. If the high frequency ripple across the capacitor C_1 is neglected, the condition to have zero current ripple at the output of the inverter is given by [according to (6)]

$$L_M = L_{g_2}. \quad (21)$$

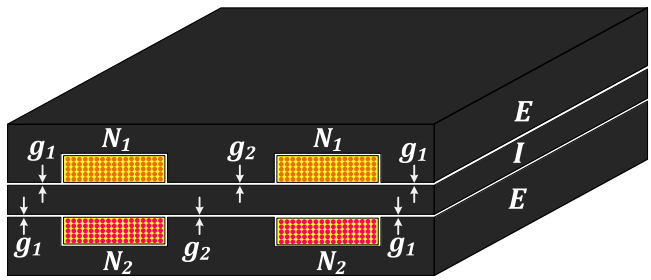


Fig. 11. Magnetic structure for the coupled inductors.

In order to satisfy this condition, a particular magnetic structure is required. Fig. 11 shows the proposed integrated structure for the ZVS inverter. According to Fig. 11, an "EIE" core structure is used to implement the coupled inductors. According to Fig. 11, the windings for L_{g_1} and L_{g_2} are wound in the middle legs of the E cores. This structure provides a flux path through the I core and allows for the adjustment of the mutual inductance and self-inductances using the air gaps (i.e., g_1, g_2) and the number of turns (i.e., N_1, N_2). Although (21) states the zero ripple condition, in practical implementation the current ripple will

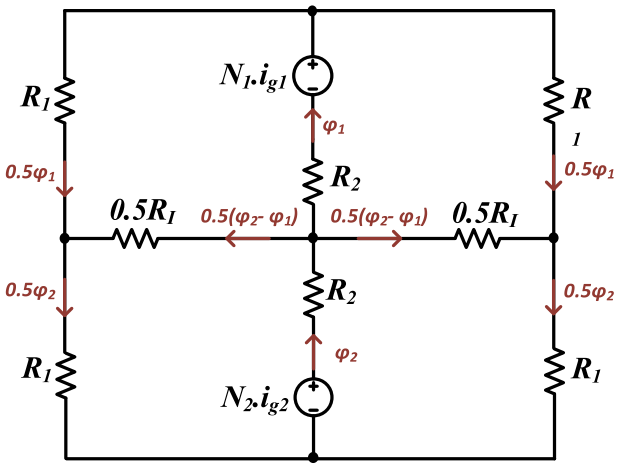


Fig. 12. Magnetic equivalent circuit of the EIE core.

not be zero due to the high-frequency ripple across the capacitor voltage v_{C_1}. Thus, this condition should slightly be modified. This modification will be determined through computer simulation of the inverter using the precise magnetic modeling of the coupled inductors (see Section V).

The magnetic equivalent circuit of the coupled inductors is shown in Fig. 12. In this figure, R_1, R_2, and R_I represent various reluctances of the proposed magnetic structure for the coupled inductors (R_1, R_2, and R_I are the reluctances due to the respective air gaps, since the reluctance of the core is negligible compared to the air gaps).

By neglecting the leakage flux of the inductors, Ampere's law results in

$$N_1 i_{g_1} = R_2\phi_1 + 0.5R_1\phi_1 - 0.25R_I(\phi_2 - \phi_1) \tag{22}$$

$$N_2 i_{g_2} = R_2\phi_2 + 0.5R_1\phi_2 + 0.25R_I(\phi_2 - \phi_1) \tag{23}$$

where N_1 and N_2 are the number of turns for the primary and secondary windings, respectively. The flux generated in the magnetic equivalent circuit is calculated by using (22) and (23) as follows:

$$\phi_1 = \frac{N_1\alpha}{\alpha^2 - (0.25R_I)^2} i_{g_1} + \frac{0.25N_2R_I}{\alpha^2 - (0.25R_I)^2} i_{g_2} \tag{24}$$

$$\phi_2 = \frac{0.25N_1R_I}{\alpha^2 - (0.25R_I)^2} i_{g_1} + \frac{N_2\alpha}{\alpha^2 - (0.25R_I)^2} i_{g_2} \tag{25}$$

where

$$\alpha = 0.5R_1 + 0.25R_I + R_2. \tag{26}$$

The voltages across the windings are calculated by using Faraday's Law and (24), (25) as follows:

$$v_{L_{g_1}} = N_1\frac{d\phi_1}{dt} = \frac{N_1^2\alpha}{\alpha^2 - (0.25R_I)^2}\frac{di_{g_1}}{dt} + \frac{0.25N_1N_2R_I}{\alpha^2 - (0.25R_I)^2}\frac{di_{g_2}}{dt} \tag{27}$$

$$v_{L_{g_2}} = N_2\frac{d\phi_2}{dt} = \frac{0.25N_1N_2R_I}{\alpha^2 - (0.25R_I)^2}\frac{di_{g_1}}{dt} + \frac{N_2^2\alpha}{\alpha^2 - (0.25R_I)^2}\frac{di_{g_2}}{dt}. \tag{28}$$

According to (1), (2), (27), and (28), the inductance matrix of the coupled inductors is given by

$$L = \begin{bmatrix} L_{g_1} & L_M \\ L_M & L_{g_2} \end{bmatrix} = \begin{bmatrix} \dfrac{N_1^2\alpha}{\alpha^2 - (0.25R_I)^2} & \dfrac{0.25N_1N_2R_I}{\alpha^2 - (0.25R_I)^2} \\ \dfrac{0.25N_1N_2R_I}{\alpha^2 - (0.25R_I)^2} & \dfrac{N_2^2\alpha}{\alpha^2 - (0.25R_I)^2} \end{bmatrix}. \tag{29}$$

In order to satisfy the ripple cancelation condition given by (21), the following relation must be held:

$$4R_2 + 2R_1 = \left(\frac{N_1}{N_2} - 1\right) R_I. \tag{30}$$

Hence, in order to have zero current ripple, the air gaps and turn ratios must be designed such that (30) is satisfied.

Also, the coupling coefficient is given by

$$k = \frac{L_M}{\sqrt{L_{g_1}L_{g_2}}} = \sqrt{\frac{L_{g_2}}{L_{g_1}}} = \frac{N_2}{N_1}. \tag{31}$$

According to (21), (29), and (31), the parameters of the coupled inductors are calculated as

$$\eta = \frac{1 - L_M/L_{g_2}}{1 - k^2} = 0 \tag{32}$$

$$\lambda_1 = \lambda_2 = \frac{1}{1 - k^2} = \frac{N_1^2}{N_1^2 - N_2^2} \tag{33}$$

$$\zeta = \frac{1 - L_M/L_{g_1}}{1 - k^2} = \frac{N_1^2\alpha - 0.25N_1N_2R_I}{\alpha(N_1^2 - N_2^2)}. \tag{34}$$

V. Design Procedure

The design procedure for various parameters of the integrated magnetics, the design of the dc blocking capacitor (C_1), and the dead time of the gate pulses of S_1 and S_2 are described in this section.

A. Inductor L_{g_2}

The value of L_{g_2} is calculated using the voltage across the inductor as follows:

$$L_{g_2} = \frac{V_{L_{g_2}}}{\dfrac{di_{g_2}}{dt}} \tag{35}$$

where

$$\frac{di_{g_2}}{dt} = \frac{-I_P.f_{\text{sw}}}{(1 - d^{\max})} \tag{36}$$

I_P is given by (18) and can further be simplified by assuming that the high-frequency component of the voltage across capacitor C_1 is negligible and $\eta = 0$ [according to (32)]. Therefore, I_P can be written as

$$I_P = I_{\text{ZVS}} + i_{g_1}. \tag{37}$$

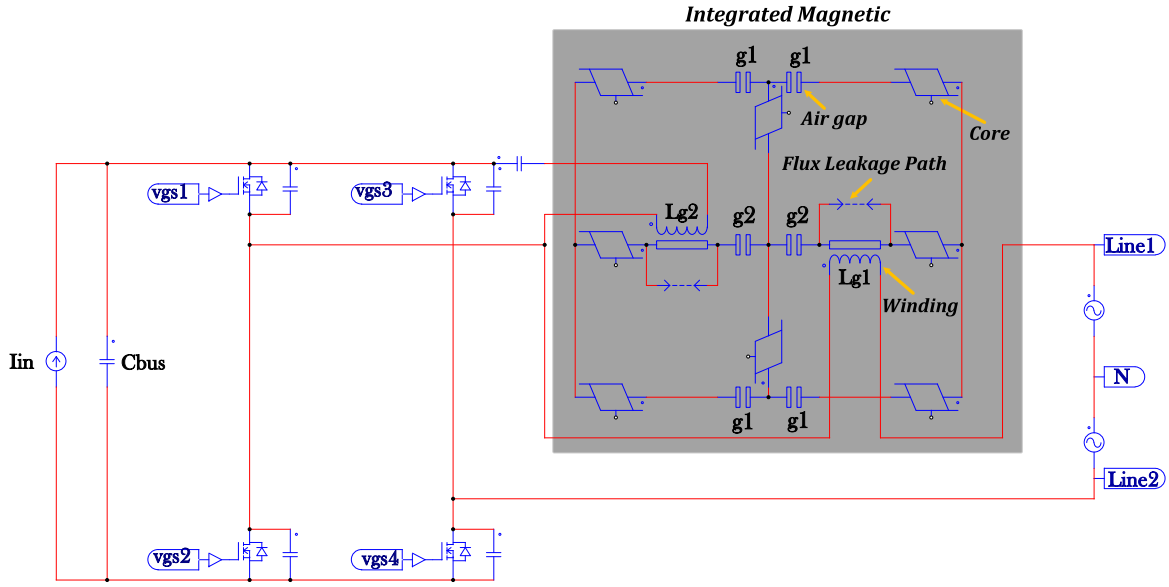


Fig. 13. Simulation of the proposed integrated magnetics.

Based on the volt-second balance equation for the coupled inductor during Mode III, $V_{L_{g_2}}$ is given by

$$V_{L_{g_2}} = -v_g. \tag{38}$$

By substituting (36)–(38) into (35), the value of L_{g_2} is derived by

$$L_{g_2} = \frac{(1 - d^{\max}) v_g^{\max}}{(I_{\text{ZVS}} + I_{g_1}).f_{\text{sw}}}. \tag{39}$$

The value of inductor L_{g_1} can then be determined by substituting (39) into (31). It is important to note that the frequency variation from 60 to 120 kHz does not impact the output current ripple due to the ripple cancelation of the coupled inductor. Therefore, the designs of L_{g_1} and L_{g_2} are not affected by the frequency variations.

B. Capacitor C_1

The capacitor C_1 should be designed such that it introduces negligible ripple to the current of the coupled inductor (i.e., grid current). In addition, this capacitor should not be too large in order to avoid the resonance with the coupled inductor. The value of the capacitor C_1 is calculated as

$$C_1 = \frac{i_{C_1}}{\dfrac{dv_{C_1}}{dt}}. \tag{40}$$

Since this capacitor is in series with L_{g_2} and the current through the capacitor is i_{g_2}. Also, the voltage ripple across the capacitor is considered to be less than 10% of V_{dc}. Thus, the capacitor is given by

$$C_1 = \frac{d^{\max}(I_{\text{ZVS}} + I_{g_1})}{0.1 V_{\text{dc}} f_{\text{sw}}}. \tag{41}$$

It is worthwhile to mention that the input capacitor is designed to attenuate the double-frequency ripple present at the dc-bus voltage. Thus, it is much larger than C_1.

C. Dead Time t_d

The optimum dead time can be designed using (13). The values of currents i_{g_1} and i_{g_2} at the instant of commutation are given by

$$i_{g_1}(t_1) = I_{g_1}.\sin(2\pi.60.t_1) \tag{42}$$

$$i_{g_2}(t_1) = I_p \tag{43}$$

where I_p is given by (37) and I_{g_1} is given by

$$I_{g_1} = \frac{P_o}{V_{g_{\text{rms}}}}.\sqrt{2}. \tag{44}$$

Since the grid current i_{g_1} is sinusoidal and varies in the line cycle, the dead time will also vary within a range. In this particular design, the optimum dead time is varying between 80 to 20 ns within a line cycle.

VI. Loss Analysis

In this section, the qualitative study of loss analysis for the proposed ZVS inverter is described. The major losses of the proposed inverter include the conduction losses and magnetic losses. Due to the ZVS operation at turn-ON instants of the power semiconductors in the high-frequency leg, the switching turn-ON loss for S_1 and S_2 is negligible. Also, the turn-OFF switching losses of the high-frequency leg are insignificant since the junction capacitors of the MOSFETs prevent the switch voltage from sharply rising and the switch voltage starts to slowly increase with a time constant. Furthermore, the other leg of the inverter is switched at the line frequency which is much smaller than the high switching frequency. Thus, the total switching losses of the inverter are considered negligible and the conduction losses and the magnetic losses are considerably dominant.

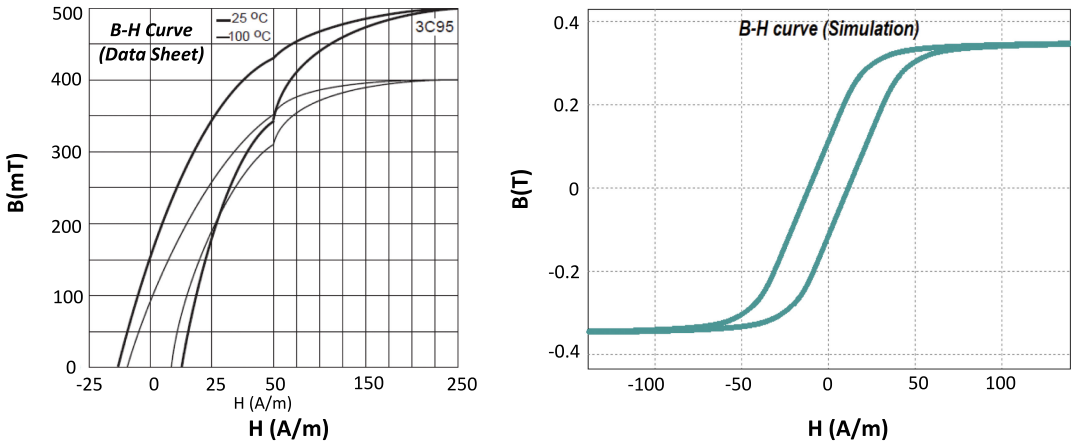


Fig. 14. *B–H* curves of the core 3C95 from the data sheet and the simulation.

A. Magnetic Losses

The power losses of the coupled inductors are given by

$$P_{\text{magnetic}} = P_{\text{core}} + P_{\text{copper}}. \tag{45}$$

1) Core losses: Core losses are generated due to the variations in the magnetic flux within the core. Based on Steinmetz equation, the actual core loss measurements can be approximated by

$$P_{\text{core}} = k.f_{\text{sw}}^{x}.\Delta B^{y}.V_e \tag{46}$$

where k, x, y are constants determined from curve fitting depending on the core material, ΔB is defined as half of the ac flux swing in Tesla (T), f_{sw} is the switching frequency in kilohertz, and Ve is the effective core volume in cm^3 [38]. The material "3C95" from Ferroxcube is selected for the cores due to its stable thermal performance. According to Steinmetz equation and the core data sheet, the overall core losses are calculated as 0.4 W.

2) Copper losses: The copper losses are generally caused by the dc resistance and the ac resistance of the wires wound on the core. The copper losses are given by

$$P_{\text{copper}} = I_{\text{rms}}^2.(R_{\text{DC}} + R_{\text{AC}}) \tag{47}$$

where I_{rms} is the rms value of the current flowing through the inductor and R_{DC} , R_{AC}, are dc and ac resistances, respectively. In order to obtain the total copper losses, (47) should be calculated for both L_{g_1} and L_{g_2}. Since the output current ripple is insignificant, the ac term is negligible. The rms currents of L_{g_1} and L_{g_2} are given by

$$I_{g_{1\text{rms}}} = \frac{P_o}{v_{g_{\text{rms}}}} \tag{48}$$

$$I_{g_{2\text{rms}}} = \frac{I_p}{\sqrt{3}}. \tag{49}$$

From (47)–(49), the overall copper losses are 0.6 W.

B. Conduction Losses

The conduction losses in the power MOSFETs are calculated using the drain–source on-state resistance (R_{DS}(ON)) and the rms currents flowing through power semiconductors ($I_{\text{sw}_{\text{rms}}}$)

$$P_{\text{cond}} = R_{\text{DS}}(\text{ON}).I_{\text{sw}_{\text{rms}}}^2. \tag{50}$$

Since i_{g_1} is varying with the line frequency, it is considered constant in each switching cycle. However, for calculating rms currents the variations during the line cycle must be taken into account. Thus, the rms values of the switch currents are calculated for a switching cycle and then the rms values for the whole line cycle are calculated as follows:

$$(I_{\text{sw}_{\text{rms}}})_{\text{total}} = \sqrt{\frac{1}{T_{\text{ac}}}\int_0^{T_{\text{ac}}} I_{\text{sw}_{\text{rms}}}^2 dt}. \tag{51}$$

The rms currents for the switches in the positive half cycle are given by

$$(I_{s_{1\text{rms}}})_{\text{total}} = \sqrt{\frac{V_g}{3\pi V_{\text{dc}}}\left(\frac{16}{3}I_g^2 + 2I_{\text{ZVS}}^2 + \pi I_{\text{ZVS}} I_g\right)} \tag{52}$$

$$(I_{s_{2\text{rms}}})_{\text{total}} = \sqrt{I_g^2\left(\frac{2}{3} - \frac{16V_g}{9\pi V_{\text{dc}}}\right) + I_{\text{ZVS}}^2\left(\frac{1}{3} - \frac{2V_g}{3\pi V_{\text{dc}}}\right) + I_{\text{ZVS}} I_g\left(\frac{4}{3\pi} - \frac{V_g}{3V_{\text{dc}}}\right)} \tag{53}$$

where I_g and V_g are the peak values of the grid current and grid voltage, respectively. As the role of power switches S_1 and S_2 change in each positive and negative half cycle, the actually rms

TABLE I
SPECIFICATIONS OF THE PROPOSED INVERTER

Symbol	Parameter	Value
P_o	Output Power	$250\ W$
V_{BUS}	Bus Voltage	$380 - 450\ VDC$
I_{in}	Input Current	$550 - 650\ mA$
v_g	Grid Voltage	$213 - 266\ VAC$
f_{sw}	Switching Frequency	$60 - 120\ kHz$
R_1	Inverter Side Resistance	$35\ m\Omega$
L_{g_1}	Grid Side Self Inductance	$1.5\ mH$
R_2	Grid Side Resistance	$15\ m\Omega$
L_{g_2}	DC-Bus Side Self Inductance	$200\ \mu H$
L_M	Mutual Inductance of Coupled Inductors	$180\ \mu H$
C_1	Series Capacitance of the Integrated Magnetics	$22\ nF$
C_{BUS}	DC-Bus Capacitor	$220\ \mu F$
S_1, S_2, S_3, S_4	Power Semiconductors	$IPB65R110CFD$

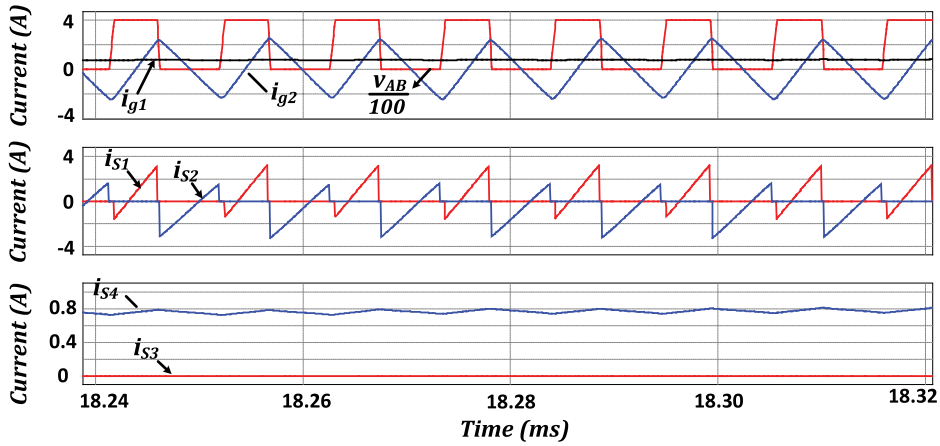


Fig. 15. Key waveforms of the proposed ZVS inverter.

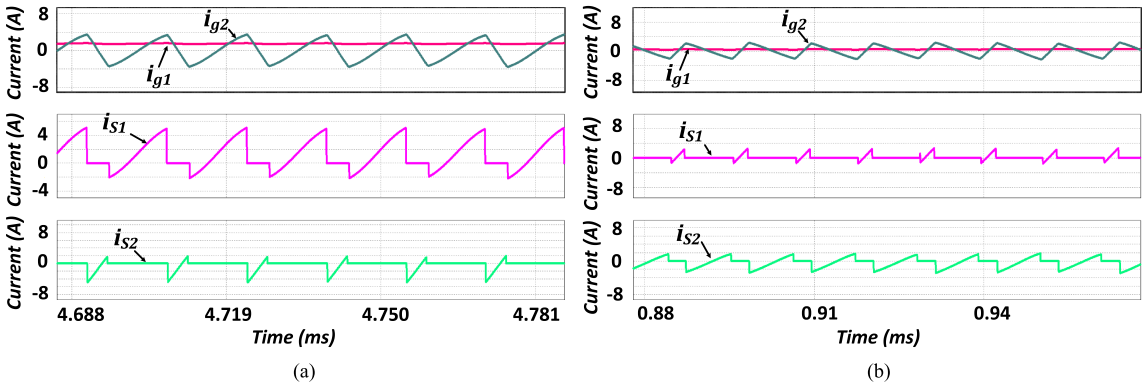


Fig. 16. Key waveforms of the ZVS inverter. (a) For Heavy load. (b) For Light load.

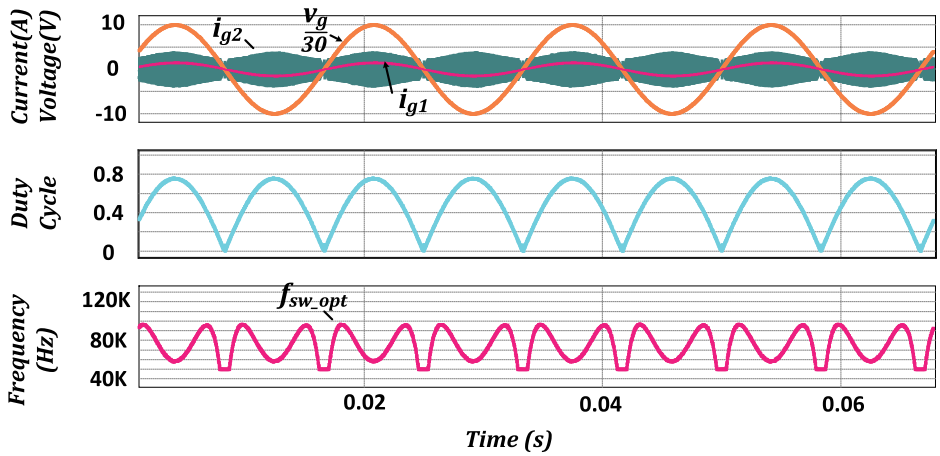
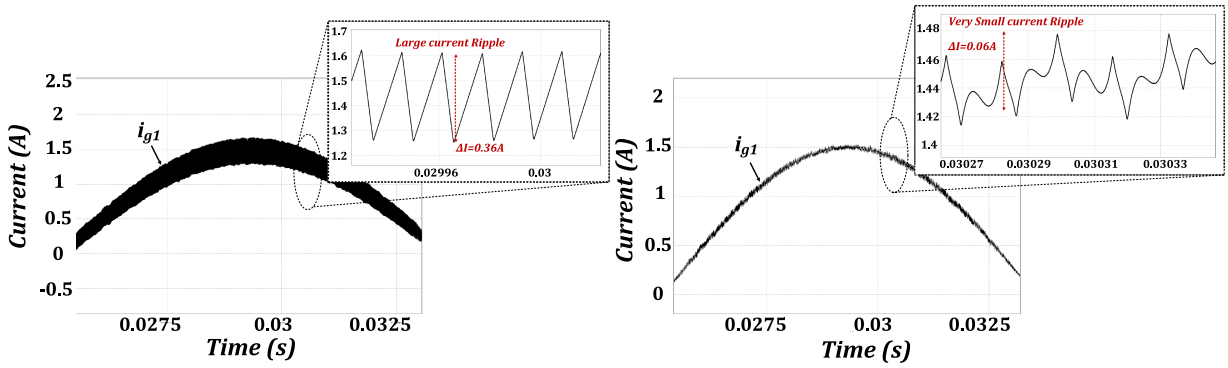


Fig. 17. Key waveforms of the closed-loop control system.

current of each switch is the average of the values we obtained for S_1 and S_2 in the positive half cycle. The overall conduction losses are 0.6 W.

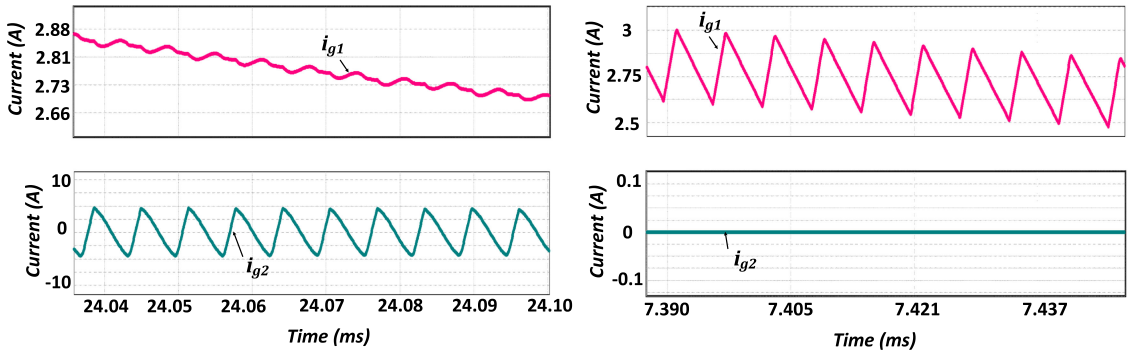
VII. Simulation Results

In this section, the simulation results for the proposed ZVS inverter is presented. The simulation is conducted using PowerSim V11.0.3 (PSIM) software. The PowerSim software has been used to cosimulate the electrical parts of the inverter as well as the magnetic parts (for the coupled inductors). The simulation utilizes "Magnetic Elements," which can precisely model the air gap, leakage inductance, the *B–H* curves of the cores, etc. Fig. 13 shows the schematic diagram of the simulated ZVS inverter using the integrated magnetics. The parameters of the simulated inverter are listed in Table I. As mentioned earlier,



(a) (b)

Fig. 18. Comparison of the output current ripples. (a) Conventional inverter. (b) Proposed ZVS inverter.



(a) (b)

Fig. 19. Comparison of current ripples when (a) the coupled inductor is in the circuit and (b) a simple inductor is in the circuit.

the "3C95" material is selected for the cores that can provide very stable thermal performance for the coupled inductors. The *B–H* curve of "3C95," which is extracted from the data sheet is depicted in Fig. 14. The *B–H* curve of the simulated cores has to correspond to the one extracted from the data sheet. This can be performed by adjusting the core coefficients in a couple of iterations. The *B–H* curve of the simulated cores is also shown in Fig. 14 (it may take several iterations to determine the core coefficients in a way that the *B–H* curve matches the data sheet).

Fig. 15 shows the key waveforms of the proposed ZVS inverter. This figure verifies the ZVS operation of power semiconductors S_1 and S_2. The performance of the proposed ZVS inverter for a heavy load and a light load is shown in Fig. 16. According to this figure, the inverter operates under soft switching for different loads.

Fig. 17 illustrates the inverter waveforms as well as the closed-loop control signals for multiple line cycles. According to this figure, the duty cycle is continuous using the proposed digital control approach. Thus, smooth transitions at zero crossings are achieved for the output current waveform. This figure also shows the performance of the frequency control loop. It demonstrates how the switching frequency is changed over a line cycle in order to guarantee soft switching for the power semiconductors.

In Fig. 18, a comparison between the output current ripple of the conventional inverter and that of the proposed inverter under similar circumstances (i.e., switching frequency, load) is presented. According to this figure, the output current ripple

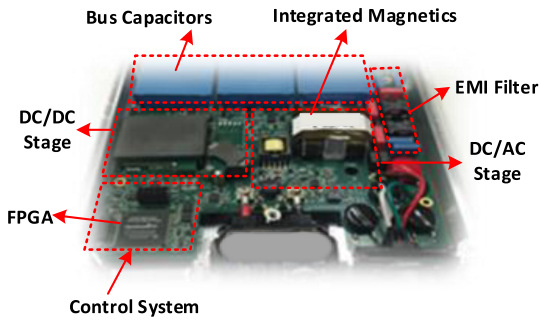


Fig. 20. Experimental setup of the proposed inverter.

is significantly attenuated for the proposed ZVS inverter and a very high quality current is injected to the grid. It is also shown that the current ripple increases linearly in the case of the conventional inverter, whereas the current ripple does not increase linearly for the proposed ZVS inverter due to the coupled inductors. The impact of the coupling between the inductors is depicted in Fig. 19. This figure shows the ripple attenuation when $i_{g2} \neq 0$ and high amount of ripple in i_{g1} when $i_{g2} = 0$.

VIII. Experimental Results

In this section, experimental results and design considerations of the proposed ZVS inverter are presented. As shown in Fig. 20, an experimental prototype has been prepared to

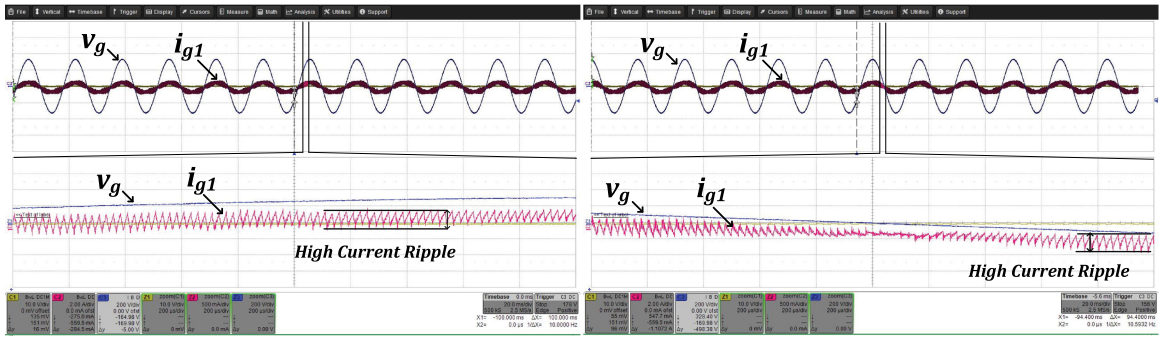


Fig. 21. High ripple and current spikes at the zero crossings of the output current for the conventional inverter (first scenario).

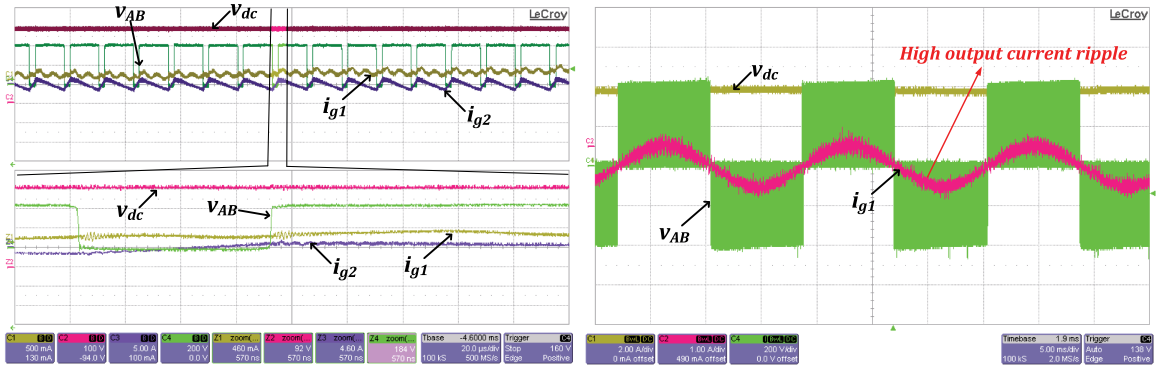


Fig. 22. Key waveforms. (a) For proposed ZVS inverter (second scenario). (b) For inverter with a simple inductor (first scenario).

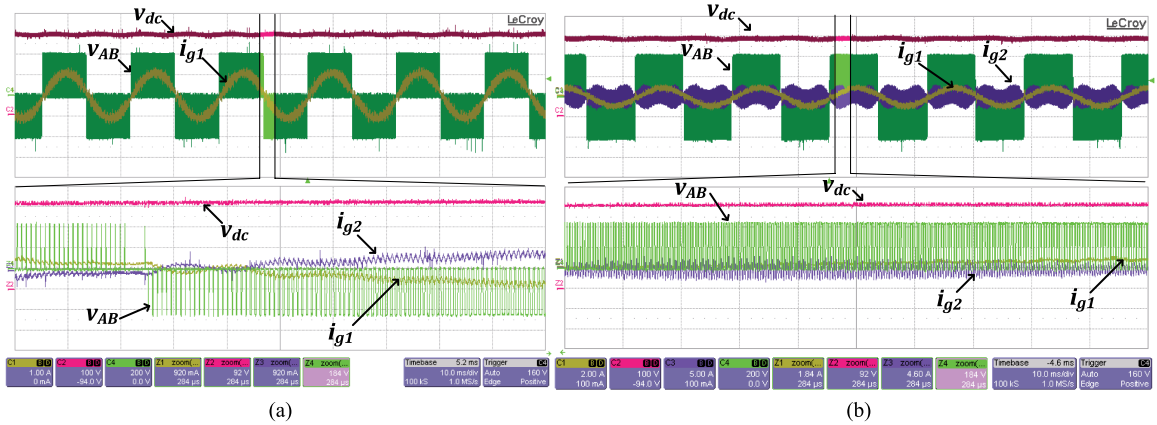


Fig. 23. Zero crossing and ripple of the output current. (a) Conventional inverter. (b) Proposed inverter with constant frequency control.

verify the feasibility of this inverter and evaluate its performance. The specifications of the implemented prototype are shown in Table I. The digital control system is implemented using a field-programmable gate array (FPGA) device capable of providing a fast and reliable solution. In particular, Cyclone IV EP4CE22F17C6N from Altera is used as the FPGA to implement the digital control system. VHSIC Hardware Description Language (VHDL) is used to implement the proposed controllers and modulator. The implemented control loops in VHDL codes are based on the IEEE "fixed-point" library, which is supported by VHDL-2008 compilers [39], [40]. The calculating speed of various operations are based on the FPGA's clock frequency, which is selected to be 100 MHz. However, the entire chain of calculations is performed by the controller once every switching cycle. In other words, once a chain of calculations has been completed for one switching cycle, the state machine waits until the next switching cycle is initiated to begin a new chain of calculations.

In order to compare the performance of the proposed ZVS inverter and the conventional one, the results have been obtained

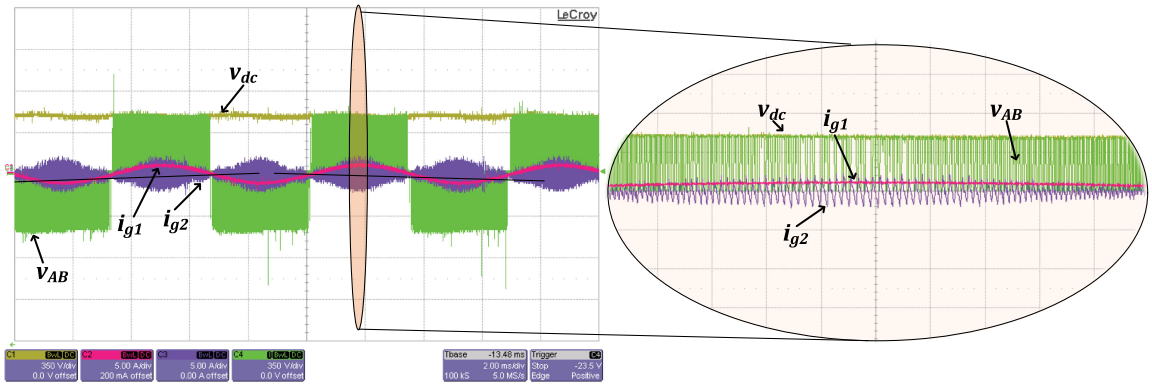


Fig. 24. Performance of the proposed inverter with variable frequency control.

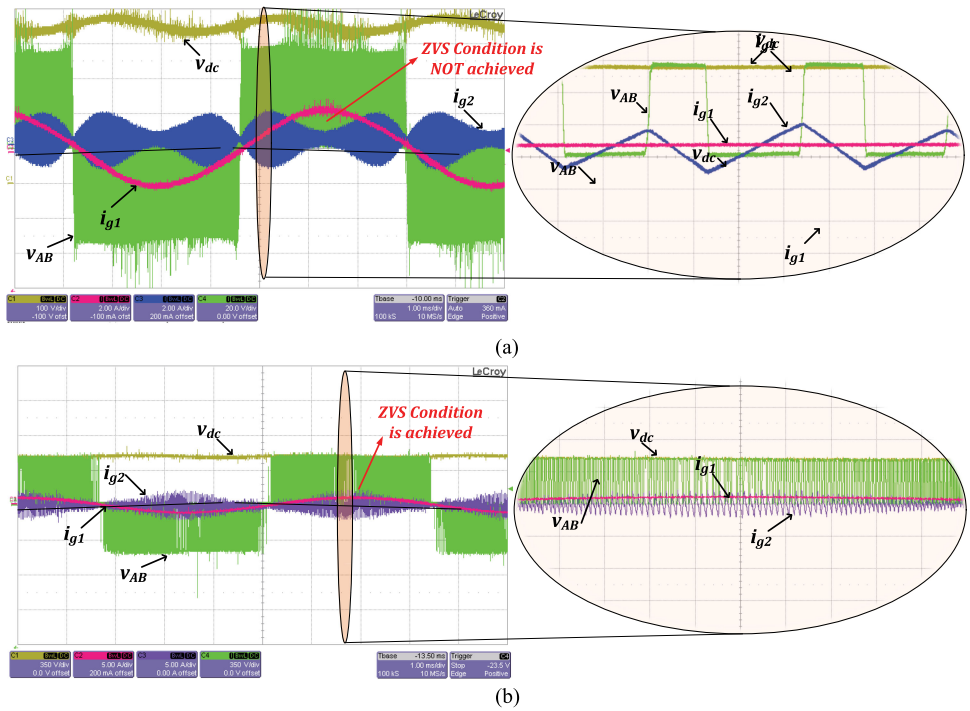


Fig. 25. Comparison of output currents with (a) constant frequency control and (b) variable frequency control.

for two scenarios. In the first scenario, a simple inductor is used and in the second scenario the proposed integrated coupled inductors is used to obtain the results. Fig. 21 shows the results when a simple inductor is used. According to this figure, a high amount of current ripple is injected to the utility grid and there are disturbances at the zero crossings of the current waveforms. Also, the current ripple is increasing linearly as expected. Fig. 22 compares the results for the proposed ZVS inverter and the conventional one. In Fig. 22(a), it is shown that the current ripple is not linear and it is significantly attenuated, whereas there is a high amount of current ripple when using a simple inductor as shown in Fig. 22(b). The comparison between the performance of the aforementioned scenarios is elaborated in Fig. 23. Fig. 23(a) shows the results of the conventional inverter and Fig. 23(b) shows the results of the proposed ZVS inverter for multiple line cycles.

In Fig. 23, the controller for the proposed inverter only utilizes the duty cycle (the frequency control is disabled and the inverter operates with a constant switching frequency). It is observed that the output current ripple is decreased remarkably. However, since the frequency is constant, the current through L_{g2} does not follow a sinusoidal envelop. Thus, the inverter loses ZVS around the peaks of the sinusoidal waveform. In Fig. 24, the frequency control loop is enabled. According to this figure, the frequency is changed such that the envelop of the current through L_{g2} follows a sinusoidal waveform to guarantee ZVS. The comparison between the constant frequency control scheme and the proposed variable frequency scheme is elaborated in Fig. 25. This figure shows that i_{g_2} cannot follow a sinusoidal envelop in Fig. 25(a), where the frequency is kept constant. However, by utilizing the frequency control loop in Fig. 25(b), i_{g_2} follows a sinusoidal envelop and guarantee the ZVS for the

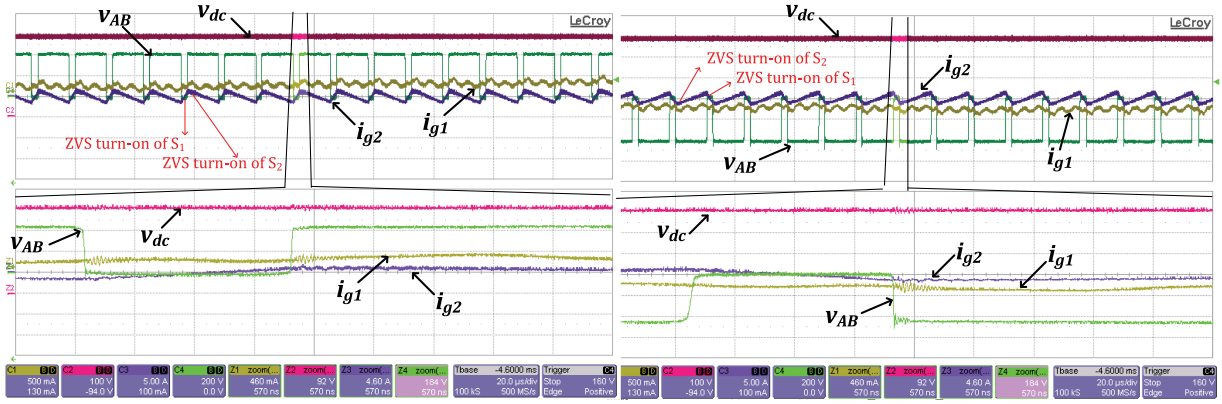


Fig. 26. Key waveforms of the proposed inverter. (a) $v_g > 0$. (b) $v_g < 0$.

Fig. 27. Frequency spectrum of the grid current.

entire line cycle. Fig. 26(a) and (b) shows the key waveforms of the inverter for $v_g > 0$ and $v_g < 0$, respectively. This figure verifies the ripple attenuation and the ZVS operation of the proposed ZVS inverter. The frequency spectrum of the grid current is shown in Fig. 27. According to this figure, the grid current contains very small amount of harmonics due to the ripple cancelation. The total harmonic distortion (THD) results are provided in Fig. 28 that also verify the small amount of harmonics in grid current.

In order to verify the superior performance of the proposed approach, a hard-switched inverter with the same specifications has been implemented. The switching frequency of the hard-switched inverter is 20 kHz. Fig. 29 depicts the efficiency curves for the proposed ZVS inverter and the hard-switched inverter. The experimental efficiencies were measured by the "LMG670" Zimmer Precision Power Analyzer. According to Fig. 29, the proposed ZVS inverter can significantly improve the efficiency performance particularly from light loads to heavy loads. As the load approaches the full power, the efficiency decreases. This is due to the fact that the RMS currents through the power semiconductors increase. Thus, there will be excessive conduction losses, which degrades the efficiency. For low power applications such as solar microinverters, the inverter operates at full-load only during fraction of its life time. Therefore, the proposed

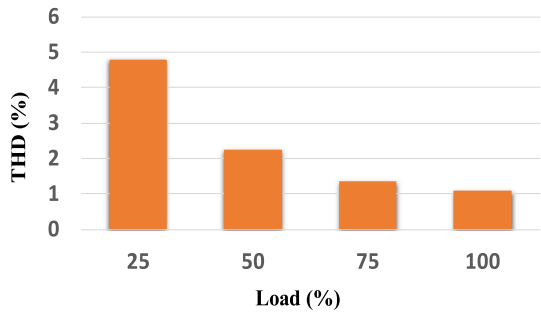


Fig. 28. THD of the proposed ZVS inverter for different loads.

approach offers substantially better efficiency performance for this application.

The abovementioned conduction losses could be substantially improved by selecting a power semiconductor with smaller on-state resistance ($R_{\mathrm{DS_{on}}}$). In this case, the conduction losses will decrease and switching losses will be the dominant factor in efficiency since the value of the output capacitance of MOSFETs increases. However, this might add to the cost of the inverter (switches with lower on-state resistance tend to be more expensive). Since in this application (solar microinverter), the inverter

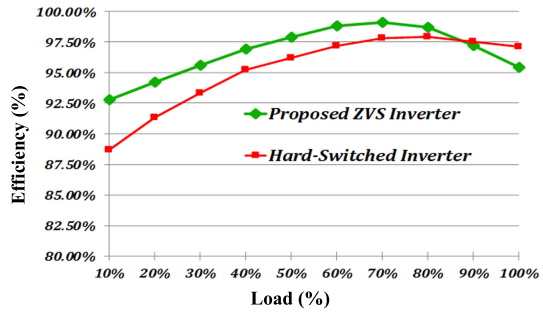


Fig. 29. Efficiency curves of the proposed ZVS inverter and the conventional hard-switched inverter.

hardly operates in full load, the more cost-effective solution has been chosen.

IX. Conclusion

A new soft-switched dc/ac inverter for low power applications (i.e., high voltage, low current applications) has been presented in this paper. The proposed inverter utilizes a ripple steering technique in order to provide ZVS for the power semiconductors and substantially attenuate the current ripple injected to the utility grid. The proposed power circuit is very simple and very similar to ones for the reliable conventional inverters. It only uses an integrated magnetics to perform ripple steering and in turn provide soft switching and ripple attenuation. A new digital control system has been proposed, which optimally perform the proposed ripple steering through the integrated magnetic. The proposed digital control approach utilizes the duty cycle and the switching frequency in order to perform the control tasks and the ripple steering. Since the inverter is operating with a high switching frequency, the switching losses will be dominant. Efficiency theoretical analysis, simulation results, and experimental results demonstrate the superior performance of the proposed ZVS inverter compared to the conventional ones.

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