Letters

A Model Predictive Current Controlled Bidirectional Three-Level DC/DC Converter for Hybrid Energy Storage System in DC Microgrids

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***Abstract*—This letter proposes a new three-level dc/dc converter configuration for a hybrid energy storage system (HESS) in dc microgrids. It effectively integrates different energy storage devices (ESDs), such as battery and ultracapacitor (UC), using one converter with bidirectional power flow. Furthermore, the proposed converter provides the flexibility of independent regulation of different ESDs with significantly reduced inductor current ripple due to the availability of three voltage levels. The voltage ratings of power semiconductors employed in this converter are also reduced. To further enhance the performance of HESS, a constant switching frequency based model predictive current control is employed for HESS regulation. The design guideline and operating principle of the proposed converter are discussed. Experimental results are presented to verify the efficacy of the proposed converter and control.**

***Index Terms*—Battery, dc microgrid, hybrid energy storage system (HESS), model predictive current control (MPCC), three-level dc/dc converter, ultracapacitor (UC).**

I. Introduction

In THE past decade, hybrid energy storage systems (HESSs) became increasingly popular as an energy buffering device in dc microgrids [1]. The main advantage of a HESS is the exploration of complementary features of different energy storage devices (ESDs), which contributes to provide excellent transient and steady-state performance as well as respecting the limitation of certain ESDs. A typical example of a HESS is the combination of a battery and an ultracapacitor (UC). It has been widely used in industry because of the fact that the high power density and long life cycle features of a UC make it a good compensation for the deficiencies of the battery [1].

However, the conventional and most widely used HESS employs one converter for each individual ESD [2]. This greatly

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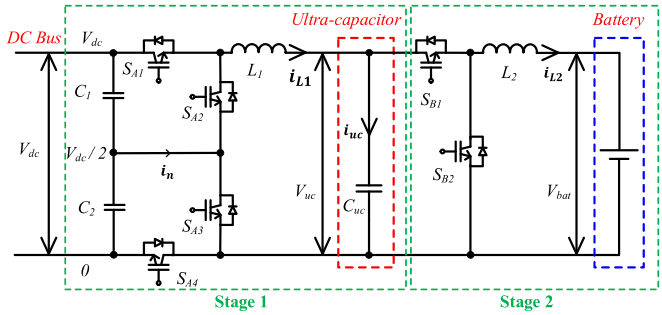

Fig. 1. Topology of the proposed three-level dc/dc converter.

Finite-set MPC is widely used in power electronics to simply the computations, but the problems of variable switching frequency and large current ripples still exist [10].

To tackle the problems associated with a HESS power converter, this letter proposes a new three-level dc/dc converter configuration as shown in Fig. 1. It allows full and independent regulation of a battery and a UC, and the usage of three voltage levels contributes to reduce inductor size in both battery and UC branches. Additionally, a finite-set model predictive current control (FS-MPCC) is presented to attenuate the current ripple while obtaining constant switching frequency and low computational complexity.

II. Operating Principle and Design Guideline of the Proposed Three-Level DC/DC Converter

A. Operating Principle of the Proposed DC/DC Converter

It is seen from Fig. 1 that three voltage levels (i.e., $V_{\rm dc}, V_{\rm dc}/2, 0$) are created by the front-end switches S_{A1}—S_{A4} and capacitors $C_1 \text{and} C_2$. Inductors L_1 and L_2 are utilized for current regulation of the UC and battery, respectively. The capacitance of the UC is given as $C_{\rm uc}$ and the terminal voltages of the UC and battery are denoted as $V_{\rm uc}$ and $V_{\rm bat}$, respectively. Due to the presence of L_1 and the comparatively small voltage gap between the terminal voltages of the UC and battery, the value of L_2 can be chosen to be reasonably small.

The power flow from the dc bus to the UC/battery, i.e., charging of ESD, is illustrated by Fig. 2, where Fig. 2(a) depicts the situation of utilizing the full dc bus voltage $V_{\rm dc}$ and Fig. 2(b) and (c) characterizes the situation of utilizing half of the dc bus voltage $V_{\rm dc}/2$. Noticeably, the scenario of discharging ESD, where the power flows from UC/battery back to the dc bus, can be easily demonstrated by reversing the current flow direction in Fig. 2, where V_L and V_R denote the left- and right-side voltage of L_1.

The operating modes of the proposed converter with a HESS are summarized in Table I. These modes are defined by referring to different battery and UC charge/discharge/idle combinations with selectable dc bus voltage levels. The converter in Fig. 1 can be interpreted as a two-stage structure. Stage 1 consists of $S_{Ai}(i = 1 \text{ to } 4)$, $C_j(j = 1, 2)$, L_1, and a UC; whereas stage 2 is composed of $S_{Bi}(i = 1, 2)$, L_2, and a battery. Its principle is analyzed in two aspects, i.e., the generation of dc bus side voltage levels at V_L in Fig. 2 and the independent control of the battery and UC

$$\frac{di_{L1}}{dt} = \frac{V_L - V_R}{L_1} = \frac{V_L - V_{\rm uc}}{L_1}. \tag{1}$$

First, the slope of inductor current i_{L1} in Fig. 1 is determined by (1), and $V_R = V_{\rm uc}$ holds. In order to produce continuous and smooth inductor current i_{L1}, moderate current slope should be generated by maintaining a small enough $|V_L - V_{\rm uc}|$. With a varying UC voltage $V_{\rm uc}$, this can be achieved by 1) properly selecting the voltage level applied at V_L, and 2) allocating suitable duty ratios for the two voltage levels to be applied in each sampling cycle. Noticeably, 1) is realized by exploring the three-level nature of the proposed converter. For instance, when $V_{\rm uc} < V_{\rm dc}/2$, the application of $V_L = V_{\rm dc}/2$ and $V_L = 0$ is sufficient for ESD regulation in steady states by turning on S_{A1}, S_{A3} or S_{A2}, S_{A4}, as shown in Fig. 2(b) and (c), respectively. During transients, large current slope is sometimes desired. In this case, $V_L = V_{\rm dc}$ and $V_L = 0$ have to be applied to increase the value of $|V_L - V_{\rm uc}|$, as shown in Fig. 2(a). So, the level of V_L that minimizes the current regulation error is always selected. To achieve target, 2) FS-MPCC is employed to calculate the duty ratio that is capable of producing a desirable average voltage drop across inductor L_1 to further diminish current regulation error.

Second, full and independent control of the UC and battery can be realized via regulating stages 1 and 2 of the converter, respectively. For the control of battery, it is achieved by manipulating $S_{Bi}(i = 1, 2)$ and is not affected by the switching actions in stage 1. This is because the battery current i_{L2} is fully controllable using duty ratio $d_{\rm bat}$ of switches S_{Bi} regardless of the variations of $V_{\rm uc}$. Similarly, inductor current i_{L1} can be solely determined by duty ratio $d_{\rm uc}$ of switches S_{Ai}, producing an independently controlled UC current $i_{\rm uc} = i_{L1} - i_{L2}$.

In the above-mentioned analysis, an assumption of $V_{c1} = V_{c2} = V_{\rm dc}/2$ is made. It is pointed out that such an assumption is not always true without a proper neutral point voltage (NPV) balancing scheme. In practice, the values of V_{c1} and V_{c2} can vary and differ from each other significantly. This is known as NPV fluctuation, which can result in increased voltage stress across capacitor and switches as well as the degraded ESD current response. Thus, an NPV balancing scheme must be employed to effectively balance V_{c1} and V_{c2}. In this letter, the scheme in Fig. 3 is proposed to satisfy such a demand. It is seen from Fig. 3 that NPV fluctuation is not considered in the scenario of $V_{\rm dc}/2 < V_{\rm uc} < V_{\rm dc}$. This is because we propose to use only the full dc bus voltage under such circumstance, as illustrated by Fig. 2(a), which does not produce any neutral point current i_n. Consequently, the NPV will not be affected. Instead, when $V_{\rm uc} < V_{\rm dc}/2$, capacitor voltage V_{c1} or V_{c2} is used depending on the NPV balancing requirement indicated by $\Delta V_c = V_{c1} - V_{c2}$ and i_{L1}. To be specific, if $\Delta V_c > 0$, i.e., $V_{c1} > V_{c2}$, the NPV balancing requires C_1 to be discharged to reduce V_{c1} or C_2 to be charged to increase V_{c2} so that $|\Delta V_c|$ can be smaller. This means if positive current $i_{L1} > 0$ is desired to charge ESD, C_1 is to be used, as shown in Fig. 2(b); otherwise, if negative current $i_{L1} < 0$ is needed to discharge ESD, C_2 is to be used, as shown in Fig. 2(c), but with reversed current flow direction.

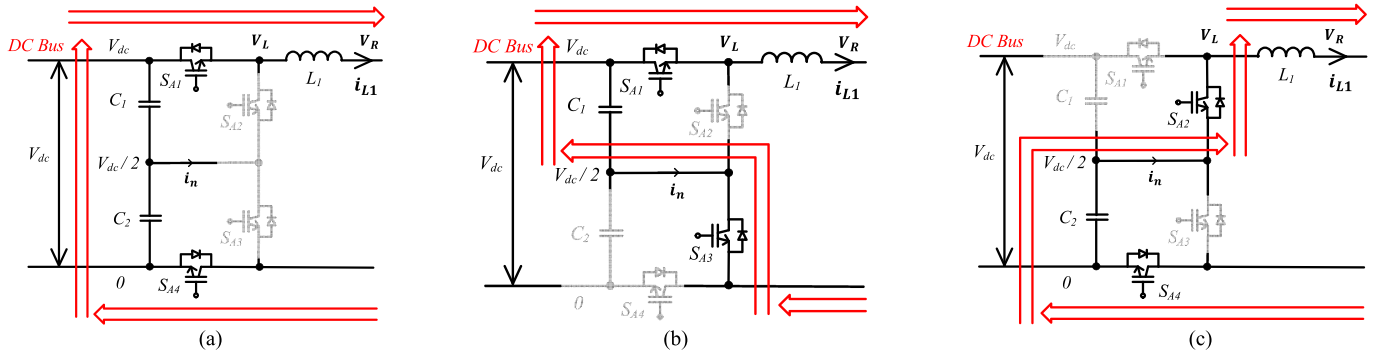

Fig. 2. Power flow from dc bus to HESS. (a) Utilization of full dc bus voltage. (b) Utilization of upper dc capacitor C_1. (c) Utilization of lower dc capacitor C_2.

TABLE I
OPERATING MODES OF THE PROPOSED CONVERTER WITH HESS

Mode	1	2	3	4	5	6	7	8	9
UC	charge			discharge			idle		
Battery	charge	discharge	idle	charge	discharge	idle	charge	discharge	idle

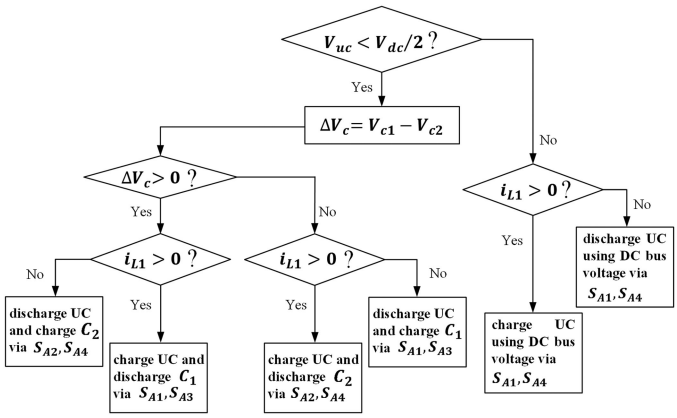

Fig. 3. Flowchart of the NPV balancing scheme.

The above-mentioned analysis is illustrated by the leftmost flowchart in Fig. 3, i.e., the logic of $\Delta V_c > 0$. The same logic of analysis can be applied to the case $\Delta V_c < 0$ with $V_{\rm uc} < V_{\rm dc}/2$, giving the flowchart in the middle of Fig. 3.

B. Design Guideline of the Proposed DC/DC Converter

From design perspective, the proposed converter allows the employment of low voltage rating power semiconductors, reduced size inductors, and wide variation range of ESD's terminal voltage. To produce a design guideline, the choice of ESDs is first discussed in this section. Then, the selection of switches and inductors is quantitatively evaluated.

Due to its three-level nature, the proposed converter allows the voltage of UC to vary in the wide range $(0, V_{\rm dc})$ without generating very large inductor current ripples. This is because voltage level $V_{\rm dc}$ or $V_{\rm dc}/2$ can be selected to ensure that the voltage drop across L_1 is small when $V_{\rm uc} > V_{\rm dc}/2$ or $V_{\rm uc} < V_{\rm dc}/2$, respectively. Additionally, the two-stage structure depicted in Fig. 1 implies that the battery must satisfy $V_{\rm bat} < V_{\rm uc}$ to avoid the uncontrollable current from the battery to the UC through the diode of S_{B1}. Therefore, the design rule of ESDs for the proposed converter can be briefly summarized as $V_{\rm bat\_rated} < V_{\rm uc\_min}$ and $V_{\rm uc\_max} < V_{\rm dc}$. Without loss of generality, one of the feasible choices of the voltage ratings of the UC and the battery is as follows:

$$V_{\rm uc\_rated} = \frac{V_{\rm dc}}{2};\ V_{\rm bat\_rated} = \frac{V_{\rm dc}}{3} \tag{2}$$

where a variation range of $V_{\rm uc} \in (V_{\rm dc}/2, V_{\rm dc})$ is achievable. The capacitance of UC and the ampere-hour of battery need to be determined based on the specific power requirements of certain dc microgrids and thus are less relevant to the converter configuration. Therefore, they are not discussed here. With the available laboratory hardware resources, $V_{\rm dc} = 50$ V, $V_{\rm uc\_rated} = 25$ V, and $V_{\rm bat\_rated} = 12$ V are used in the selection of components, which follows the above-mentioned design rule.

With the selected ESDs in (2), the voltage stresses of switches $S_{Ai}(i = 1-4)$ and $S_{Bi}(i = 1, 2)$ are found to be as follows:

$$V_{S_{Ai}} = \frac{V_{\rm dc}}{2};\ V_{S_{Bi}} = V_{\rm uc\_rated} \tag{3}$$

where both of them are only half of the switch ratings in the conventional HESS using two-level buck/boost converter [2]. Although the number of switches employed by the conventional HESS is four, instead of six for the proposed converter, their significantly larger voltage rating leads to a higher overall semiconductor cost. Moreover, larger current ripples are experienced by the conventional HESS in [2] due to the availability of only two voltage levels. Noticeably, even if $V_{\rm uc\_rated} > \frac{V_{\rm dc}}{2}$ is selected for some applications that require extended UC voltage range, the voltage rating of S_{Ai} remains to be half of the conventional HESS and the rating of S_{Bi} is still lower than its counterpart in the conventional HESS.

The sizing of inductors for the proposed converter follows the general rule of boost converter design [9] given by the following:

$$L = \frac{v_{\rm in}\left(v_{\rm out} - v_{\rm in}\right)}{\Delta i_L f_s v_{\rm out}} \tag{4}$$

where $v_{\rm in}, v_{\rm out}, \Delta i_L$, and f_s are the input voltage, output voltage, inductor current ripple, and switching frequency, respectively. For the proposed converter in Fig. 1, L_1 and L_2 can be estimated as follows:

$$\begin{cases} L_1 \approx \frac{V_{\rm uc\_rated}\left(V_{\rm dc} - V_{\rm uc\_rated}\right)}{\Delta i_{L_1} f_s V_{\rm dc}} = \frac{1}{4}\frac{V_{\rm dc}}{\Delta i_{L_1} f_s} \\ L_2 \approx \frac{V_{\rm bat\_rated}\left(V_{\rm uc\_rated} - V_{\rm bat\_rated}\right)}{\Delta i_{L_2} f_s V_{\rm uc\_rated}} = \frac{1}{9}\frac{V_{\rm dc}}{\Delta i_{L_2} f_s}. \end{cases} \tag{5}$$

TABLE II
PARAMETERS OF THE EXPERIMENTAL SETUP

Symbol	V_{dc}	V_{bat}	V_{uc}	C_{uc}
Value	$50V$	$12V$	$22V$~$27V$	$29F$
Symbol	C_1, C_2	T_s	L_2	L_1
Value	$440\mu F$	$50\mu s$	$0.5mH$	$1mH$

By following the same rule, inductors for a UC and battery circuit in the conventional HESS are estimated as $L_1' = L_1$ and $L_2' = 2L_2$. Thus, if the proposed converter is used, battery inductor can be reduced by half, reducing the system volume, weight, and cost. In the experiments, a rated current of 2.5 A is chosen for both inductors L_1 and L_2 for down-scaled demonstration. To constrain current ripples Δi_{L_1} and Δi_{L_2} to be within 20% of the rated current, $f_s = 20$ kHz, $L_1 = 1$ mH, and $L_2 = 0.5$ mH are chosen in the experiments, as shown in Table II.

III. PROPOSED MPCC

To attain good charging/discharging current control of a battery and a UC, a constant switching frequency based FS-MPCC is employed in this letter. The algorithm searches for the optimal duty cycle for both the battery and UC regulation in a finite set. Hence, two voltage levels are applied in each sampling cycle, which contributes to attenuate the current ripples compared to the conventional FS-MPCC [10]. This is because the proposed FS-MPCC applies an adjustable voltage level of $dV_{\text{in}} \in [0, V_{\text{in}}]$ to one side of the inductor, where d and V_{in} represent the controlled duty ratio and the input voltage. In comparison, the conventional FS-MPCC [10] applies a fixed voltage level of 0 or V_{in}. So, when the voltage at the other side of the inductor is fixed, the proposed method has better capability of producing a smaller voltage drop across the inductor and thus generates smoother inductor current slope in general.

For better illustration of the proposed FS-MPCC, the model of the HESS system in Fig. 1 is first described by the following equations:

$$L_1 \frac{di_{L1}}{dt} = d_{\text{uc}} V_{\text{bus}} - V_{\text{uc}} \tag{6}$$

$$L_1 \frac{di_{L1}}{dt} = V_{\text{uc}} - (1 - d_{\text{uc}}) V_{\text{bus}} \tag{7}$$

$$L_2 \frac{di_{L2}}{dt} = d_{\text{bat}} V_{\text{uc}} - V_{\text{bat}} \tag{8}$$

$$L_2 \frac{di_{L2}}{dt} = V_{\text{bat}} - (1 - d_{\text{bat}}) V_{\text{uc}} \tag{9}$$

$$i_{L1} = i_{\text{uc}} + i_{L2} \tag{10}$$

where

V_{bus} voltage from dc bus side ($V_{\text{dc}}/2$ or V_{dc});
i_{uc} current flowing through the UC;
$d_{\text{uc}}, d_{\text{bat}}$ duty cycle of switches controlling UC and battery power flow, respectively;
i_{L1}, i_{L2} current flowing through L_1 and L_2, respectively.

Noticeably, (6) and (7) characterize the dynamics of inductor current i_{L1} under HESS charging and discharging conditions, respectively. The value of V_{bus} can be half or full dc bus voltage depending on the actual terminal voltage of the UC, as illustrated by the logic in Fig. 3. Similarly, (8) and (9) capture the charging and discharging dynamics of battery. The relation between UC and battery currents is given in (10).

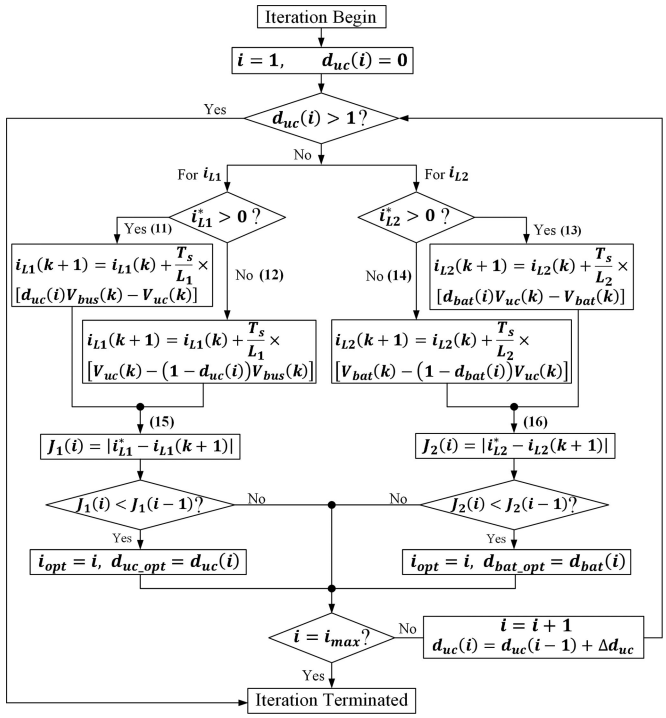

Fig. 4. Flowchart of the proposed FS-MPCC.

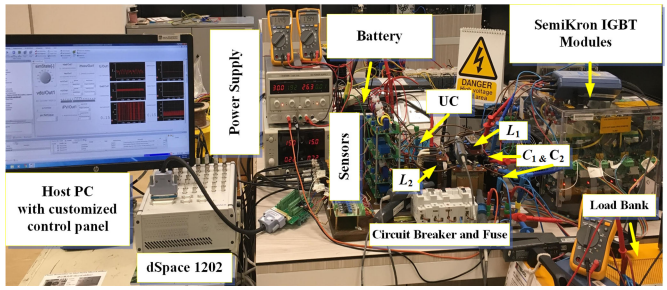

Fig. 5. Experimental setup of the proposed three-level dc/dc converter incorporating battery and UC.

With the simple model in (6)–(10), an FS-MPCC algorithm is proposed to regulate the charging/discharging current of battery and UC. The algorithm predicts the inductor current using the forward Euler approach as shown by (11)–(14) in Fig. 4. Then, the errors between the desired reference currents i^*_{L1}, i^*_{L2} and the predicted currents $i_{L1}(k+1), i_{L2}(k+1)$ are evaluated iteratively to find out the duty cycles that minimizes such errors. By comparing the optimal duty cycles with carrier, pulsewidth modulation (PWM) signals are generated with constant switching frequency.

IV. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed converter and FS-MPCC, an experimental set-up is built as shown in Fig. 5, where lead-acid batteries are used to emulate a regulated dc

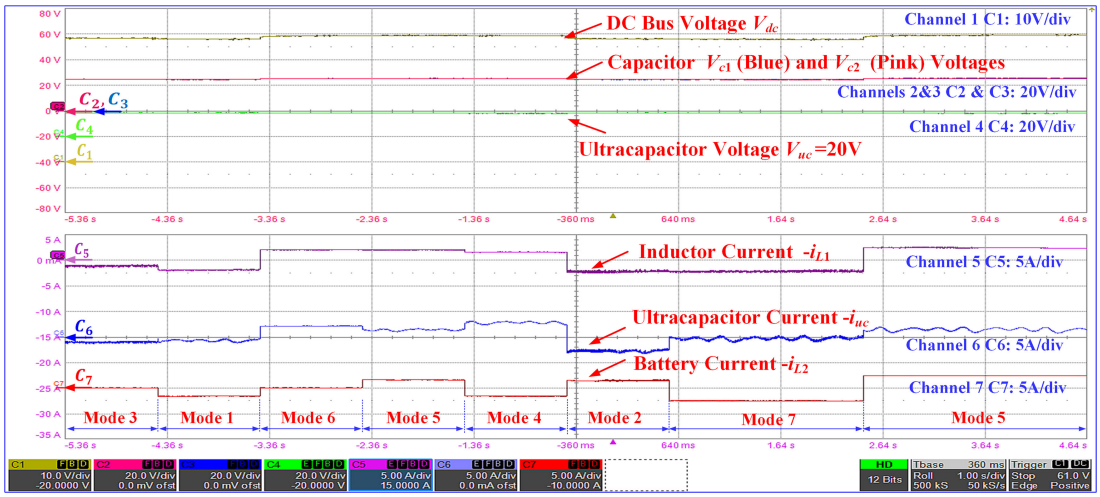

Fig. 6. Response of HESS with the proposed three-level dc/dc converter and FS-MPCC under the scenario of low UC terminal voltage ($V_{\rm uc} < V_{\rm dc}/2$).

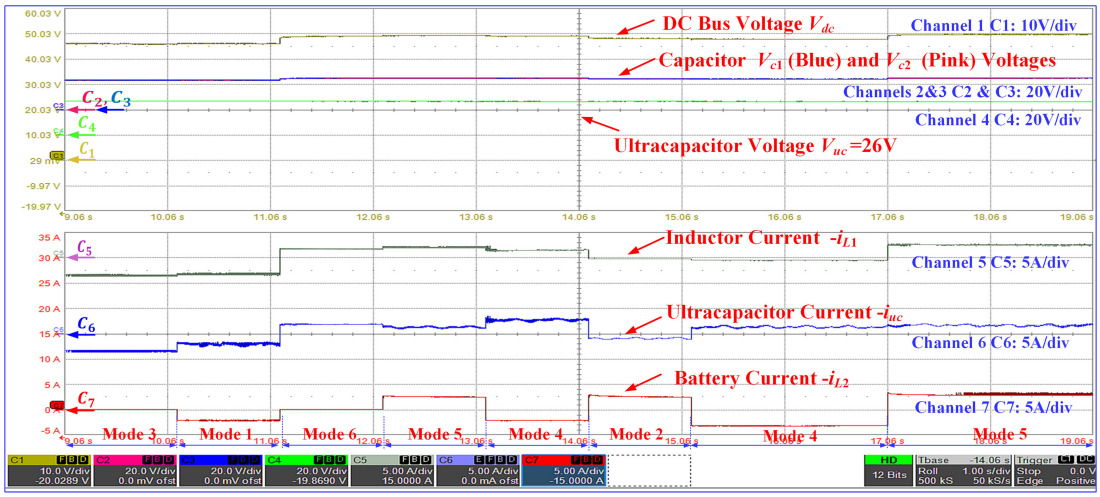

Fig. 7. Response of HESS with the proposed three-level dc/dc converter and FS-MPCC under the scenario of high UC terminal voltage ($V_{\rm uc} > V_{\rm dc}/2$).

microgrid with a nearly constant dc bus voltage. The parameters of this set-up are listed in Table II. It is noticed that $V_{\rm uc}$ varies from 22 to 27 V in the experiments to investigate the cases of $V_{\rm uc} > V_{\rm dc}/2$ and $V_{\rm uc} < V_{\rm dc}/2$.

A. Operation of the Proposed Converter With Low UC Voltage

The responses of battery and UC with the proposed converter and FS-MPCC under low UC terminal voltage are illustrated in Fig. 6. Under such circumstances, voltage levels $V_{\rm dc}/2$ and 0 are utilized to reduce current ripples. Different operating modes defined in Table I are tested as shown in Fig. 6. For instance, the test in Fig. 6 starts with mode 3, where the battery is idling with no current flow and all the current flowing through inductor L_1 is pumped into the UC for charging. Similarly, in the subsequent test mode, which is mode 1, both battery and UC are charged by the current coming through L_1. However, since the battery current i_{L2} takes up the main portion of current i_{L1}, the average UC charging current $i_{\rm uc}$ becomes very small. It is seen from channels C5 and C7 that the inductor currents i_{L1} and i_{L2} are tightly and smoothly regulated to track their reference values. The transient response of the HESS under step current reference change is fast and accurate. The overshoots, which are usually experienced by PI regulators during fast dynamics, do not occur. Channel C6 indicates that the UC current is indirectly controlled to handle comparatively rapid variations for the smoothness of inductor current i_{L1} and battery current i_{L2}. In addition, the capacitor voltages V_{c1} and V_{c2} are well balanced as seen from channels C2 and C3 of Fig. 6, validating the proposed NPV balancing scheme. It is pointed out that small voltage level fluctuations in dc bus is seen in channel C1. This is due to the employment of lead-acid batteries with limited capacity to provide $V_{\rm bus}$.

B. Operations of the Proposed Converter With High UC Voltage

As mentioned above, voltage levels $V_{\rm dc}$ and 0 are applied when $V_{\rm uc}$ rises above $V_{\rm dc}/2$. In this case, the operation of the proposed converter system under different modes is depicted in Fig. 7. For example, the first and second test modes in Fig. 7, which are mode 3 and mode 1, respectively, give similar

performances as their counterparts in Fig. 6. This proves the effectiveness of the converter regulation with high UC terminal voltage and full dc bus voltage. It is observed from channels C5 and C7 that smooth and overshoot-free inductor current control is realized by the proposed FS-MPCC. Low current ripples are also obtained for the indirectly controlled UC current depicted in channel C6. Furthermore, NPV balancing is autonomously achieved as illustrated by channels C2 and C3 since there is no neutral point current flow with the application of full dc bus voltage.

V. Comparison With Previous Works

First, compared to the dc/dc converters used by the conventional HESS [2], the proposed converter has two advantages owing to its three-level nature. On the one hand, the ratings of the power switches and inductors are significantly reduced compared to those in [2] as analyzed in Section II-B, resulting in hardware cost reduction. On the other hand, the burden on battery can be alleviated since the ripple of battery current i_{L2} is significantly diminished, prolonging the battery lifespan.

In addition, the proposed FS-MPCC method possesses much lower computational complexity compared to the existing MPCC method for the HESS in [8]. So, it is more feasible for real-time implementation. As shown in Fig. 4, the proposed FS-MPCC method sets both control and prediction horizons to be 1. The execution time of the proposed FS-MPCC method is 50 μs. However, the MPCC method with complex model in [8] requires larger control and prediction horizons as well as many matrix operations, leading to high computational burden. Hence, its execution time is 0.01 [8], which is much larger than the proposed FS-MPCC.

VI. Conclusion

This letter proposes a new three-level dc/dc converter configuration for a HESS. It provides the flexibility of independent battery and UC control with bidirectional power flow. Compared to the conventional HESS converters, it contributes to reduce the size and cost of power semiconductors and inductor owing to the presence of more voltage levels. In addition, a simple but effective FS-MPCC approach is proposed to achieve fast and accurate current regulation with diminished current ripples compared to the conventional FS-MPCC. Optimal duty ratio is computed by the FS-MPCC for PWM generation and thus constant switching frequency is realized.

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