Optimal Design of Planar Magnetic Components for a Two-Stage GaN-Based DC–DC Converter

Minfan Fu, *Member, IEEE*, Chao Fei, *Member, IEEE*, Yuchen Yang, *Student Member, IEEE*, Qiang Li, *Member, IEEE*, and Fred C. Lee, *Life Fellow, IEEE*

***Abstract*—This paper develops a 200-W wide-input-range (64–160-to-24-V) rail grade dc–dc converter based on gallium nitride devices. A two-stage configuration is proposed. The first regulated stage is a two-phase interleaved buck converter (>400 kHz), and the second unregulated stage is an *LLC* (2-MHz) dc transformer. In order to achieve high frequency and high efficiency, the critical-mode operation is applied for the buck converter, and the negative coupled inductors are used to reduce the frequency and the conduction losses. Then, a systematical methodology is proposed to optimize the planar-coupled inductors. For the unregulated *LLC* converter, it can always work at its most efficient point, and an analytical model is used to optimize the planar transformer. Finally, the proposed dc–dc converter, built in a quarter brick form factor, is demonstrated with a peak efficiency of 95.8% and a power density of 195 W/in^3.**

***Index Terms*—Coupled inductors, critical current mode, gallium nitride (GaN) devices, *LLC* converter, planar magnetic integration.**

I. Introduction

THE increased power consumption and power density demands of modern technologies have increased the demands on various power supplies. Combined with the focus on global energy savings and size reduction, there are continuous research efforts on developing high-efficiency and high-power-density converters. Currently, most of the commercial converters are still based on silicon (Si) devices. It is difficult to further improve the efficiency and power density because the Si-based semiconductor devices approach their theoretical performance limit. The emerging wide-bandgap device, such as the gallium nitride (GaN) device, will certainly become the game changer because of its better figure of merit and significantly smaller body diode reverse-recovery effect [1].

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M. Fu is with the School of Information Science and Technology, ShanghaiTech University, Shanghai 201210, China, and also with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061 USA (e-mail:

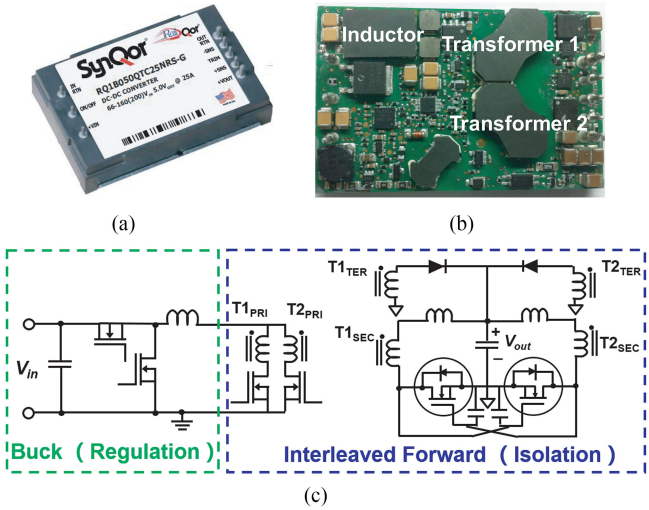


Fig. 1. Rail-grade dc–dc module manufactured by SynQor. (a) Outside view. (b) Inside view. (c) Circuit topology.

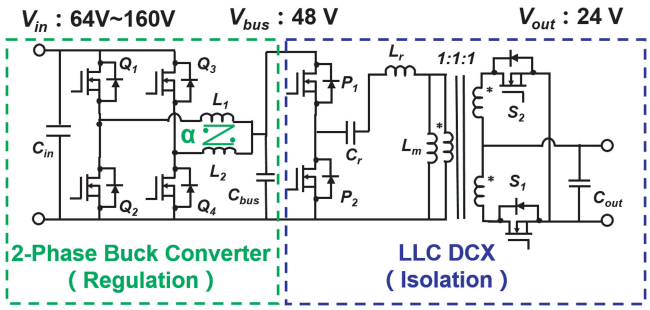


Fig. 2. Proposed two-stage topology.

Fig. 1(b). Finally, the large loss would further restrict the power level because of the heat issue.

Usually, the GaN-based converter can naturally achieve better efficiency and power density than the Si-based one. However, the improvement due to the device is not sufficient to compensate the increased cost presently. Therefore, the most appealing condition is that the topology, the device, and the magnetic benefit each other, which finally can lead to a significant improvement in both the efficiency and the power density. To achieve this, a GaN-based converter is proposed for the railway application (64–160 V/24 V) with the same footprint (quarter brick form) and increased output power (200 W). The two-stage configuration is still used, but with quite different topology (refer to Fig. 2). The first stage is a two-phase interleaved buck converter working under the CRM. The CRM is the simplest way to achieve ZVS and can fully utilize the benefits of GaN devices [16], [17]. This regulation stage should convert the wide input voltage (64–160 V) to constant 48-V bus voltage, and the switching frequency is above 400 kHz. The second stage is a 2-MHz unregulated 48-V/24-V *LLC* converter (DCX). This LLC DCX can always work at its most efficient point at even several megahertz [18]–[20]. For the entire converter, the topology enables the ZVS operation for all devices, and very high switching frequency is used. Finally, it is achievable to build

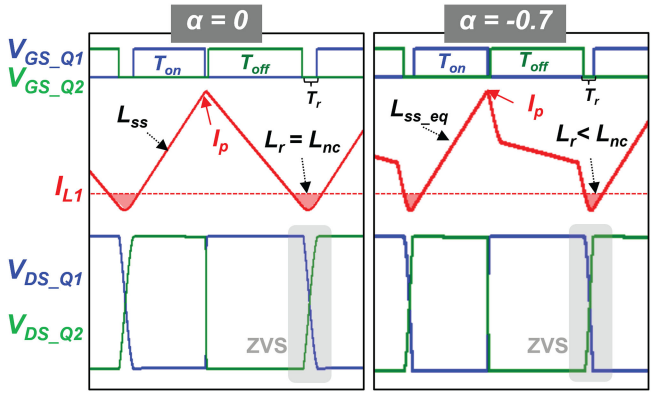


Fig. 3. Waveform comparison between noncoupled and coupled cases under the CRM.

well-performed planar inductor and transformer with limited PCB layers.

This paper focuses on the design and optimization of planar inductors and transformer with a six-layer PCB. For the buck converter, the benefits of negative coupled inductors are discussed. It is helpful to reduce the conduction losses under the CRM, decrease the switching frequency within a frequency range, and integrate the inductors for core size reduction. In order to reduce the inductor loss, the planar-coupled inductors with winding interleaving are optimized based on a finite-element simulation. Two inductors are easy to couple through a customized EI core, and a same-air-gap design is proposed to improve the manufacturability. Similarly, the planar transformer of the LLC DCX is optimized with a customized EI core based on an analytical model [18], [19]. Finally, all the devices, magnetic components, the digital controller, the auxiliary power supply, and the sensing and communication chips are integrated on a single quarter-brick PCB to build a standalone dc–dc module.

II. Design of the Interleaved Buck Converter

A. Benefits of Negative Coupling

Fig. 2 shows the proposed topology. The CRM is employed for the buck converter to achieve ZVS. Thus, the high switching frequency can be used and help build well-performed planar inductors. The high peak current introduced by the CRM is reduced by using a two-phase interleaving configuration. Each phase requires an individual inductor (i.e., L_1 and L_2), and α is the coupling coefficient. The coupled inductor concept has been widely used in many power conversion applications, such as voltage regulators, photovoltaic (PV) inverters, and high-step-up converters [21]–[23]. In this paper, the negatively coupled inductors are applied to the two-phase interleaved CRM buck converter. It is helpful for the CRM operation and the magnetic integration.

Fig. 3 shows the waveforms of the nominal full-load condition ($V_{\text{in}} = 110$ V and $V_{\text{bus}} = 48$ V), where $V_{\text{GS\_}Q1}$ and $V_{\text{GS\_}Q2}$ are the gate driving signal of Q_1 and Q_2, respectively, I_1 is the current of L_1, and $V_{\text{DS\_}Q1}$ and $V_{\text{DS\_}Q2}$ are the drain–source voltage of Q_1 and Q_2, respectively. When $\alpha = 0$, the inductor

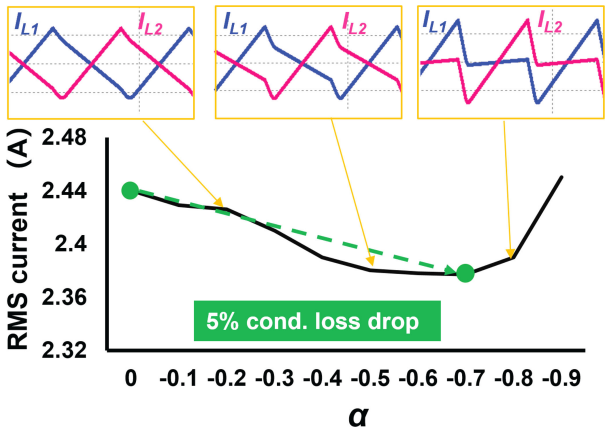


Fig. 4. Influence of the coupling coefficient on the inductor current.

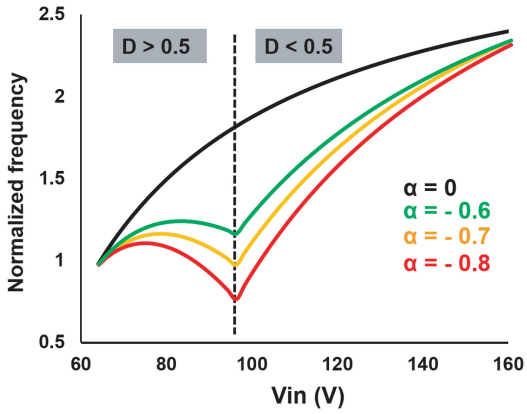


Fig. 5. Influence of the coupling coefficient on the switching frequency.

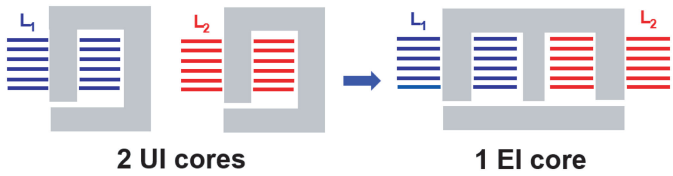


Fig. 6. Magnetic integration for coupled inductors.

current (I_1) is a typical triangular waveform under the CRM. A small negative current is purposely left for the main switch (Q_1), and ZVS is achieved by the resonance between the inductor ($L_1 = L_2 = L_{\rm nc}$) and the switch junction capacitors ($C_{\rm oss}$). The resonant time (i.e., the red-shaded area) is determined by $T_r = \pi\sqrt{2L_rC_{\rm oss}}$, where $L_r = L_{\rm nc}$ for the noncoupled case. With negative coupling, the current of one phase is also affected by the other phase. According to [10], the equivalent resonant inductance of the coupled case becomes smaller (i.e., $L_r < L_{\rm nc}$) to keep the same frequency as the noncoupled case. It means the circulating energy is reduced, and the smaller red-shaded area means smaller root-mean-square current. Meanwhile, different α leads to different current waveform, as shown in Fig. 4. Based on the simulation, it is shown that a suitable negative coupling coefficient, i.e., $\alpha = -0.7$, can minimize the conduction loss.

As shown in Fig. 3, the peak current I_p is controlled by the conduction time of Q_1 ($T_{\rm on}$), and then, the conduction time of Q_2 ($T_{\rm off}$) should be fine-tuned to achieve ZVS. The static-state inductance is used to roughly calculate $T_{\rm on}$, $T_{\rm off}$, and f_s, i.e.,

$$\begin{cases} T_{\rm on} = \frac{I_p L_{\rm ss}}{V_{\rm in}-V_{\rm bus}} = \frac{I_p L_{\rm ss}}{(1/D-1)*V_{\rm bus}} \\ T_{\rm off} = \frac{I_p L_{\rm ss}}{V_{\rm bus}} \\ f_s = \frac{1}{T_{\rm on}+T_{\rm off}} = \frac{(1-D)V_{\rm bus}}{I_p L_{\rm ss}} \end{cases} \tag{1}$$

where $D = V_{\rm bus}/V_{\rm in}$. Note that the resonant time T_r is small and ignored. As shown in Fig. 5, the frequency increases with the decreasing duty cycle D or the increasing $V_{\rm in}$ for the noncoupled case ($\alpha = 0$), whose static-state inductance is constant. However, according to [10], the equivalent static-state inductance ($L_{\rm ss\_eq}$) for a coupled case is no longer a constant and is affected by D. It has

$$\begin{cases} L_{\rm ss\_eq} = \frac{L(1-\alpha^2)}{1+\alpha(1-D)/D}, & D > 0.5 \\ L_{\rm ss\_eq} = \frac{L(1-\alpha^2)}{1+\alpha D/(1-D)}, & D < 0.5 \end{cases} \tag{2}$$

where L is the self-inductance. If both cases have the same frequency at 64 V, their static-state inductance should be equal, i.e., $L_{\rm ss\_eq}(64\ {\rm V}) = L_{\rm ss}(64\ {\rm V})$, and then, the required L is obtained for each specific α. Finally, $L_{\rm ss\_eq}$ of the other $V_{\rm in}$'s are derived and used to estimate f_s based on (1). With negative coupling, the frequency characteristics change significantly, as shown in Fig. 5. The selected α ($= -0.7$) can lower the switching frequency given the same frequency range, and this is another benefit of the coupled inductor.

In this paper, the most attractive benefit of the coupled inductors is the ability for magnetic integration. As shown in Fig. 6, two UI cores are required to implement two inductors in the traditional noncoupled case. By using the coupling concept, the two UI cores can be easily integrated into an EI core. Besides, the flux cancellation can be utilized to further shrink the core size and improve the power density. The details will be discussed later. Considering the above benefits, the negative coupled inductors are used in this paper with $\alpha = -0.7$. In order to achieve high power density, the minimum frequency is selected at 400 kHz.

B. Optimal Design of Planar-Coupled Inductors

The coupled inductors are optimized under the nominal input voltage (110 V) and full-load condition. The use of high frequency can help reduce the turn number, and then, the coupled inductors can be easily integrated with a six-layer PCB. Four winding structures are considered, as shown in Fig. 7, where N_1 is the number of noninterleaved turns and N_2 is the number of interleaved turns. Each inductor has six turns ($N_1 + N_2 = 6$), and the most straightforward integration option is shown in Fig. 7(a), which has no turn interleaved. However, the coupling is very weak in this structure, and the flux of the out legs is large, which would lead to large inductor losses. By using winding interleaving, the coupling becomes stronger and the magnetomotive force (MMF) is reduced [24]. The benefits of PCB winding interleaving have been briefly discussed in [25] and [26] for totem-pole PFC. This paper is to develop a systematic design methodology for the planar-coupled inductors

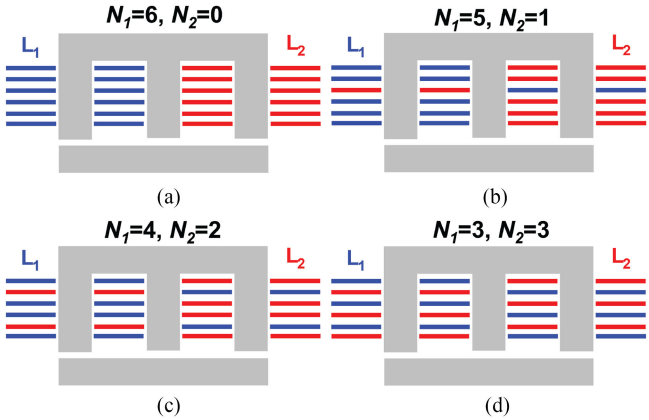


Fig. 7. Different winding structures. (a) No turn interleaved. (b) One turn interleaved. (c) Two turns interleaved. (d) Three turns interleaved.

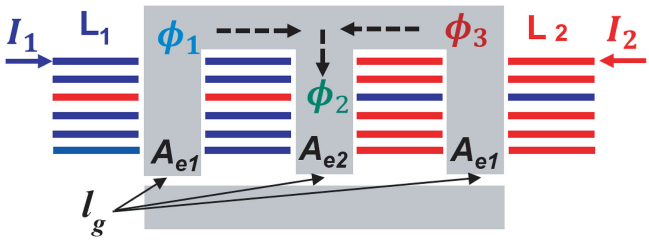


Fig. 8. Flux in the core.

with winding interleaving. The objective is first to achieve the required self-inductance and coupling coefficient for a given winding structure and then minimize the losses by optimizing the core size parameters. There are mainly five steps, and here, the case with one turn interleaved would serve as an example [refer to Fig. 7(b)].

1) Calculate the Inductance: The two-phase interleaved buck converter is working at the CRM. Under the 110-V input voltage and full-load condition, the target switching frequency f_s can be used to derive the required static-state inductance $L_{\rm SS}$ based on the simulation. In [10], the equivalent inductances of a CRM buck converter with coupled inductors have been derived under different switching transition. It also comprehensively explains the relationship among the self-inductance $L(=L_1=L_2)$, the coupling coefficient (α), and $L_{\rm SS}$, which is summarized as

$$L=\frac{L_{\rm SS}+[1+\alpha D/(1-D)]}{1-\alpha^2} \tag{3}$$

where $D=V_{\rm bus}/V_{\rm in}=0.44$. Therefore, the self-inductance L can be derived based on the required $L_{\rm SS}$ and α.

2) Calculate the Reluctance: Fig. 8 gives the cross-sectional view of the EI core. A_{e1} and A_{e2} are the cross-sectional areas of the out leg and the center leg, respectively. The same air gap l_g is applied for all legs because it is good for manufacturing. Based on the winding structure, a reluctance model is built in Fig. 9, where R_{g1} and R_{g2} are the reluctances of the out leg and the center leg, respectively. For the coupled inductors, L and α are directly affected by R_{g1} and R_{g2}. This step is to derive R_{g1} and R_{g2} in terms of the required L and α.

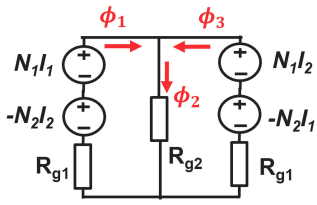


Fig. 9. Reluctance model.

First of all, the flux in each leg can be derived as

$$\phi_1=\frac{N_1I_1-N_2I_2}{R_{g1}+R_{g1}||R_{g2}}+\frac{N_2I_1-N_2I_2}{R_{g1}+R_{g1}||R_{g2}}\frac{R_{g2}}{R_{g1}+R_{g2}} \tag{4}$$

and

$$\phi_2=\frac{N_1I_1-N_2I_2+N_1I_2-N_2I_1}{R_{g1}+R_{g1}||R_{g2}}\frac{R_{g1}}{R_{g1}+R_{g2}}. \tag{5}$$

Then, according to the definition of the self-inductance and mutual inductance, we have

$$L=\frac{N_1\phi_1-N_2\phi_3}{I_1}|_{I_2=0}=\frac{({N_1}^2+{N_2}^2)R_{g1}+(N_1+N_2)^2R_{g2}}{R_{g1}(R_{g1}+2R_{g2})} \tag{6}$$

and

$$\begin{aligned}M&=\frac{N_1\phi_1-N_2\phi_3}{I_2}|_{I_1=0}\\&=\frac{({N_1}^2+{N_2}^2)R_{g2}+2N_1N_2(R_{g1}+R_{g2})}{-R_{g1}(R_{g1}+2R_{g2})}.\end{aligned} \tag{7}$$

For the example interleaving structure with N_1=5 and N_2=1, L and α can be simplified as

$$L=\frac{18}{R_{g1}}+\frac{8}{R_{g1}+2R_{g2}} \tag{8}$$

and

$$\alpha=\frac{M}{L}=-\frac{144R_{g2}}{13(13R_{g1}+18R_{g2})}-\frac{5}{13}. \tag{9}$$

Finally, given the targeted L and α, R_{g1} and R_{g2} are obtained.

3) Calculate A_{e1}, A_{e2}, and l_g: This step calculates A_{e1}, A_{e2}, and l_g based on R_{g1} and R_{g2}. It is well known that the loop reluctance is mainly determined by the air-gap reflectance because the reluctance inside the core can be ignored. Therefore, we have

$$\begin{cases}R_{g1}=\frac{l_g}{A_{e1}\mu_0}\\R_{g2}=\frac{l_g}{A_{e2}\mu_0}.\end{cases} \tag{10}$$

Since R_{g1} and R_{g2} are known, one more constraint is required to uniquely determine A_{e1}, A_{e2}, and l_g, and the core loss density should be used. First of all, the suitable core materials should be first compared in Fig. 10. The ML91S from Hitachi, Ltd., is selected due to its minimum core loss density. Assuming a specific power density P_{V1} for the out leg, a corresponding B_{m1} can be obtained on the green line, such as the star in Fig. 10. According to (4) and (5), the current waveform can be used to plot the flux in each leg, as shown in Fig. 11. The flux magnitude

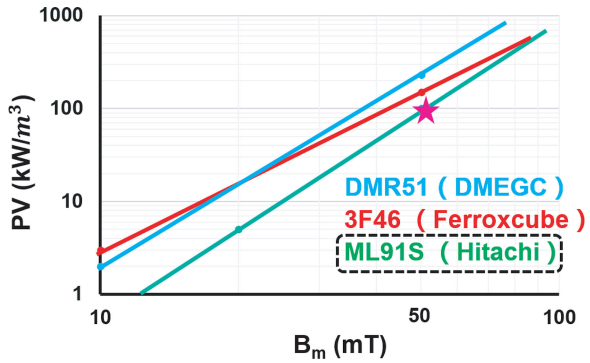


Fig. 10. PV comparison of different core materials.

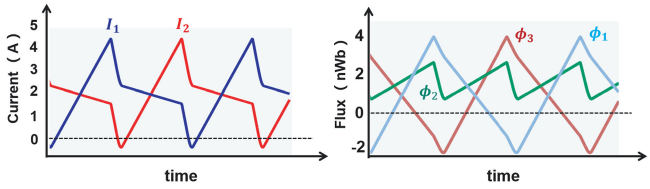


Fig. 11. Inductor currents and the flux of each leg.

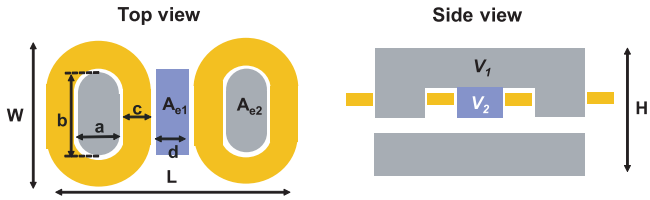


Fig. 12. Top and side views of the inductor core.

in the out leg can then be given by

$$\phi_{1m} = \frac{\text{Max}[\phi_1] - \text{Min}[\phi_1]}{2}. \tag{11}$$

Since

$$\phi_{1m} = B_{m1} A_{e1}, \tag{12}$$

this constraint together with (10) can finally determine the cross-sectional areas and the air gap. It should be noted that the selected P_{V1} is only for the out leg. The core loss density of the center leg P_{V2} is different from P_{V1}. Once A_{e1}, A_{e2}, and l_g are determined, the magnitude of the flux density in the center leg is calculated as

$$B_{m2} = \frac{\phi_{2m}}{A_{e2}} \tag{13}$$

where ϕ_{2m} is the flux magnitude of the center leg. Finally, P_{V2} is obtained from Fig. 10.

4) Relate Inductor Loss to Size Parameters: The proposed EI core is shown in Fig. 12. L, W, and H are the length, width, and height of the coupled inductors, respectively. a is the width of the out leg, b is the length of the out leg, c is the winding width, and d is the width of the center leg. These size parameters a, b, c, and d can uniquely determine the core dimension. Since

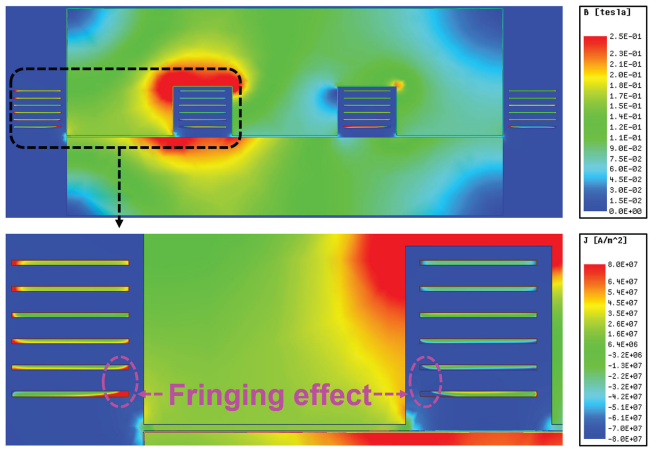


Fig. 13. Magnetic field and current distribution of the planar inductor.

A_{e1} and A_{e2} are known, we have

$$\begin{cases} A_{e1} = 0.25\pi a^2 + b^2 - ba \\ A_{e2} = bd \\ b2a = b : a \\ F_p = L * W = (4c + 2a + d)(2c + b) \end{cases} \tag{14}$$

where Fp is the footprint of the inductors and $b2a$ is the ratio of core length and width for the out leg. Given $b2a$ and F_p, the core size (i.e., a, b, c, and d) is uniquely determined. The volume of the center leg V_2 and the rest parts V_1 are calculated as shown in Fig. 12. The total core loss is

$$P_{\text{core}} = P_{V1} V_1 + P_{V2} V_2. \tag{15}$$

Note that the core loss density (P_{V1} or P_{V2}) is calculated based on the well-known Steinmetz equation. For example, $P_{V1} = k {B_{m1}}^{\sigma} {f_s}^{\tau}$, where k, σ, and τ are provided by the core material datasheet, B_{m1} has been derived based on the reluctance model above, and f_s is known. For a given inductor (i.e., the size is known), the finite-element simulation software, like Maxwell, is used to analyze the winding loss P_{winding}. Fig. 13 shows the magnetic field distribution (in the air and the core) and the current distribution (in the winding). In one inductor, although the total current of each layer is equal, the current is not evenly distributed within each layer because of the nonuniform flux above the layer surface and the fringing effect around the air gap. Therefore, this paper has to use simulation to accurately obtain the winding loss for the inductor. Finally, the total inductor loss is obtained as

$$P_{\text{ind}} = P_{\text{core}} + P_{\text{winding}}. \tag{16}$$

5) Parameter Optimization: The design process to obtain the inductor loss is briefly summarized in Fig. 14. P_{V1}, $b2a$, and F_P should be assumed to uniquely determine the core size, i.e., a design case. In theory, it requires a three-dimensional parameter sweeping to find an optimal design case.

Fig. 15 and 16 show the results of parameter sweeping. It first assumes $P_{V1} = 500\ \text{kW/m}^3$, and then, the inductor loss with different F_p and $b2a$ is shown in Fig. 15. It is interesting to find that the valley region is around $b2a = 2$. This optimal

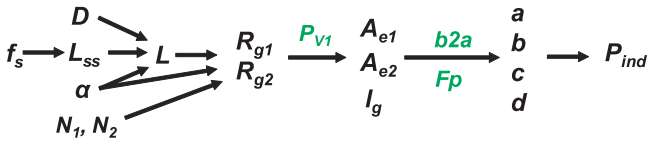


Fig. 14. Design flowchart for the planar-coupled inductors.

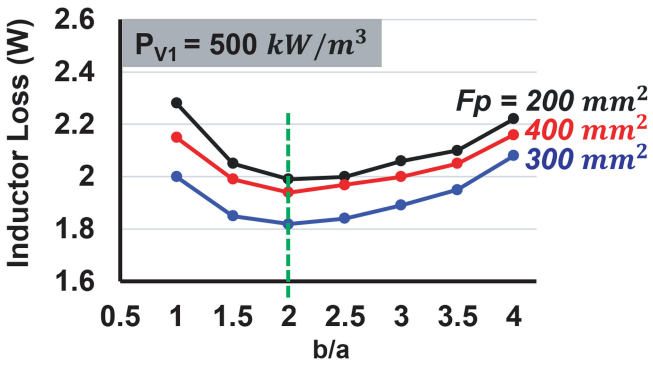


Fig. 15. Inductor loss under different F_p and $b2a$ when $P_{V1} = 500$ kW/m^3.

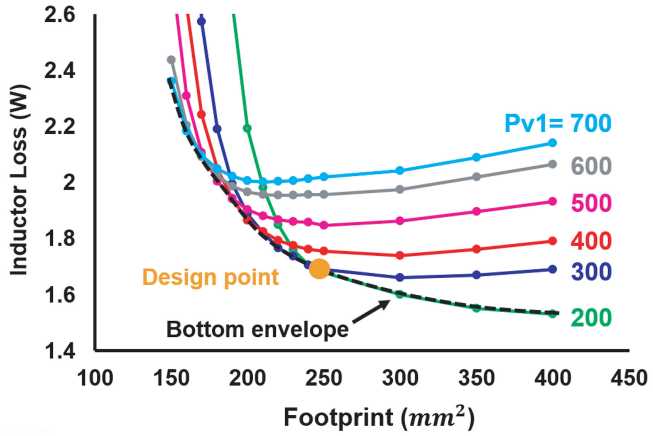


Fig. 16. Inductor loss under different P_{V1}.

ratio is a tradeoff between the core loss and the winding loss. These valley points are used to plot the pink line in Fig. 16, i.e., $P_{V1} = 500$ curve. Similarly, a series of curves for other P_{V1} s are also obtained and compared. The bottom envelope of these curves is the final footprint-loss curve for the example case (see the black-dashed line). This bottom curve clearly shows the tradeoff between the efficiency and the power density. In this paper, the knee point at $F_p = 250$ mm^2 is selected as the final design point.

As mentioned in Fig. 14, the loss-footprint curve obtained from Fig. 16 is only for the example one-turn interleaving structure, i.e., $N_1 = 5$ and $N_2 = 1$. The loss-footprint curve of other interleaving structures can also be obtained in the same way. Fig. 17 compares the two-turn interleaving structure with the one-turn interleaving one. Obviously, the structure with one-turn interleaving is a better option. It should be noted that the coupling of no-turn interleaving and three-turn interleaving is either too small or too large, and thus, these two options are not compared in Fig. 17. Although the inductor is optimized at a given switching frequency, this method is able to be used in a converter optimization by including the device losses, and then, the influence of f_s can be discussed.

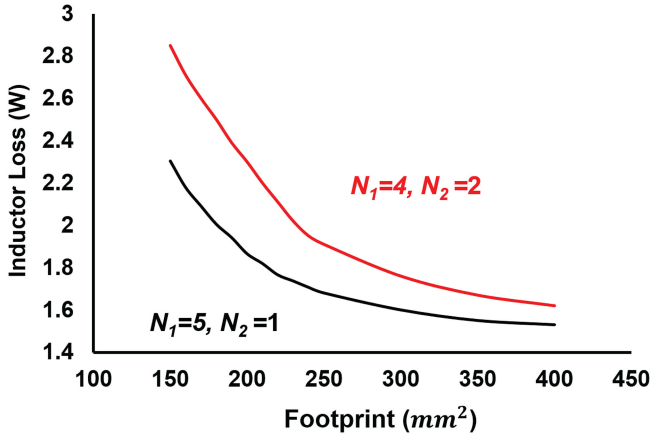


Fig. 17. Inductor loss comparison for different winding interleaving structures.

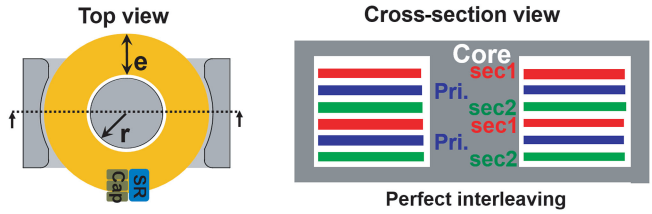


Fig. 18. EI core for the planar transformer.

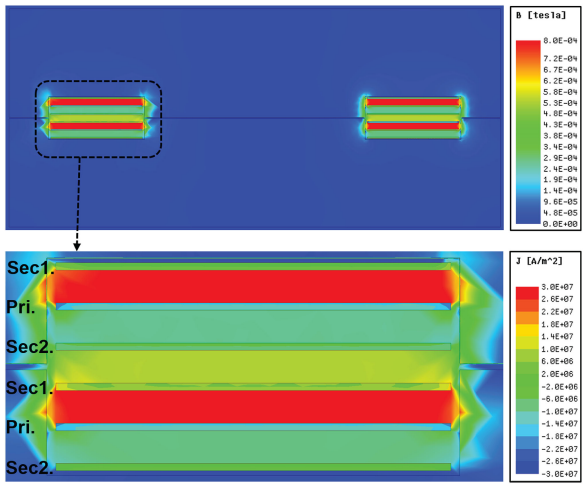


Fig. 19. Magnetic field and current distribution of the planar transformer.

III. Design of the LLC DCX

In this paper, the second power conversion stage is a 48-V/24-V LLC DCX. Considering the output current (= 8 A), there is no need to parallel the secondary devices, i.e., the synchronous rectifier (SR). By using the center-tag configuration, the required turn ratio is 1:1:1. An EI core is used to implement the planar transformer, as shown in Fig. 18. Since a six-layer PCB is used, two layers are paralleled for each turn, and a perfect interleaving structure can be applied to reduce the common-node

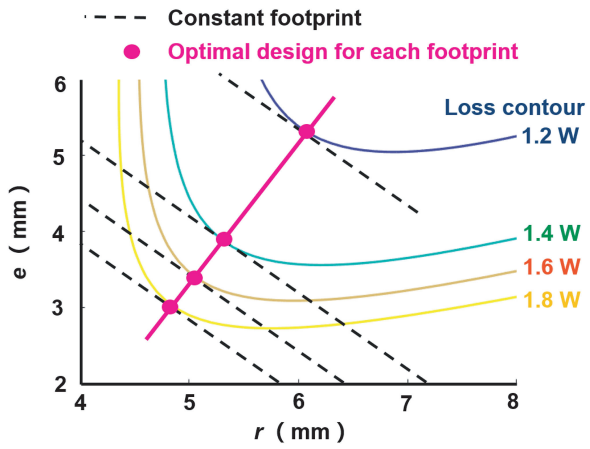


Fig. 20. Transformer loss with different e and r.

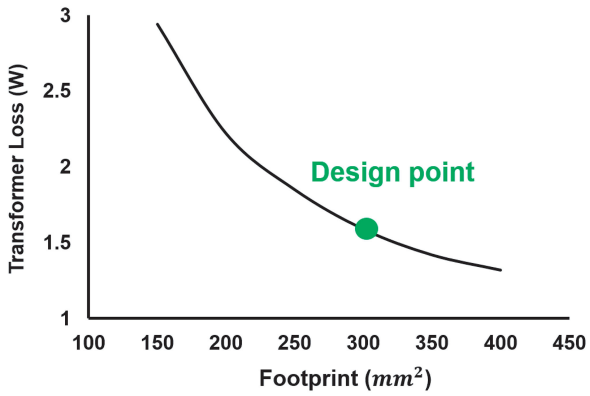


Fig. 21. Loss-footprint curve of the planar transformer.

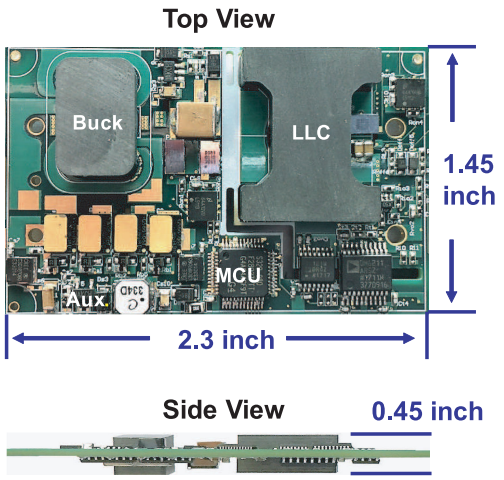


Fig. 22. Prototype system.

noise and the transformer loss. Besides, both the SRs and the output capacitors (i.e., S_1, S_2, and C_{out} in Fig. 2) are integrated with the transformer to reduce the termination loss [19]. The transformer optimization is carried out at the target frequency of 2 MHz. Similar to the inductor, the analytical model based on the Steinmetz equation can still be applied to get the transformer core loss. The major difference here is that the winding loss is also based on the calculation. Fig. 19 shows the magnetic field and current distribution for the proposed transformer. In one half cycle (no current in the layers of Sec2.), the current sharing is good among the paralleled layers (i.e., the layers of Pri. and Sec1.), and the current of each layer is also quite evenly distributed. Note that the fringing effect is very small because of the small air gap. In this case, an analytical loss model can be used to simplify the transformer optimization [18], [27].

TABLE I
SPECIFICATIONS OF THE PROPOSED DC–DC CONVERTER

Buck	Frequency range	>400 kHz
	Devices	G66506T
	Driver	Si8273
	Core material	ML91S
	Inductor self-inductance	7.5 uH
	Coupling coefficient	-0.69
LLC	Frequency	2 MHz
	Dead time	50 ns
	Devices	EPC2031
	Driver	LM5113
	Core material	ML91S
	Magnetizing inductance	500 nH
	Resonant inductance	6.4 nH
	Resonant capacitor	1000 nF

The dimension parameters are shown in Fig. 18, where r is the radius of the center leg, and e is the winding width. The dc winding resistances of the both sides are the same in this structure, i.e.,

$$R_{\text{dc}} = \frac{2\pi\rho}{h}\frac{1}{\ln(r+e)-\ln(r)} \tag{17}$$

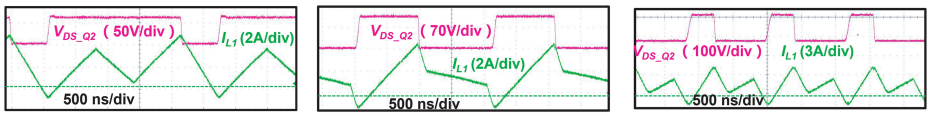
where h is the copper thickness, and ρ is the copper resistivity. The ac wining resistance can be derived using the eddy current model in [18] and [27]

$$R_{\text{ac}} = R_{\text{dc}}[m\text{Real}(M_w) + \frac{m(m^3-1)}{3}\text{Real}(D_w)] \tag{18}$$

where

$$\begin{cases} M_w = \lambda h \coth(\lambda h) \\ D_w = \lambda h \tanh(\lambda h) \\ \lambda = \sqrt{\frac{j2\pi f_{\text{llc}}\mu_0\eta}{\rho}} \end{cases} \tag{19}$$

where f_{llc} is the switching frequency of the LLC DCX and m is the number of the layers till reaching peak MMF. Since perfect interleaving is applied, m equals 1 for both the primary and secondary windings. Finally, the winding loss is calculated. Through comparison, it is found that only small error (=3%) exists between the calculation and the simulation because of the nonperfect current distribution. Therefore, the analytical winding loss model is effective and convenient for the transformer design because it can significantly simplify the optimization.



(a) (b) (c)

Fig. 23. Open-loop waveforms of the buck converter under the 200-W output. (a) $V_{\text{in}} = 64$ V. (b) $V_{\text{in}} = 110$ V. (c) $V_{\text{in}} = 160$ V.

Similar to the coupled inductor design, the core material should be selected at the targeted switching frequency. Again, ML91S is used based on the same consideration (refer to Fig. 10). The maximum core flux density is calculated as

$$B_m = \frac{V_{\text{out}} D_{\text{llc}}}{2 f_{\text{llc}} A_e} \tag{20}$$

where A_e is the cross-sectional area of the core leg and D_{llc} is the duty cycle of the *LLC* converter. Then, the core loss density is calculated by

$$P_v = \frac{8}{\pi^2} k (B_m)^{\beta} (f_{\text{llc}})^{\sigma} \tag{21}$$

where the material parameters k, β, and σ are provided by the datasheet. Finally, the core loss is obtained by

$$P_{c,\text{tran}} = P_v V_{\text{tran}} \tag{22}$$

where V_{tran} is the volume of the core.

Based on the aforementioned winding and core loss models, the total transformer loss is evaluated for different r and e in Fig. 20. The constant loss contours are represented by different solid colored curves. Since the proposed EI core can be roughly viewed as a square, its footprint is estimated as $4(r+e)^2$. Therefore, a constant-footprint curve is a straight dot line (i.e., $r + e$ = constant) in Fig. 20. At those tangent points (i.e., the pink points), the transformer loss is minimized for the given footprint. Finally, these optimal design points can be connected and plotted in Fig. 21. This footprint-loss curve is similar to that of the coupled inductor. The final design point is selected to have a good tradeoff between the efficiency and the power density.

IV. Experimental Verification

The proposed dc–dc converter with the optimized coupled inductors and transformer is shown in Fig. 22. This prototype system is compatible with the benchmark (i.e., SynQor module: RQ1B240QTx06). Therefore, the footprint is a standard quarter brick (2.3 in $\times$ 1.45 in). The final standalone system also includes all the required circuits for a commercial product, such as the power stages, the digital controller, the auxiliary power supply, the protection circuits, and the PMBus chips (supporting external communication). This paper focuses on the design of the planar-coupled inductors and transformer, and the other parts will not be discussed here. The specifications for the power stage are given in Table I.

Two power stages can be tested individually with the open-loop signal. At the full-load condition (i.e., 200 W), the open-loop waveforms of the buck converter are shown in Fig. 23 under different input voltages. $V_{\text{DS\_}Q2}$ is the drain–source voltage of Q_2 (refer to Fig. 2). This regulated stage is to maintain a bus voltage of 48 V. When the input voltage varies, the negative current (I_1) is always used to achieve ZVS under CRM operation. The open-loop waveform of the LLC DCX is shown in Fig. 24, where $V_{\text{DS\_}S1}$ is the drain–source voltage of S_1 and I_{Lr} is the current of L_r (refer to Fig. 2). All the waveforms clearly indicate the ZVS operation of the whole converter.

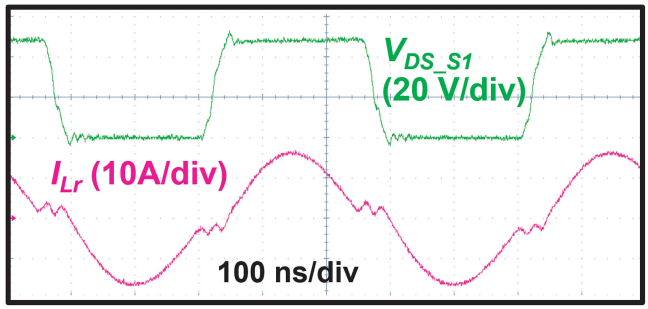


Fig. 24. Open-loop waveform of the LLC DCX under the 200-W output.

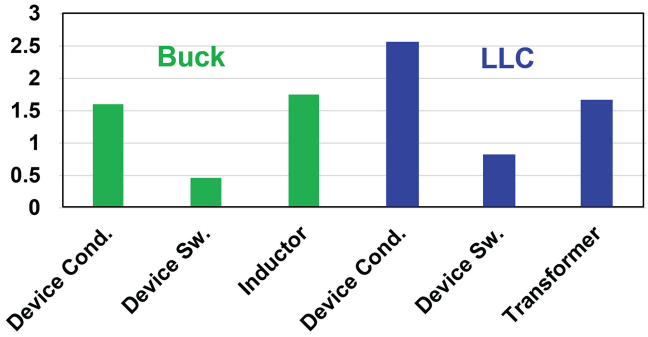


Fig. 25. Loss breakdown under the 200-W output.

In an open-loop system, the loss breakdown of the converter under the 200-W output is shown in Fig. 25, and the efficiencies of both stages are given in Fig. 26. Since the buck converter is regulated, different efficiency curves are obtained for different V_{in}. Under the CRM, larger V_{in} means a higher switching frequency; then, both the device switching losses and inductor loss will increase. Therefore, the efficiency decreases with the increasing V_{in}. The 48-V/24-V LLC DCX is always working at its optimal operating point with the efficiency shown in Fig. 26.

In the final closed-loop system, V_{out} is sensed by the microcontroller unit (MCU) to control the buck converter. The test platform is shown in Fig. 27 under an ambient temperature of 25 °C and a fan speed of 200 linear feet per minute (LFM). The first test is conducted at the output power 200 W for different V_{in}. The highest temperature (=50 °C) occurs at the primary switch of the *LLC* converter when $V_{\text{in}} = 160$ V. There is still a large margin for the temperature rise. It indicates that the converter loss is very small, and the original target output power (=200 W) is too conservative. Therefore, the output power is further

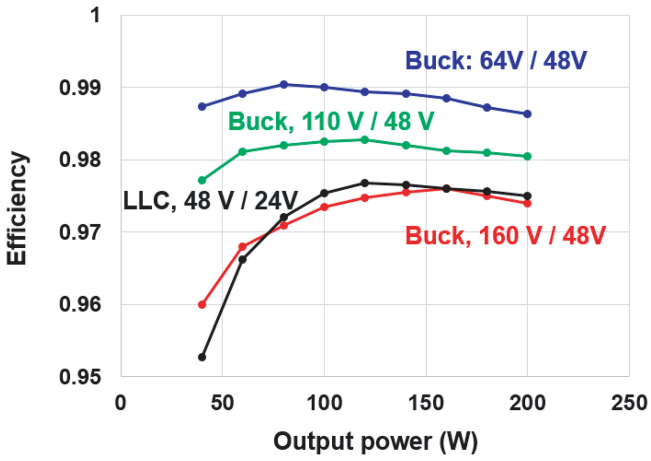


Fig. 26. Open-loop efficiency of both stages.

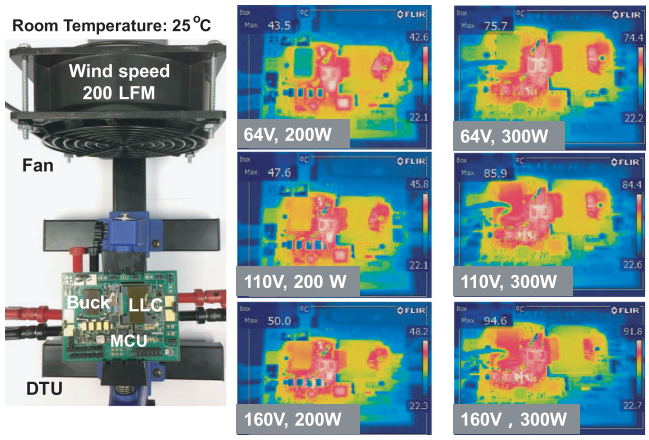


Fig. 27. Thermal test for a closed-loop system.

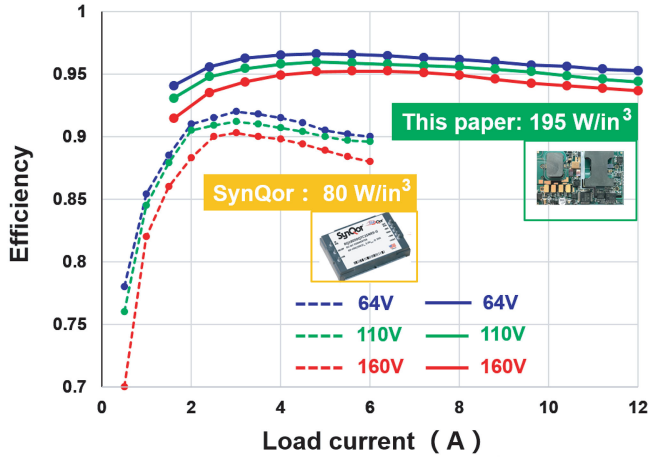


Fig. 28. Efficiency and power density comparison for a closed-loop system.

pushed to 300 W. The highest premature increases to 95 °C, which is durable for the GaN devices. The measured efficiency under different load currents is shown in Fig. 28. The efficiency of the benchmark is also given and compared, whose maximum output current is only 6 A. With the same footprint, the proposed GaN-based converter can achieve much higher efficiency (peak 95.8% at an input voltage of 110 V) and power density (195 W/in^3 at the 300-W output). Note that the closed-loop efficiency is lower than the open-loop one because of the voltage regulation and the MCU power consumption.

V. Conclusion

This paper develops a novel two-stage dc–dc converter for railway applications. In order to have high efficiency and high power density, GaN devices are used, and ZVS is achieved for all devices with the proposed topology. Thus, switching frequency can be pushed to at least ten times higher than the state-of-the-art products, which helps build high-efficiency planar magnetic components with limited PCB layers. For the two-phase interleaved CRM buck converters, the negative coupled inductors are used to reduce the conduction losses, lower the switching frequency, and help achieve magnetic integration. A systematic design methodology is proposed to optimize the planar-coupled inductors based on the finite-element simulation. For the LLC DCX, an analytical model is used to optimize the transformer loss. Finally, a standalone prototype converter is built with the proposed planar-coupled inductors and transformer in a quarter brick form. The measured peak efficiency can reach 95.8% with the power density at 195 W/in^3. The future work is to develop the modeling and control for this converter.

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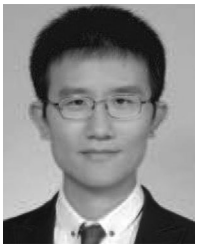
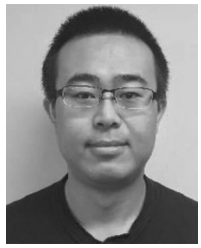


Minfan Fu (S'13–M'16) received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from the University of Michigan–Shanghai Jiao Tong University Joint Institute, Shanghai Jiao Tong University, Shanghai, China, in 2010, 2013, and 2016, respectively.

He is currently an Assistant Professor with the School of Information Science and Technology, ShanghaiTech University, Shanghai. Between 2016 and 2018, he was a Postdoctoral Researcher with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. His research interests include megahertz wireless power transfer, high-frequency power conversion, high-frequency magnetic design, and application of wide-bandgap devices.



Chao Fei (S'13–M'18) received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2012, and the M.S. and Ph.D. degrees in electrical engineering from the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, in 2015 and 2018, respectively.

He is currently a Hardware Engineer with Google Inc., Mountain View, CA, USA. His research interests include high-frequency power conversion, resonant converters, digital control, and high-frequency magnetics.

Yuchen Yang (S'12) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2011, and the M.S. degree in electrical engineering in 2014 from the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, where he is currently working toward the Ph.D. degree.

His research interests include electromagnetic interference/electromagnetic compatibility in power electronics systems, high-frequency power conversion, and high-frequency magnetic components.

Qiang Li (M'11) received the B.S. and M.S. degrees in power electronics from Zhejiang University, Hangzhou, China, in 2003 and 2006, respectively, and the Ph.D. degree in electrical engineering from Virginia Tech, Blacksburg, VA, USA, in 2011.

He is currently an Associate Professor with the Center for Power Electronics Systems, Virginia Tech. His research interests include high-density electronics packaging and integration, high-frequency magnetic components, and high-frequency power conversion.

Fred C. Lee (S'72–M'74–SM'87–F'90–LF'12) received the B.S. degree in electrical engineering from the National Cheng Kung University, Tainan, Taiwan, in 1968, and the M.S. and Ph.D. degrees in electrical engineering from Duke University, Durham, NC, USA, in 1972 and 1974, respectively.

He is currently a University Distinguished Professor with Virginia Tech, Blacksburg, VA, USA, and the Director of the Center for Power Electronics Systems (CPES), a National Science Foundation Engineering Research Center (NSF ERC) established in 1998, with four university partners: University of Wisconsin–Madison, Rensselaer Polytechnic Institute, North Carolina A&T State University, and University of Puerto Rico-Mayagüez and more than 80 industry members. The Center's vision is "to provide leadership through global collaboration to create electric power processing systems of the highest value to society." Over the ten-year NSF ERC Program, the CPES has been cited as a model ERC for its industrial collaboration and technology transfer, as well as education and outreach programs. He holds 82 U.S. patents and has authored or coauthored 296 journal articles and more than 722 refereed technical papers. During his tenure with Virginia Tech, he has supervised 84 Ph.D. and 93 master's students. His research interests include high-frequency power conversion, distributed power systems, renewable energy, power quality, high-density electronics packaging and integration, and modeling and control.

Dr. Lee was a recipient of the William E. Newell Power Electronics Award in 1989, the Arthur E. Fury Award for Leadership and Innovation in Advancing Power Electronic Systems Technology in 1998, and the Ernst-Blickle Award for achievement in the field of power electronics in 2005. He was the President of the IEEE Power Electronics Society in 1993–1994. He was named to the U.S. National Academy of Engineering in 2011. He was named to the Academia Sinica of Taiwan in 2012. He was also named to the Chinese Academy of Engineering in 2013.