Indirect Input-Series Output-Parallel DC–DC Full Bridge Converter System Based on Asymmetric Pulsewidth Modulation Control Strategy

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***Abstract*—This paper proposes an indirect input-series output-parallel (I^2SOP) dc–dc full-bridge converter system based on asymmetric pulsewidth modulation (APWM) control strategy for high input voltage applications. When a short-circuit fault occurs in a high input voltage dc bus, the proposed I^2SOP system can disconnect from the dc bus effectively and avoid the input filter capacitors of constituent modules discharge compared with the traditional ISOP system, facilitating fault handling and protecting the input filter capacitors. Moreover, with the proposed I^2SOP structure, it is easy to achieve redundancy design when one or a few constituent modules fail. The APWM control strategy is introduced to the I^2SOP system rather than the classical phase-shifted control strategy for the basic full-bridge module to reduce the voltage stress of power switch and the filter requirement. The characteristics of input voltage sharing and output current sharing of the I^2SOP system are also analyzed. A three-module I^2SOP system prototype was built, and the experimental results verify the correctness and effectiveness of the proposed solution.**

***Index Terms*—Asymmetric pulsewidth modulation (APWM) control strategy, full-bridge converter, fault handling, indirect input-series output-parallel (I^2SOP).**

I. Introduction

A SERIES–parallel combined power conversion system, in which multiple standardized modules are connected in series and/or parallel at the input and output sides, is an effective approach to improve the voltage and/or current ratings of power electronics equipment. Generally, the series–

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voltage will collapse and experience discharge, leading to high transient current under dc bus short-circuit fault condition [20]. If this high transient current is not limited, the stored energy in the capacitors will cause hazard to capacitors as well as connected equipment. Moreover, a much higher break capability of the dc breakers will be required if the discharging current from the concentrated capacitor is not limited [21]. In order to alleviate the damage caused by the discharging concentrated capacitor, it is desirable to disconnect the concentrated capacitor as soon as the fault is detected. In [21], a semiconductor switch (such as IGBT with an antiparallel diode) is connected in series with the capacitor, and under normal condition, the IGBT is always turned ON to flow ripple current of the capacitor. When the short-circuit fault is detected, the IGBT is turned OFF and the capacitor will not discharge. This dc fault protection method is also effective when it is used to each constituent modules of the ISOP system [22]. Zhao *et al.* [23]–[25] proposed a solution based on half-bridge switched capacitor submodule to address the aforementioned issue. One terminal of a constituent module is connected to the dc terminal of a half-bridge switched capacitor submodule and all the ac terminals of the half-bridge switched capacitor submodules are connected in series to interface the dc bus voltage. It can be seen that there is no single concentrated capacitor, and when the dc short-circuit fault is detected, the IGBTs of all half-bridge switched capacitor submodules are turned OFF and the discrete capacitors will not discharge. These methods solve the dc bus fault issues at the price of external switches, drivers, and conduction and switching losses.

For the ISOP system, the input terminal of the faulted module has to be shorted to keep the remaining modules operate normally and the dc capacitor of the faulted module will be short-circuited [26], [27]. In [26], a protection circuit for fault-tolerant operation using a thyristor was proposed, and a current limiting inductor was also required to suppress the large transient discharge current of the capacitor. In [27], an active gate controlled power transfer switch using SiC-MOSFET to suppress the surge current was proposed to achieve the fault-tolerant operation of the ISOP system. It can be seen that additional active devices and/or passive components are required in order to suppress the large transient discharge current of the capacitor of the faulted module.

With a special focus on issues of the concentrated capacitor discharge under dc bus fault and the discrete capacitor discharge under fault-tolerant operation of the ISOP system, this paper proposes an indirect ISOP (I^2SOP) system with a full-bridge converter as the basis module. Compared with the aforementioned solutions, the proposed I^2SOP structure is a very simple approach with almost no additional device and component. Furthermore, an asymmetric pulsewidth modulation (APWM) control strategy [28] is introduced for the basic full-bridge module to decrease the voltage stress of power switch compared with the traditional phase-shifted (PS) control strategy [29], which will be thoroughly discussed in the following section. The analysis and comprehensive experimental results are provided in this paper.

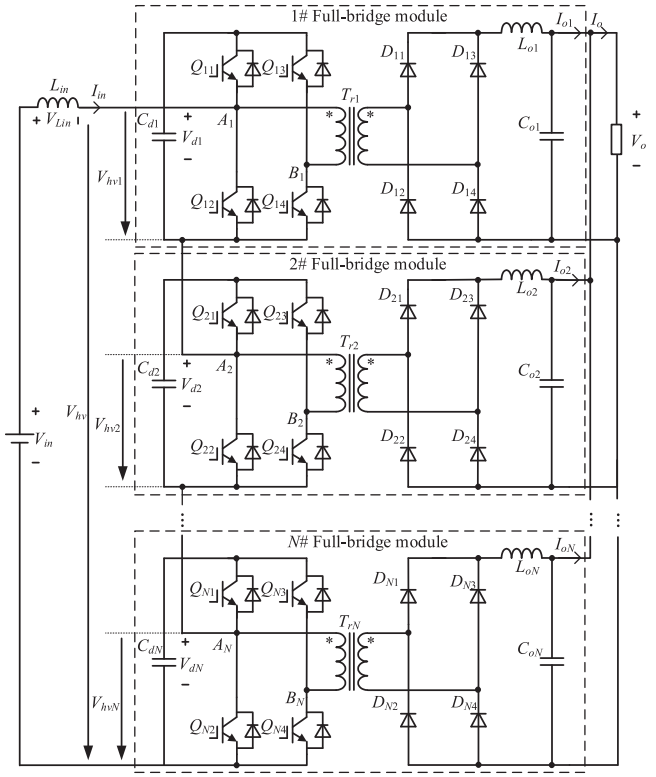

Fig. 1. Topology of the proposed I^2SOP system.

II. Circuit Configuration and Operation Principles

A. Description of the Proposed I^2SOP System and Control Strategy

The topology of the proposed I^2SOP system with a full-bridge converter as the basic module is shown in Fig. 1. The main circuit consists of N series-connected full-bridge modules, compared with the traditional ISOP system where the positive terminal of system input voltage is directly (or through a filter inductor) connected to the positive electrode of the filter capacitor of the first module [3], [12], the positive terminal of I^2SOP system input voltage is connected to a midpoint (A_1) of a bridge leg of the first full-bridge module through a filter inductor, and the negative electrode of the filter capacitor of the first module is connected to a midpoint (A_2) of a bridge leg of the second full-bridge module; thus, in this way, all the full-bridge modules are indirectly connected, as shown in Fig. 1. It can be seen that unlike the traditional ISOP system where all the filter capacitors of modules are directly connected in series to form a concentrated capacitor, in the I^2SOP system, there is no physical connection among the filter capacitors of modules, and the electrical connections are achieved by the switches.

In Fig. 1, $V_{\rm in}$ and $I_{\rm in}$ are the system input voltage and current, respectively. V_o and I_o are the system output voltage and current, respectively. V_{dj} and $V_{{\rm hv}j}$ are the input terminal voltage and bridge leg midpoint voltage of each full-bridge module, respectively, and $V_{\rm hv}$ is the sum of all $V_{{\rm hv}j}$ $(j = 1,\ldots,N)$.

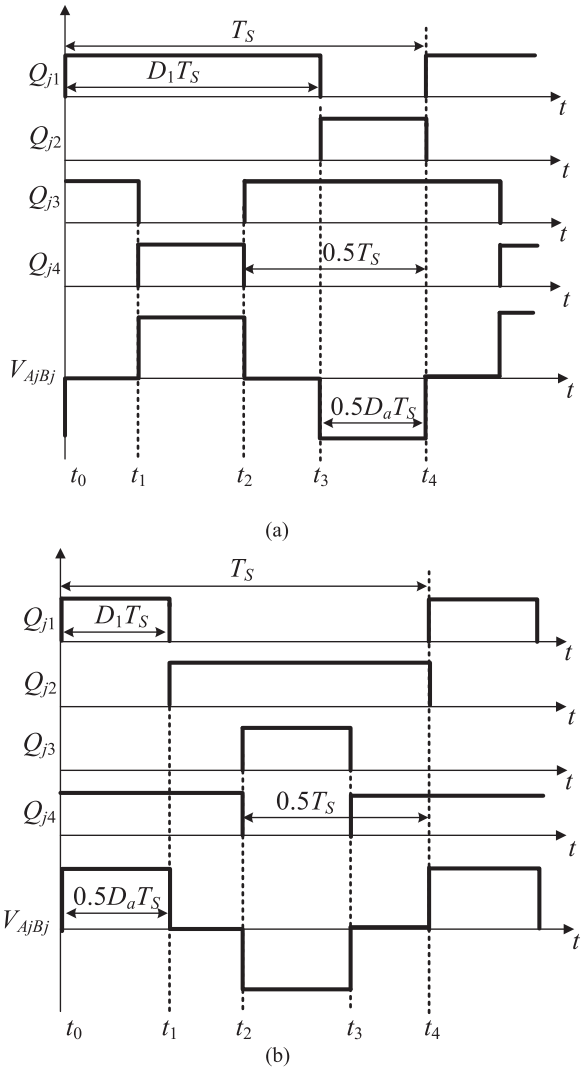

Fig. 2. Main waveforms of the APWM control strategy. (a) #1 control method. (b) #2 control method.

$V_{L\text{in}}$ is the voltage across the input filter inductor. Turns ratios of all transformers are the same and are equal to 1:*K*.

In order to analyze the operation principle of the proposed structure, the following conditions are assumed.

1) All the switches, diodes, inductors, and capacitors are ideal.
2) The input inductance L_{in} is large enough so that the input current I_{in} is considered as a constant current at steady state.
3) The output filter capacitors C_{oj} $(j = 1,\ldots,N)$ are large enough so that the output voltage V_o is considered as a constant voltage at steady state.
4) The leakage inductance of transformers T_{rj} $(j = 1,\ldots,N)$ is small enough so that can be ignored.

Fig. 2 shows the main waveforms of the APWM control strategy [28], where switches Q_{j1} and Q_{j2} are switched out of phase and Q_{j3} and Q_{j4} are switched out of phase. T_S is the switching period and D_a is the duty cycle to regulate the system output voltage to a desired value. V_{AjBj} is symmetrical as Q_{j2} and Q_{j4} are gated with the same duty cycle.

According to [28], two gating signal methods can be applied to $Q_{j1} \sim Q_{j4}$ to obtain the same output voltage for a single full-bridge converter. The first method is shown in Fig. 2(a), where the duty cycle of Q_{j1} is controlled as $0.5 \le D_1 < 1$, which is called as #1 control method. The second method is shown in Fig. 2(b), where the duty cycle of Q_{j1} is controlled as $0 < D_1 \le 0.5$, which is called as #2 control method. Although both control methods can be used to obtain the same output voltage for a single full-bridge converter, they have total different effects on the I^{2}SOP system, which will be discussed at present. Assuming the duty cycles of all the full-bridge modules are identical and the input voltages of modules are the same, i.e., $V_{d1} = V_{d2} = \cdots = V_{dN} = V_d$.

Then, we have

$$V_{\text{hv}1} = V_{\text{hv}2} = \cdots = V_{\text{hv}N} = D_1 V_d. \tag{1}$$

For the input filter inductor L_{in}, the average voltage across it during one period can be derived as follows:

$$V_{L\text{in}} = V_{\text{in}} - \sum_{j=1}^{N} V_{\text{hv}j} = V_{\text{in}} - N D_1 V_d. \tag{2}$$

At steady state, the average voltage across L_{in} is zero. Thus, the following equation is obtained:

$$V_d = \frac{V_{\text{in}}}{N D_1}. \tag{3}$$

For the full-bridge module, ignoring the duty cycle loss, the system output voltage is

$$V_o = V_d D_a K \tag{4}$$

where D_a is the duty cycle of V_{AjBj} and $D_a = 2(t_4 - t_3)/T_s$.

For the #1 control method [see Fig. 2(a)], we have

$$D_1 T_s + 0.5 D_a T_s = T_s. \tag{5}$$

From (3)–(5), we have

$$V_o = 2(1 - D_1) K \frac{V_{\text{in}}}{N D_1}, \quad (0.5 \le D_1 < 1). \tag{6}$$

For the #2 control method [see Fig. 2(b)], we have

$$D_1 T_s = 0.5 D_a T_s. \tag{7}$$

From (3), (4), and (7), we have

$$V_o = 2K \frac{V_{\text{in}}}{N}, \qquad (0 < D_1 \le 0.5). \tag{8}$$

Combining (6) and (8), the system output voltage can be expressed as

$$V_o = \begin{cases} 2(1 - D_1) K \frac{V_{\text{in}}}{N D_1}, & (0.5 \le D_1 < 1) \\ 2K \frac{V_{\text{in}}}{N}, & (0 < D_1 \le 0.5). \end{cases} \tag{9}$$

From (9), it can be seen that the system output voltage is directly proportional to the system input voltage when #2 control method is used. In other words, the system output voltage cannot

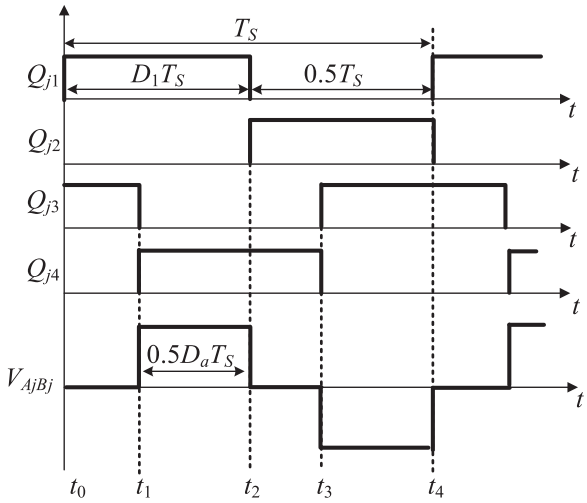

Fig. 3. Main waveforms of the PS control strategy.

be regulated to a constant desired value in system input voltage range with #2 control method, while the system output voltage can be regulated to a constant desired value with a variation of D_1 when #1 control method is used. Hence, only #1 control method is effective for the I^{2}SOP system with the full-bridge converter as the basic module, which is different from [28].

From (3), it can be seen that compared to the traditional ISOP system, the voltage rating of devices and capacitors in each module is boosted up. Therefore, there might be some limitations in the proposed scheme in terms of the duty cycle range or step gain range in a practical application, when comparing it with the traditional ISOP system, assuming the transfer gain and module numbers are the same for cost and loss concerns. So, to keep the voltage rating of devices and capacitors constant, more modules are needed, but the transfer power of each module is reduced at the same time.

B. Comparison Between the APWM Control Strategy and the PS Control Strategy

Fig. 3 shows the main waveforms of the PS control strategy for a full-bridge converter, in which the duty cycle of each switch is fixed to be 50%, i.e., $D_1 = 0.5$.

According to (3), the input voltage of full-bridge module of the I^{2}SOP system with the PS control strategy can be expressed as

$$V_{d\_p} = 2\frac{V_{\text{in}}}{N}. \tag{10}$$

Then, the system output voltage can be expressed as

$$V_{o\_p} = V_{d\_p} D_a K = 2D_a K \frac{V_{\text{in}}}{N}. \tag{11}$$

Equation (10) indicates that the module input voltage is proportional to the system input voltage with the PS control strategy, while for the APWM control strategy, according to (3) and (6), the module input voltage is related to not only with the system input voltage but also with the duty cycle of the switch.

A simple example is given here to compare the effects of the different control strategies on the module input voltage. The

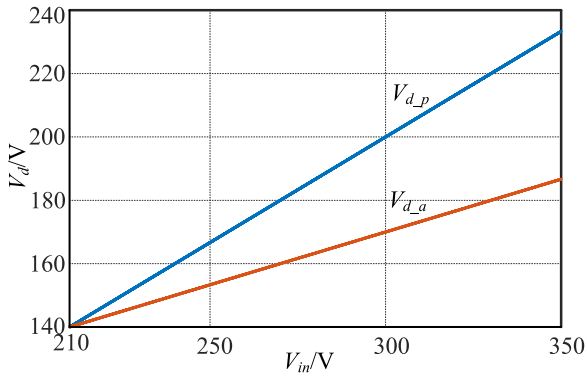

Fig. 4. Comparison of the module input voltages with two different control strategies in the system input voltage range.

number of modules is $N = 3$, the system input voltage V_{in} ranges from 210 to 350 V, the system output voltage is 70 V, and the transformer turns ratio is $K = 0.5$. For both control strategies, the duty cycle D_a is designed to be 1 at the minimum system input voltage.

According to (10), we have

$$V_{d\_p} = 2\frac{V_{\text{in}}}{3}. \tag{12}$$

Combining (3) and (6), we have

$$V_{d\_a} = \frac{2KV_{\text{in}} + V_o N}{2KN} = 70 + \frac{V_{\text{in}}}{3}. \tag{13}$$

Fig. 4 shows the curves of module input voltages with different control strategies in the system input voltage range. Note that 210 V is the minimum input voltage with closed-loop control. It can be seen that with the introduction of the APWM control strategy, the voltage stress of switches can be effectively reduced compared with that with the PS control strategy.

Furthermore, a comparison of duty cycle D_a in two different control strategies is also presented.

According to (11), the duty cycle of the PS control strategy can be expressed as

$$D_{a\_p} = \frac{NV_o}{2KV_{\text{in}}} = \frac{210}{V_{\text{in}}}. \tag{14}$$

Combining (5) and (6), the duty cycle of the APWM control strategy can be expressed as

$$D_{a\_a} = \frac{NV_o}{KV_{\text{in}} + 0.5NV_o} = \frac{420}{V_{\text{in}} + 210}. \tag{15}$$

Fig. 5 shows the curves of duty cycle D_a with different control strategies in the system input voltage range. Note that 210 V is the minimum input voltage with closed-loop control. It can be seen that the duty cycle of the APWM control strategy is obviously larger than that of the PS control strategy. For the APWM control strategy, the basic full-bridge module has lower input voltage and larger duty cycle, leading to much smaller input/output voltage/current ripples, and the filter requirement can be decreased.

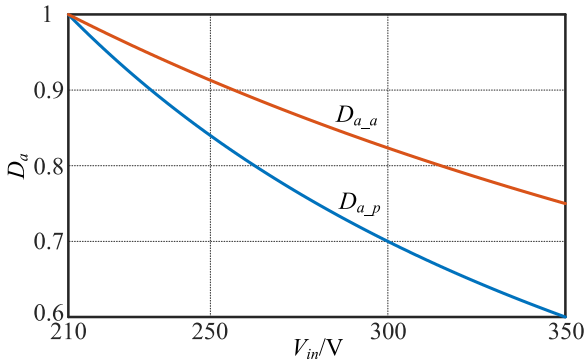

Fig. 5. Comparison of the duty cycles with two different control strategies in the system input voltage range.

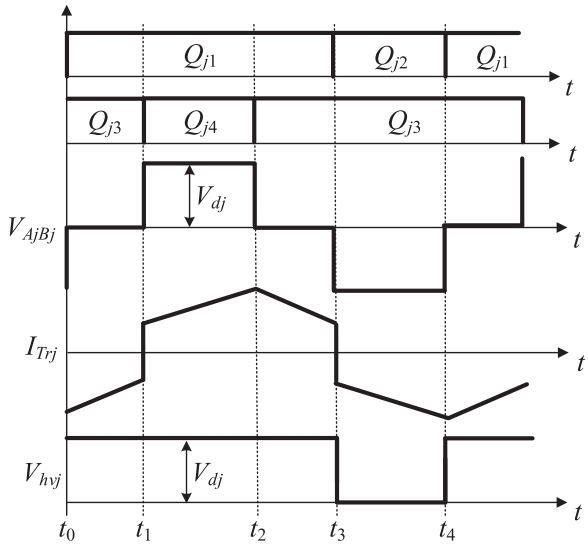

Fig. 6. Key waveforms of the *j*th full-bridge module.

C. Operation Principle

In [28], the operation principle of a new zero-voltage and zero-current switching full-bridge converter with the APWM control strategy has been presented. In this subsection, the operation principle of a traditional full-bridge converter (the basic module of the I^{2}SOP system) with the APWM control strategy will be simply analyzed. The key waveforms are shown in Fig. 6, and the equivalent circuits of each operation stages are shown in Fig. 7. It should be noted that to realize the soft-switching for power switches, extra capacitors are connected in parallel with power switches, which are not shown in Figs. 1 and 7.

1) Stage 1 $[t_0, t_1]$ [see Fig. 7(a)]: At t_0, Q_{j2} is turned OFF and Q_{j1} is turned ON with a certain dead time, and Q_{j1} is turned ON with zero-voltage condition due to L_{rj} and L_{oj}. During this stage, the voltage $V_{AjBj} = 0$ and the primary current of the transformer freewheels through Q_{j3} and body diode of Q_{j1}. The input terminal voltage $V_{\text{hv}j} = V_{dj}$, and the input capacitor C_{dj} is charged.
2) Stage 2 $[t_1, t_2]$ [see Fig. 7(b)]: At t_1, Q_{j3} is turned OFF and Q_{j4} is turned ON with a certain dead time, and Q_{j4} is turned ON with zero-voltage condition (also depends on the load condition) due to L_{rj}. During this stage, C_{dj} powers the load. $V_{\text{hv}j} = V_{dj}$, and C_{dj} is discharged.
3) Stage 3 $[t_2, t_3]$ [see Fig. 7(c)]: At t_2, Q_{j4} is turned OFF and Q_{j3} is turned ON with a certain dead time, and Q_{j3} is turned ON with zero-voltage condition due to L_{rj} and L_{oj}. The full-bridge module operates in freewheeling state in this stage. $V_{\text{hv}j} = V_{dj}$, and C_{dj} is charged.
4) Stage 4 $[t_3, t_4]$ [see Fig. 7(d)]: At t_3, Q_{j1} is turned OFF and Q_{j2} is turned ON with a certain dead time, and Q_{j2} is turned ON with zero-voltage condition (also depends on the load condition) due to L_{rj}. During this stage, C_{dj} powers the load. $V_{\text{hv}j} = 0$, and C_{dj} is discharged.

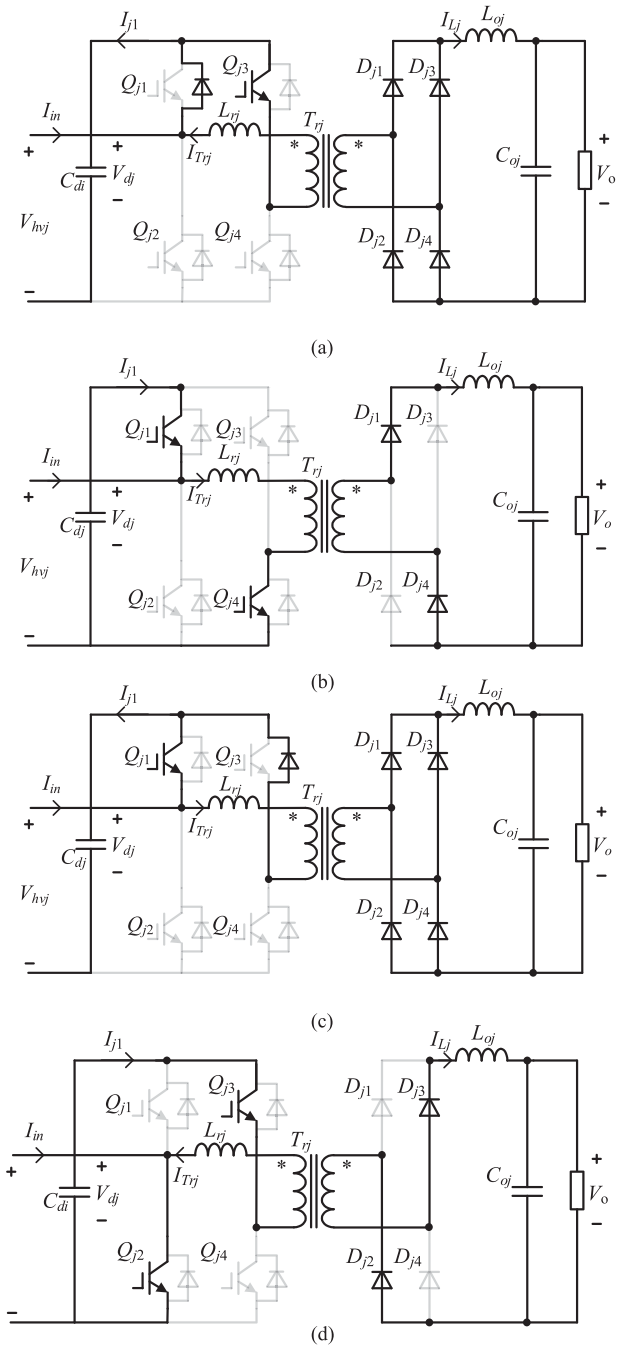

Fig. 7. Equivalent circuits of all operation stages. (a) Stage 1 $[t_0, t_1]$. (b) Stage 2 $[t_1, t_2]$. (c) Stage 3 $[t_2, t_3]$. (d) Stage 4 $[t_3, t_4]$.

From the above-mentioned analysis, it is concluded that Q_{j1} and Q_{j3} are easy to realize zero-voltage turn-ON, and Q_{j2} and Q_{j4} are relatively difficult to realize zero-voltage turn-ON. While for the PS control strategy, Q_{j1} and Q_{j2} (or Q_{j3} and Q_{j4}) are easy to realize zero-voltage turn-ON, while Q_{j3} and Q_{j4} (or Q_{j1} and Q_{j2}) are relatively difficult to realize zero-voltage turn-ON [28]. Hence, the APWM control strategy has the similar soft-switching characteristics compared with those of the PS control strategy. It also should be noted that due to the shorter conduction times of Q_{j2} and Q_{j4} compared to those of Q_{j1} and Q_{j3} in the APWM control strategy, the conduction losses of Q_{j2} and Q_{j4} are lower than those of Q_{j1} and Q_{j3}. While for the PS control strategy, the conduction losses of four switches are approximately the same.

For the control of the I²SOP system, a fixed phase shift of $2\pi/N$ is added between adjacent full-bridge modules to reduce the input and output current ripples. Fig. 8 shows the main waveforms of a three-module I²SOP system. The operation can be divided into the following two states.

1) $0.5 \le D_1 \le 2/3$

$$V_{\rm hv}(t) = \begin{cases} V_d & t \in \left[\frac{kT_s}{3}, \frac{kT_s}{3} + \left(\frac{2}{3} - D_1\right)T_s\right] \\ 2V_d & t \in \left[\frac{kT_s}{3} + \left(\frac{2}{3} - D_1\right)T_s, \left(\frac{k+1}{3}\right)T_s\right] \end{cases} \quad k = 0, 1, 2. \tag{16}$$

2) $2/3 < D_1 < 1$

$$V_{\rm hv}(t) = \begin{cases} 2V_d & t \in \left[\frac{kT_s}{3}, \frac{kT_s}{3} + (1 - D_1)T_s\right] \\ 3V_d & t \in \left[\frac{kT_s}{3} + (1 - D_1)T_s, \left(\frac{k+1}{3}\right)T_s\right] \end{cases} \quad k = 0, 1, 2. \tag{17}$$

Similarly, for *N* modules, we have

$$V_{\rm hv}(t) = \begin{cases} (N - m - 1)V_d & t \in \left[\frac{kT_s}{N}, \left(\frac{k-m}{N} + 1 - D_1\right)T_s\right] \\ (N - m)V_d & t \in \left[\left(\frac{k-m}{N} + 1 - D_1\right)T_s, \left(\frac{k+1}{N}\right)T_s\right] \end{cases} \quad k = 0, 1, 2, \ldots, N - 1 \tag{18}$$

where *m* is an integer.

When N is an odd number, $D_1 \in [\frac{1}{2}, \frac{N+1}{2N}) \cup [1 - \frac{m+1}{N}, 1 - \frac{m}{N}) m \in [0, \frac{N-3}{2}]$.

When N is an even number, $D_1 \in [1 - \frac{m+1}{N}, 1 - \frac{m}{N})$ $m \in [0, \frac{N-2}{2}]$.

The current ripple of the input filter inductor can be derived as

$$\begin{aligned} \Delta I_p &= I_{\max} - I_{\min} \\ &= -\frac{[V_{\rm in} - (N - m)V_d]}{L_{\rm in}} \left[\frac{m+1}{N} - (1 - D_1)\right] T_s \\ &= \frac{V_{\rm in}(1 - D_1)T_s}{L_{\rm in}} \\ &\quad \times \left\{\frac{[N(1 - D_1) - m][m + 1 - N(1 - D_1)]}{(N - ND_1)(ND_1)}\right\}. \end{aligned} \tag{19}$$

According to (19), the current ripple still changes with D_1. It can be seen from Fig. 8 that with the same switching frequency, the ripple frequencies of $V_{\rm hv}$ and $I_{\rm in}$ increase by *N* times, thus decreasing the input current ripple. Besides the input current ripple, the output current ripple is also decreased due to the fixed phase shift control among the constituent modules.

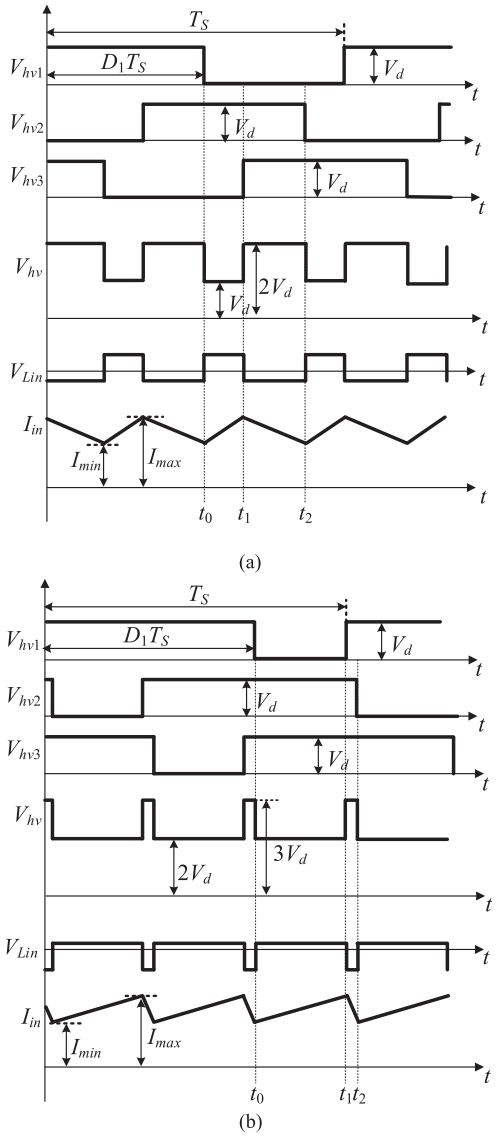

Fig. 8. Key waveforms of the three-module I²SOP system. (a) $0.5 \le D_1 \le 2/3$. (b) $2/3 < D_1 < 1$.

If no phase shift angle existed between the modules, based on (2), the current ripple of the input filter inductor can be derived as

$$\Delta I'_p = I'_{\max} - I'_{\min} = \frac{V_{\rm in}(1 - D_1)}{L_{\rm in}} T_s. \tag{20}$$

Based on (19) and (20), G_P is defined as the current ripple ratio as follows:

$$G_P = \frac{\Delta I_p}{\Delta I'_p} = \frac{[N(1 - D_1) - m][m + 1 - N(1 - D_1)]}{(N - ND_1)(ND_1)}. \tag{21}$$

Fig. 9 shows the curves of the current ripple ratio G_p varying with the duty cycle D_1. It can be seen that G_p is always smaller than 1/*N*, which means that the current ripple is reduced

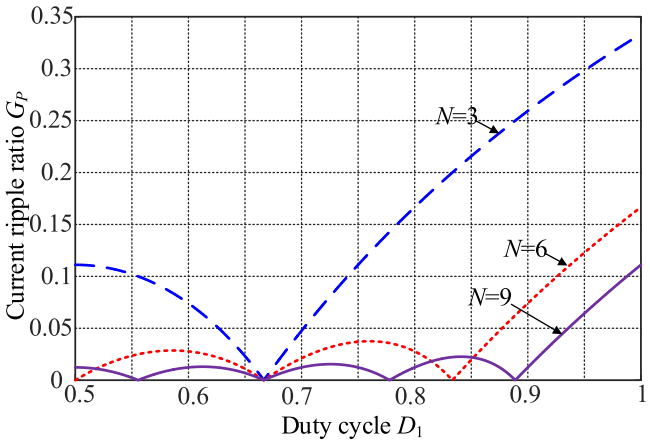

Fig. 9. Curves of the current ripple ratio G_P with the duty cycle D_1.

TABLE I
MAIN PARAMETERS

Parameters	Module 1	Module 2	Module 3
Input voltage V_{in}	220 V		
Input inductor L_{in}	1.2 mH		
Turns Ratios of transformers	1:0.65	1:0.6	1:0.55
Input capacitor C_d	1 mF		
Resistor R	1 Ω		
Output voltage V_o	70 V		

dramatically with the phase shift angle between modules. Thus, the voltage ripple and current impact are also decreased, which can reduce the volume of the input filter inductor with the same standard for the current ripple in the I^{2}SOP system. Furthermore, as the input current ripple is reduced, the current ripple of the input capacitor can also be reduced, which is beneficial for its lifespan.

III. Balance Analysis and Control Strategies

A. Balance Characteristic Analysis

For the traditional ISOP system, a plenty of control strategies were proposed aiming at the balance operation of the system, i.e., IVS and OCS [2]–[14]. By power conservation, the following conclusion can be obtained for the ISOP system: If the module input voltages are equal, the module output currents will be nearly equal, and, on the other hand, if the module output currents are equal, the module input voltages will be nearly equal; in other words, once IVS is achieved, OCS is nearly achieved automatically and vice versa [1]. However, for the proposed I^{2}SOP system, the input currents of modules are not necessarily equal due to their input terminals are not directly connected in series, unlike the ISOP system in which the input currents of modules are naturally equal. Hence, the balance characterization of the I^{2}SOP system will be somewhat different from that of the ISOP system.

At steady state, since both the input voltage and the output voltage are constant, by power conservation, we have

$$\begin{cases} V_{d1} I_{\text{in}} D_1 \eta_1 = V_o I_{o1} \\ V_{d2} I_{\text{in}} D_2 \eta_2 = V_o I_{o2} \\ \quad \vdots \\ V_{dN} I_{\text{in}} D_N \eta_N = V_o I_{oN} \end{cases} \tag{22}$$

where $\eta_1, \eta_2, \ldots, \eta_N$ are the conversion efficiencies of the modules, and $D_1, D_2, \ldots, D_N$ are the duty cycles of $Q_{11}, Q_{21}, \ldots, Q_{N1}$, respectively.

In practice, as the topologies of the modules are identical, the mismatches in the power stages are not so large, so the difference among the module efficiencies is negligible, and we assume $\eta_1 = \eta_2 = \cdots = \eta_N = \eta$. When Q_{j2} is ON and Q_{j1} is OFF, the *j*th full-bridge module is bypassed from the system input current, and when Q_{j2} is OFF and Q_{j1} is ON, the system input current flows through the *j*th full-bridge module; hence, $I_{\text{in}} D_j$ and $V_{dj} I_{\text{in}} D_j$ are regarded as the input current and input power of the *j*th full-bridge module, respectively. And, (22) can be rewritten as

$$V_{d1} D_1 : V_{d2} D_2 : \cdots : V_{dN} D_N = I_{o1} : I_{o2} : \cdots : I_{on} \tag{23}$$

where $V_{dj} D_j$ is regarded as the equivalent input voltage of *j*th full-bridge module.

From (23), we can see that if the module output currents are controlled to be equal, the module equivalent input voltages $(V_{dj} D_j)$ will be equal, while the module real input voltages (V_{dj}) are not necessarily equal. One may say that if the module output currents are controlled to be equal and in the meantime keeping all the duty cycles D_j the same, then the module real input voltages will be equal. However, we should know that the duty cycles D_j are used to regulate the module output currents to be equal; hence, the duty cycles D_j are impossible to be equal when the modules are unmatched to a certain extent, especially some key parameters such as the turns ratios of the power transformers in the individual modules are different. In other words, the module output currents and duty cycles D_j are impossible to be equal at the same time. Hence, if the module output currents are controlled to be equal, the module real input voltages (V_{dj}) are not necessarily equal. Similarly, if the module real input voltages (V_{dj}) are controlled to be equal, the module output currents are not necessarily equal. It can be seen that the balance characteristic is different from that of the traditional ISOP system.

In order to validate the balance characteristic analysis, an I^{2}SOP system with three full-bridge modules is simulated, and the specifications of the system are presented in Table I. The turns ratios of the three transformers are purposely made to have a difference of about 8%. In the simulation, the OCS control strategy is changed to the IVS control strategy (the control

strategies are presented in the following section) at instant 1 s. Fig. 10 shows the simulation results of input voltages, output currents, duty cycles of Q_{j1} ($j = 1, 2, 3$), and system output voltage of the three modules. It can be seen that before 1 s, the OCS of the three modules is achieved, while the input voltages and duty cycles of Q_{j1} of three modules are not equal; however, the products of $V_{dj}D_j$ ($j = 1, 2, 3$) are equal. After 1 s, the input voltages of the three modules converge due to the function of the IVS control strategy, while the output currents of the three modules diverge. At about 4 s, the system enters the new steady state, and the input voltages of three modules are equal, while the output currents are not equal.

B. Balance Control Strategies

According to the aforementioned analysis, both the OCS control strategy and IVS control strategy can be used for the I^{2}SOP system. In the viewpoint of power balance or thermal balance of all constituent modules, the OCS control strategy is a better option, while the IVS control strategy is a better option if the voltage stress balance of the active switches is of more concern.

Fig. 11(a) and (b) shows the IVS and OCS control strategies of the I^{2}SOP system, respectively. In Fig. 11(a), the output voltage regulator takes the difference value between the sampled voltage v_o and reference value V_{ref} to a PI controller, and the output v_{o_EA} is used as the basic common duty cycle of all Q_{j1}. The IVS controller samples the module input voltage V_{dj} and compares it with V_{d_ave} to calculate the correcting value $v_{d\_\text{EA}j}$, where V_{d_ave} is the sampled average value and $V_{d\_ave} = (V_{d1} + V_{d2} + \cdots + V_{dN})/N$. The actual duty cycle of Q_{j1} is the summation of v_{o_EA} and $v_{d\_\text{EA}j}$. Compared with the IVS control strategy, in Fig. 11(b), the difference is that the output currents of modules are sampled and used as for the OCS control loop.

IV. Fault Characterization of the I^{2}SOP System

The ISOP power conversion system is usually used in high-voltage applications, such as dc grids. For the dc grids, no matter at what voltage level, protections against dc short-circuit fault still remain a big challenge due to lower impedance in dc systems and fast development of dc fault. It has been proved that the discharging current of the dc bus capacitor plays an important role in the initial stage of short-circuit current [21]. For the traditional ISOP system, the concentrated capacitor formed by the input filter capacitors of modules is directly connected to the dc bus and the concentrated capacitor will collapse and experience discharge, leading to high transient current under dc bus short-circuit fault condition, which causes more difficulty in fault handling, while for the proposed I^{2}SOP system, there is no single concentrated capacitor directly connected to the dc bus. When a dc fault is detected, all the switches should be turned OFF; hence, the input filter capacitors of the modules are disconnected fully from the dc bus and these capacitors will not be discharged, resulting in no additional transient current from the I^{2}SOP system to the fault position and facilitating fault handing. If the fault is cleared promptly in a short time,

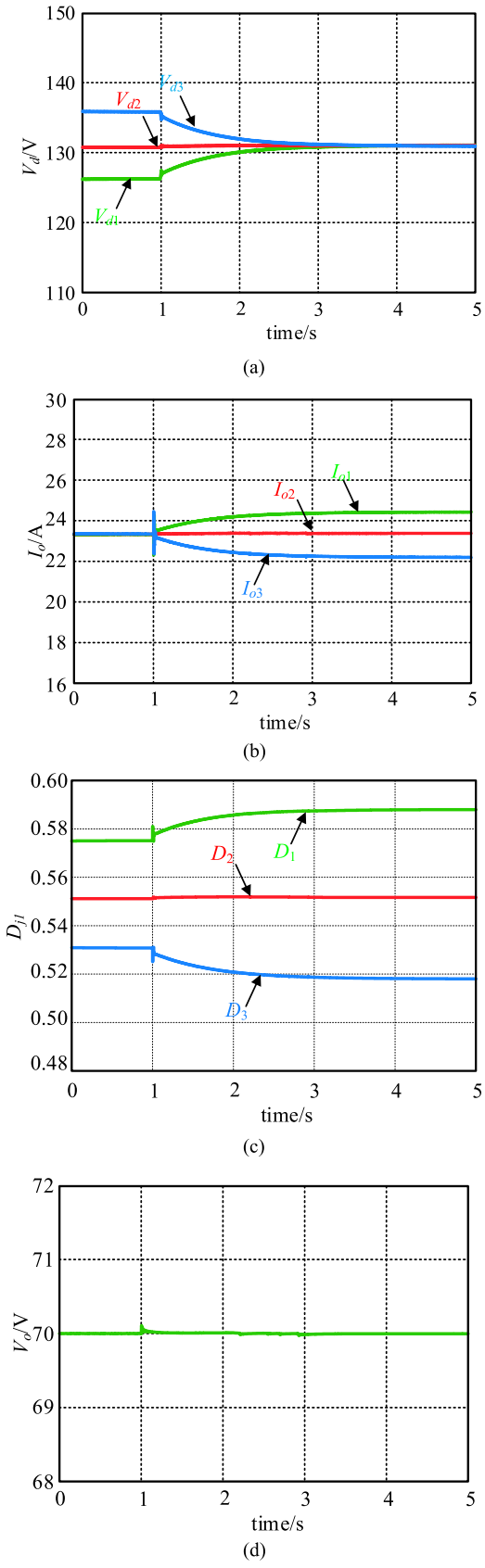

Fig. 10. Simulation results of the OCS control versus IVS control. (a) Input voltages V_{d1}, V_{d2}, and V_{d3}. (b) Output currents I_{o1}, I_{o2}, and I_{o3}. (c) Duty cycles of Q_{j1} D_1, D_2, and D_3. (d) Output voltage V_o.

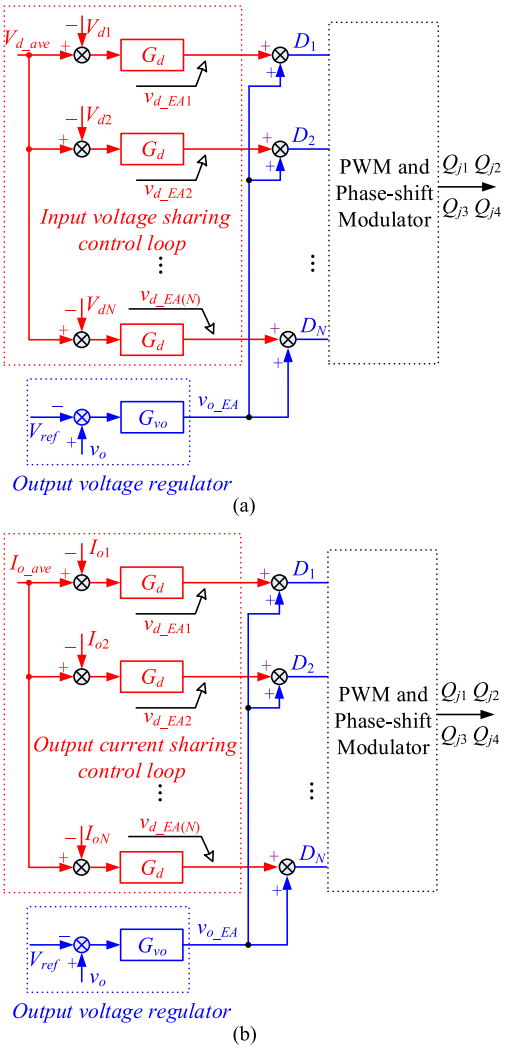

Fig. 11. Control strategies of the I²SOP system. (a) IVS control strategy. (b) OCS control strategy.

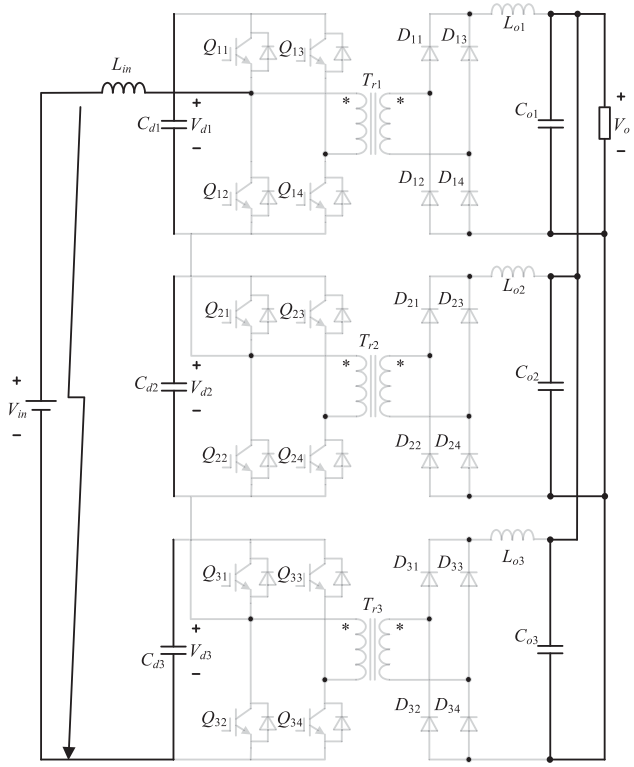

Fig. 12. Equivalent circuit under dc bus short-circuit fault.

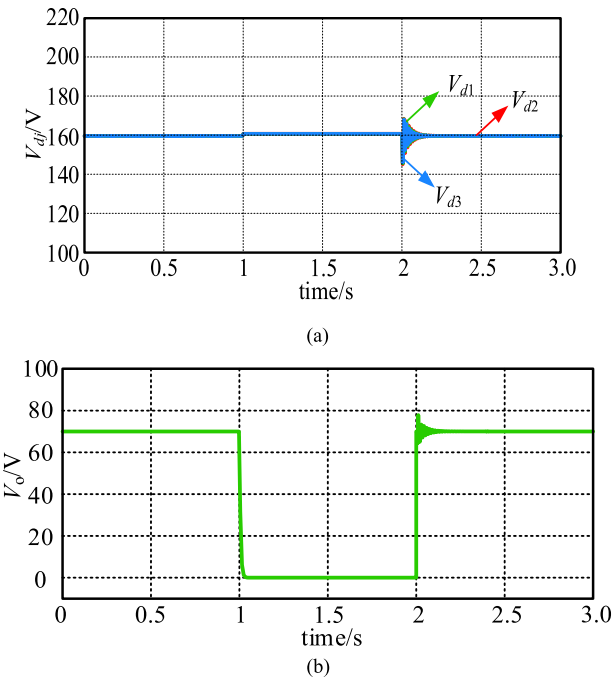

Fig. 13. Simulation waveforms of the I²SOP system responding to a dc bus short-circuit fault. (a) V_{d1}, V_{d2}, and V_{d3}. (b) V_o.

the voltages of the input filter capacitors will remain almost unchanged and the I²SOP system can rapidly recover the normal operation, eliminating the soft startup process of the traditional ISOP system. An example circuit of an I²SOP system with three full-bridge modules to handle the dc fault is shown in Fig. 12. Fig. 13 shows the simulation results of a three-module I²SOP system responding to a dc bus short-circuit fault at 1 s and cleared at 2 s. At 1 s, all the three modules are locked and their input voltages V_{d1}, V_{d2}, and V_{d3} are kept constant, and the system output voltage V_o falls rapidly to zero. At 2 s, the short-circuit fault is cleared and the I²SOP system can rapidly recover the normal operation.

One of the advantages of the ISOP or I²SOP system is the high system reliability, i.e., the systems can still run normally when one or a few constituent modules fail. In [30]–[32], the detailed methods to detect the failures within a single module are presented. In the proposed I²SOP system, when the *j*th module failure is detected, Q_{j1}, Q_{j3}, and Q_{j4} are turned OFF and Q_{j2} is turned ON immediately; then, the *j*th module is switched out from operation, the input capacitor C_{dj} will not discharge, and the system can still run normally. Actually, the switch Q_{j2} may also be damaged in some cases, then an additional bypass contactor *S* is required to be connected in parallel with Q_{j2}, and when a failure occurs in the *j*th module, the bypass contactor is turned ON. Fig. 14 shows an example of an I²SOP system when

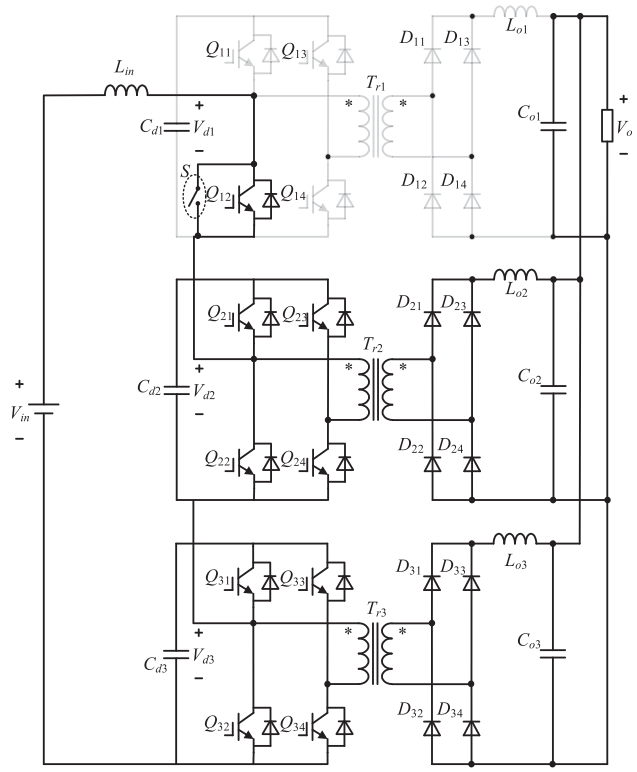

Fig. 14. Equivalent circuit under the first module fault.

the first module fails. Fig. 15 shows the simulation waveforms of the I^{2}SOP system responding to the first module switched out and in. Before 1 s, all three modules are in balance state. At 1 s, assuming a failure occurs in the first module, then the fault control strategy makes the first module switched out through turning OFF Q_{11}, Q_{13}, and Q_{14} and turning ON Q_{12}. It can be seen that the voltage V_{d1} remains constant, and both the input voltages V_{d2} and V_{d3} increase to sustain the system input voltage, and V_{d2} and V_{d3} still remain equal. The system output voltage V_o recovers 70 V after a short time of regulation. The transformer current of the first module reduces to zero and the transformer currents of second and third modules increase accordingly to supply the load. At 3 s, the first module is switched into the system and the I^{2}SOP system returns to the normal operation. From the simulation results, the I^{2}SOP system can operate well when submodule failure occurs and the reliability can be improved.

V. Experimental Results

In order to verify the effectiveness of the proposed I^{2}SOP structure, a 1-kW system with three full-bridge modules was built in the laboratory. The system input voltage ranges from 175 to 350 V, the output voltage is 70 V, the input filter inductance is 1.2 mH, the input capacitors $C_{d1} = C_{d2} = C_{d3} = 470\,\mu$F, the turns ratios of three transformers are 1:0.6, and the switching frequency $f_s = 10$ kHz. For the prototype, the IVS control strategy was used.

Fig. 16 shows the experimental waveforms of the I^{2}SOP system at steady state. It can be seen the three full-bridge modules

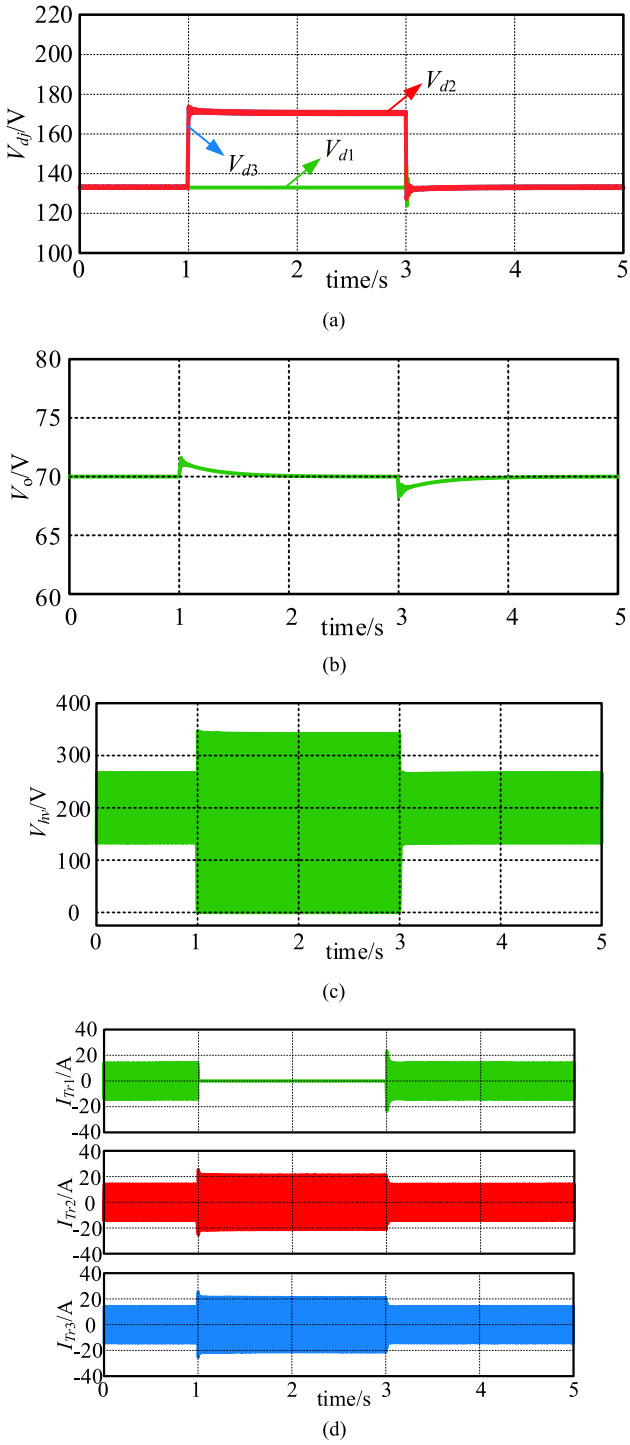

Fig. 15. Simulation waveforms of the I^{2}SOP system responding to the first module switched out and in. (a) V_{d1}, V_{d2}, and V_{d3}. (b) V_o. (c) $V_{\rm hv}$. (d) Transformer currents of the three modules I_{Tr1}, I_{Tr2}, and I_{Tr3}.

are interleaved controlled. It is easy to find that the system reaches a well voltage balance state due to the positive amplitude of V_{AjBj} equals the module input voltage. The ripple frequency of the input current is three times of the switching frequency, leading to much lower input current ripple. The system output voltage stays steadily at 70 V.

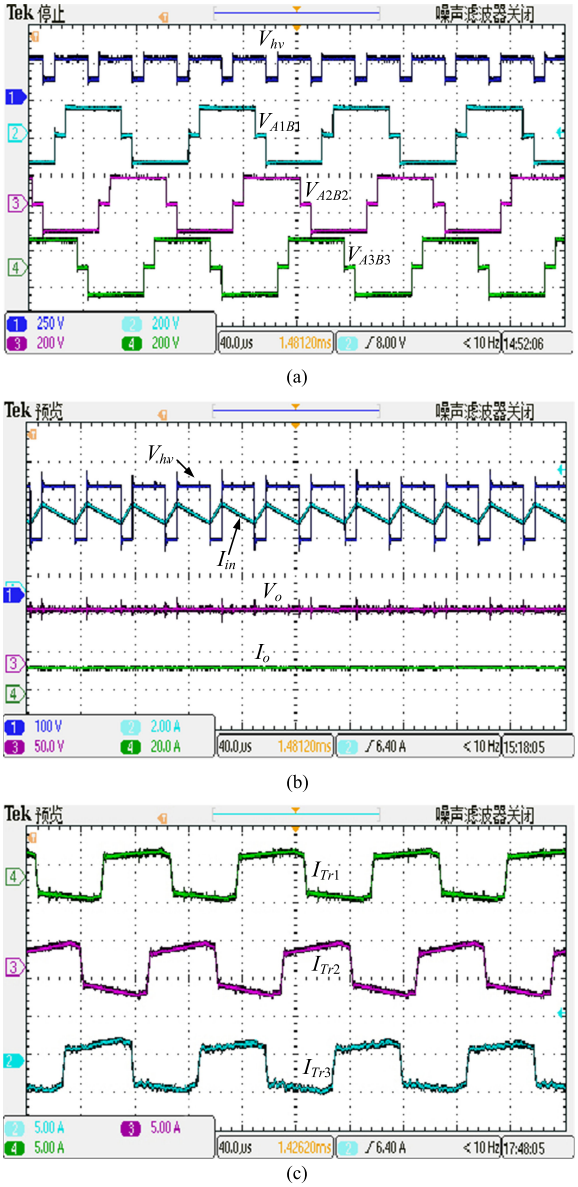

Fig. 16. Experimental waveforms of the I^{2}SOP system at steady state. (a) V_{A1B1}, V_{A2B2}, V_{A3B3}, and $V_{\rm hv}$. (b) $V_{\rm hv}$, $I_{\rm in}$, V_o, and I_o. (c) I_{Tr1}, I_{Tr2}, and I_{Tr3}.

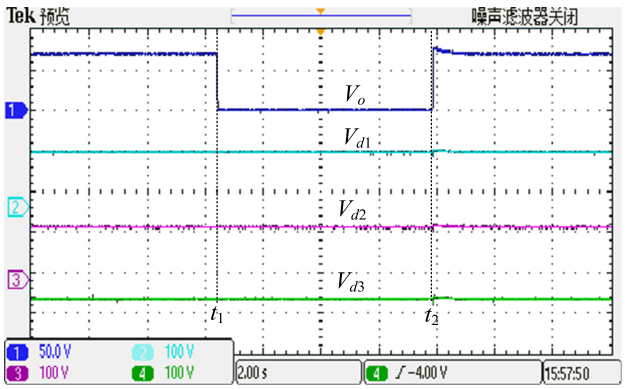

Fig. 17. Experimental waveforms of the I^{2}SOP system when the whole system is disabled and enabled.

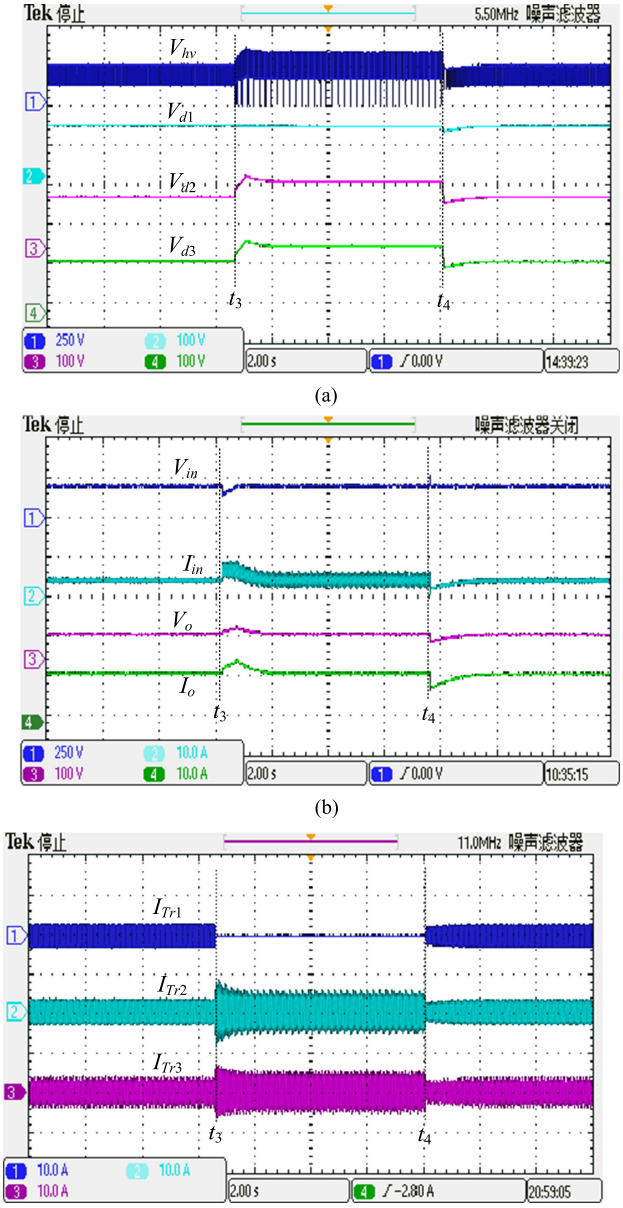

Fig. 18. Experimental waveforms of the I^{2}SOP system when the first module is switched out and in. (a) V_{d1}, V_{d2}, V_{d3}, and $V_{\rm hv}$. (b) $V_{\rm in}$, $I_{\rm in}$, V_o, and I_o. (c) I_{Tr1}, I_{Tr2}, and I_{Tr3}.

Due to the danger and damage caused by the dc bus short-circuit fault to the input voltage source and other equipment in the lab, the real short-circuit fault experiment is not done. However, the I^{2}SOP system responding to a short-circuit fault was simulated by disabling the system, and the system is enabled again when the fault is cleared; the experimental results are shown in Fig. 17. At t_1, the I^{2}SOP system is disabled, the input voltages of three modules remain almost unchanged, and the system output voltage reduces to zero. At t_2, the I^{2}SOP system is enabled again and we can see that there is no soft startup process to charge the input capacitors, and the system output voltage recovers rapidly at 70 V.

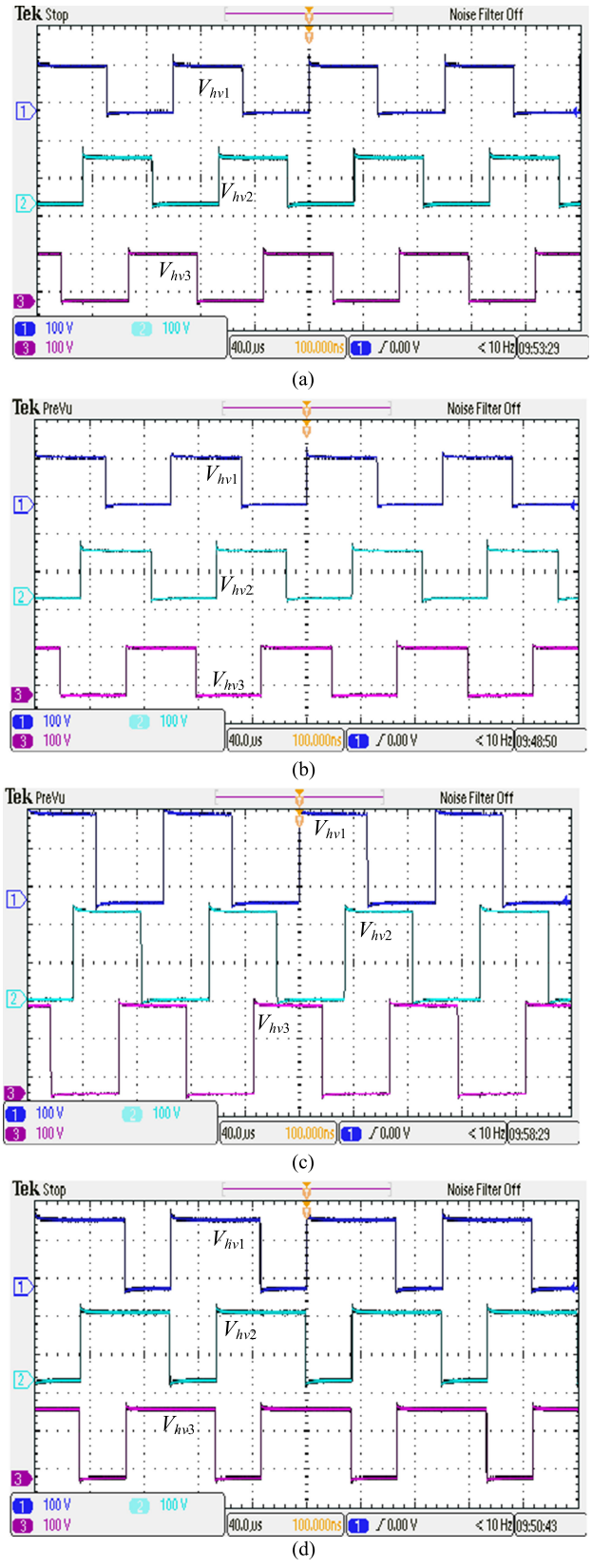

Fig. 19. Voltages across Q_{j2} with the APWM control strategy and the PS control strategy under different input voltages. (a) PS control strategy with $V_{\text{in}} = 190$ V. (b) APWM control strategy with $V_{\text{in}} = 190$ V. (c) PS control strategy with $V_{\text{in}} = 350$ V. (d) APWM control strategy with $V_{\text{in}} = 350$ V.

Fig. 18 shows the experimental waveforms of the I^{2}SOP system when the first module is switched out and in to simulate whether a failure has occurred and repaired, respectively. At t_3, Q_{11}, Q_{13}, and Q_{14} are turned OFF and Q_{12} is turned ON to simulate the failure of the first module. It can be seen that V_{d1} remains constant, both V_{d2} and V_{d3} increase to sustain the system input voltage, and V_{d2} and V_{d3} still remain equal. The transformer current of the first module reduces to zero and the transformer currents of second and third modules increase accordingly to keep the system output voltage constant. At t_4, the first module is switched into the system and the I^{2}SOP system returns to the normal operation.

Both the APWM control strategy and PS control strategy are applied to the I^{2}SOP system to compare their effects on the voltage stress of power switches of full-bridge module. The voltage waveforms across Q_{j2} with the APWM control strategy and the PS control strategy under different input voltages are shown in Fig. 19. Fig. 19(a) and (b) shows the voltage waveforms when $V_{\text{in}} = 190$ V; the duty cycles D_a are both close to 0.5 for the two control strategies when $V_{\text{in}} = 190$ V, and the voltage stresses of switches are almost the same with the two control strategies. Fig. 19(c) and (d) shows the voltage waveforms when $V_{\text{in}} = 350$ V; the duty cycles D_a are both much lower than 0.5 for the two control strategies, and the voltage stresses of switches with the APWM control strategy are 45 V lower than those with the PS control strategy, which agrees well with the theoretical analysis. Hence, with the introduction of the APWM control strategy, the voltage stress of power switch can be effectively reduced.

VI. Conclusion

The ISOP system is very suitable for high input voltage, low output voltage, and high output current applications. This paper proposes a novel I^{2}SOP dc–dc power conversion system with a full-bridge converter as the basic module based on the APWM control strategy. Through the indirect series method, the concentrated capacitor of the traditional ISOP system is eliminated and the input filter capacitors of modules of the I^{2}SOP system will not discharge under a dc bus short-circuit fault. Moreover, the fault module can be easily switched out from the system with the indirect series method. However, compared to [23], the I^{2}SOP system requires less devices at the expense of voltage regulation flexibility and modular voltage control independence. With the introduction of the APWM control strategy, the voltage stress of switch can be decreased compared to that with the traditional PS control strategy. Simulation and experimental results have verified the feasibility of the I^{2}SOP system.

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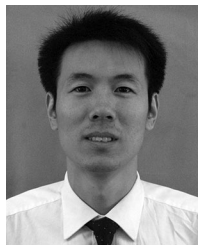

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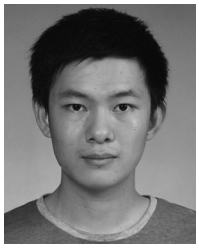

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