Indirect IGBT Over-Current Detection Technique Via Gate Voltage Monitoring and Analysis

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***Abstract*—This paper presents a new insulated gate bipolar transistor (IGBT) over-current detection method based on the analysis of the gate voltage waveform. The IGBT's gate voltage turn-ON transient pattern is analyzed for the detection of IGBT hard switching fault (HSF). The ON-state gate voltage is monitored to detect IGBT fault under load (FUL). The IGBT's turn-OFF Miller plateau voltage is extracted and measured to sense the IGBT collector current in case of an over-load condition. Compared to the commonly used IGBT short-circuit detection methods or collector current sensing methods, this method can provide indirect fast detection of IGBT short circuit and accurate measurement of over-load within one switching period. The feasibility and effectiveness of the proposed approach are validated both by simulation and experimental results. Measurement results show that HSF and FUL can be detected within 0.6 and 0.5 μs, respectively. By comparing the extracted plateau voltage ($V_{\rm PL}$) with a preset reference voltage ($V_{{\rm OC}x}$), the IGBT over-load can be detected with a maximum deviation of $\pm$1.2 A when $I_{\rm C}$ ranges from 3 to 110 A.**

***Index Terms*—Insulated gate bipolar transistor (IGBT), Miller plateau, over-current detection.**

I. Introduction

INSULATED gate bipolar transistor (IGBT) over current can be classified as short-circuit over current or over-load over current [1]. Generally, short-circuit over current is a result of IGBT hard switching fault (HSF) or fault under load (FUL) [2]. Most IGBTs can withstand short circuit for only several microseconds because the fault current can be very large. The IGBT experiencing high electrical and thermal stress under large current would lead to thermal breakdown. Therefore, fast protection methods are needed for IGBT short-circuit over-current conditions. In contrast, IGBT over-load current comes from in-rush current, filter in-rush, and a change in load. In this case,

Manuscript received February 6, 2018; revised May 20, 2018; accepted July 2, 2018. Date of publication July 16, 2018; date of current version February 20, 2019. This work was supported by the National Key Research and Development Program of China under Grant 2016YFB0010700. Recommended for publication by Associate Editor S. S. Ang. *(Corresponding author: Dawei Xu.)*

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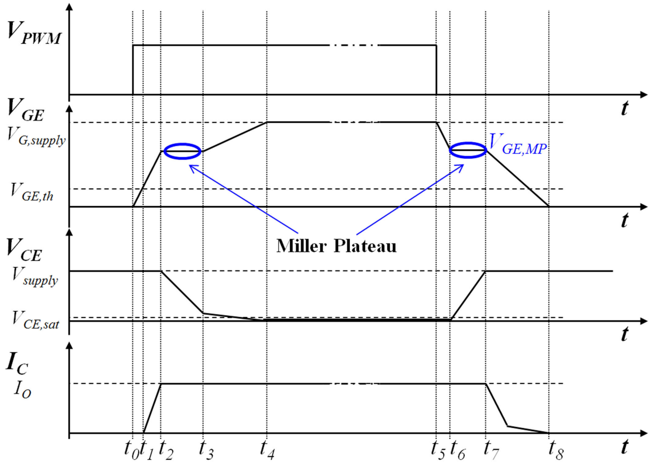


Fig. 1. Switching transient of an IGBT [1].

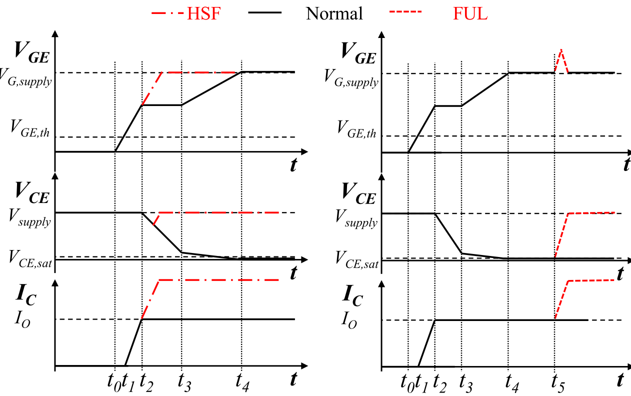


Fig. 2. Comparison of the gate voltage waveforms under different loading conditions.

simulation results of the proposed IGBT over-current detection scheme. Section IV discusses the implementation and measurement results. Finally, conclusions are provided in Section V.

II. Literature Review

A. IGBT Switching Transient

Switching waveform of the IGBT with an inductive load is shown in Fig. 1 [1]. The turn-ON switching waveforms are very similar to MOSFET switching characteristics, turn-OFF switching characteristics are similar as well except for the IGBT's tail current. The following are descriptions of each region, as shown in Fig. 1, and their principle of operation.

1) Turn-On Switching Transient: At time t_0, the gate current starts to charge the parasitic input capacitance C_{ge} and C_{gc} of the IGBT, and V_{GE} rises. There is no change in V_{CE} and I_C during the period $t_0 - t_1$.

At time t_1, as V_{GE} exceeds the IGBT threshold voltage $V_{\mathrm{GE,th}}$, a channel is formed in the *p*-base region below the gate oxide, and collector current I_C begins to conduct. During this time, the IGBT is turned ON, and I_C increases in relation to the increase in V_{GE} and finally reaches the full load current I_O.

At time t_2, the gate current starts to charge the Miller capacitance C_{gc}, and V_{GE} remains constant. This is the Miller plateau voltage $V_{\mathrm{GE,MP}}$. During the period $t_2 - t_3$, I_C also remains constant and is equal to I_O, while V_{CE} begins to fall.

At time t_3, V_{CE} drops to a level where the MOS channel inside the IGBT goes into the triode region and the Miller effect disappears. V_{GE} starts to increase again until it reaches $V_{G,\mathrm{supply}}$ with $R_G\ (C_{\mathrm{ge}} + C_{\mathrm{gc}})$ as the time constant, where R_G is the gate resistance, and C_{gc} is the intrinsic IGBT gate to collector capacitance. During this period, V_{CE} slowly diminishes to the collector-to-emitter ON-state voltage $(V_{\mathrm{CE,sat}})$. By time t_4, V_{GE} reaches the maximum gate supply voltage $V_{G,\mathrm{supply}}$.

2) IGBT On-State: During the period $t_4 - t_5$, the IGBT is in the normal ON-state with full load current I_O, and V_{GE} and V_{CE} maintain at $V_{G,\mathrm{supply}}$ and $V_{\mathrm{CE,sat}}$, respectively.

3) Turn-Off Switching Transient: At time t_5, V_{GE} starts to fall from $V_{G,\mathrm{supply}}$ to $V_{\mathrm{GE,MP}}$ with a time constant of $R_G\ (C_{\mathrm{ge}}+C_{\mathrm{gc}})$. During the period $t_5 - t_6$, there is no change in the values for V_{CE} and I_C. By time t_6, the reduction in V_{GE} causes the internal MOS channel to enter saturation mode, bringing back the Miller effect. V_{CE} starts to increase toward V_{supply}, while V_{GE} and I_C maintain their values at $V_{\mathrm{GE,MP}}$ and I_O, respectively. The relationship between V_{GE} and I_C has been investigated and reported extensively in [11].

By time t_7, V_{CE} almost reaches V_{supply}, I_C starts to decrease rapidly from I_O to zero with a current tail caused by the recombination of the minority carriers inside the IGBT. This tail current will eventually dissipate by time t_8, completing the turn-OFF process.

B. Gate Voltage Pattern at FUL and HSF

The IGBT's gate voltage waveforms under normal, HSF, and FUL conditions are discussed in this section. As shown in Fig. 2, gate voltage remains constant during the period t_2 to t_3 due to the Miller effect as explained in the previous section. Under normal operation, V_{GE} has two rising edges during the turn-ON transient. However, only one rising edge appears on V_{GE} under the HSF condition because there is no Miller plateau during the fault turn-ON process. In contrast, FUL is a situation where the short circuit takes place when the device is in the ON-state. I_C and V_{CE} will rise quickly, and at this time, a gate current begins to flow in C_{gc}. Due to the gate resistance, V_{GE} could rise above $V_{G,\mathrm{supply}}$. Fig. 2 shows the differences in the V_{GE}, V_{CE}, and I_C waveforms between normal and HSF or FUL conditions [12].

C. Relationship Between $V_{GE,MP}$ and I_C

The gate voltage at which the Miller plateau occurs corresponds to the collector current (I_C) waveform, and there is a distinct relationship between $V_{\mathrm{GE,MP}}$ and I_C during IGBT turn-ON and turn-OFF. This correlation can be identified with the analysis below by means of an equivalent circuit for the IGBT, as shown in Fig. 3. The equivalent circuit consist a *pnp* transistor with a MOS transistor controlling its base current [13]. The relationship between the MOS drain current (I_D) and I_C can

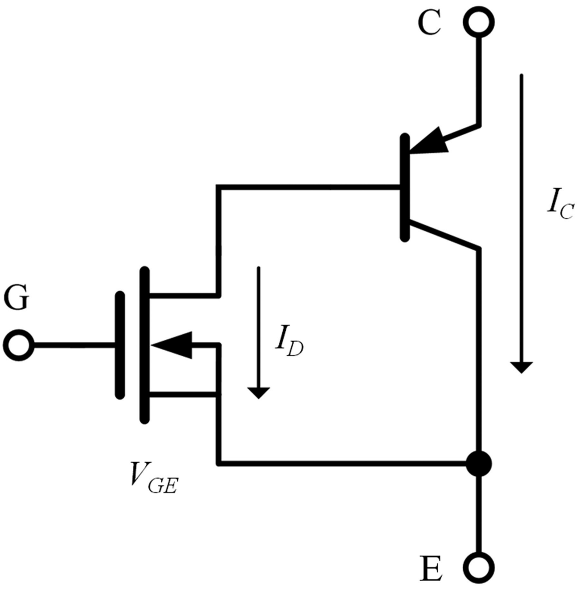


Fig. 3. Equivalent circuit for the IGBT.

be depicted as

$$I_C = \frac{I_D}{1 - \alpha_{\mathrm{PNP}}} \tag{1}$$

where α_{PNP} is defined as $\alpha_{\mathrm{PNP}} = \frac{\beta}{\beta+1}$, and β is the common emitter current gain of a bipolar junction transistor. The MOS transistor is in the saturation region during turn-ON or turn-OFF; therefore,

$$I_D = \frac{1}{2}\mu_n C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GE,MP}} - V_{\mathrm{TH}})^2. \tag{2}$$

Re-arranging this equation for $V_{\mathrm{GE,MP}}$ yields the approximate value of the Miller plateau as a function of the drain current, as follows [14]:

$$V_{\mathrm{GE,MP}} = V_{\mathrm{TH}} + \sqrt{\frac{2I_D}{\mu_n C_{\mathrm{ox}} W/L}}. \tag{3}$$

Substituting (1) into (3), the relationship between $V_{\mathrm{GE,MP}}$ and I_C becomes

$$V_{\mathrm{GE,MP}} = V_{\mathrm{TH}} + \sqrt{\frac{2I_C\,(1 - \alpha_{\mathrm{pnp}})}{\mu_n C_{\mathrm{ox}} W/L}}. \tag{4}$$

III. Proposed Fault Detection Circuit

A. Block Diagram

Fig. 4 shows the proposed block diagram for the detection of both short-circuit over-current and over-load conditions. The gate voltage pattern analyzer analyzes the turn-ON transient and the ON-state of the IGBT gate voltage to judge whether the IGBT is under HSF or FUL conditions, respectively. Given the fact that $V_{\mathrm{GE,MP}}$ monotonically increases with I_C, the over-load detector extracts the IGBT Miller plateau voltage $V_{\mathrm{GE,MP}}$ during the turn-OFF transient. The IGBT over-load condition can be detected by comparing the extracted $V_{\mathrm{GE,MP}}$ with a predefined threshold voltage $V_{\mathrm{OC}x}$.

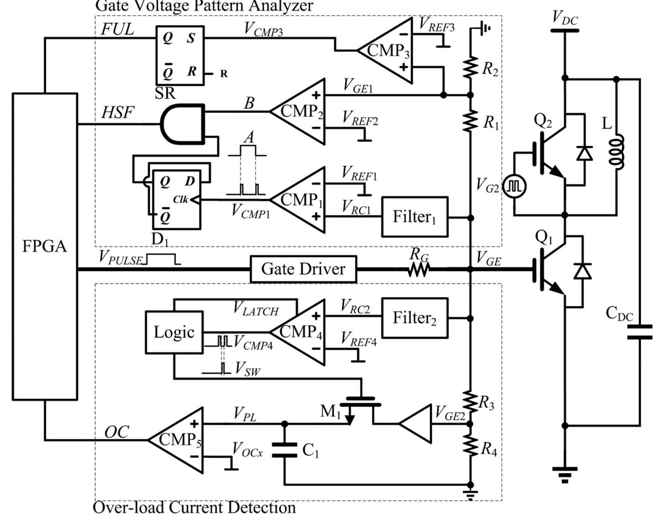


Fig. 4. Schematic of the proposed over-current detection circuit.

B. Gate Voltage Pattern Analyzer for the HSF

As shown in Fig. 4, the gate voltage pattern analyzer for the HSF is composed of Filter$_1$, two comparators CMP_{1-2}, a T flip-flop, and an AND gate. Filter$_1$ detects the rising edges on V_{GE1} during the IGBT turn-ON transient and outputs corresponding V_{RC1} pulses (as shown in Fig. 5). The number of V_{CMP1} pulses is determined by the rising edges on V_{GE1}, when Q_1 is normally turned ON, the number of pulses is 2, otherwise it is 1. Signal *A* is generated from the T flip-flop, which is triggered by the rising edges of V_{CMP1}. If Q_1 suffers an HSF, only one V_{CMP1} pulse will appear, then signal *A* will be triggered high and keep the state until Q_1 is forced to shutdown, as the green area shown in Fig. 5(b). Under this condition, I_C would increase so dramatically that Q_1 could breakdown within a few microseconds. V_{REF2} is defined as follows to set a reference voltage to shutdown Q_1 in time

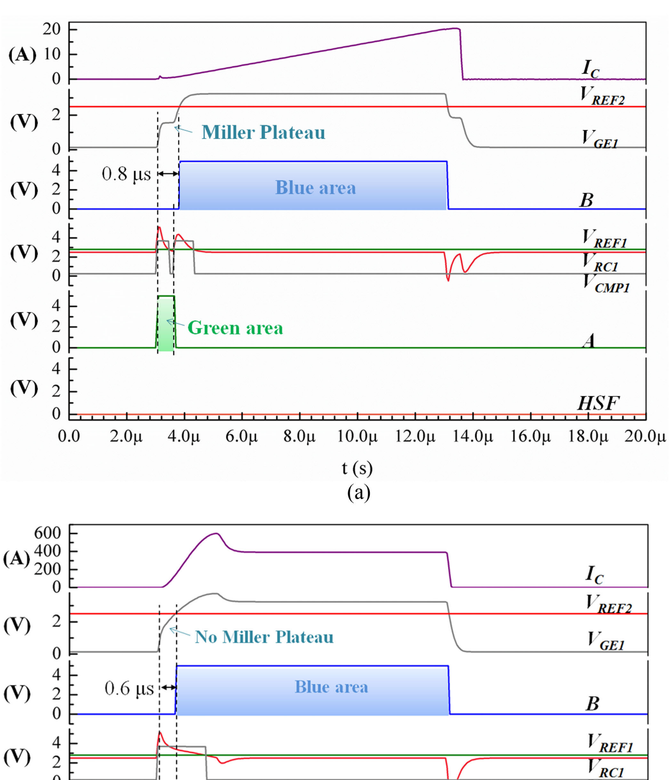
$$V_{\mathrm{REF2}} = \frac{R_2}{R_1 + R_2} V_{\mathrm{GE,MP,HSF}} \tag{5}$$

where $V_{\mathrm{GE,MP,HSF}}$ is the Miller plateau voltage corresponding to the HSF threshold current $I_{C,\mathrm{HSF}}$. Signal *B* will turn to high as V_{GE1} rising above V_{REF2} and the output of the AND gate will be set to high, which indicates an HSF.

On the contrary, if Q_1 turns ON normally, as shown in Fig. 5(a), signal *A* will be triggered high at the first rising edge of V_{CMP1} pulse and turn to low at the second one. As $V_{\mathrm{GE,MP,HSF}}$ is higher than $V_{\mathrm{GE,MP}}$, which is the Miller plateau voltage under the normally turn-ON condition, signal *A* always goes low before signal *B* goes high. Therefore, signal *HSF* will maintain at a low level, indicating the IGBT is turning ON normally.

C. Gate Voltage Pattern Analyzer for FUL

As shown in Fig. 4, the gate voltage pattern analyzer for FUL is composed of CMP_3 and an SR latch. During the FUL



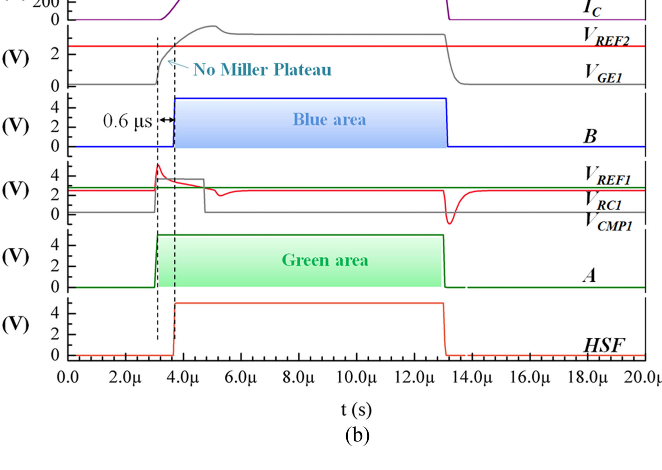


Fig. 5. Simulated waveform of the gate voltage pattern analyzer for the HSF. (a) IGBT normally turn-ON condition. (b) IGBT HSF turn-ON condition (V_{dc}=250 V, $V_{G,\mathrm{supply}} = 13$ V, $R_G = 50\ \Omega$, $R_1/R_2 = 3/1$, $L_{SC} = 0.5\ \mu$H).

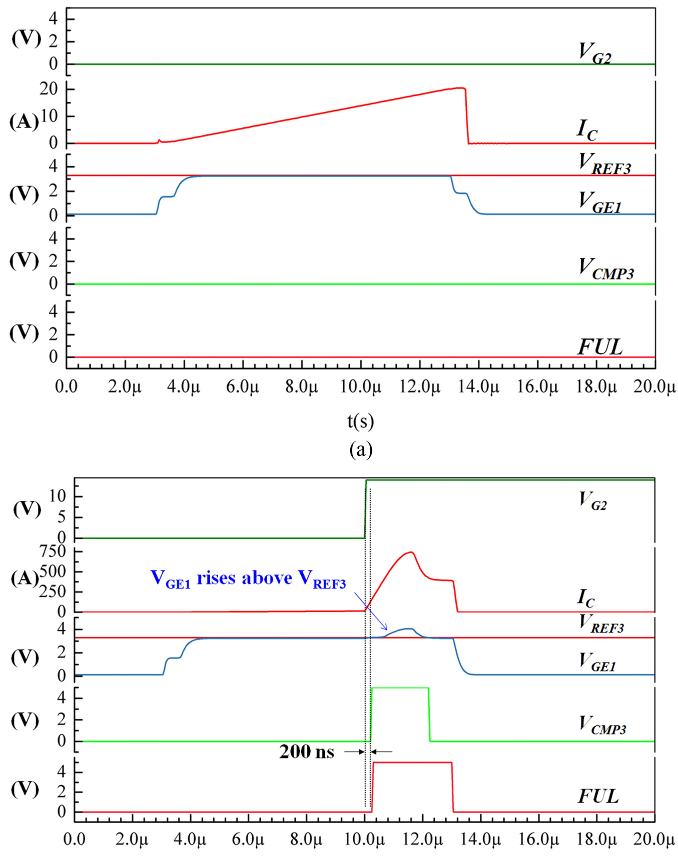


Fig. 6. Simulated waveform of the gate voltage pattern analyzer for FUL. (a) IGBT normal ON-state. (b) IGBT under the FUL condition ($V_{dc} = 250$ V, $V_{G,\mathrm{supply}} = 13$ V, $R_G = 50\ \Omega$, $R_1/R_2 = 3/1$, $L_{SC} = 0.5\ \mu$H).

detection, CMP_3 will compare V_{GE1} with a predefined voltage V_{REF3}

$$\frac{R_2}{R_1+R_2}V_{G,\mathrm{supply}} < V_{\mathrm{REF3}} < \frac{R_2}{R_1+R_2} \times \left(V_{G,\mathrm{supply}} + R_G C_{\mathrm{gc}}\frac{dV_{\mathrm{CG}}}{d_t}\right). \quad (6)$$

Simulated waveforms of the gate voltage pattern analyzer are shown in Fig. 6. Under the normal condition, signal *FUL* keeps low because V_{GE1} is always lower than V_{REF3}. However, when FUL occurs, signal V_{CMP3} will turn to high immediately after V_{GE1} has rose above V_{REF3}. So the SR latch will be triggered high and maintain the state until Q_1 is forced shutdown.

D. Over-Load Detector Operation

The IGBT over-load detector mainly consists of three parts, including a Miller plateau recognition circuit, a Miller plateau voltage extraction circuit, and an over-current comparator. The schematic is shown in Fig. 4. Given the fact that there is always an initial ringing on IGBT turn-ON Miller plateau [15]–[17], we focus on the turn-OFF Miller plateau for the detection.

1) Miller Plateau Recognition Circuits: The Miller plateau recognition circuit contains a passive band-pass filter (Filter_2), a latch comparator CMP_4, and a Logic module. The main function of the circuit is to sense the onset of the plateau when the IGBT is turning OFF and to provide a control signal V_{SW}, which is high only during the plateau region. Fig. 7 shows the simulated waveforms for the circuit. Filter_2 is used to sense the gate node of the IGBT, where the time derivative of the gate voltage plateau region equals zero. The output of Filter_2, V_{RC2}, is then shaped to digital pulses by a latch comparator CMP_4. The digitized V_{CMP4} is then sent to the Logic module, generating V_{SW} and V_{LATCH}. A high level for V_{SW} corresponds to the presence of a Miller plateau region.

The latch function of comparator CMP_4 can improve the stability of the sensing circuit. When a large current spike flows through the power loop, V_{GE} will oscillate intensely. Consequently, CMP_4 will generate an erroneous logic output. In this case, V_{LATCH} is enabled at the second negative edge of V_{CMP4} to block the subsequence undesired pulses. Therefore, the latch comparator will generate the correct output logic output for the proper operation of the entire sensing circuit.

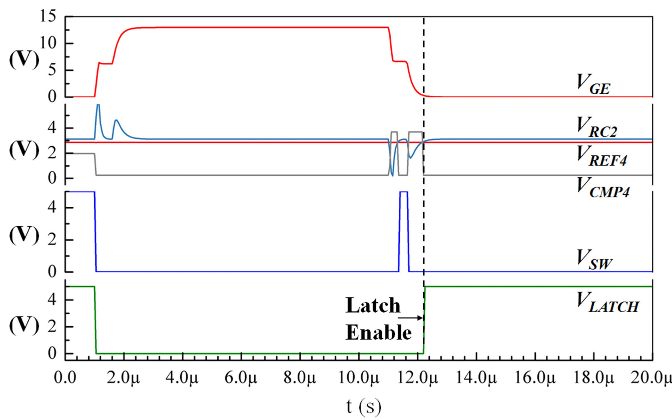


Fig. 7. Simulated waveform of the turn-OFF plateau sensing (V_{dc} = 250 V, V_{PULSE}: period = 1 ms, pulsewidth = 10 μs, R_3/R_4 = 3/1, R_G = 50 Ω).

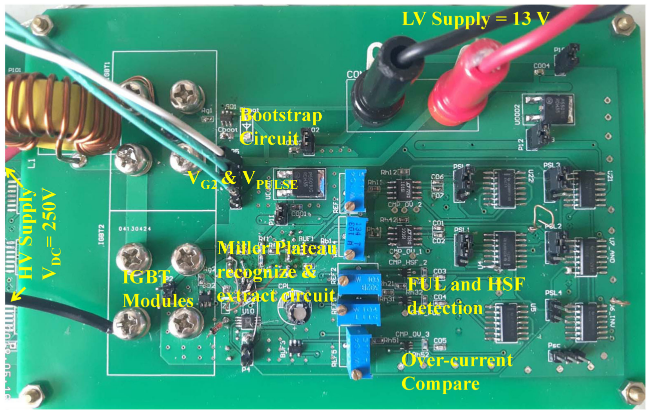


Fig. 9. Test bench setup for the proposed circuit.

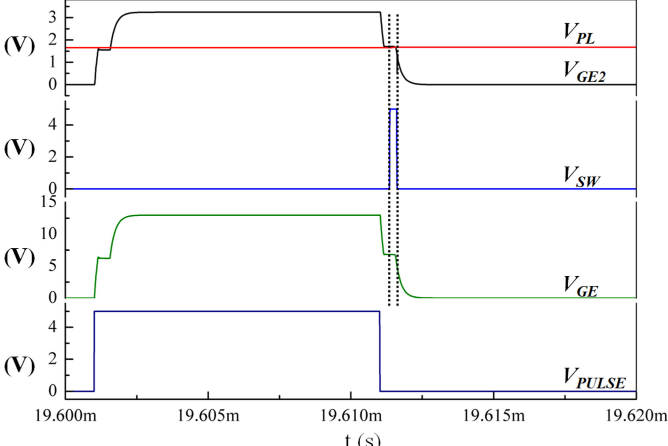
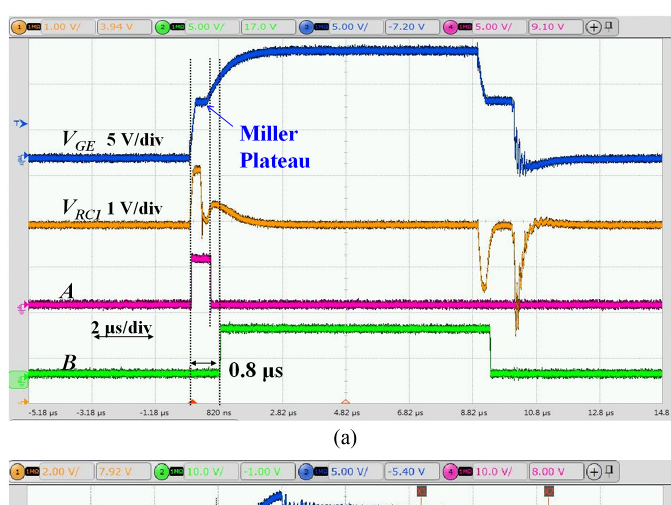


Fig. 8. Simulated waveform of the Miller plateau voltage extraction circuit (V_{dc} = 250 V, V_{PULSE}: period = 1 ms, pulsewidth = 10 μs, R_3/R_4 = 3/1, R_G = 50 Ω).



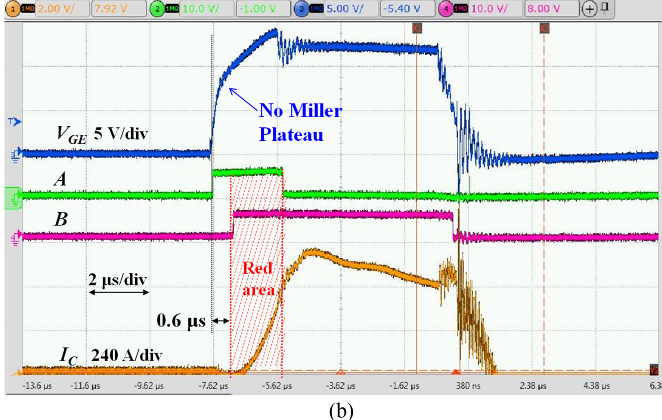


Fig. 10. Measured waveform of the gate voltage pattern analyzer for the HSF. (a) Under normal turn-ON. (b) Under the HSF condition (V_{dc} = 250 V, $V_{G,supply}$ = 13 V, R_G = 50 Ω, R_1/R_2 = 3/1, L_{SC} = 0.5 μH).

2) Miller Plateau Voltage Extraction Circuits: The Miller plateau voltage extraction is realized by a sample and hold circuit (M_1 and C_1), as shown in Fig. 4. The gate voltage V_{GE} will be scaled and amplified by a wide bandwidth amplifier. In the plateau region, by controlling a switch (M_1) with V_{SW}, a large capacitor (C_1) will be charged to the plateau voltage, and the voltage will be held after M_1 is turned OFF until the next plateau appears. Finally, the extracted plateau voltage V_{PL} equals to

$$V_{PL} = V_{GE,MP} \times \frac{R_4}{R_3 + R_4}. \tag{7}$$

Simulated waveform of V_{PL} and Miller plateau voltage extraction circuit are shown in Fig. 8.

3) IGBT Over-Load Detection: Ideally, every Miller plateau has the same level for a given I_C. The output of the sample and hold circuit V_{PL} should be a dc value. Therefore, it is relatively simple to determine the monotonically increasing relationship between I_C and V_{PL}. By comparing V_{PL} with V_{OCx}, which is the reference voltage of CMP_5, we can determine whether the IGBT exceeds the limited current or not. V_{OCx} is a preset according to the I_C–V_{PL} curve.

IV. Experimental Results

A. Test Bench

The measurement system implemented on a printed circuit board (PCB) to verify the over-current detection circuit is shown in Fig. 9. The IGBT power modules IXXN110N65C4H1 un-

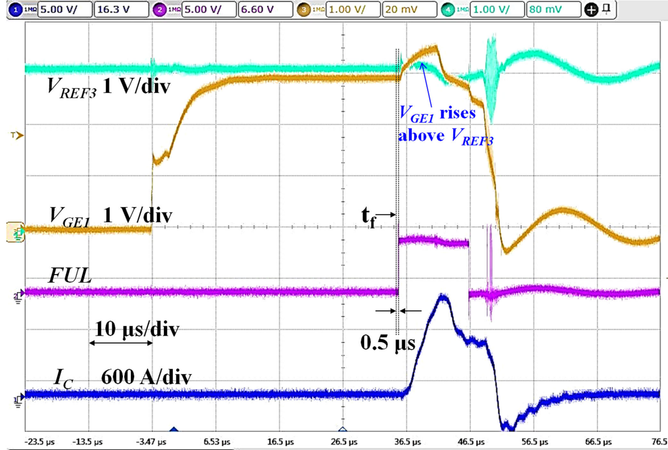


Fig. 11. Measured hard switching fault turn-ON process of the FUL detection module ($V_{\rm dc}$ = 250 V, $V_{G,\rm supply}$ = 13 V, R_1/R_2 = 3/1, $L_{\rm SC}$ = 0.5 μH).

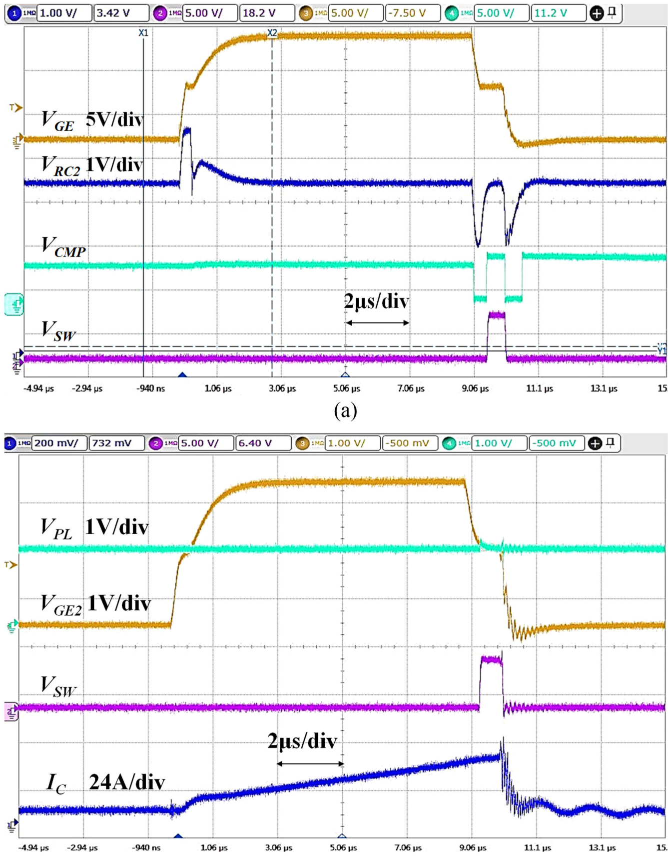


Fig. 12. (a) Measured waveform for the Miller plateau recognition circuit. (b) Measured waveform of the Miller plateau voltage extraction circuit ($V_{\rm dc}$ = 250 V, $V_{G,\rm supply}$ = 13 V, R_G = 50 Ω, R_3/R_4 = 3/1, $L_{\rm SC}$ = 0.5 μH).

der test is also assembled on the PCB together with an inductive load L. By defining the reference voltages of the gate comparators, the short-circuit detection area can be adjusted in order to guarantee no misdetection during normal operation. In the test setup, the reference value for CMP$_2$ is chosen to be $V_{\rm REF2}$ = 2.5 V, which corresponds to a turn-ON Miller

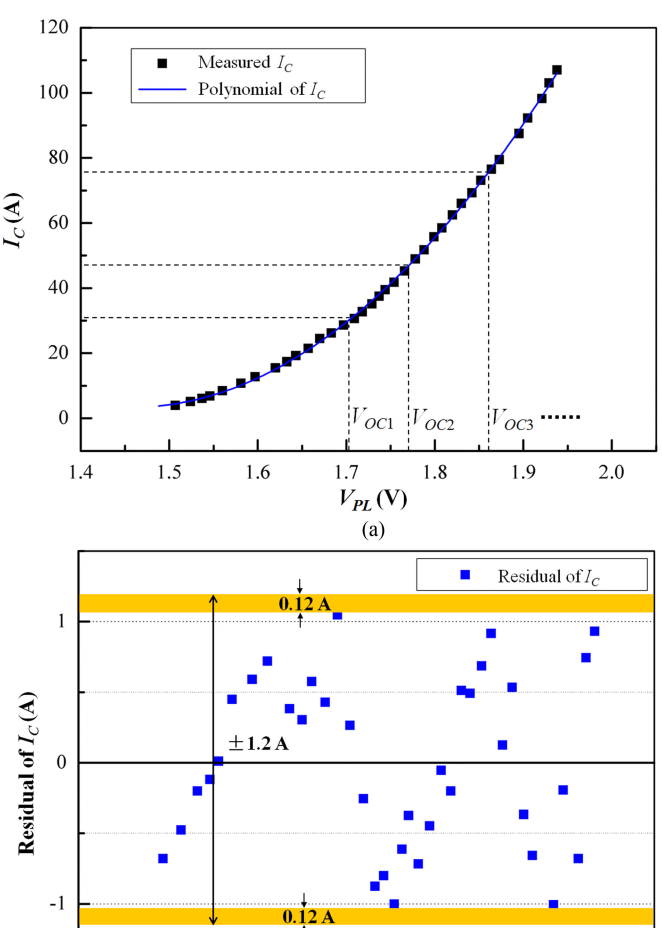


Fig. 13. (a) IGBT collector current I_C–$V_{\rm PL}$ curve at room temperature. (b) Error analysis of IGBT over-load detection ($V_{\rm dc}$ = 250 V, $V_{\rm PULSE}$: period = 1 ms, 4 μs < pulsewidth < 50 μs, R_3/R_4 = 3/1, R_G = 50 Ω).

plateau voltage of $V_{\rm GE,MP}$ = 10 V when the collector current $I_C \approx$ 110 A. The reference value for CMP$_3$ is chosen to be $V_{\rm REF3}$ = 3.3 V.

B. Hard Switching Fault Detection

Fig. 10(a) presents the measured waveform of an HSF detection module for a normal IGBT turn-ON process. The shapes of both signals A and B is coincident with the simulation. No high state overlap between A and B indicates that Q_1 is turning ON normally. In comparison, Fig. 10(b) shows the waveforms of the HSF. Under this condition, there is no load except for the small stray inductance ($L_{\rm SC}$ = 0.5 μH), I_C can reach up to 720 A, and no Miller plateau exists at the IGBT gate node. The red highlighted area of signals A and B indicates that the IGBT suffered an HSF, which is detected within 0.6 μs.

C. Fault Under Load Detection

Fig. 11 shows the waveform of FUL detection with a total stray inductance of about $L_{\rm SC}$ = 0.5 μH. FUL occurs at t_f

when Q_2 is turned ON. IGBT collector current surges rapidly to more than 900 A and the gate voltage rises above $V_{\rm REF3}$. FUL is detected in 0.5 μs according to the measured result.

D. IGBT Over-Load Detection

Fig. 12 shows the measured waveforms of the IGBT turn-OFF Miller plateau recognition circuit and the Miller plateau voltage extraction circuit. The turn-OFF plateau position is marked with $V_{\rm SW}$ and the plateau voltage is extracted and held with $V_{\rm PL}$. In Fig. 13, the extracted plateau voltage $V_{\rm PL}$ is plotted against I_C. When I_C changes from 3 to 110 A, $V_{\rm PL}$ varies from 1.485 to 1.945 V. Due to the one-to-one correlation between I_C and $V_{\rm PL}$, specific reference voltages $V_{{\rm OC}x}$ $(x = 1, 2, 3\ldots)$ of the over-current comparator can be acquired according to the I_C–$V_{\rm PL}$ curve. The over-current detection test is implemented by comparing $V_{\rm PL}$ with the reference voltage $V_{{\rm OC}x}$ in different current levels. When $V_{\rm PL}$ is higher than $V_{{\rm OC}x}$, the comparator will send an error signal back to the controller. Considering the fact that $V_{{\rm OC}x}$ is acquired from the I_C–$V_{\rm PL}$ curve, regression analysis is performed on $V_{\rm PL}$ and I_C in order to evaluate the accuracy of the technique. Moreover, the detection error, which is provided by input offset voltage $V_{\rm OS}$ of the over-current comparator, is also analyzed. When less than 1 mV, $V_{\rm OS}$ contributes to a 0.12 A detection error. Finally, the total maximum IGBT over-current detection error is ±1.2 A.

Given that the IGBT Miller plateau is affected by temperature and device aging, more I_C–$V_{\rm PL}$ curves should be obtained in future work. Moreover, a temperature sensing system should also be adopted, so that the field programmable gate array controller could calibrate $V_{{\rm OC}x}$ to make the detection more accurate.

V. Conclusion

In this work, a unique method is introduced to monitor the IGBT collector over current indirectly from the gate node. The proposed technique leverages the Miller effect to allow the IGBT short-circuit and over-load conditions to be detected simply on the low-voltage gate drive circuit. A gate voltage pattern analyzer is presented to detect HSF and FUL short circuit. In order to obtain the Miller plateau voltage, which occurs during IGBT turn-OFF, an automatic IGBT Miller plateau voltage extraction system constructed with discrete components is designed and tested. IGBT over load can be identified by comparing the Miller plateau voltage to a preset threshold voltage. Measurement result shows that HSF and FUL can be detected within 0.6 and 0.5 μs, respectively. IGBT over load can be predicted within ±1.2 A maximum deviation when I_C ranges from 3 to 110 A. Future work should be focused on the over-current detection at different temperatures.

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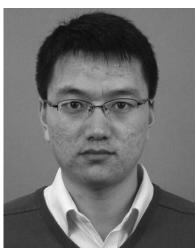

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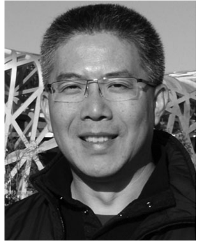

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