Enhanced Hybrid Modular Multilevel Converter With Improved Reliability and Performance Characteristics

Ramin Razani, Mohammad Hasan Ravanji, and Mostafa Parniani, *Senior Member, IEEE*

***Abstract*—This paper proposes an enhanced hybrid modular multilevel converter (MMC), which utilizes a combination of half-bridge submodules (HBSM) and at least one full-bridge submodule (FBSM). In the proposed structure, FBSMs work with half of the HBSMs nominal voltage in each arm. Due to the presence of FBSMs, HBSMs switching frequency drops significantly, which reduces the converter power loss compared to half-bridge based MMCs. Furthermore, because of redundant FBSMs, ($2N + 1$)-modulation can be employed to generate the output voltage without increasing the circulating current, thus, the converter performance is improved notably. Besides, with the redundant FBSMs, the converter can continue its operation even if a fault occurs in one of HBSM switches. All the control procedure is accomplished using model predictive control strategy and performance of the proposed converter is verified by several simulation and experimental studies. The obtained results confirm the feasibility of the proposed scheme in reducing the converter loss, improving its performance and fault-tolerant operation.**

***Index Terms*—Fault-tolerant operation, hybrid modular multilevel converter (HMMC), model predictive control (MPC), power loss, 2 $N + 1$ modulation.**

I. Introduction

MODULAR multilevel converters (MMC) are the-state-of-the-art converters with salient features, such as lower harmonic contents, higher efficiency, and more modularity and scalability [1]. MMCs are also suitable for medium/high power applications, such as high-voltage direct current (HVdc) transmission [2], motor drives [3], photovoltaic generation [4], and static synchronous compensator (STATCOM) [5].

A typical MMC is made up of series connection of submodules (SMs). The half-bridge submodule (HBSM) has been the most common topology due to its lower fixed cost and power losses [1]. However, several different configurations have been proposed in the literature. In [6] and [7], some of the HBSMs are replaced with full-bridge submodules (FBSMs) and in [8] various hybrid modular multilevel converters (HMMC) are studied.

Manuscript received December 12, 2017; revised March 11, 2018 and May 13, 2018; accepted June 29, 2018. Date of publication July 5, 2018; date of current version February 20, 2019. Recommended for publication by Associate Editor J. Clare. *(Corresponding author: Mostafa Parniani.)*

The authors are with the Department of Electrical Engineering, Sharif University of Technology, Tehran 11365-8639, Iran (e-mail:

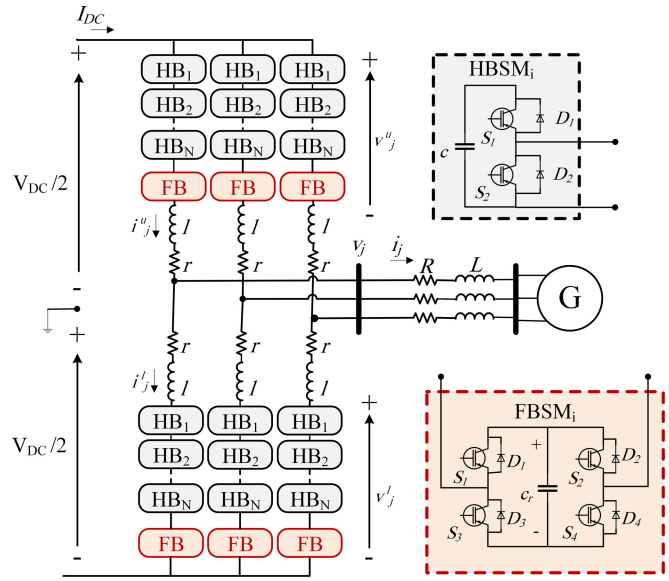

Fig. 1. Circuit configuration of the proposed EHMMC.

verter power loss is reduced. In addition, the proposed EHMMC can tolerate the faults that may occur in the HBSMs and continues its operation.

The rest of the paper is organized as follows. In Section II, the operation principle of the proposed EHMMC is expressed. Section III presents the control scheme of EHMMC in both steady state and fault-tolerant operation. In Section IV, the simulation results are reported and then compared with a typical HB-MMC results, and at the end experimental results are illustrated. Eventually, this paper is concluded in Section V.

II. EHMMC Operation

Fig. 1 shows the proposed three-phase EHMMC topology. Each phase-leg consists of two arms where each of them comprises *N* HBSMs, at least one FBSM, an inductance *l* and a resistance *r,* which models inductor parasitic resistance. Capacitance of the HBSMs capacitor is shown by *c*. The total voltage produced by the upper and lower arms in phase-j are illustrated by $v^u{}_j$ and $v^l{}_j$, and the currents in the upper and lower arms are shown by $i^u{}_j$ and $i^l{}_j$, respectively. The output voltage v_j and differential voltage $v_{\text{diff},j}$ can be expressed as (1) and (2), and the output current i_j and differential current $i_{\text{diff},j}$ are defined as (3) and (4), respectively [14]

$$v_j = \frac{v^l{}_j - v^u{}_j}{2} \tag{1}$$

$$v_{\text{diff},j} = \frac{V_{\text{DC}} - v^l{}_j - v^u{}_j}{2} \tag{2}$$

$$i_j = i^u{}_j - i^l{}_j \tag{3}$$

$$i_{\text{diff},j} = \frac{i^u{}_j + i^l{}_j}{2} = \frac{I_{\text{DC}}}{3} + i_{\text{circ},j} \tag{4}$$

where I_{DC} is the dc-link current and $i_{\text{circ},j}$ represents the circulating current, which contains mostly even harmonics [15].

TABLE I
Arms Voltage in Different Situations

	m=2k	*m=2k+1*
p=2z	$v^u{}_j = \frac{k-z}{N}V_{DC}$ $v^l{}_j = V_{DC} - \frac{k+z}{N}V_{DC}$	$v^u{}_j = \frac{k-z}{N}V_{DC} + \frac{V_{DC}}{2N}$ $v^l{}_j = V_{DC} - \frac{k+z}{N}V_{DC} - \frac{V_{DC}}{2N}$
p=2z+1	$v^u{}_j = \frac{k-z}{N}V_{DC} - \frac{V_{DC}}{2N}$ $v^l{}_j = V_{DC} - \frac{k+z}{N}V_{DC} - \frac{V_{DC}}{2N}$	$v^u{}_j = \frac{k-z}{N}V_{DC}$ $v^l{}_j = V_{DC} - \frac{k+z}{N}V_{DC} - \frac{V_{DC}}{N}$

TABLE II
Example of Arms Voltage in Specific Situations

m=2, p=1	*m=3, p=0*
$v^u{}_j = \frac{1}{N}V_{DC} - \frac{V_{DC}}{2N}$ $v^l{}_j = \frac{N-1}{N}V_{DC} - \frac{V_{DC}}{2N}$	$v^u{}_j = \frac{1}{N}V_{DC} + \frac{V_{DC}}{2N}$ $v^l{}_j = \frac{N-1}{N}V_{DC} - \frac{V_{DC}}{2N}$

A. Circulating Current

The circulating current does not affect the output current, however flows through the arms and increases the capacitors voltage variation and power losses [16]. Accordingly, it is necessary to limit the circulating current. In the proposed EHMMC, a $(2N+1)$-modulation is employed to improve the internal and external performance measures of the converter. However, as mentioned in [17]–[19], when the $(2N+1)$-modulation is used, the circulating current will be increased, which in turn leads to a higher arm current amplitude. This is due to the absence of specific voltage levels in $v_{\text{diff},j}$. To prove this assertion, at first it is assumed that the extra FBSM does not exist and *N* is an even number. The feasible output and differential voltages in an MMC with $(2N+1)$-modulation are expressed as follows:

$$v_j = \frac{(N-m).V_{\text{DC}}}{2N} \tag{5}$$

$$v_{\text{diff},j} = \frac{V_{\text{DC}}}{2N}p. \tag{6}$$

Here *m* is an integer variable from 0 to $2N$ and *p* is an integer variable between $-N$ and *N*. Using (1), (2), (5), and (6), the upper and lower arm voltages can be calculated as follows:

$$v^u{}_j = \frac{m}{2N}V_{\text{DC}} - \frac{p}{2N}V_{\text{DC}} \tag{7}$$

$$v^l{}_j = V_{\text{DC}} - \frac{m}{2N}V_{\text{DC}} - \frac{p}{2N}V_{\text{DC}}. \tag{8}$$

In Table I, the upper and lower arm voltages are calculated based on (8) and (9) for even and odd values of *m* and *p*. It can be seen that when *m* is odd and *p* is even, the arms voltage has a $V_{\text{DC}}/2N$ term, which cannot be produced by the HBSMs because the nominal capacitor voltage of each HBSM is V_{DC}/N. The same situation occurs when *m* is even and *p* is odd. In Table II, for example, arms voltages are calculated for specific values of *p* and *m* which cannot be generated by HBSMs. This issue will reduce controllability of the circulating current, since

TABLE III
FEASIBLE COMBINATION OF HBSM AND FBSM

$m=2k+1$, $v_{diff,j}=0$		
	v^u_j	v^l_j
1	$\frac{k}{N}V_{DC}+\frac{V_{DC}}{2N}$	$\frac{N-k}{N}V_{DC}-\frac{V_{DC}}{2N}$
2	$\frac{k}{N}V_{DC}+\frac{V_{DC}}{2N}$	$\frac{N-k-1}{N}V_{DC}+\frac{V_{DC}}{2N}$
3	$\frac{k+1}{N}V_{DC}-\frac{V_{DC}}{2N}$	$\frac{N-k}{N}V_{DC}-\frac{V_{DC}}{2N}$
4	$\frac{k+1}{N}V_{DC}-\frac{V_{DC}}{2N}$	$\frac{N-k-1}{N}V_{DC}+\frac{V_{DC}}{2N}$

TABLE IV
FEASIBLE COMBINATION OF HBSM AND FBSM IN SPECIFIC OUTPUT VOLTAGE LEVELS

		$v_j=+V_{DC}/2$	$v_j=-V_{DC}/2$
$v_{diff,j}=-\frac{V_{DC}}{2N}$	1	$v^u{}_j=\frac{V_{DC}}{2N}$ $v^l{}_j=V_{DC}+\frac{V_{DC}}{2N}$	$v^u{}_j=V_{DC}+\frac{V_{DC}}{2N}$ $v^l{}_j=\frac{V_{DC}}{2N}$
	2	$v^u{}_j=\frac{V_{DC}}{N}-\frac{V_{DC}}{2N}$ $v^l{}_j=V_{DC}+\frac{V_{DC}}{2N}$	$v^u{}_j=V_{DC}+\frac{V_{DC}}{2N}$ $v^l{}_j=\frac{V_{DC}}{N}-\frac{V_{DC}}{2N}$
$v_{diff,j}=\frac{V_{DC}}{2N}$	1	$v^u{}_j=-\frac{V_{DC}}{2N}$ $v^l{}_j=V_{DC}-\frac{V_{DC}}{2N}$	$v^u{}_j=V_{DC}-\frac{V_{DC}}{2N}$ $v^l{}_j=-\frac{V_{DC}}{2N}$
	2	$v^u{}_j=-\frac{V_{DC}}{2N}$ $v^l{}_j=\frac{N-1}{N}V_{DC}-\frac{V_{DC}}{2N}$	$v^u{}_j=\frac{N-1}{N}V_{DC}+\frac{V_{DC}}{2N}$ $v^l{}_j=-\frac{V_{DC}}{2N}$

the circulating current is controlled mostly by changing $v_{\text{diff},j}$ [14], [20], and [21].

B. Differential Voltage Generation by the Extra SMs

Based on the previous discussion, it is impossible to generate specific values of $v_{\text{diff},j}$ in some situations. However, by using an extra SM with half of the HBSMs voltage rating in each arm, all the required $v_{\text{diff},j}$ in any situation can be generated. For instance, in Table III all possible combinations of ordinary HBSMs and one extra SM are expressed for an odd *m* and zero $v_{\text{diff},j}$. As can be seen, there are four combinations of the activated HBSM number and the extra SM voltage polarity for every odd value of *m*. In each combination, the upper and lower arm voltages have a $V_{\text{DC}}/2N$ term generated by the extra SM. As shown in Table IV, when the output voltage is $\pm V_{\text{DC}}/2$ there are two states to generate the required arm voltages, while in the usual MMCs it is infeasible to control the circulating current by changing $v_{\text{diff},j}$ when the output voltage is $\pm V_{\text{DC}}/2$. This is due to the fact that in the usual MMCs the only possible value for $v_{\text{diff},j}$ in this case is zero.

C. Characterizing the Extra SM

In order for the extra SM to have two output voltage polarities, at least one FBSM is required to be concatenated to the HBSMs in each arm. The extra FBSM is depicted in Fig. 1, in which c_r is the SM capacitance. The FBSM nominal capacitor voltage is $V_{\text{DC}}/2N$ and is controlled using a capacitor voltage balancing scheme. The FBSM output voltage polarity is determined based on the arm current direction in order to charge or discharge the capacitor. Based on the output voltage polarity, the FBSM in arm-*t* of phase-*j* has three switching states $S^t{}_{r,j} \in \{-1, 0, 1\}$. The operation principle of the extra FBSM is shown in Table V. In this table, $v^t{}_{r,j}$ illustrates the FBSM capacitor voltage in arm-*t* of phase-*j*.

TABLE V
OPERATION PRINCIPLE OF THE FBSM

Switching state	S_1	S_2	S_3	S_4	Output voltage
$S^t{}_{r,j}=1$	1	0	0	1	$v^t{}_{r,j}$
$S^t{}_{r,j}=0$	1	1	0	0	0
	0	0	1	1	
$S^t{}_{r,j}=-1$	0	1	1	0	$-v^t{}_{r,j}$

III. CONTROL OF THE EHMMC

A. Steady-State Control

Proper operation of MMCs require the output current control, circulating current elimination, and SMs capacitor voltage balancing. Furthermore, it is necessary to control the capacitor voltage of the extra FBSM in the proposed EHMMC. All these requirements are addressed with a model predictive control (MPC) system [14], [20], [21]. In the MPC strategy, system variables are first predicted using discrete-time equations of the system and the optimal switching state is selected by minimizing a cost function, as mentioned in the following sections. In the control procedures, it is assumed that a three-phase RL load is connected to the converter terminal.

1) Output Current Control: In order to regulate the converter output power, the output current must track the predefined reference value. The discrete-time equation of the output current is expressed as [20]

$$i_j(t+T_s)=\frac{T_s}{L+0.5l}.v_j(t+T_s)+\left(1-\frac{2T_sR}{2L\ +\ l}\right).i_j(t) \tag{9}$$

where $i_j(t+T_s)$ and $v_j(t+T_s)$ show the output current and output voltage in the next switching period and $i_j(t)$ represents the present value of the output current. T_s represents the sampling period. If the output current reference in the next switching state is represented by $i_{j,\text{ref}}(t+T_s)$, the associated cost function can be designed as

$$C_{i_j}=\left|i_{j,\text{ref}}(t+T_s)-i_j(t+T_s)\right|. \tag{10}$$

To determine the output voltage level, $i_j(t+T_s)$ is calculated for every possible value of $v_j(t+T_s)$, which is expressed in (5) and the one that minimizes C_{i_j} is selected as the optimal output voltage level in the next switching period.

2) Circulating Current Elimination: The discrete-time equation of the differential current can be defined as follows [20]:

$$i_{\text{diff},j}(t+T_s)=\frac{T_s}{l}.v_{\text{diff},j}(t+T_s)+i_{\text{diff},j}(t) \tag{11}$$

in which $i_{\text{diff},j}(t+T_s)$ and $v_{\text{diff},j}(t+T_s)$ represent the differential current and the differential voltage in the next sampling period and $i_{\text{diff},j}(t)$ shows the differential current instantaneous value calculated from (4). By setting the reference value of $i_{\text{circ},j}(t)$ to zero, the differential current reference $I_{\text{diff,ref}}$ can be calculated as follows:

$$I_{\text{DC}} = \frac{P}{V_{\text{DC}}}, I_{\text{diff,ref}} = \frac{I_{\text{DC}}}{3} \tag{12}$$

where *P* illustrates the active power transmitted to the load. To control the circulating current, a cost function is designed as (13) and the optimal value of the $v_{\text{diff},j}(t+T_s)$ which minimizes the $C_{i_{\text{diff},j}}$ is determined

$$C_{i_{\text{diff},j}} = \left|I_{\text{diff,ref}}(t+T_s) - i_{\text{diff},j}(t+T_s)\right|. \tag{13}$$

3) FBSM Capacitor Voltage Balancing: By determination of the $v_j(t+T_s)$ and $v_{\text{diff},j}(t+T_s)$, the required upper and lower arm voltages can be calculated as expressed in the following:

$$v^u{}_j(t+T_s) = \frac{V_{\text{DC}} - 2v_j(t+T_s) - 2v_{\text{diff},j}(t+T_s)}{2} \tag{14}$$

$$v^l{}_j(t+T_s) = \frac{V_{\text{DC}} + 2v_j(t+T_s) - 2v_{\text{diff},j}(t+T_s)}{2}. \tag{15}$$

As mentioned earlier, in some situations it is impossible to generate the required arms voltages by the HBSMs. To overcome this problem, in this paper, FBSMs are employed as the extra SM, which make it possible to generate the required arms voltages in any situation. In the proposed EHMMC control scheme, the extra FBSMs are only used when the required arms voltages cannot be generated by the HBSMs. In the meantime, it is necessary to control the FBSM capacitor voltage, which is accomplished by determination of the FBSM switching state. Based on the FBSM output voltage polarity, the FBSM capacitor can be charged or discharged with respect to the arm current. Using this feature, the FBSM capacitor voltage can be kept balanced. When the FBSM is needed to be activated, the appropriate polarity is determined using a two-objective cost function as expressed in (16). The proposed cost function is evaluated for the two possible polarities and eventually the one with less value for $C_{v^t{}_{r,j}}$ will be selected

$$C_{v^t{}_{r,j}} = \left|v^t{}_{r,j}(t) \pm i^t{}_j(t+T_s).\frac{T_s}{c_r} - \frac{V_{\text{DC}}}{2N}\right| + w_F.\left|S^t{}_{r,j}(t) - S^t{}_{r,j}(t+T_s)\right|. \tag{16}$$

In this equation, $v^t{}_{r,j}(t)$ shows the measured value of the FBSM capacitor voltage in arm-*t* of phase-*j* and $i^t{}_j(t+T_s)$ represents the arm current in the next switching period. The current and the next state of FBSM is presented by $S^t_{r,j}(t)$ and $S^t{}_{r,j}(t+T_s)$, respectively, and w_F is the weighting factor. The first term is obtained by discretization of the capacitor voltage-current equation, and calculates the capacitor voltage deviation from the nominal voltage for the next switching period. In this term, when $C_{v^t{}_{r,j}}$ is calculated for the FBSM with positive polarity, the plus sign must be used and when $C_{v^t{}_{r,j}}$ is calculated for the FBSM with negative polarity, the minus sign must be used.

The second term in (16) includes the FBSM transition state and its target is to reduce the FBSM switching frequency. Finally, by determination of the FBSM output voltage polarity, one of the possible combinations of the activated HBSM number and the FBSM voltage polarity will be selected.

4) HBSMs Capacitor Voltage Balancing: In order for the proposed EHMMC to operate stably, it is necessary to keep the HBSMs capacitor voltage balanced. The upper and lower arms voltages to be generated by the HBSMs can be calculated as follows:

$$v^t{}_{h,j}(t+T_s) = v_{tj}(t+T_s) - v^t{}_{r,j}(t+T_s).\text{sign}(S^t{}_{r,j}(t+T_s)) \tag{17}$$

where $v^t{}_{h,j}(t+T_s)$ and $v_{tj}(t+T_s)$ are the total voltage that is generated by the HBSMs and the required voltage in the arm-*t* respectively. The number of on-state HBSMs in the next switching period n^t_j can be obtained as follows:

$$n^t{}_j(t+T_s) = \left[\frac{v^t{}_{h,j}(t+T_s)}{\frac{V_{\text{DC}}}{N}}\right]. \tag{18}$$

To select the on-state SMs in the next switching period, the cost function (19), which is proposed in [21], is evaluated for all of the SMs capacitors in each arm, and finally $n^t{}_j$ lowest values are selected as the on-state SMs

$$C_{v^t{}_{n,j}} = \frac{i^t{}_j(t+T_s)}{c}.T_s\left(v^t{}_{i,j}(t) + i^t{}_j(t+T_s).\frac{T_s}{c} - \frac{V_{\text{DC}}}{N}\right) + w_H.\left|S^t{}_{i,j}(t) - S^t{}_{i,j}(t+T_s)\right|. \tag{19}$$

In the above equation, $v^t{}_{i,j}(t)$ represents the measured voltage of the *i*th HBSM capacitor in arm-*t* of phase-*j,* and $S^t{}_{i,j}(t+T_s)$ and $S^t{}_{i,j}(t)$ are the next and present SM states.

B. Reducing States Transitions

By using $(2N+1)$-modulation, the number of output voltage levels is doubled, which results in significant improvement in the performance quality of the converter. However, to increase the converter efficiency, unnecessary changes of the output and differential voltages need to be prevented. For this purpose, one term is added to the associated cost functions introduced in (10) and (13). This term penalizes the cost function whenever the next values of the output and differential voltages change in comparison to their current values. Since the variables in the cost functions have different dimensions [22], the cost functions are normalized and presented as follows:

$$C^m{}_{i_j} = \left|i_{j,\text{ref}}(t+T_s) - i_j(t+T_s)\right|.\left(\frac{1}{I_m}\right) + w_{v_o}.\left|v_j(t+T_s) - v_j(t)\right|.\left(\frac{1}{V_{\text{DC}}}\right) \tag{20}$$

$$C^m{}_{i_{\text{diff},j}} = \left|I_{\text{diff,ref}}(t+T_s) - i_{\text{diff},j}(t+T_s)\right|.\left(\frac{3}{I_{\text{DC}}}\right) + w_{v_{\text{diff}}}.\left|v_{\text{diff},j}(t+T_s) - v_{\text{diff},j}(t)\right|.\left(\frac{1}{V_{\text{DC}}}\right) \tag{21}$$

where I_m is the nominal output current and w_{v_o} and $w_{v_{\text{diff}}}$ are the weighting factors. By increasing these weighting factors, the

TABLE VI
FEASIBLE STATES IN FAULT-TOLERANT OPERATION

v_j	v^u_j	v^l_j
$+V_{DC}/2$	$-\frac{V_{DC}}{2N}$	$\frac{N-1}{N}V_{DC}+\frac{V_{DC}}{2N}$
$-V_{DC}/2$	$\frac{N-1}{N}V_{DC}+\frac{V_{DC}}{2N}$	$-\frac{V_{DC}}{2N}$

cost functions will be more penalized if v_j and $v_{\text{diff},j}$ differ from their current states. Consequently, unnecessary changes in the output and differential voltages are prevented and the switching frequency and power losses are reduced, which is favorable. On the other hand, increasing w_{v_o} and $w_{v_{\text{diff}}}$ will increase the total harmonic distortion (THD) of the output voltage and the circulating current, and degrade the converter performance quality. To distinguish between these cases, the approach uses cost functions (10) and (13) is called EHMMC-I and the one uses (20) and (21) in the normal operation is called EHMMC-II hereafter.

C. Fault-Tolerant Operation

One of the major advantages of the proposed EHMMC over the usual HB-MMCs and the other HMCs, is its fault-tolerant operation. When a fault occurs in one of the HBSM switches, for specific values of the output and differential voltage, the states that require the faulty arm voltage to be V_{DC} cannot be generated. In the regular MMCs, then, the output voltage of $\pm V_{\text{DC}}$ will be infeasible. In contrast, with the proposed EHMMC the maximum total voltage generated by the faulty arm is reduced to $v^t_j = (2N-1)\cdot V_{\text{DC}}/2N$. In spite of this voltage reduction, there are feasible states that can generate output voltage of $\pm V_{\text{DC}}/2$. Even in the worst case that simultaneous faults occur in one HBSM in each of the two arms of one phase and the required output voltage is $\pm V_{\text{DC}}/2$, there is one feasible combination of HBSM and the FBSM (see Table VI).

In case of fault occurrence, however, it is necessary to control the average HBSMs capacitor voltage of each arm. Instantaneous input power related to the HBSMs in arm-*t* of phase-*j* is shown by ${p^t}_{h,j}$ and is calculated as follows:

$$ {p^t}_{h,j} = \frac{d{w^t}_{h,j}}{dt} = {v^t}_{h,j}.i_{tj} \tag{22}$$

where $w^t_{h,j}$ is the HBSMs instantaneous energy, which can be approximated as follows:

$$ {w^t}_{h,j} \approx \frac{N}{2}.c.\left({v^t}_{\text{avg},j}\right)^2. \tag{23}$$

In (23), ${v^t}_{\text{avg},j}$ is the average HBSMs capacitor voltage. By discretization of (22) and using (23), this voltage is calculated as follows:

$$ {v^t}_{\text{avg},j}(t+T_s) = \left(\frac{{w^t}_j(t) + T_s.{v^t}_{h,j}(t+T_s).{i^t}_j(t+T_s)}{\frac{1}{2}c.N}\right)^{\frac{1}{2}}. \tag{24}$$

In order to control the average HBSMs capacitor voltages, two terms containing errors of the arms average voltage are added to the cost function (21) as follows:

$$\begin{aligned} {C^n}_{i_j} &= |I_{\text{diff,ref}}(t+T_s) - i_{\text{diff},j}(t+T_s)|\,.\left(\frac{3}{I_{\text{DC}}}\right) \\ &+ w_{v_{\text{diff}}}.\,|v_{\text{diff},j}(t+T_s) - v_{\text{diff},j}(t)|\,.\left(\frac{1}{V_{\text{DC}}}\right) \\ &+ w_v.\left|{v^u}_{\text{avg},j}(t+T_s) - \frac{V_{\text{DC}}}{N}\right|.\left(\frac{N}{V_{\text{DC}}}\right) \\ &+ w_v.\left|{v^l}_{\text{avg},j}(t+T_s) - \frac{V_{\text{DC}}}{N}\right|.\left(\frac{N}{V_{\text{DC}}}\right) \end{aligned} \tag{25}$$

where w_v is the weighting factor used to adjust the effect of the associated terms.

The overall control procedure of the proposed EHMMC in normal operation is illustrated in Fig. 2. The optimal values of the output and differential voltages are selected by minimizing the cost functions (20) and (25), subsequently. The total arms voltages are calculated and if it is necessary to use the FBSM, the optimal switching state of the FBSM is selected by minimizing (15). Eventually, the number of on-state HBSMs in the next switching period is obtained and using (17) and (18), and by optimizing (19) the on-state HBSMs are determined.

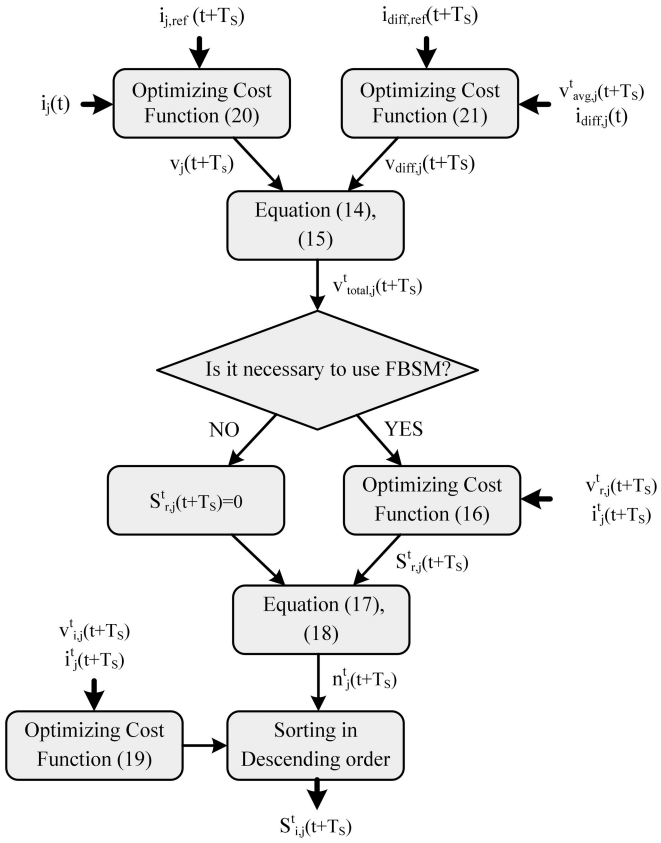

Fig. 2. Flowchart of the proposed EHMMC control procedure.

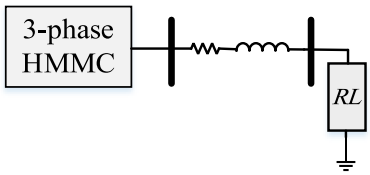

Fig. 3. Simulated system in the case studies.

TABLE VII
SIMULATION SYSTEM PARAMETERS

Parameter	Symbol	Value
Rated Power	S	2.7 MVA
AC System Frequency	F_S	60 Hz
Load Inductance	L	0.01 H
Load Resistance	R	20 Ω
DC Bus Voltage	V_{DC}	12 kV
Arm Inductance	l	0.01 H
HBSM Capacitance	c	0.001 F
HBSM Capacitor Voltage	V_{HBSM}	3 kV
FBSM Capacitance	c_r	0.003F
FBSM Capacitor Voltage	V_{FBSM}	1.5kV
Number of HBSMs per Arm	N	4
Sampling and Control Period	T_S	100 µs

TABLE VIII
WEIGHTING FACTORS

Weighting factor	Symbol	Value
output voltage	w_{v_o}	0.2
differential voltage	$w_{v_{diff}}$	0.7
average upper arm voltage	w_{v_u}	0.5
average lower arm voltage	w_{v_l}	0.5
FBSM transision state	w_F	8
HBSM transision state	w_H	200

IV. PERFORMANCE EVALUATION OF THE PROPOSED EHHMC

A. Simulation Results

To evaluate the proposed EHMMC performance, a three-phase EHMMC connected to a three-phase *RL* load is simulated (see Fig. 3). The main system parameters and the weighting factors are listed in Tables VII and VIII, respectively. Before investigation the characteristics of the proposed scheme as compared to the existing MMCs, transient response and fault tolerant operation of the proposed EHMMC will be examined in the following situations. For this purpose, two case studies are considered. The first case verifies the transient-state operation and second one evaluates the fault-tolerant operation of the proposed EHMMC. All simulation results here belong to the EHMMC-II, since there are no meaningful differences between the EHMMC-I and EHMMC-II results, as discussed later.

1) Case I: In Fig. 4, initially the converter operates as a standard MMC with disabled FBSMs and $2N + 1$ modulation [21]. Then, at $t = 0.2$ s, the FBSMs are enabled and the converter operates as the proposed EHMMC. The output current reference amplitude is 300 A until $t = 0.3$, and it is changed to 150 A at $t = 0.3$. Fig. 4(a) demonstrates three-phase output

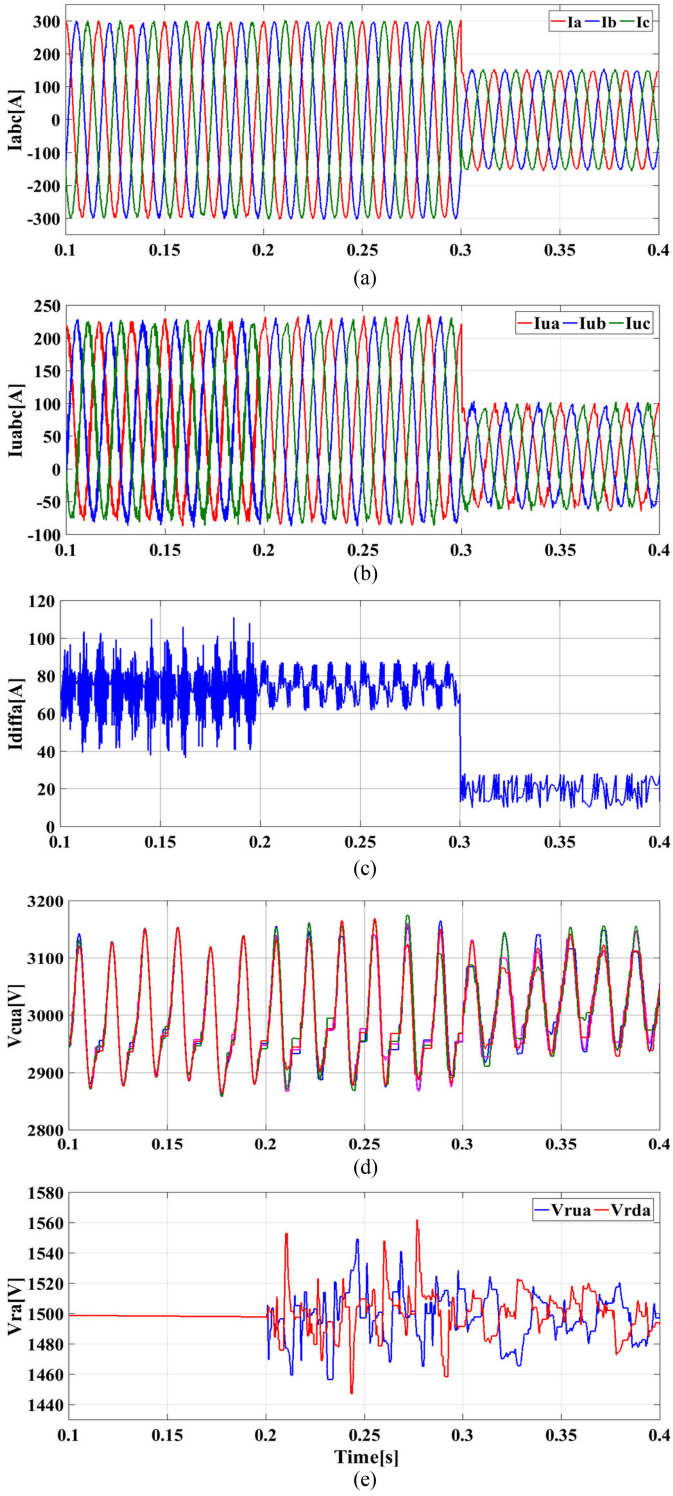

Fig. 4. Simulation results of the EHMMC in normal operation. (a) Output currents. (b) Upper arms current. (c) Phase-*a* differential current. (d) HBSMs capacitor voltage in the upper arm of phase-*a*. (e) FBSM capacitor voltage of both arm of phase-*a*.

currents. As can be seen, the output currents follow its sinusoidal smoothly and with negligible delay. The upper arms current and the differential current of phase-*a* are shown in Fig. 4(b) and (c), respectively. The results indicate the effectiveness of the proposed topology in satisfactory suppression of the circulating

current, while the converter operates in $2N + 1$ modulation. The HBSMs capacitor voltage in the upper arm and the FBSMs capacitor voltage of phase-*a* are illustrated in Fig. 4(d) and (e), respectively. As shown in these figures, the capacitor voltages are well balanced, and although increasing the output current reference raises the capacitors voltage variations, these variations are always bounded to the permissible range of 5% nominal capacitor voltage.

2) Case II: In this case study, fault-tolerant operation of the proposed EHMMC is investigated. The output current reference is set to 200 A and is maintained constant. In Fig. 5(a) and (b), the upper arms and the differential current of phase-*a* are represented. As expected, when one HBSM in each arm is bypassed, a higher ripple and THD in the differential current of phase-*a* is observed compared to the normal operation, which leads to higher arm current amplitude in the phase-*a*. This is due to the reduction in the feasible states that can generate the required arms voltage. In order to show the available voltage margin (i.e., the difference between demand and maximum available voltages) in one arm before and after the fault events, the sum of capacitors voltages (maximum available arm voltage) and generated voltage (demand voltage) in the upper arm of phase-a are shown in Fig. 5(c). As it is observed, although the maximum available voltage is reduced significantly after the fault, the proposed topology still operates stably by employing alternative switching states. The capacitors voltages of the upper arm of phase-*a* is illustrated in Fig. 5 (d). As it is observed, at $t = 1$ s, one of the HBSMs in each arm is bypassed and its voltage remains constant. In addition, variations and average voltage of the HBSMs are increased; however, they still operate stably. The main reason for this increase is that for generating specific output voltage the number of feasible switching states is reduced after the fault. It is noteworthy that although this increase is not too high to damage converter components, it should be considered in HBSMs design. In Fig. 5(e), the capacitors voltages of the FBSMs in phase-*a* are shown. As can be seen, by changing the modulation from $2N + 1$ to $N + 1$ due to the bypassed HBSM, the capacitor voltage variations of FBSMs are reduced significantly.

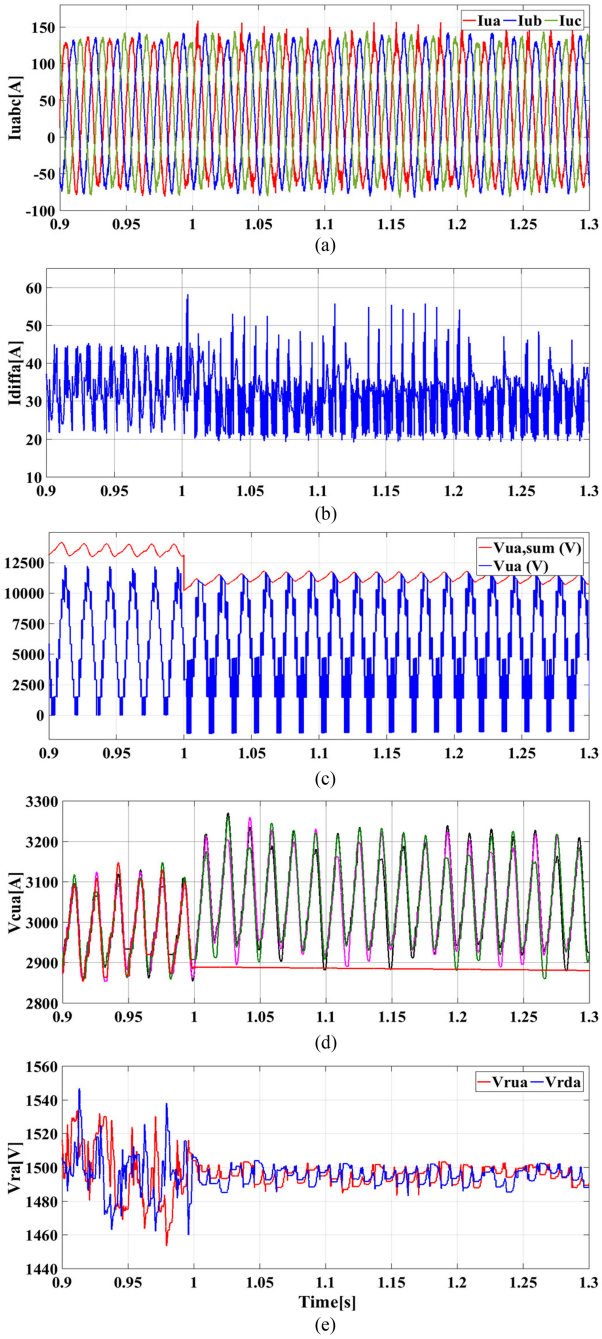

Fig. 5. Simulation results of the EHMMC in fault-tolerant operation. (a) Upper arms current. (b) Phase-*a* differential current. (c) Sum of capacitors voltages in upper arm and the voltage generated by the upper arm of phase-a. (d) HBSMs capacitor voltage in upper arm of phase-*a*. (e) FBSM capacitor voltage of both arm of phase-*a*.

B. Comparison Between EHMMC and HB-MMC

1) Converter Efficiency: All of the previously-mentioned HMMCs have more power losses compared to the usual HB-MMC [8], [23], [24]. Although by using an extra FBSM the number of semiconductor devices in the current path is increased, the proposed EHMMC has less power losses than the usual HB-MMC. This is due to two main reasons: first, the extra FBSM undertakes part of the HBSMs tasks, leading to lower switching frequency in HBSMs. In addition, FBSM has lower switching loss because of lower nominal voltage. Consequently, as it is shown in Table IX, the total loss of EHMMC-I is lower than HB-MMC. Second, by eliminating unnecessary changes in the output and differential voltage levels the switching frequency of HBSMs and FBSM will be reduced, resulting in lower total power loss than EHMMC-I. In Table IX, switching frequencies and power losses of the three schemes are presented. For this calculation, the output current reference is set to 300 A. To evaluate the power losses, the main parameters of semiconductor devices are derived from the datasheet of the 5SNG 0200Q170300 and 5SNG 0250P330305 components [25], [26]. According to Table IX, the HBSMs conduction loss is constant in all cases and the total conduction loss is increased by using the extra FBSM in the proposed EHMMC-I and EHMMC-II. The HBSMs switching loss, however, is reduced significantly

TABLE IX
POWER LOSSES COMPARISON OF THE PROPOSED EHMMCS WITH HB-MMC

	HB-MMC	EHMMC-I		EHMMC-II	
		HBSM	FBSM	HBSM	FBSM
Switching loss (kW)	24.3	16.31	2.37	12.15	1.37
		Total: 18.7		Total: 13.52	
Switching frequency (Hz)	640	430	810	320	520
Conduction loss (kW)	8.02	8.04	2.96	8.08	2.9
		Total: 11		Total: 10.98	
No. devices in conduction	4	6		6	
Total power loss (kW)	32.3	29.7		24.5	

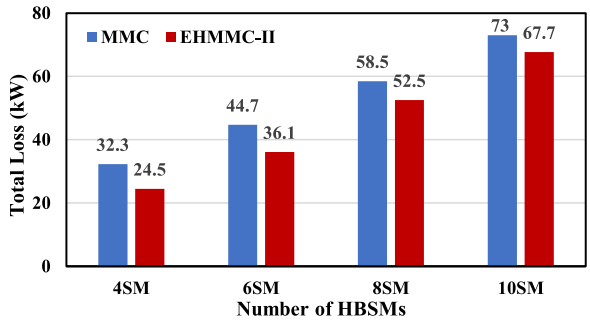

Fig. 6. Total power loss in the regular MMC and EHMMC-II.

TABLE X
PERFORMANCE QUALITY COMPARISON OF THE PROPOSED TOPOLOGIES WITH HB-MMC

Item	HB-MMC	EHMMC-I	EHMMC-II
Output Voltage levels	5	9	9
%THD (v_p)	17.03	8.04	8.1
%THD (v_{ll})	13.84	6.37	6.5
%THD (I_{diff})	14.8	9.4	9.6
%THD (I_{in})	7.23	4.64	4.86

in the EHMMC-I and EHMMC-II schemes, compared to the HB-MMC, which leads to the reduced total power losses. The best results belong to the EHMMC-II. In order to perform a more comprehensive comparison, total loss of HB-MMC and EHMMC-II with different numbers of HBSMs are presented in Fig. 6. As it is observed, total loss of EHMMC-II is lower than HB-MMC in all cases; however, the effectiveness of the proposed topology is more significant in the cases with low number of HBSMs.

2) Converter Performance Quality: Using an extra FBSM in the proposed EHMMCs, makes it possible to generate the output voltage by $(2N + 1)$-modulation without increase in the circulating current ripples. In Table X, power quality indices of the

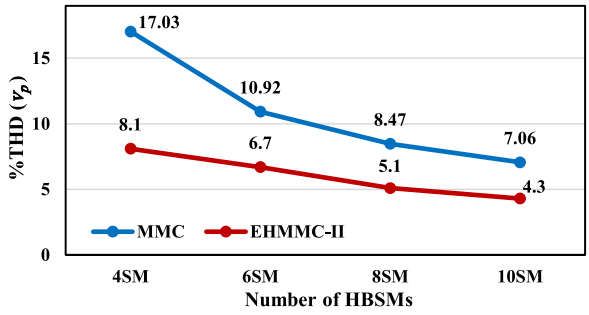

Fig. 7. THD of the phase voltage in HB-MMC and EHMMC-II.

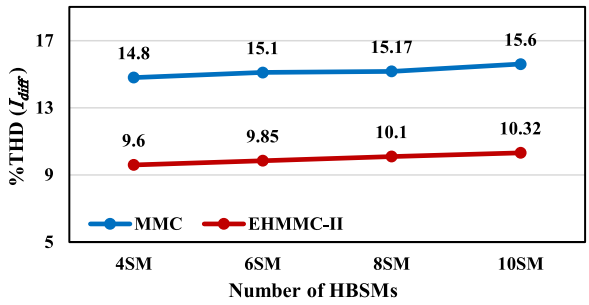

Fig. 8. THD of the differential current in HB-MMC and EHMMC-II.

TABLE XI
SWITCH LOSSES COMPARISON BETWEEN THE PROPOSED TOPOLOGIES AND THE HB-MMC

Device	HB-MMC	EHMMC-I	EHMMC-II
S_1	317.5 W	195.4 W	150 W
D_1	243.4 W	178 W	148.4 W
S_2	780.6 W	604.5 W	532.8 W
D_2	75.9 W	45.6 W	29 W

three schemes are compared in which THD (v_p) and THD (v_{ll}) are relative to the voltage fundamental harmonic and THD (I_{diff}) and THD (I_{in}) are relative to the dc current component. As can be seen, the EHMMC-I and EHMMC-II have more appropriate internal and external performance compared to the HB-MMC. The differences between the EHMMC-I and EHMMC-II results are negligible. Moreover, THD (v_p) and THD (I_{diff}) of HB-MMC and EHMMC-II with different numbers of HBSMs are compared in Figs. 7 and 8, respectively. As shown in Fig. 7, THD (v_p) of EHMMC-II is lower than HB-MMC due to the utilization of $2N + 1$ modulation. Furthermore, although using $2N + 1$ modulation leads to higher THD of differential current, THD (I_{diff}) of EHMMC-II is lower than THD (I_{diff}) of HB-MMC in all cases (see Fig. 8).

3) Converter Reliability: The redundant FBSMs in the proposed EHMMC enable the converter to operate even in the case an SM fault occurs. Furthermore, since the switch losses of the HBSMs are reduced as in Table XI, life-times of the switches and diodes increase. In this table, S_1, D_1, S_2, and D_2 represent

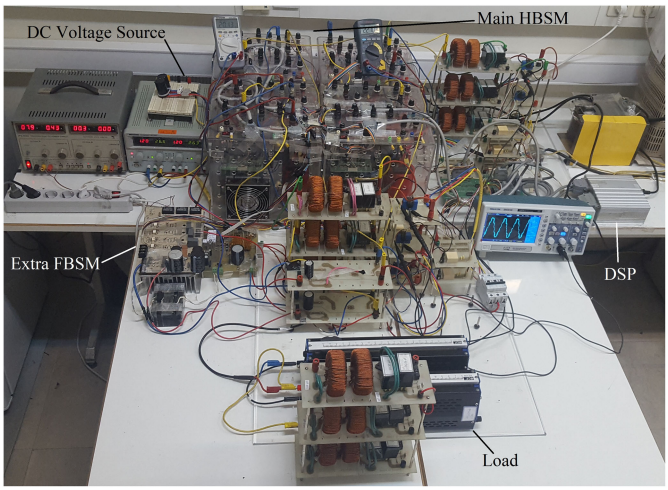

Fig. 9. Laboratory setup.

TABLE XII
EXPERIMENTAL SETUP PARAMETERS

Parameter	Symbol	Value
AC System Frequency	F_S	50 Hz
Load Inductance	L	0 H
Load Resistance	R	4.5 Ω
DC Bus Voltage	V_{DC}	48 V
Arm Inductance	l	0.6 mH
HBSM Capacitance	c	0.00235 F
HBSM Capacitor Voltage	V_{HBSM}	24 V
FBSM Capacitance	c_r	0.007 F
FBSM Capacitor Voltage	V_{FBSM}	12 V
Number of HBSMs per Arm	N	2
Sampling and Control Period	T_S	100 µs

the upper and lower arm switches and diodes, respectively. The tolerable SM-fault scenarios are as follows.

1) When a fault occurs in one or two FBSMs of one phase, the converter cannot continue its operation by the proposed method; however, it can still operate similar to the standard HB-MMC. In this case, the FBSMs will be bypassed and the HBSMs will be controlled by conventional strategies such as the one discussed by [21] in $(N+1)$-modulation.
2) When a fault occurs in one of the HBSMs, the converter can operate with $(N+1)$-modulation while it is necessary to control the HBSMs average capacitor voltage. In the worst case, if fault occurs in one of the HBSMs in two arms of one phase, the converter is still capable to continue its operation.

It is worth mentioning that the conventional HB-MMC cannot tolerates any of the above fault condition. Comparing EHMMC-I and EHMMC-II, the latter has less total power loss compared to the EHMMC-I and HB-MMC, however, performance quality of the EHMMC-I is slightly higher than the EHMMC-II.

C. Experimental Results

The proposed EHMMC is investigated by an experimental setup shown in Fig. 9. The converter comprises two HBSMs

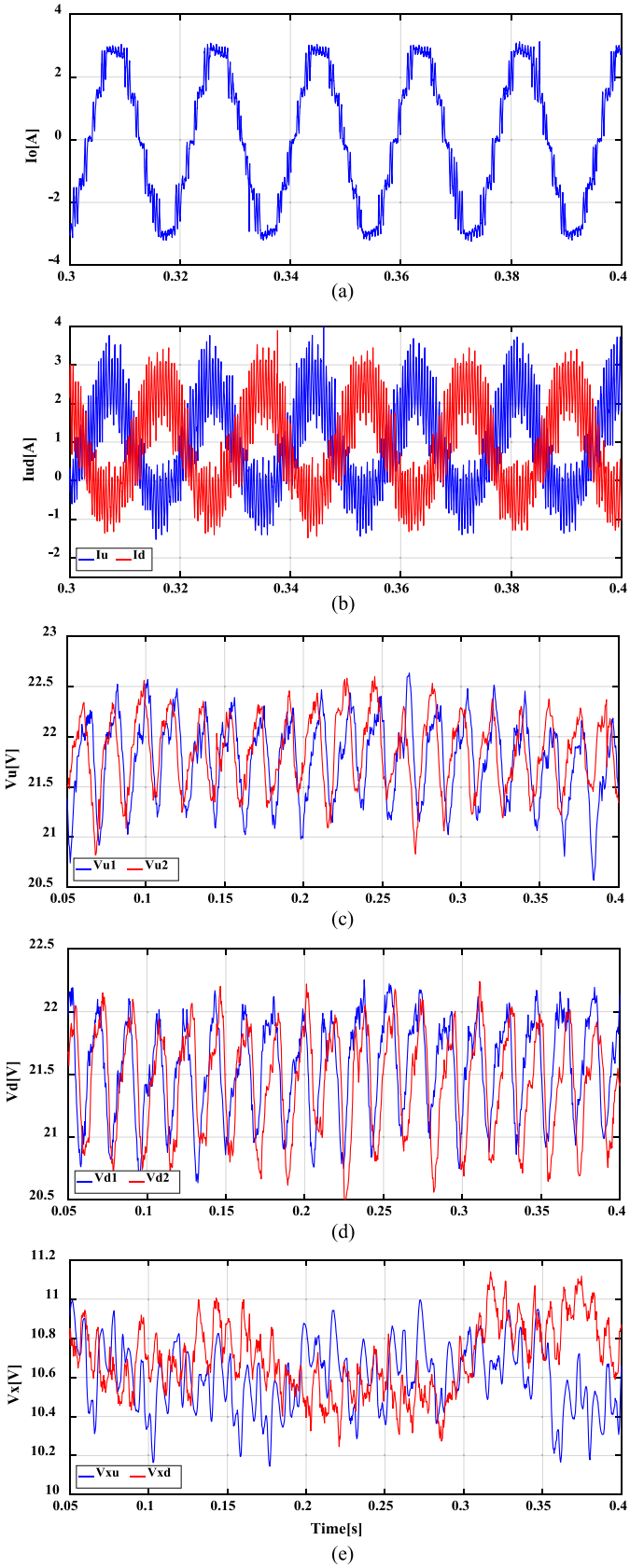

Fig. 10. Experimental results of the EHMMC in normal operation. (a) Output current. (b) Upper and lower arm currents. (c) HBSMs capacitor voltage in the upper arm. (d) HBSMs capacitor voltage in the lower arm (e) FBSM capacitor voltage of both arms.

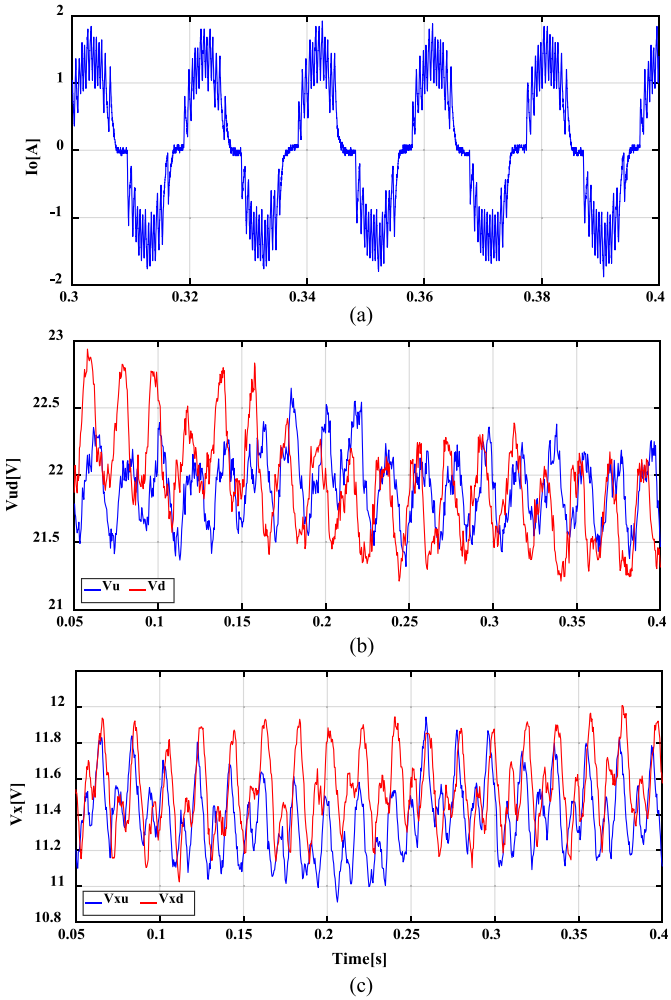

Fig. 11. Experimental results of the EHMMC in fault tolerant operation. (a) Output current. (b) HBSMs capacitor voltage in upper and lower arm. (c) FBSM capacitor voltage of both arm.

and one HBSM in each arm. The main parameters of the setup are given in Table XII. Satisfactory performance of the proposed scheme in the normal and fault conditions is verified as explained in the following.

1) Case I: In this case, normal operation of the proposed EHMMC is evaluated. Fig. 10(a) shows the output current. As the converter is controlled with $2N + 1$ modulation, it exhibits five current levels with low harmonic contents. The arms currents are illustrated in Fig. 10(b), which contain half of the output current and the differential current. The capacitors voltages of the HBSMs in the upper and lower arms and FBSMs are shown in Fig. 10(c)–(e) respectively, which confirm stable operation of the EHMMC. All the experimental and simulation results are in good agreement, justifying the proposed EHMMC.

2) Case II: In this experiment, the fault tolerant operation is investigated. In Fig. 11(a), the output current is shown while one of HBSMs in each arm has been bypassed. The capacitors voltage of the HBSMs and FBSMs are illustrated in Fig. 11(b) and (c), respectively. The obtained results confirm proper operation of the EHMMC under SMs fault.

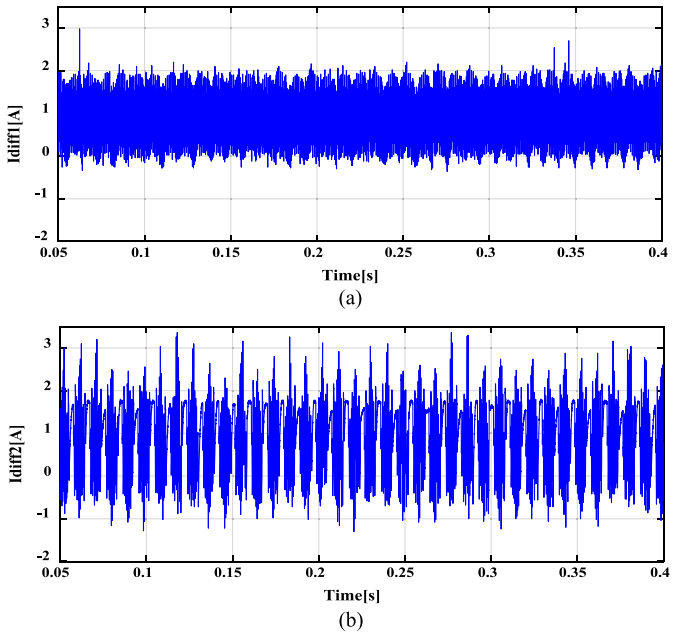

Fig. 12. (a) Differential current in the EHMMC. (b) Differential current in the HB-MMC with $2N + 1$ modulation.

3) Differential Current Comparison in the EHMMC and Conventional HB-MMC: In the second section of this paper, it was proved that due to inability of HB-MMC in generation of specific arm voltages, the circulating current is increased in $2N + 1$ modulation. To verify this claim, the differential current of the HB-MMC and the proposed EHMMC in $2N + 1$ modulation are compared. For implementing the HB-MMC control the method of [21] is used. Fig. 12(a) and (b) show these differential currents. As it can be seen, the circulating current in the HB-MMC is much higher than the EHMMC, which substantiate the superiority of the proposed EHMMC. It is noteworthy that absence of specific arm voltages can have more adverse impacts on the circulating current if the nominal voltage of SMs increases.

V. Conclusion

In this paper, first circulating current of MMCs in $2N + 1$ modulation has been studied carefully. Then, a novel EHMMC has been proposed to improve the converter reliability and to suppress the circulating current. This topology includes HBSMs and at least one FBSM in each arm. In comparison to the conventional HB-MMC, the EHMMC has less power loss and higher performance characteristics. In addition, the proposed EHMMC tolerates any one HBSM or FBSM fault in each arm, either individually or simultaneously. The control principles in both steady-state and fault-tolerant operations have been developed based on model predictive control and have been verified by several simulation and experimental studies. In this regard, the power loss, switching frequency, and performance quality of the proposed EHMMC have been compared with the HB-MMC. The results show that the EHMMC have advantageous characteristics in low power (up to several megawatts) applications, in which the number of submodules is relatively small.

REFERENCES

[1] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel Converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[2] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel Back-to-Back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[3] M. Hagiwara, I. Hasegawa, and H. Akagi, "Start-up and low-speed operation of an electric motor driven by a modular multilevel cascade inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1556–1565, Jul./Aug. 2013.

[4] J. Mei, B. Xiao, K. Shen, L. M. Tolbert, and J. Y. Zheng, "Modular multilevel inverter with new modulation method and its application to photovoltaic Grid-Connected generator," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5063–5073, Nov. 2013.

[5] M. Hagiwara, R. Maeda, and H. Akagi, "Negative-Sequence Reactive-power control by a PWM STATCOM based on a modular multilevel cascade converter (MMCC-SDBC)," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 720–729, Mar./Apr. 2012.

[6] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1137–1146, Mar. 2015.

[7] M. B. Ghat, A. Shukla, and E. C. Mathew, "A new hybrid modular multilevel converter with increased output voltage levels," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 1634–1641.

[8] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Trans. Power Del.*, vol. 30, no. 1, pp. 385–394, Feb. 2015.

[9] B. S. Riar and U. K. Madawala, "Decoupled control of modular multilevel converters using voltage correcting modules," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 690–698, Feb. 2015.

[10] G. T. Son *et al.*, "Design and control of a modular multilevel HVDC converter with redundant power modules for noninterruptible energy transfer," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1611–1619, Jul. 2012.

[11] B. Li, S. Shi, B. Wang, G. Wang, W. Wang, and D. Xu, "Fault diagnosis and tolerant control of single IGBT Open-Circuit failure in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3165–3176, Apr. 2016.

[12] G. Liu, Z. Xu, Y. Xue, and G. Tang, "Optimized control strategy based on dynamic redundancy for the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 339–348, Jan. 2015.

[13] B. Li, Y. Zhang, R. Yang, R. Xu, D. Xu, and W. Wang, "Seamless transition control for modular multilevel converters when inserting a Cold-Reserve redundant submodule," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4052–4057, Aug. 2015.

[14] F. Zhang, W. Li, and G. Jo, "A Voltage-Level-Based model predictive control of modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 5301–5312, Aug. 2016.

[15] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "Steady-State analysis of interaction between harmonic components of Arm and line quantities of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 57–68, Jan. 2012.

[16] R. Picas, J. Pou, S. Ceballos, V. Agelidis, and M. Saeedifard, "Minimization of the capacitor voltage fluctuations of a modular multilevel converter by circulating current control," in *Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc.*, 2012, pp. 4985–4991.

[17] J. Böcker, B. Freudenberg, A. The, and S. Dieckerhoff, "Experimental comparison of model predictive control and cascaded control of the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 422–430, Jan. 2015.

[18] R. Darus, G. Konstantinou, J. Pou, S. Ceballos, and V. G. Agelidis, "Carrier interleaved PWM techniques in modular multilevel converters: A comparison based on same voltage level waveforms," in *Proc. IEEE Energy Conversion Congress Expo.*, 2014, pp. 3725–3730.

[19] G. Konstantinou, J. Pou, S. Ceballos, R. Picas, J. Zaragoza, and V. G. Agelidis, "Control of circulating currents in modular multilevel converters through redundant voltage levels," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7761–7769, Nov. 2016.

[20] Z. Gong, P. Dai, X. Yuan, X. Wu, and G. Guo, "Design and experimental evaluation of fast model predictive control for modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3845–3856, Jun. 2016.

[21] J. W. Moon, J. S. Gwon, J. W. Park, D. W. Kang, and J. M. Kim, "Model predictive control with a reduced number of considered states in a modular multilevel converter for HVDC system," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 608–617, Apr. 2015.

[22] P. Cortes *et al.*, "Guidelines for weighting factors design in model predictive control of power converters and drives," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2009, pp. 1–7.

[23] R. Darus, G. Konstantinou, J. Pou, S. Ceballos, and V. G. Agelidis, "Comparison of phase-shifted and level-shifted PWM in the modular multilevel converter," in *Proc. Int. Power Electron. Conf.*, 2014, pp. 3764–3770.

[24] M. M. C. Merlin *et al.*, "The alternate Arm Converter: A new hybrid multilevel converter with DC-Fault blocking capability," *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 310–317, Feb. 2014.

[25] 62Pak phase leg IGBT Module Datasheet. 2018. [Online]. Available: www.abb.com/semiconductors

[26] HiPak IGBT Module Datasheet. 2018. [Online]. Available: www.abb.com/semiconductors

Ramin Razani received the B.Sc. degree in electrical engineering from Isfahan University of Technology, Isfahan, Iran, in 2015, and the M.Sc. degree in power electrical engineering from Sharif University of Technology, Tehran, Iran, in 2017.

His current research interests include multilevel converters and application of power electronics in power systems.

Mohammad Hasan Ravanji received the B.Sc. degree in 2012 and the M.Sc. degree in 2014 both in electrical engineering from Sharif University of Technology (SUT), Tehran, Iran, where he is currently working toward the Ph.D. degree.

His current research interests include renewable energy systems.

Mostafa Parniani (SM'06) received the Ph.D. degree in electrical engineering from the University of Toronto, Canada, in 1995.

He is a Professor of electrical engineering at Sharif University of Technology, Tehran, Iran. He was a Visiting Scholar at Rensselaer Polytechnic Institute, USA, during 2005–2006. His research interests include power system dynamics and control, applications of power electronics in power systems, and renewable energies.