Differences Between Continuous Single-Phase and Online Three-Phase Power-Decoupled Converters

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***Abstract*—Second-order oscillating power is always generated by a single-phase converter. To decouple this oscillating power from its dc link requires a power decoupling circuit to operate continuously. In contrast, ac grid voltages supplying a three-phase converter are usually balanced. There will, hence, be no oscillating power, if grid currents are balanced too. However, grid voltages may become unbalanced during fault or other disturbances, which, when multiplied with balanced currents, will result in oscillating power. Power decoupling for a three-phase converter is, thus, only necessary during fault, rather than continuously. Its target should also be to improve power quality even during fault, rather than to prolong lifetimes of capacitors claimed with single-phase decoupling. Those differences cause criteria applicable to selecting a power decoupling circuit for single- and three-phase converters to be different, especially when there are seven different types of faulted voltage conditions to consider. These considerations are now studied, before presenting experimental results for verifying the effectiveness of all studied three-phase power-decoupled converters.**

***Index Terms*—Power decoupling, second-order power oscillation, three-phase unbalance, voltage and current stresses.**

I. Introduction

A UNIQUE feature of all single-phase converters is their ever-present second-order oscillating power. This oscillating power may degrade performances and/or lifetimes of maximum-power-point trackers [1], fuel cells [2], light-emitting diodes [3], and other electronic loads connected to the dc link. Diverting it away from the dc link may, therefore, be necessary, and the technique to do so is referred to as power decou-

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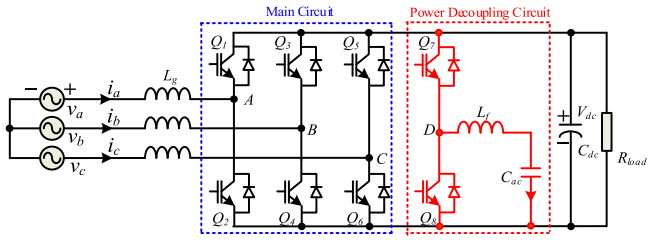


Fig. 1. Possible topology with offline three-phase power decoupling.

lower voltages, and hence further deteriorating them. In other words, the extent of voltage unbalance may worsen, if the increased currents have not unintentionally triggered overcurrent protection.

Other more flexible power control schemes have, hence, been proposed to arrive at an acceptable tradeoff between balanced currents and constant powers [32]–[37]. For instance, in [33]–[36], some mechanisms have been added to cap the peak current, and hence avoiding the unbalanced overcurrent condition. Another control scheme has targeted to keep only the active power constant, so that the grid currents can be less unbalanced under unbalanced voltage conditions [37]. The extent of current unbalance, however, depends on the extent of voltage unbalance. All in all, it is not possible to always meet independent ac and dc specifications with a standard three-phase converter, if only its control scheme can be varied. One example is balanced grid currents and ripple-free dc-link power, which, as understood from the existing literature, cannot be simultaneously attained by a standard three-phase converter. Independent tuning can only be achieved with topological variations, whose purpose is to decouple oscillating power away from the dc link, so that the grid currents can continue to be balanced or follow any desired waveforms during fault.

Therefore, unlike a single-phase converter where power decoupling is always functioning, a three-phase converter only needs power decoupling when the grid voltages become unbalanced. Its target should, hence, be to improve power quality for sensitive loads or sources during fault, rather than to prolong lifetimes of capacitors associated with single-phase power decoupling. For that, offline and online options are possible for the three-phase converter, just like with an uninterruptible power supply [38], [39] or a dynamic voltage restorer (DVR) [40], [41]. Offline solutions are mostly implemented by inserting a standalone circuit. An obvious example is the half-bridge circuit shown in Fig. 1, which, under the normal balanced condition, should be turned OFF to avoid operating losses. The added half-bridge is, therefore, somewhat underutilized and may lead to inrush current and prolonged transient during its activation and deactivation.

In contrast, online solutions are faster, but they should avoid extra components, which, otherwise, will generate losses even under the balanced condition with no oscillating power. Their constraints are, hence, more stringent. Moreover, unlike a single-phase converter, online power decoupling for a three-phase converter must be examined with seven types of faulted voltages. They are now evaluated in this paper, after a short explanation in Section II about how a three-phase converter produces oscillating power. Section III then presents possible online power-decoupled converters, whose minimum dc-link voltages and current stresses have been quantified in Section IV for all types of faulted voltages. The quantification then permits the preferred three-phase power-decoupled converter to be identified, before discussing its justifications as a power quality enhancer in Section V. Experimental results and conclusions are finally presented in Sections VI and VII, respectively.

II. Oscillating Power

To mathematically demonstrate the existence of second-order oscillating power, ac grid voltages seen by a standard three-phase converter can be represented generally as (1). Corresponding grid currents, if regulated to be sinusoidal and balanced, can also be represented as (2)

$$\begin{cases} v_a = \sqrt{2}V_a \sin(\omega t + \alpha_a) \\ v_b = \sqrt{2}V_b \sin(\omega t + \alpha_b) \\ v_c = \sqrt{2}V_c \sin(\omega t + \alpha_c) \end{cases} \tag{1}$$

$$\begin{cases} i_a = \sqrt{2}I \sin(\omega t + \varphi) \\ i_b = \sqrt{2}I \sin(\omega t - 120^\circ + \varphi) \\ i_c = \sqrt{2}I \sin(\omega t + 120^\circ + \varphi). \end{cases} \tag{2}$$

Instantaneous power flowing through the three-phase converter can then be computed as

$$\begin{aligned} p_{\text{ac}}(t) &= v_a i_a + v_b i_b + v_c i_c = P_{\text{dc}} + p_{2\omega}(t) \\ &= P_{\text{dc}} + P_{2\omega} \cos(2\omega t + \delta) \end{aligned} \tag{3}$$

where P_{dc} is the average constant active power, and $P_{2\omega}$ and δ are the magnitude and phase of the second-order oscillating power $p_{2\omega}(t)$. Expressions for P_{dc} and $p_{2\omega}(t)$ can further be derived as

$$\begin{aligned} P_{\text{dc}} = {} & V_a I \cos(\alpha_a - \varphi) + V_b I \cos(\alpha_b - \varphi + 120^\circ) \\ & + V_c I \cos(\alpha_c - \varphi - 120^\circ) \end{aligned} \tag{4}$$

$$\begin{aligned} p_{2\omega}(t) = {} & -(V_a I \cos(2\omega t + \alpha_a + \varphi) \\ & + V_b I \cos(2\omega t + \alpha_b + \varphi - 120^\circ) \\ & + V_c I \cos(2\omega t + \alpha_c + \varphi + 120^\circ)). \end{aligned} \tag{5}$$

With balanced voltages, $V_a = V_b = V_c$, $\alpha_a = 0^\circ$, $\alpha_b = -120^\circ$, and $\alpha_c = 120^\circ$, which, when substituted into (5), yield $p_{2\omega}(t) = 0$, as initially seen in Fig. 2. It is, however, not zero when voltages in Fig. 2 become unbalanced. The nonzero oscillating power then causes dc-link voltage and/or current to vary. It is, thus, not possible to nullify oscillating power at the dc link of a standard three-phase converter while regulating the grid currents to be balanced. In other words, power decoupling is necessary for diverting oscillating power away from the dc link, if grid currents need to be balanced. It should, however, only have an effect when the grid voltages become unbalanced, rather than continuously. Three-phase power decoupling should, hence, be designed differently from single-phase power decoupling, even though their topologies operate based on the same principles to be described next.

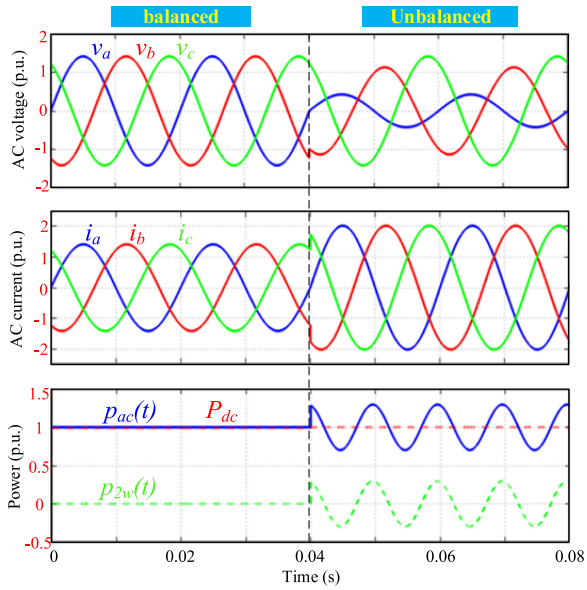


Fig. 2. AC voltages, currents, and their instantaneous power components under initially balanced and then unbalanced conditions.

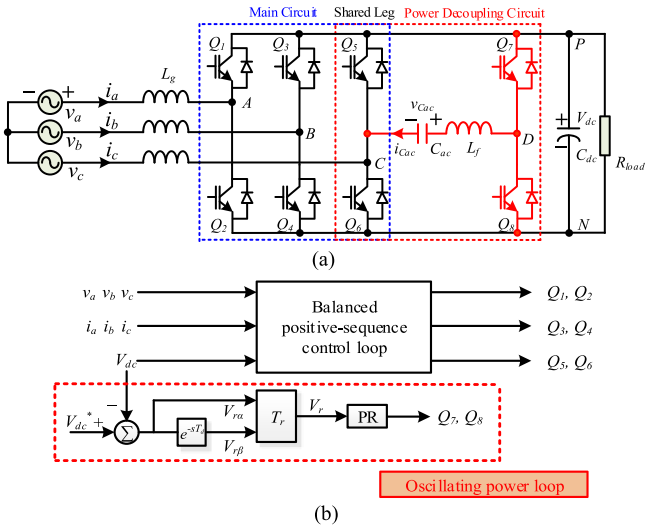


Fig. 3. Modified four-leg converter (MFC).

III. Online Three-Phase Power Decoupling

As explained in Section I, three-phase power decoupling may either be offline or online. Offline configurations are relatively straightforward, since they merely add extra independent circuits, like the half-bridge shown in Fig. 1. The added half-bridge will only be turned ON for power decoupling when the grid voltages become unbalanced. It is, thus, underutilized and may experience large inrushes and poor transients at the beginning and end of power decoupling. Alternatively, the added half-bridge may operate online for faster responses, but its accompanied losses may be sizable. Extra components should, hence, be avoided in case of online power decoupling, provided ratings of existing components do not increase significantly, as evaluated in the next section. Before that, three three-phase power-decoupled converters, extended from recent single-phase topologies found in [11]–[13], are described.

A. Topology 1: Modified Four-Leg Converter

The modified four-leg converter (MFC) shown in Fig. 3(a) is from [11], where switches Q_1 and Q_2 have not been used for single-phase operation. But, regardless of whether single- or three-phase, the MFC uses an extra half-bridge. It is, thus, like the example shown in Fig. 1, but has its extra passive components $C_{\rm ac}$ and L_f connected from the extra half-bridge to a shared phase-leg, rather than to the negative rail of the dc link. It is, thus, not a favorable online power decoupling circuit, because of its added components. Despite that, its single-phase precedence has been proven in [11] to offer considerable rating advantages. The intention here is, thus, to evaluate whether these advantages apply to three-phase decoupling, and if not, to what extent they deviate. The MFC in Fig. 3(a) has, hence, been retained for evaluation, noting particularly that its voltage and current of $C_{\rm ac}$ must be controlled according to

$$\begin{cases} v_{C\rm ac} = \sqrt{2} V_{C\rm ac} \sin(\omega t + \phi) \\ i_{C\rm ac} = \sqrt{2}\omega C_{\rm ac} V_{C\rm ac} \cos(\omega t + \phi). \end{cases} \tag{6}$$

Their instantaneous power is thus

$$p_{C\rm ac}(t) = v_{C\rm ac} i_{C\rm ac} = \omega C_{\rm ac} V_{C\rm ac}^2 \sin(2\omega t + 2\phi). \tag{7}$$

The target is then to equate (7) with the time-varying term of (3), in order to divert oscillating power to $C_{\rm ac}$. This equality, upon solved, yields

$$\begin{cases} V_{C\rm ac} = \sqrt{\frac{P_{2\omega}}{\omega C_{\rm ac}}} \\ \phi = \frac{\delta}{2} + \frac{\pi}{4} \quad \text{or} \quad \phi = \frac{\delta}{2} - \frac{3\pi}{4}. \end{cases} \tag{8}$$

Accurate computation of (8), and hence (6), is, however, not practical, because of possible variation of parameters, including $C_{\rm ac}$. The desired voltage in (6) should, hence, be obtained autonomously through realizing the oscillating power control loop shown in Fig. 3(b). Also shown in the figure is the usual balanced positive-sequence current regulation, whose principle has widely been discussed in the literature, and hence not repeated here. As for the oscillating power loop, it has been mentioned in [13], but only for the third power-decoupled converter to be described later. Also, an inner current loop has been included in [13], which is operationally not necessary, and hence not adopted here to avoid an accurate current sensor for the added half-bridge.

Irrespective of that, its operation begins by extracting constant reference $V_{\rm dc}^*$ from the actual dc-link voltage $V_{\rm dc}$ to yield its second-order ripple $V_{r\alpha}$ only. Ripple $V_{r\alpha}$ is then delayed by a quarter cycle T_d to obtain $V_{r\beta}$, whose angular frequency is still 2ω, and not ω demanded by the capacitive voltage reference in (6). A way to meet the target is to transform $V_{r\alpha}$ and $V_{r\beta}$ from the 2ω- to fundamental ω-frame by using the following orthogonal transfer matrix

$$T_r = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix}. \tag{9}$$

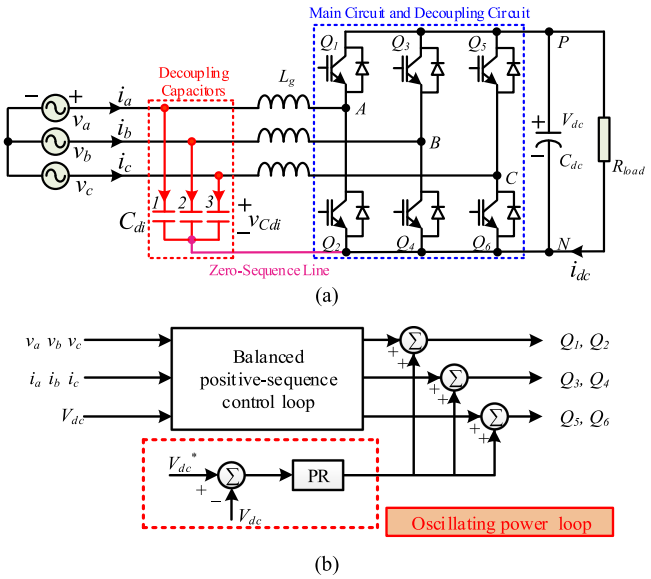


Fig. 4. Differential buck converter (DBC).

One of the two signals produced by (9) and notated as V_r can subsequently be regulated to zero by a proportional-resonant (PR) controller tuned to ω. The PR output can then be directly used for modulation of phase-leg D, whose modulating reference will autonomously ensure the generation of capacitive voltage in (6).

B. Topology 2: Differential Buck Converter

Another converter with online power decoupling built-in is the three-phase differential buck converter (DBC, assuming power from dc to ac), whose single-phase precedence with one lesser phase-leg has earlier been studied in [12]. Its topology is shown in Fig. 4(a). Clearly, the DBC does not require additional switches. Moreover, if *LCL*-filters are already included, their middle capacitances $C_{di} = C_d$ ($i = 1, 2,$ and 3) can simply be enlarged slightly for storing the oscillating power, instead of adding more passive components. The star point of the capacitances must, however, be tied to the negative dc rail, instead of floating like with most standard *LCL*-filtered converters. The equation that will diverge oscillating power in (3) to the decoupling capacitors can then be expressed as

$$C_d v_{Cd1}\frac{dv_{Cd1}}{dt} + C_d v_{Cd2}\frac{dv_{Cd2}}{dt} + C_d v_{Cd3}\frac{dv_{Cd3}}{dt} = P_{2\omega}\cos(2\omega t + \delta) \tag{10}$$

where v_{Cdi} ($i = 1$, 2, or 3) represents the voltage across each decoupling capacitor.

Additionally, solutions for (10) must satisfy (11), where approximated relationships among v_{Cdi} and the line grid voltages v_{ab} and v_{bc} are given

$$\begin{cases} v_{Cd1} - v_{Cd2} = v_{ab} = \sqrt{2}V_{ab}\sin(\omega t + \theta_{ab}) \\ v_{Cd2} - v_{Cd3} = v_{bc} = \sqrt{2}V_{bc}\sin(\omega t + \theta_{bc}). \end{cases} \tag{11}$$

The final expressions for v_{Cdi} are comparably more complex, as seen from (12) shown at the bottom of this page, for v_{Cd1} as an example. Where V_{C0} is the initial voltage across C_{d1} at $t = 0$.

It is, thus, not easy to rely on (12) for implementation, even though it does inform that v_{Cdi} must include components at ω for countering the line grid voltages and components at 2ω for diverting oscillating power to C_{di}. Therefore, the single-loop scheme in Fig. 4(b) should be considered, where second- or more even-order ripples of the dc-link voltage $V_{\rm dc}$ have been forced to zero by PR controllers tuned to those frequencies. The summed output from all resonant controllers is then at $2n\omega$, where $2n$ is usually 2 and 4, since ripples at higher frequencies are usually very small. Adding it to the output at ω from the balanced positive-sequence control block finally gives modulating reference needed for generating v_{Cdi} in (12).

C. Topology 3: Split-Capacitor Converter

The third converter considered for online power decoupling is the three-phase split-capacitor converter (SCC) shown in Fig. 5(a). Its single-phase precedence has been discussed in [13], where switches Q1 and Q2 have been removed. Despite that, both single- and three-phase SCCs have a shared phase-leg, connected to the midpoint of two capacitors at the dc link. The two capacitors, in turn, carry the diverted oscillating power, in addition to maintaining a constant dc-link voltage. Their respective voltages must, thus, be controlled as

$$\begin{cases} v_{\rm dc1} = \frac{V_{\rm dc}}{2} + \sqrt{2}V_{Cf}\sin(\omega t + \theta) \\ v_{\rm dc2} = \frac{V_{\rm dc}}{2} - \sqrt{2}V_{Cf}\sin(\omega t + \theta) \end{cases} \tag{13}$$

where $V_{\rm dc}$ is the dc-link voltage, and $\sqrt{2}V_{Cf}$ is the common peak of the two 180°-shifted ac components varying at ω. Their values must further satisfy $\sqrt{2}V_{Cf} \le V_{\rm dc}/2$, to keep both voltages v_{dc1} and v_{dc2} always positive.

$$v_{Cd1} = \frac{1}{3}(2\sqrt{2}\sin(\omega t + \theta_{ab}))V_{ab} + \sqrt{2}\sin(\omega t + \theta_{bc})V_{bc} + \sqrt{\begin{array}{l} \frac{1}{\omega C_d}(3P_{2\omega}\sin(2\omega t + \delta) - 3P_{2\omega}\sin(\delta) + 9\omega C_d V_{C0}^2 + 2\omega C_d(2 - 3\cos(2\theta_{ab}) \\ + V_{ab}^2\cos(2\omega t + 2\theta_{ab})) + 2\omega C_d V_{ab}V_{bc}(2\cos(\theta_{ab} - \theta_{bc}) - 3\cos(\theta_{ab} + \theta_{bc}) \\ + \cos(2\omega t + \theta_{ab} + \theta_{bc})) + 2\omega C_d V_{bc}^2\cos(2\omega t + 2\theta_{bc}) - 3\omega C_d V_{bc}^2\cos(2\theta_{bc}) \\ + \omega C_d V_{bc}^2 - 6\sqrt{2}\omega C_d V_{C0}(2V_{ab}\sin(\theta_{ab}) + V_{bc}\sin(\theta_{bc}))) \end{array}} \tag{12}$$

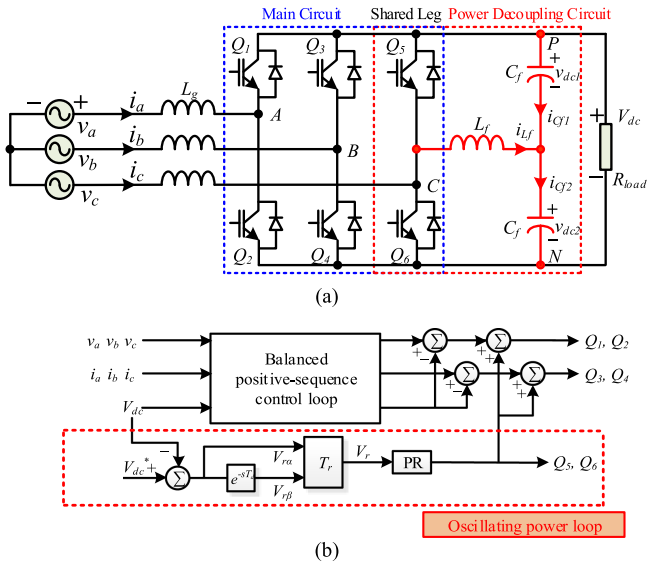


Fig. 5. Split-capacitor converter (SCC).

From (13), the two capacitive currents i_{Cf1} and i_{Cf2}, and filter inductive current i_{Lf} can then be determined as

$$\begin{cases} i_{Cf1} = C_f \frac{dv_{\rm dc1}}{dt} = \sqrt{2}\omega C_f V_{Cf} \cos(\omega t + \theta) \\ i_{Cf2} = C_f \frac{dv_{\rm dc2}}{dt} = -\sqrt{2}\omega C_f V_{Cf} \cos(\omega t + \theta) \end{cases} \tag{14}$$

$$i_{Lf} = -i_{Cf1} + i_{Cf2} = -2\sqrt{2}\omega C_f V_{Cf} \cos(\omega t + \theta) \tag{15}$$

from which total instantaneous power of the two capacitors can be determined as

$$p_{Cf}(t) = p_{Cf1}(t) + p_{Cf2}(t) = 2\omega C_f V_{Cf}^2 \sin(2\omega t + 2\theta). \tag{16}$$

Again, equating (16) with the time-varying term of (3) yields the following expressions for computing magnitude V_{Cf} and phase θ in (13):

$$\begin{cases} V_{Cf} = \sqrt{\frac{P_{2\omega}}{2\omega C_f}} \\ \theta = \frac{\pi}{4} + \frac{\delta}{2} \quad \text{or} \quad \theta = -\frac{3\pi}{4} + \frac{\delta}{2}. \end{cases} \tag{17}$$

Direct computation of the reference capacitor voltages can, however, be avoided by using the control scheme shown in Fig. 5(b), which, when compared with Fig. 3(b) for the MFC, is found to be closely similar. But, without an extra fourth phase-leg, the SCC can only regulate its balanced positive-sequence currents with two phase-legs, since its third phase-leg has been tasked to regulate the oscillating power. Terminal voltages of its two current-regulated phase-legs must, hence, be computed by summing the desired fundamental line voltages v_{ac} and v_{bc} in Fig. 5(b) with the terminal voltage of the third phase-leg. This has been ensured by the four summing nodes shown after the balanced positive-sequence control block in the figure.

D. Simulation Results

To better demonstrate working principles of the three online power-decoupled converters, simulations have been performed with their results organized in Fig. 6. Expectedly, results in Fig. 6(a) have shown nonzero oscillating power $p_{2\omega}(t)$, which, in a standard three-phase converter, will cause oscillating dc-link voltage $V_{\rm dc}$, when its grid currents i_a, i_b, and i_c are balanced, but not its grid voltages v_a, v_b, and v_c. A constant $V_{\rm dc}$ can only be achieved by one of the power-decoupled converters, whose grid currents can continue to be balanced under the same grid voltage unbalance. Related results can be seen in Fig. 6(b) to (d), where all $V_{\rm dc}$ traces are indeed constant, even though their values are different, and differ from the average value of the standard converter in Fig. 6(a). Explanation for that can be found in the next section, where minimum dc-link voltages demanded by the converters are derived. In the meantime, it should be emphasized that nonzero $p_{2\omega}(t)$ can still be seen in all three figures. This is expected, since $p_{2\omega}(t)$ has merely been diverted from the dc link to the decoupling capacitors. Instantaneous power traces of the power decoupling capacitors, notated as $p_{C\_pd}(t)$ in all figures, are, hence, similar to those of $p_{2\omega}(t)$.

It should, moreover, be observed that the three power-decoupled converters generate different voltage wave-shapes across their decoupling capacitors. For the MFC and SCC, their capacitive voltages have the same angular frequency of ω, as seen from the top traces in Fig. 6(b) and (d). The SCC, however, has two capacitive voltages with opposing ac components, which, no doubt, is in accordance with (13). Further seen from the top in Fig. 6(c) are distorted capacitive voltages of the DBC, which, as understood from (12), are due to the presence of both components at ω and 2ω.

IV. Rating Requirements

Voltage and current stresses of a converter must always be determined, before its power devices can be sized properly. They are, thus, evaluated now for the three power-decoupled converters when in single- and three-phase operations. It should, however, be pointed out that although their single-phase performances have earlier been assessed separately in [11]–[13], their consolidated comparison has not yet been considered. It is, thus, performed here near the end of the section to unambiguously project differences between single- and three-phase power decoupling.

A. Types of Three-Phase Voltage Unbalance

Online power decoupling is for diverting oscillating power away from the dc link when the grid voltages become unbalanced during fault. The fault duration may sometimes be short, but its effects are usually more severe than long-term voltage unbalance linked to, e.g., single-phase loads. It is, thus, necessary to evaluate all known faults and their accompanied voltage unbalances, before recommending an online three-phase power-decoupled converter that can offer continuous power quality even during fault. The faults considered are three-phase, phase-to-phase with and without ground, and single-line-to-ground faults [42], which may collectively result in seven types of dipped voltage conditions shown in Fig. 7. Mathematically, the voltage conditions may be summarized as in Table I, where V is the voltage-dip magnitude.

Among them, type A is the only balanced three-phase dip, which has nevertheless been considered for comprehensiveness. The remaining six types are all unbalanced with each type

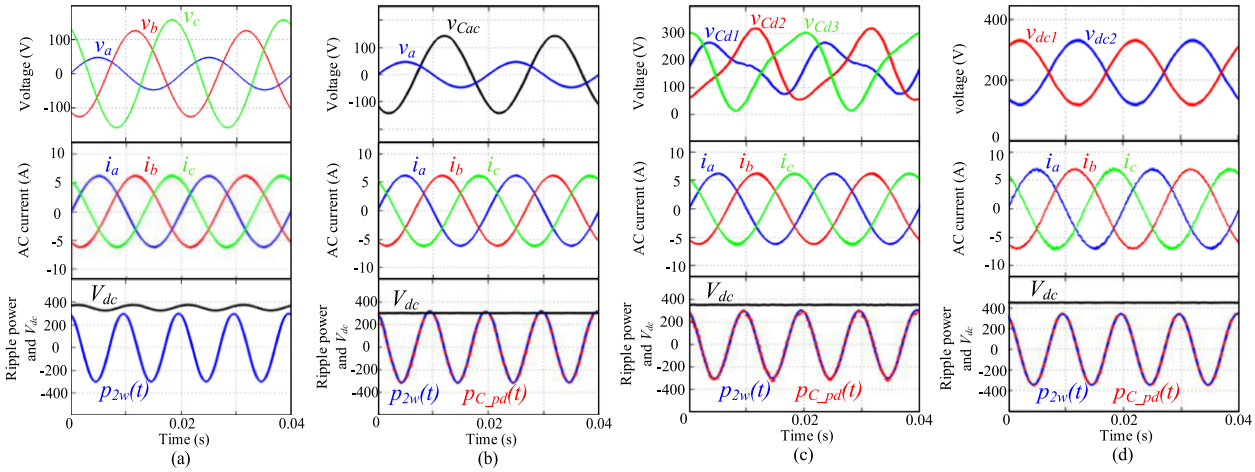


Fig. 6. Simulation results of (a) standard three-phase converter, (b) MFC, (c) DBC, and (d) SCC under the unbalanced voltage condition.

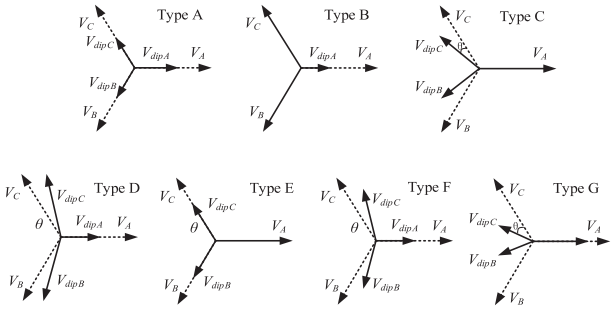


Fig. 7. Three-phase voltages before (dotted) and during fault (solid).

TABLE I
VOLTAGE EXPRESSIONS DURING FAULT

Type A	Type B
$\begin{cases} \dot{v}_{dipa} = \dot{V} \\ \dot{v}_{dipb} = -\frac{1}{2}\dot{V} - \frac{1}{2}j\dot{V}\sqrt{3} \\ \dot{v}_{dipc} = -\frac{1}{2}\dot{V} + \frac{1}{2}j\dot{V}\sqrt{3} \end{cases}$	$\begin{cases} \dot{v}_{dipa} = \dot{V} \\ \dot{v}_{dipb} = -\frac{1}{2} - \frac{1}{2}j\sqrt{3} \\ \dot{v}_{dipc} = -\frac{1}{2} + \frac{1}{2}j\sqrt{3} \end{cases}$
Type C	**Type D**
$\begin{cases} \dot{v}_{dipa} = 1 \\ \dot{v}_{dipb} = -\frac{1}{2} - \frac{1}{2}j\dot{V}\sqrt{3} \\ \dot{v}_{dipc} = -\frac{1}{2} + \frac{1}{2}j\dot{V}\sqrt{3} \end{cases}$	$\begin{cases} \dot{v}_{dipa} = \dot{V} \\ \dot{v}_{dipb} = -\frac{1}{2}\dot{V} - \frac{1}{2}j\sqrt{3} \\ \dot{v}_{dipc} = -\frac{1}{2}\dot{V} + \frac{1}{2}j\sqrt{3} \end{cases}$
Type E	**Type F**
$\begin{cases} \dot{v}_{dipa} = 1 \\ \dot{v}_{dipb} = -\frac{1}{2}\dot{V} - \frac{1}{2}j\dot{V}\sqrt{3} \\ \dot{v}_{dipc} = -\frac{1}{2}\dot{V} + \frac{1}{2}j\dot{V}\sqrt{3} \end{cases}$	$\begin{cases} \dot{v}_{dipa} = \dot{V} \\ \dot{v}_{dipb} = -\frac{1}{2}\dot{V} - j(\frac{1}{3} + \frac{1}{6}\dot{V})\sqrt{3} \\ \dot{v}_{dipc} = -\frac{1}{2}\dot{V} + j(\frac{1}{3} + \frac{1}{6}\dot{V})\sqrt{3} \end{cases}$
Type G	
$\begin{cases} \dot{v}_{dipa} = \frac{2}{3} + \frac{1}{3}\dot{V} \\ \dot{v}_{dipb} = -(\frac{1}{3} + \frac{1}{6}\dot{V}) - \frac{1}{2}j\dot{V}\sqrt{3} \\ \dot{v}_{dipc} = -(\frac{1}{3} + \frac{1}{6}\dot{V}) + \frac{1}{2}j\dot{V}\sqrt{3} \end{cases}$	

having two phasors of the same length, placed symmetrically along the axis of the third phasor. The two mirrored phasors can additionally be any two out of three phases, which means there are three combinations to consider for each voltage unbalance. The three combinations, in turn, affect the asymmetrical MFC and SCC differently. Their "worst cases" must, hence, be considered when assessing them.

B. Voltage and Current Expressions From Equivalent Models

Minimum voltage and current stresses of the three power-decoupled converters can be easily analyzed by referring to their equivalent circuits in Fig. 8. For each circuit, controlled sources $v_{\text{con}A}$, $v_{\text{con}B}$, $v_{\text{con}C}$, and $v_{\text{con}D}$ are for representing terminal voltages of the phase-legs, whose expressions and those of terminal currents of the MFC in Fig. 8(a) can be derived as

$$\begin{cases} v_{\text{con}A} = v_a - L_g \frac{di_a}{dt} + \text{offset} \\ v_{\text{con}B} = v_b - L_g \frac{di_b}{dt} + \text{offset} \\ v_{\text{con}C} = v_c - L_g \frac{di_c}{dt} + \text{offset} \\ v_{\text{con}D} = v_{C\text{ac}} + v_{\text{con}C} + L_f \frac{di_{C\text{ac}}}{dt} \end{cases} \tag{18}$$

$$\begin{cases} i_{a\_\text{in}} = i_a \\ i_{b\_\text{in}} = i_b \\ i_{c\_\text{in}} = i_c + i_{C\text{ac}} \\ i_{d\_\text{in}} = -i_{C\text{ac}} \end{cases} \tag{19}$$

where offset is

$$\text{offset} = \frac{-(v_a + v_b + v_c)}{3}. \tag{20}$$

To avoid over-modulation, the minimum dc-link voltage must then be higher than the maximum peak-to-peak value among the four controlled voltages computed using (18). Meanwhile, the highest current stress should be determined by considering i_{c_in} in (19), where an extra current from the decoupling capacitor has been added. This capacitive current is, in turn, related to the capacitive voltage $v_{C\text{ac}}$ in (8), where there are two acceptable,

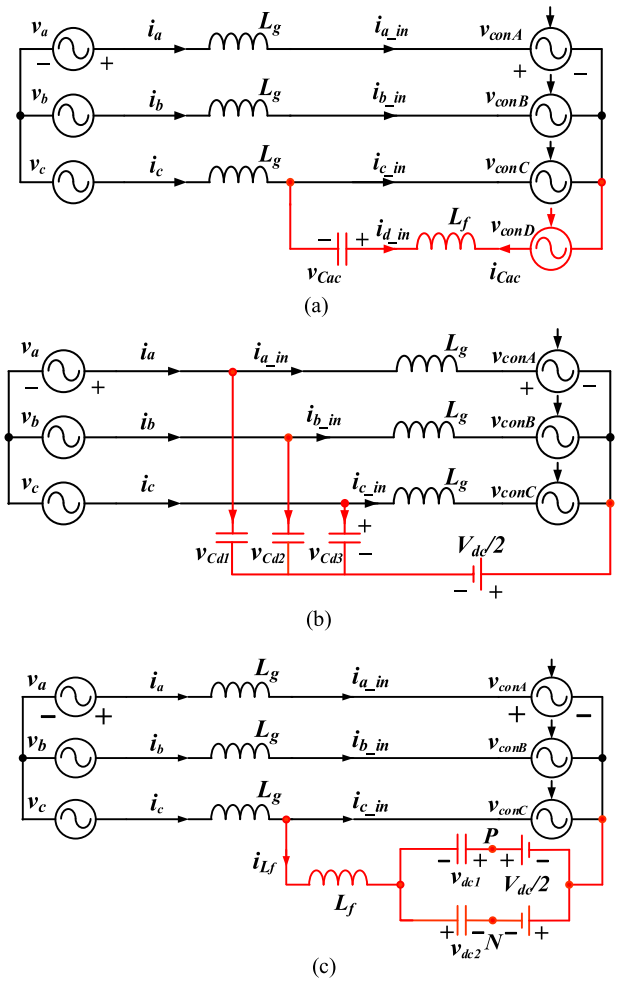


Fig. 8. Equivalent circuits of (a) MFC, (b) DBC, and (c) SCC.

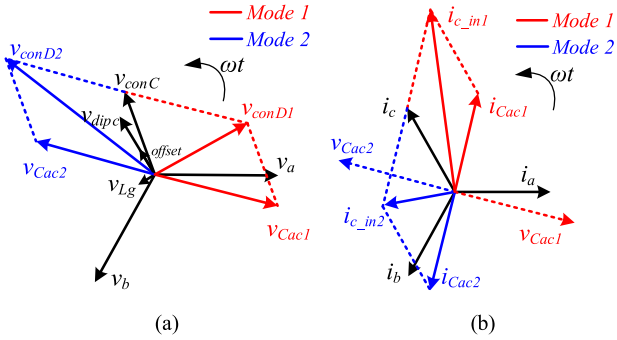


Fig. 9. Phasor diagrams showing (a) voltages and (b) currents of the MFC subjected to type-B voltage unbalance.

but different angles. There are, hence, two different modes to consider, as illustrated by phasor diagrams in Fig. 9 for type-B voltage unbalance and the "worst case" of phases A and B being symmetrical along the axis of phase C.

Starting with Fig. 9(a), v_a, v_b, and v_{dipc} are the unbalanced grid voltages, while v_{Cac1} and v_{Cac2} are the two capacitive voltages with the same magnitude, but different angles. They yield two different terminal voltages $v_{\text{con}D1}$ and $v_{\text{con}D2}$ for phase-leg D with the former having a smaller magnitude. The smaller $v_{\text{con}D1}$ then gives rise to the larger i_{c_in1} in Fig. 9(b), while $v_{\text{con}D2}$ yields i_{c_in2} in the same figure. It is, therefore, not possible to have smaller $v_{\text{con}D}$ and i_{c_in} simultaneously to lessen losses. An objective must, hence, be defined, which may probably be to lower dc-link voltage to better suit renewable sources and electronic loads. The combination of $v_{\text{con}D1}$ and i_{c_in1} is, thus, preferred for the MFC and must be used for deciding the minimum dc-link voltage and minimum switch current rating.

As for the DBC, because of its symmetry, each voltage unbalance can be analyzed without considering which two phases are symmetrical along the axis of the third phase, as seen in Fig. 7. Moreover, as deduced from (12), the DBC can only have one unique capacitive voltage, and hence only one operating mode. Equivalent circuit for analyzing this operating mode is shown in Fig. 8(b), from which terminal voltages and currents of the controlled sources can be determined as (21) and (22). The minimum dc-link voltage must then be higher than the maximum peak-to-peak value among all controlled sources represented in (21). At the same time, the minimum current rating of switches must be higher than the maximum peak value among all terminal currents in (22)

$$\begin{cases} v_{\text{con}A} = v_{Cd1} - L_g \frac{di_{a\_\text{in}}}{dt} - \frac{V_{\text{dc}}}{2} \\ v_{\text{con}B} = v_{Cd2} - L_g \frac{di_{b\_\text{in}}}{dt} - \frac{V_{\text{dc}}}{2} \\ v_{\text{con}C} = v_{Cd3} - L_g \frac{di_{c\_\text{in}}}{dt} - \frac{V_{\text{dc}}}{2} \end{cases} \tag{21}$$

$$\begin{cases} i_{a\_\text{in}} = i_a - C_d \frac{dv_{Cd1}}{dt} \\ i_{b\_\text{in}} = i_b - C_d \frac{dv_{Cd2}}{dt} \\ i_{c\_\text{in}} = i_c - C_d \frac{dv_{Cd3}}{dt}. \end{cases} \tag{22}$$

The same procedure can be repeated with the SCC, whose equivalent circuit is shown in Fig. 8(c). Terminal voltages and currents of the controlled sources in the equivalent circuit can then be determined as (23) and (24). The former informs that terminal voltages of controlled sources A and B are each equal to the sum of line-to-line grid voltage, terminal voltage of controlled source C, and inductive voltage across L_g. Terminal voltage of controlled source C is, in turn, equal to the sum of decoupling capacitive voltage, voltage across L_f, and a dc component. Terminal voltages of the SCC will, hence, be larger than those of a standard three-phase converter

$$\begin{cases} v_{\text{con}A} = v_a - v_c + v_{\text{con}C} + L_g \frac{d(i_c - i_a)}{dt} \\ v_{\text{con}B} = v_b - v_c + v_{\text{con}C} + L_g \frac{d(i_c - i_b)}{dt} \\ v_{\text{con}C} = v_{\text{dc}2} + L_f \frac{di_{Lf}}{dt} - \frac{V_{\text{dc}}}{2} \end{cases} \tag{23}$$

$$\begin{cases} i_{a\_\text{in}} = i_a \\ i_{b\_\text{in}} = i_b \\ i_{c\_\text{in}} = i_c - i_{Lf}. \end{cases} \tag{24}$$

To illustrate, voltage and current phasor diagrams of the SCC are drawn in Fig. 10 with the earlier type-B voltage unbalance again considered as an example. Furthermore, from (17), there are two different values, which voltage v_{dc2} of the lower decoupling capacitor in Fig. 8(c) can assume. They lead to two different terminal voltages for phase-leg D, notated as $v_{\text{con}C1}$ and $v_{\text{con}C2}$. Two operating modes associated with them can, thus, be drawn, as in Fig. 10(a), where $v_{\text{con}A1}$ and $v_{\text{con}B1}$ are terminal voltages of controlled sources A and B due to $v_{\text{con}C1}$.

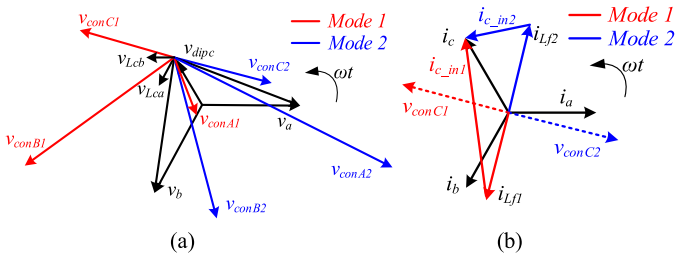


Fig. 10. Phasor diagrams showing (a) voltages and (b) currents of the SCC subjected to type-B voltage unbalance.

Voltages $v_{\text{con}A2}$ and $v_{\text{con}B2}$ are then terminal voltages of the same controlled sources due to $v_{\text{con}C2}$. Besides those, other voltages marked in the figure are $v_{Lca} = L_g d(i_c - i_a)/dt$ and $v_{Lcb} = L_g d(i_c - i_b)/dt$ extracted from (23).

Voltages in Fig. 10(a) then lead to currents in Fig. 10(b), where the highest terminal current is from controlled source C, marked as i_{c_in1}. This highest current is associated with $v_{\text{con}C1}$, $v_{\text{con}A1}$, and $v_{\text{con}B1}$, which being shorter phasors will demand a smaller dc-link voltage. Therefore, like the MFC, it is not possible to demand a lower dc-link voltage and current stress simultaneously under most grid voltage unbalanced conditions, as shown in Fig. 10. A tradeoff is, hence, necessary, which, like the MFC, is to opt for a smaller dc-link voltage, which most renewable sources and electronic loads may require. The chosen decoupling capacitive voltage for the SCC should, hence, have an ac component represented by $v_{\text{con}C1}$.

C. Voltage and Current Stress Comparison

Terminal voltages and currents of the power-decoupled converters have now been defined. They can progressively be used for determining the minimum dc-link voltage and switch current rating, which must, respectively, be higher than the maximum peak-to-peak terminal voltage and peak terminal current. The determined minimum values may then be normalized as indexes for comparing the converters over a common scale. These indexes are defined as follows.

1) *DC voltage index (VI):* Minimum dc-link voltage required by power-decoupled converter normalized with that required by a standard three-phase converter with an ideal infinite dc-link capacitance.
2) *Current index (CI):* Minimum switch current rating of power-decoupled circuit normalized with magnitude of balanced grid currents.

Their mathematical expressions can, thus, be expressed as

$$VI = \text{Max}\left[\frac{V_{p-pi}}{2\sqrt{2}V_g}\right]\begin{cases} i = A, B, C, \text{and } D & MFC \\ i = A, B, \text{and } C & DBC \\ i = A, B, \text{and } C & SCC \end{cases} \quad (25)$$

$$CI = \text{Max}\left[\frac{I_{\text{peak}i}}{\sqrt{2}I_g}\right]\begin{cases} i = C & MFC \\ i = A, B, \text{and } C & \text{DBC} \\ i = C & \text{SCC} \end{cases} \quad (26)$$

where V_{p-pi} is the peak-to-peak value of terminal voltage $v_{\text{con}i}$ produced by the considered phase-leg, V_g is the balanced root mean square (rms) grid voltage before fault, $I_{\text{peak}i}$ is the peak of terminal current i_{i_in}, and I_g is the balanced rms grid current.

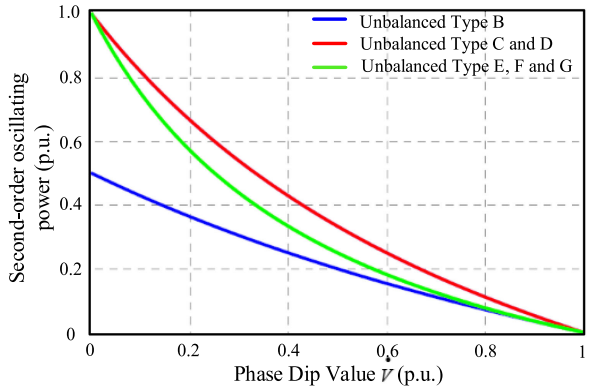


Fig. 11. Relationship between the second-order oscillating power and phase dip value under unbalanced types B–G.

Furthermore, it is important to compare the three converters with the same parameters, which, in this work, have been set as 110 V [1 per unit (p.u.)] for the prefault grid voltage, 1 kW (1 p.u.) as the common rated power with unity power factor, and an always equal total capacitance summed from decoupling and dc-link capacitances. This common total capacitance can, in turn, be varied for studying its impact on power decoupling without affecting the amount of second-order oscillating power generated at the ac grid side of the converter.

In other words, the oscillating power can always be computed using (5) regardless of capacitance, which, when applied to types B–G voltage unbalances in Table I, yields those power curves in Fig. 11, in terms of voltage-dip magnitude V. The figure, together with earlier explained equations in (5), (6), (8), (11)–(13), (15), and (17)–(26), can then be used for plotting VI and CI of the three converters, as V varies. Traces obtained with type-B voltage unbalance are shown in Fig. 12, while those with other unbalanced types are documented in the Appendix. Regardless of that, key ranges of VI and CI for all converters with a total capacitance of 120 μF each are given in Table II, together with their other qualitative features.

The table unquestionably indicates that VI and CI of the SCC are the highest among all converters. They must be at least 1.9 and 1.85 p.u., in order to ride-through all voltage unbalances with a total capacitance of 120 μF. The MFC, on the other hand, achieves the lowest VI of 1.2 p.u. with the same total capacitance, but its CI of 1.7 p.u. is unfavorably high. Therefore, the most attractive topology is likely the DBC, whose VI and CI are 1.25 and 1.2 p.u., respectively. In other words, the minimum dc-link voltage and switch current rating demanded by the DBC must be 25% and 20% higher than those of a standard converter, in order to decouple properly, while maintaining balanced grid currents. It should, however, be re-emphasized that an ideal infinite dc-link capacitance has been assumed with the standard converter when defining VI. This is certainly not realistic. Deviations from the ideal have, hence, been discussed in the next section, which, when viewed holistically, will further strengthen the advantages of the DBC.

Meanwhile and where necessary, VI values of all converters can be lowered by increasing decoupling capacitance, and hence a smaller voltage across it for absorbing oscillating power. A smaller increase in dc-link voltage is, thus, needed for generating the capacitive voltage. However, CI values of all converters increase with decoupling capacitance, which now carries a

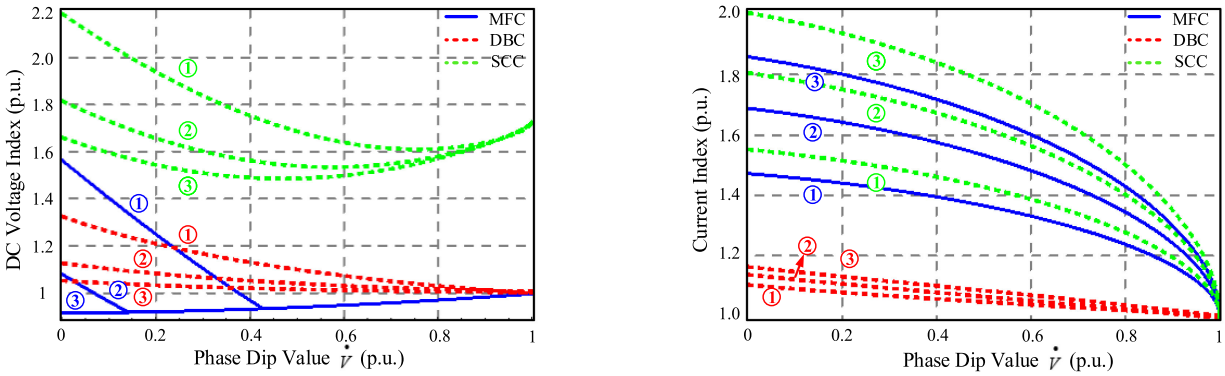


Fig. 12. Indexes of three-phase power-decoupled converters under type-B voltage unbalance with total capacitance of ① 60 μF, ② 120 μF, and ③ 180 μF.

TABLE II
SUMMARY OF FEATURES AND PERFORMANCE INDEXES OF THREE POWER-DECOUPLED CONVERTERS

Topology structure		Topology 1: MFC	Topology 2: DBC	Topology 3: SCC
Extra switches with antiparallel diodes		2	0	0
DC voltage quality		Almost constant	Almost constant	Almost constant
AC grid current quality		Balanced sinusoidal	Balanced sinusoidal	Balanced sinusoidal
Control implementation		Fig. 3(b)	Fig. 4(b)	Fig. 5(b)
Decoupling capacitance		1 capacitor of 90 μF	3 capacitors of 30 μF each	2 capacitors of 60 μF each
DC-link capacitance		30 μF	30 μF	---
DC voltage Index (p.u.)	Balanced Type A	Less than 1.0	Less than 1.0	Less than $\sqrt{3}$
	Unbalanced Type B	0.85 ~ 1.1	1.0 ~ 1.15	1.50 ~ 1.85
	Unbalanced Type C	1.0 ~ 1.2	1.0 ~ 1.25	1.35 ~ 1.8
	Unbalanced Type D	0.85 ~ 1.05	1.0 ~ 1.15	1.55 ~ 1.9
	Unbalanced Type E	0.9 ~ 1.1	0.85 ~ 1.0	1.25 ~ 1.8
	Unbalanced Type F	0.75 ~1.0	0.9 ~ 1.0	1.35 ~ $\sqrt{3}$
	Unbalanced Type G	0.9 ~ 1.1	0.85 ~ 1.0	1.25 ~ 1.8
Current index (p.u.)	Balanced Type A	1.0	1.0	1.0
	Unbalanced Type B	1.0 ~ 1.7	1.0 ~ 1.2	1.0 ~ 1.8
	Unbalanced Type C	0.25 ~ 1.0	1.0 ~ 1.2	0.25 ~ 1.0
	Unbalanced Type D	1.0 ~ 1.7	1.0 ~ 1.2	1.0 ~ 1.85
	Unbalanced Type E	0.4 ~ 1.0	1.0 ~ 1.2	0.3 ~ 1.0
	Unbalanced Type F	1.0 ~ 1.5	1.0 ~ 1.2	1.0 ~ 1.6
	Unbalanced Type G	0.4 ~ 1.0	1.0 ~ 1.2	0.3~ 1.0

larger capacitive current. This capacitive current flows through the converter, which must, hence, have a higher current rating. Despite that, it has been noticed that capacitive currents of the DBC are much smaller than the balanced grid currents. According to Fig. 8(b), terminal currents flowing through semiconductors of the DBC will, hence, be dominated by the grid currents. This explains why CI of the DBC does not vary a lot in Fig. 12, as the decoupling capacitance changes. It has also not varied much, as the dip magnitude V changes, according to Table II. The range has, in fact, stayed almost unchanged between 1.0 and 1.2 p.u. for all voltage unbalances.

D. Three-Phase Versus Single-Phase

Power decoupling has mostly been associated with single-phase converters, whose purpose is to continuously divert oscil-

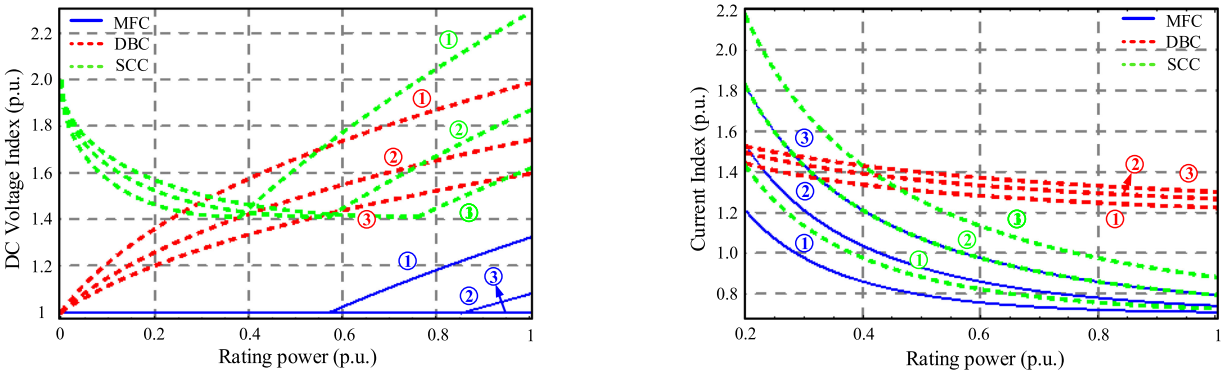


Fig. 13. Indexes of single-phase power-decoupled converters with total capacitance of ① 200 μF, ② 300 μF, and ③ 400 μF.

lating power away from their dc links. Their components have, hence, been mostly sized for nominal operating conditions. Related sizing requirements are now evaluated for comparison with those demanded by intermittent three-phase power decoupling for power quality improvement. To do that, power-decoupled converters in Figs. 3–5 are reconsidered, whose single-phase implementations simply do not include switches $Q1$ and $Q2$, and their associated passive components. Their VI and CI with a grid voltage of 110 V or 1 p.u. are then plotted in Fig. 13, where it can be seen that VI of the MFC is far lower than those of the other two topologies at close to nominal power of 1 kW or 1 p.u. Its value can indeed be lowered to unity by increasing the decoupling capacitance. When that happens, it simply means minimum dc voltage demanded by the MFC is the same as that demanded by a standard full-bridge inverter with an ideal infinite capacitance.

As for CI, MFC and SCC have smaller values that fall below unity over a wide power range. Unfortunately, for the SCC, its VI and, hence, minimum dc-link voltage are the highest. Therefore

1) For continuous single-phase operation, the MFC has the best operating advantages, but it uses more switches than the others. A tradeoff may, hence, be unavoidable.
2) For intermittent online three-phase operation, the DBC has clear operating advantages, while using the same number of switches as a standard three-phase converter. It should, hence, be recommended for riding through all voltage unbalances, rather than the other two converters.

V. Standard Converter Versus DBC and Other Power-Related Issues

Upon identifying the DBC as the preferred online power-decoupled converter, it should now be thoroughly compared with a standard converter to better convince that three-phase power decoupling should generally be encouraged in practice. This is especially so, since it provides power quality enhancement, and where necessary, reactive power support when riding through a fault. Both capabilities have also been described here.

A. Standard Converter With Balanced Grid Currents

A standard three-phase converter can be derived from the DBC by removing only its zero-sequence line marked in Fig. 4(a). Both converters are, thus, closely similar, and both may have additional grid inductances included for forming *LCL* filters, where necessary. Inclusion of grid inductances will, however, not impact their comparison, which, in sequence, may start by keeping their total capacitances the same at 120 μF. For the DBC, its specific values are $C_{di} = C_{\rm dc} = 30$ μF according to Table II, where $i = 1$, 2, and 3 are for notating the three ac phases. But, for the standard converter, notated with subscript ST from here on, because its C_{di_ST} does not store second-order oscillating power, its value may be lowered to 5 μF to roughly provide a reactive capacity of 5% of the rated power [43], [44]. Capacitive current through C_{di_ST} is, thus, insignificant, implying that current rating of the semiconductor switches can solely be determined by magnitude of the balanced grid currents. In other words, CI of the standard converter is close to 1, as compared to 1.2 for the DBC.

The extra 25 μF per phase from C_{di_ST} of the standard converter may then be added to $C_{\rm dc\_ST}$ to give a higher 105 μF for better dc-link filtering. Despite that, a second-order oscillating voltage component will still appear across $C_{\rm dc\_ST}$ of the standard converter, if its grid currents continue to be balanced during an unbalanced grid fault. A peak dc-link voltage, thus, exists, which will, hence, raise ratings of semiconductors of the standard converter. Expression for this peak can be derived as

$$V_{\rm dc\_pk\_ST} = 2\sqrt{2}V_g + 2 \times (2\sqrt{2}\gamma_{\rm ST}V_g) \tag{27}$$

where $V_{\rm dc\_min\_ST} = 2\sqrt{2}V_g$ represents the minimum dc-link voltage of the standard converter, when its dc-link capacitance is infinite, as earlier assumed with VI in (25). Also involved in (27) is $\gamma_{\rm ST}$ for representing the ratio of oscillating voltage magnitude in the parentheses, in terms of $V_{\rm dc\_min\_ST}$.

By next differentiating to find the dc capacitive current and performing some simple multiplications, magnitude of the second-order oscillating power absorbed by $C_{\rm dc\_ST}$ of the standard converter can be derived as

$$P_{C{\rm dc\_2}\omega{\rm \_ST}} = 16\gamma_{\rm ST}(1+\gamma_{\rm ST})\omega C_{\rm dc\_ST}V_g^2 = \aleph_{\rm ST}P_{2\omega{\rm \_worst}} \tag{28}$$

where $P_{2\omega{\rm \_worst}} = 1$ kW is the worst-case oscillating power magnitude read in Fig. 11, and $\aleph_{\rm ST}$ is its fractional amount flowing through $C_{\rm dc\_ST}$, while the remainder flows through the dc load. Substituting $P_{2\omega{\rm \_worst}} = 1$ kW, $C_{\rm dc\_ST} = 105$ μF, and $V_g = 110$ V into (28) then results in

$$\gamma_{\rm ST}^2 + \gamma_{\rm ST} - 0.1566\aleph_{\rm ST} = 0 \tag{29}$$

where $\aleph_{ST}$ depends on the type of dc load, and a higher $\aleph_{ST}$ generally leading to a higher γ_{ST} or oscillating voltage component in (27).

Assuming now that $\aleph_{ST} = 0.85$ (85% of oscillating power filtered by C_{dc_ST}) as a numerical example, γ_{ST} can be computed as 0.1190, which, from (27), corresponds to an oscillating dc-link voltage with a peak of 1.238 $V_{dc\_min\_ST}$. This peak is, thus, comparable to the constant dc-link voltage of 1.25 $V_{dc\_min\_ST}$ demanded by the DBC, as read from Table II. In other words, both standard converter and DBC with the same total capacitance will demand the same voltage rating for their semiconductors. However, with the standard converter, its sizable second-order oscillating voltage may be a power quality concern to sensitive sources and loads connected to its dc link.

To avoid the concern, the most straightforward approach is to increase C_{dc_ST} of the standard converter, which, ideally, should be infinite to reduce γ_{ST} to zero. This is not realizable in practice, meaning a small amount of oscillating voltage will always exist. Because of that, γ_{ST} may be set to 1% as a numerical example, and with a large C_{dc_ST}, $\aleph_{ST} \rightarrow 100\%$ may be assumed. Those values, after substituting into (28) and (27), yield $C_{dc_ST} = 1628\ \mu$F with a peak voltage of 1.02 $V_{dc\_min\_ST}$ across it. No doubt, it represents a significant improvement in voltage quality, but at the cost of C_{dc_ST} being around 54 times larger than $C_{dc} = 30\ \mu$F of the DBC. Whether such a large dc-link capacitance is acceptable depends generally on whether it requires series–parallel connection of smaller physical capacitors. As described in [45], any series–parallel connection of mostly electrolytic capacitors may require voltage-equalizing resistors and may be prone to failure, if a single capacitor becomes shorted. These issues are less burdensome with the DBC, whose only topological difference is the addition of a zero-sequence line to the standard converter, as indicated in Fig. 4(a).

B. Standard Converter With Constant Power

Instead of balanced grid currents during fault, Shabestary *et al.* [27]–[31] have suggested an alternative set of unbalanced grid currents for keeping the generated power constant, and hence no dc-link oscillating voltage for the standard converter. The tradeoff is unrealistically high grid currents. To illustrate, type-B voltage unbalance can again be assumed, which, according to Fig. 7 and Table I, involves the shortening of a voltage phasor from unity to V. Its angle and the other two voltage phasors are, however, unchanged. Power generated can, hence, be maintained constant by lengthening current phasor of the affected phase only. The factor of increase is $1/V$, which, in case of a severe voltage sag, may become excessive. It may, thus, be difficult for a standard converter to ride-through all voltage unbalances, if its generated power is to be always kept constant.

C. Power Decoupling Within Power Quality Enhancement

Involvement of three-phase power decoupling during short-term power quality enhancement may generally be not too obvious, since power decoupling has mostly been presented with a single-phase converter during its continuous operation. This involvement can better be projected now by borrowing the DVR [46], [47], an established power quality enhancer, as an illustrative example. Its single-line diagram is shown in Fig. 14, which, during the normal grid condition, may have either the DVR bypassed or generating zero fundamental voltage. The DVR only responds upon sensing a grid-voltage dip, which, in most instances, is caused by an unbalanced fault. The DVR then injects a set of series unbalanced voltages, which, when summed with the grid voltages, will keep the load voltages, and hence its currents, unchanged at their prefault balanced conditions. The load can, therefore, continue its normal operation without having to deal with second-order oscillating power.

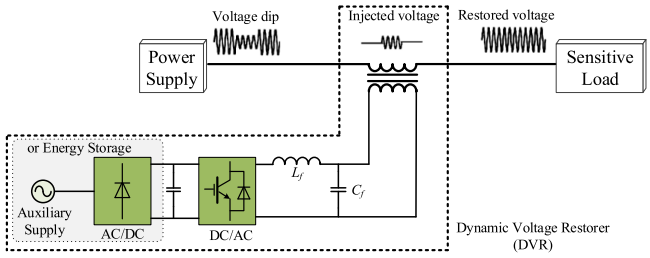


Fig. 14. Single-line diagram of the DVR for demonstrating implicit power decoupling.

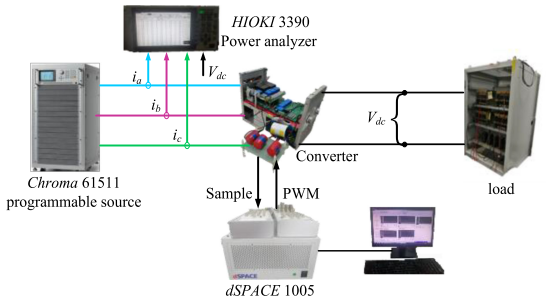


Fig. 15. Experimental setup for verifying power-decoupled converters.

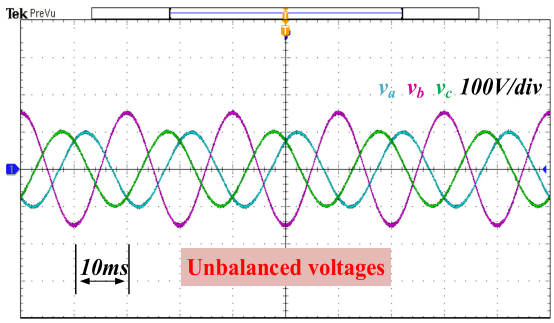


Fig. 16. Unbalanced grid voltages for experimental testing.

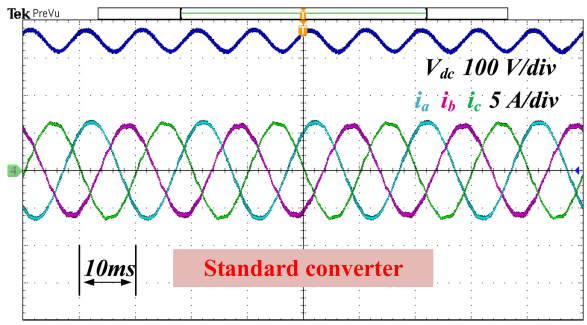
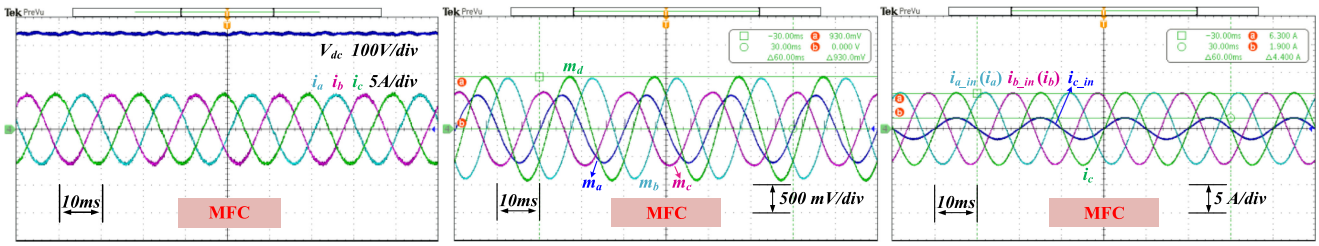


Fig. 17. Experimental grid currents and dc-link voltage from a standard converter.

TABLE III
KEY PARAMETERS

Topology	*Standard*	*MFC*	*DBC*	*SCC*
DC voltage , V_{dc}	350 V	350 V	350 V	450 V
Switching frequency, f_s	10 kHz	10 kHz	10 kHz	10 kHz
DC-link capacitance, C_{dc}	50 μF	50 μF	50 μF	------
Decoupling capacitance, C_{ac}	------	100 μF	30/30/30 μF	100/100 μF
Total capacitance	50 μF	150 μF	140 μF	200 μF
Unbalanced type	C	C	C	C
Voltage-dip magnitude V	0.5	0.5	0.5	0.5
VI and CI in theory	------	1.05 and 0.305	1.095 and 1.135	1.36 and 0.305
Grid voltage A, v_a	73.7∠19°	73.7∠19°	73.7∠19°	73.7∠19°
Grid voltage B, v_b	110∠240°	110∠240°	110∠240°	110∠240°
Grid voltage C, v_c	73.7∠101°	73.7∠101°	73.7∠101°	73.7∠101°
Grid inductance, L_g	8 mH	8 mH	8 mH	8 mH
Filter inductance, L_f	------	1 mH	------	1 mH
Nominal power, P_n	1 kW	1 kW	1 kW	1 kW



(a) (b) (c)

Fig. 18. Experimental (a) dc-link voltage and ac grid currents, (b) modulating references, and (c) terminal currents of the MFC.

The balanced load currents, however, flow through the grid and DVR, which both have unbalanced terminal voltages. Second-order oscillating power is, hence, generated by the grid, but instead of reaching the load, it is decoupled and diverted to the DVR during the short fault duration. Power decoupling is, thus, an implicit mechanism of power quality enhancement, regardless of whether it is for protecting an ac load with a DVR or a dc load with the DBC.

D. Injection of Reactive Power

When riding through a fault, reactive power support may sometimes be recommended, which both standard converter and DBC can achieve with almost matching performances, because of their topological closeness. The only topological difference between them is, in fact, the zero-sequence line in Fig. 4(a) used only by the DBC. This line provides a path for second-order zero-sequence currents to flow between the ac capacitances C_{di} ($i = 1$, 2, and 3) and six-switch converter bridge, so that second-order oscillating power does not progress to the dc link. It, thus, has no influence on reactive power support provided to the grid. On the other hand, if the DBC has been operated as a transformer-less photovoltaic (PV) converter, the added zero-sequence line may provide a low-impedance path for high-frequency common-mode currents to flow. Otherwise, they will leak through stray capacitances between each PV panel and ground, before returning through the grounded grid. These phenomena do not need additional control, as have been demonstrated in [48], even though with only a single-phase DBC.

VI. EXPERIMENTAL RESULTS

To verify practicalities of the three power-decoupled converters, an experimental setup, with main parameters listed in Table III, has been developed, as shown in Fig. 15. The setup has been connected to a *Chroma* 61511 programmable source for emulating the ac grid, while its control has been implemented with a *dSPACE* 1005 controller. Its generated voltage and current harmonics have subsequently been measured with a *HIOKI* 3390 power analyzer, when tested with those type-C unbalanced voltages in Fig. 16. Type-C unbalanced voltages have been considered here merely because they result in smaller currents that can be tolerated by the experimental converters. Their associated results are now described, as follows.

Beginning with Fig. 17, it shows balanced grid currents and a dc-link voltage distorted by second-order ripple from a standard three-phase converter. These are expected, since balanced grid currents and a smooth dc-link voltage can only be achieved through power decoupling, like in Figs. 18(a), 19(a), and 20(a) for the three power-decoupled converters. Quantification of their improvements can also be read in Fig. 21(a) and (b). The former shows second-order dc-link voltages of the three power-decoupled converters being all below 0.15%, as compared to 6.3% of the standard converter. The latter reinforces by verifying that ac grid current harmonics up to the 15th order are all below 1%, while their summed total harmonic distortions (THDs) are all approximately 2.0%.

Next, to validate minimum VIs and CIs of the three power-decoupled converters, other useful waveforms generated by

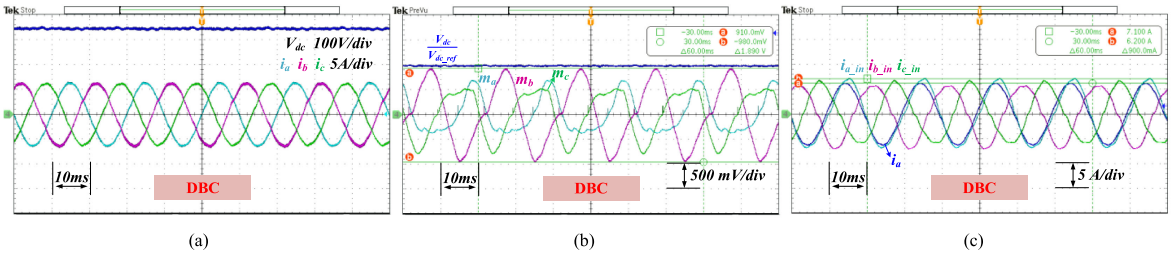


Fig. 19. Experimental (a) dc-link voltage and ac grid currents, (b) modulating references, and (c) terminal currents of the DBC.

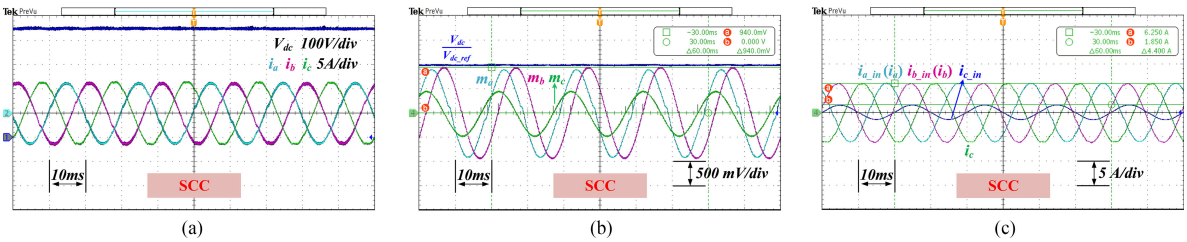


Fig. 20. Experimental (a) dc-link voltage and ac grid currents, (b) modulating references, and (c) terminal currents of the SCC.

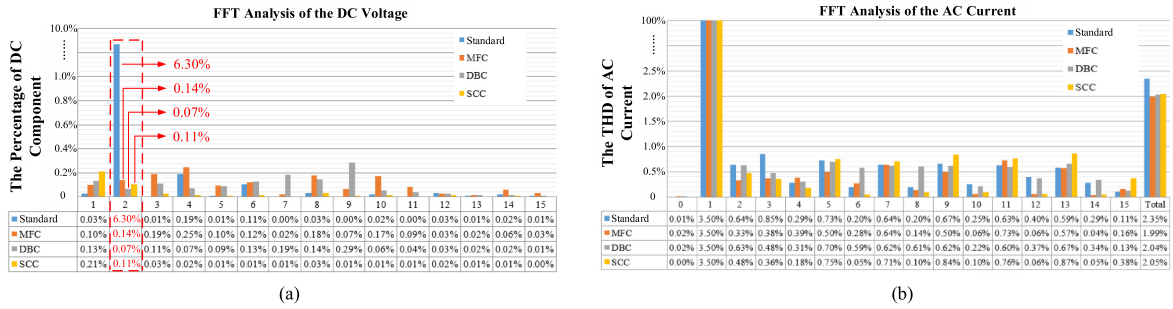


Fig. 21. Spectrums of (a) dc-link voltages and (b) ac grid currents of the standard and power-decoupled converters.

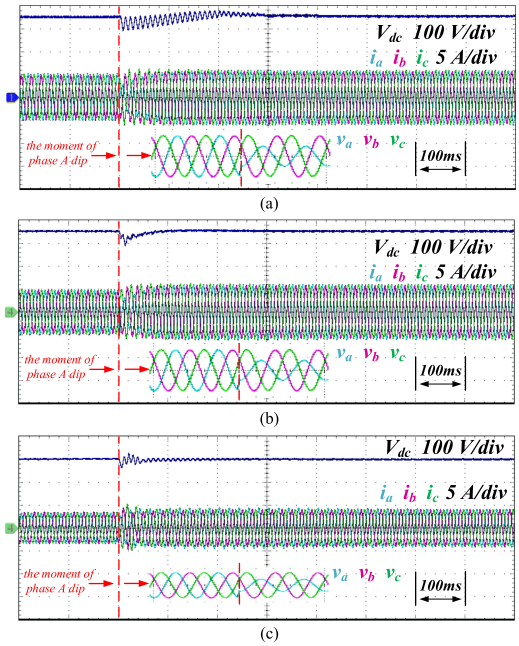


Fig. 22. Experimental dynamic responses of (a) MFC, (b) DBC, and (c) SCC.

TABLE IV
TURNAROUND TIMES NEEDED FOR CONTROL CODE EXECUTIONS

Topology	*Standard*	*MFC*	*DBC*	*SCC*
Turnaround time (μs)	16.5	18.69	17.20	18.03
Percentage difference compared with standard	0	13.3%	4.24%	9.27%

them are discussed. But, before doing so, it should be clarified that total capacitances used with the three converters are not exactly the same, because of limited capacitance values available commercially. Their specific values are given in Table III, which, with a dip of $V = 0.5$, give rises to those theoretically determined VI and CI values in the same table. Furthermore, because $v_{\text{con}A}$, $v_{\text{con}B}$, $v_{\text{con}C}$, and $v_{\text{con}D}$ in Fig. 8 represent actual switched terminal voltages of phase-legs, they cannot be measured for calculating VIs experimentally. Therefore, modulating references for the phase-legs are plotted instead, together with terminal currents i_{a_in}, i_{b_in}, and i_{c_in} flowing through the phase-legs. It should, moreover, be noted that switching noises of the terminal currents have been removed by the scope to better show their respective peaks.

Related results are then documented in Fig. 18(b) and (c) for the MFC, Fig. 19(b) and (c) for the DBC, and Fig. 20(b) and (c) for the SCC. Their experimentally determined indexes

are $\text{VI} = m_d * \frac{V_{\text{dc}}}{2\sqrt{2}V_g} = 0.93 * 350/311 \approx 1.047$ and $\text{CI} = \frac{I_{\text{peakC}}}{\sqrt{2}I_g} = 1.9/6.3 \approx 0.302$ for the MFC, $\text{VI} = \frac{\Delta m_b}{2} * \frac{V_{\text{dc}}}{2\sqrt{2}V_g} = 1.89/2 * 350/311 \approx 1.064$ and $\text{CI} = \frac{I_{\text{peakA}}}{\sqrt{2}I_g} = 7.1/6.2 \approx 1.145$ for the DBC, and $\text{VI} = m_b * \frac{V_{\text{dc}}}{2\sqrt{2}V_g} = 0.94 * 450/311 \approx 1.36$ and $\text{CI} = \frac{I_{\text{peakC}}}{\sqrt{2}I_g} = 1.85/6.25 \approx 0.296$ for the SCC. They are, thus, in a close agreement with those theoretical values listed in Table III. Additionally, by measuring with the *HIOKI* 3390 power analyzer, efficiencies of the MFC, DBC, and SCC are read as 92%, 93%, and 93%, respectively, when operating with those type-C unbalanced voltages shown in Fig. 16. They are, thus, slightly lower than 94% measured with the standard three-phase converter during the same voltage unbalance

For the MFC, its lower efficiency may further be attributed to losses of its extra phase-leg in Fig. 3(a), even during the balanced condition, if it is realized as an online solution. This explanation is, however, not applicable to both DBC and SCC, whose extra losses are contributed by extra current components, rather than hardware. For the DBC, it is due to second-order zero-sequence currents flowing between C_{di} and the converter bridge in Fig. 4(a). These currents, however, do not exist during the normal voltage condition. Normal efficiencies of the DBC and standard converter are, thus, very close, since they match closely in terms of topology and most component ratings. Extra current components also exist in the SCC, but at the fundamental frequency, and flow through both dc-link C_f in Fig. 5(a). These extra currents again do not flow during the normal voltage condition, but the much higher minimum dc-link voltage of the SCC may still compromise its efficiency.

As for their dynamic responses, Fig. 22(a) and (b) shows waveforms obtained with the MFC and DBC, when their common phase A voltage drops from 110 to 55 V. These voltage values are, however, not used with the SCC, since they will need a high dc-link voltage of 539 V, which the experimental setup cannot sustain. A different drop of phase A voltage from 60 to 30 V has, thus, been tested to keep dc-link voltage of the SCC at 300 V in Fig. 22(c). Regardless of that, the drop causes second-order voltage ripple to surface at the dc link of each converter. For the MFC and SCC, their ripples are attenuated 0.3 s later, while for the DBC, it is around 0.1 s. During this time, the ac grid currents also increase to keep the output active power constant while remaining balanced (alternatively, power can be reduced to keep the ac grid currents unchanged).

The three power-decoupled converters are, thus, proven to be effective, except the MFC and SCC are dynamically slower. This may be due to their respective shared phase-legs in Figs. 3 and 5, which, when disturbed, will affect both phase C and their decoupling circuits simultaneously. It may, thus, take longer for both MFC and SCC to reach their respective steady states, as verified in Fig. 22. Computational resources wise, both MFC and SCC are also more demanding, according to Table IV, where their experimental turnaround times for control code executions are shown to be longer than others. The cause is their common quarter-wave delay blocks included in Figs. 3(b) and 5(b) for power decoupling. This block is, however, not used by the DBC, which, in turn, has a shorter turnaround time. The shortest turnaround time is nonetheless still retained by the standard converter, since it cannot realize power decoupling, and hence has no extra control code.

VII. Conclusion

Suitable converters for realizing continuous single-phase and online three-phase power decoupling are evaluated. In case of single-phase decoupling, the MFC has been identified as demanding the smallest minimum dc-link voltage and minimum switch current rating. Its minimum dc-link voltage can, in fact, be reduced to that of a standard full-bridge converter by simply choosing a larger decoupling capacitance. Its operating advantages are, thus, unmatched, but it uses two extra switches. On the other hand, online three-phase power decoupling should be activated only during fault, when the grid voltages become unbalanced. Its focus should, hence, be power quality enhancement, rather than usual objectives claimed with single-phase decoupling. Evaluation with all types of voltage unbalances then reveals that the DBC has the best voltage and current characteristics while using no extra hardware and only very slight lengthening of computational time. It is, thus, the preferred topology for online three-phase power decoupling and power quality improvement, while the MFC is a better choice for traditional single-phase decoupling. Future work will, hence, focus only on the three-phase DBC under both unbalanced and distorted grid conditions.

Appendix

Figs. 23–27 show VI and CI of all three power-decoupled converters, subjected to types C–G voltage unbalances. The figures are plotted by varying voltage dip magnitude V listed in Table II.

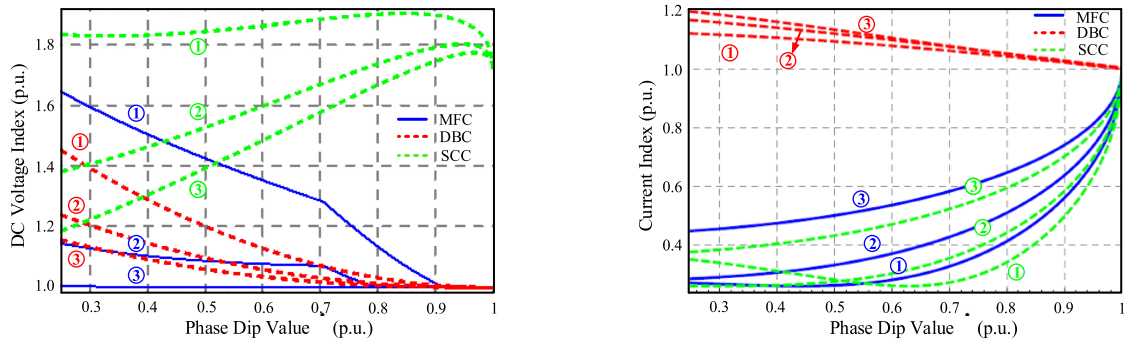


Fig. 23. Indexes of three-phase power-decoupled converters under type-C voltage unbalance with total capacitance of ① 60 μF, ② 120 μF, and ③ 180 μF.

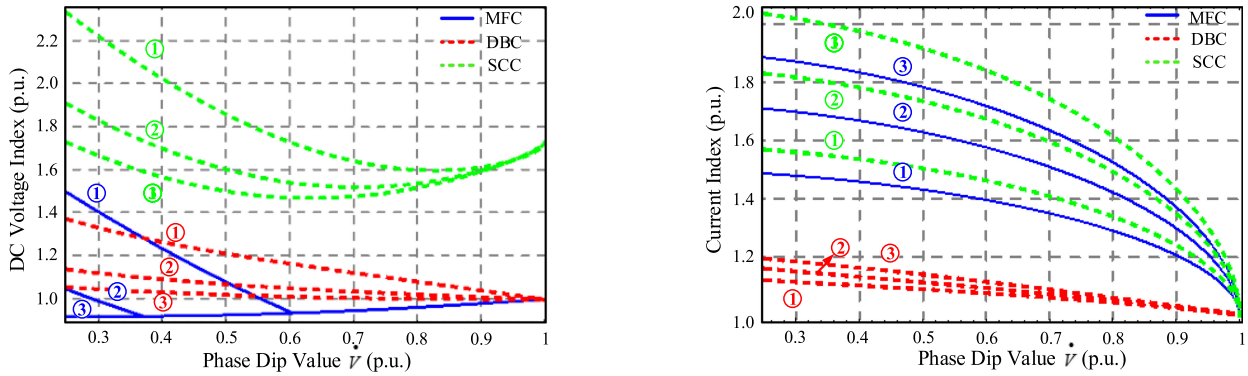


Fig. 24. Indexes of three-phase power-decoupled converters under type-D voltage unbalance with total capacitance of ① 60 μF, ② 120 μF, and ③ 180 μF.

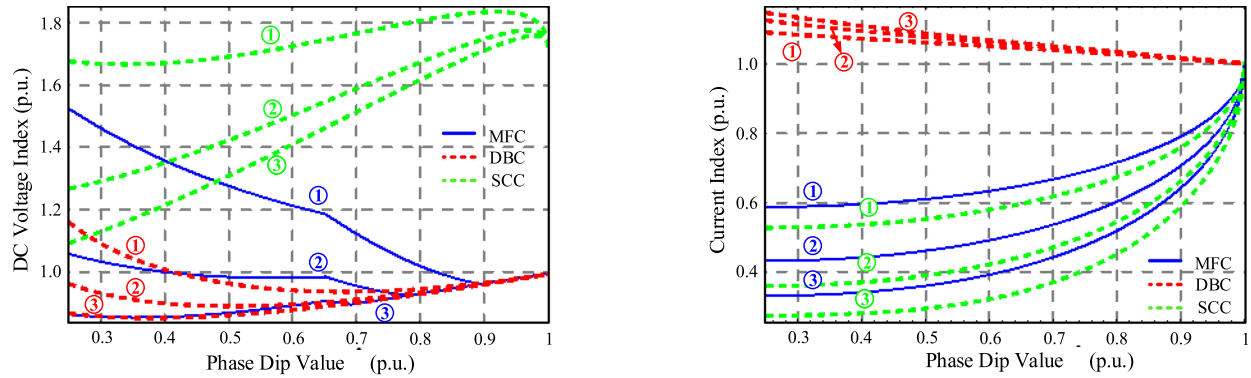


Fig. 25. Indexes of three-phase power-decoupled converters under type-E voltage unbalance with total capacitance of ① 60 μF, ② 120 μF, and ③ 180 μF.

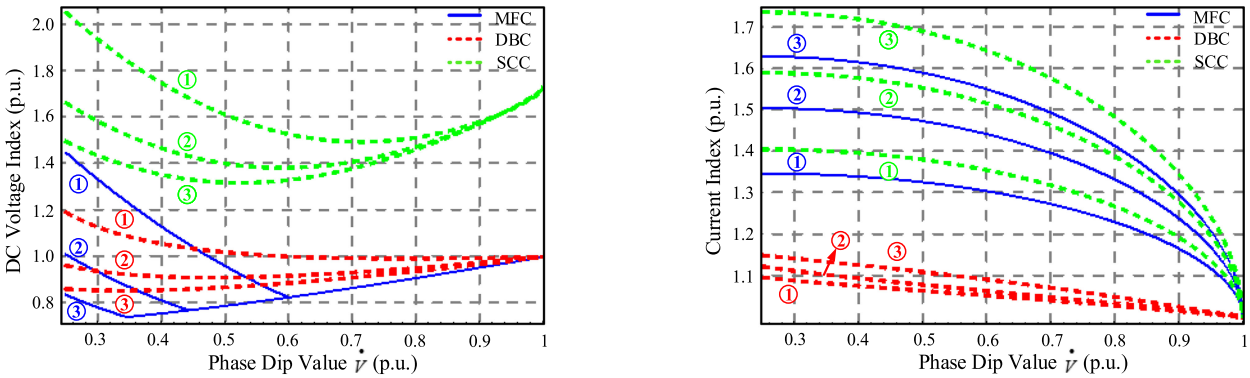


Fig. 26. Indexes of three-phase power-decoupled converters under type-F voltage unbalance with total capacitance of ① 60 μF, ② 120 μF, and ③ 180 μF.

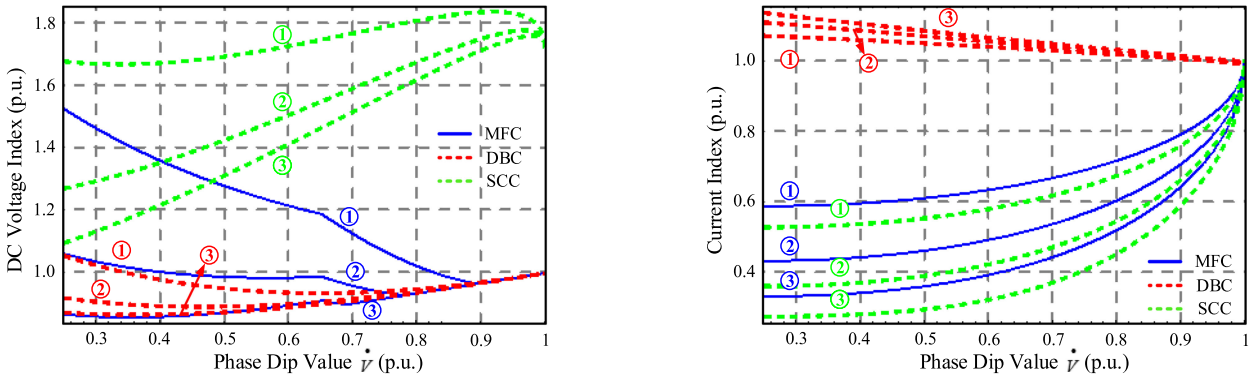


Fig. 27. Indexes of three-phase power-decoupled converters under type-G voltage unbalance with total capacitance of ① 60 μF, ② 120 μF, and ③ 180 μF.

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