Constant ON/OFF-Time Hybrid Modulation in Digital Current-Mode Control Using Event-Based Sampling

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***Abstract*—Ripple-based constant ON-time and OFF-time control techniques can achieve fast step-down and step-up transient performance along with an improved light-load efficiency. However, they suffer from varying switching frequency at the steady state and often require a phase-locked loop for frequency regulation. This paper proposes a constant ON/OFF-time hybrid modulation technique in a digitally current-mode controlled synchronous buck converter. The proposed technique considers an event-based sampling mechanism using one sample per switching cycle, which makes it useful for high-frequency implementation. This requires a monoshot timer and a digital voltage controller $G_c(z)$. The proposed technique can be configured to a constant ON-time or OFF-time modulator with seamless transition because of sharing $G_c(z)$; thus, improved step-up/down transient performance can be retained. Furthermore, a discrete-time framework is proposed for fast-scale stability analysis, and the effects of finite sampling and practical parasitics are discussed. Discrete-time small-signal models are derived for the direct digital control design with enhanced stability and performance. A frequency adaptation method is discussed to customize the switching frequency in real time. A buck converter prototype is tested, and the usefulness of the proposed modulation technique is verified experimentally.**

***Index Terms*—Antiwindup, constant ON-time, current-mode digital control, event-based sampling, OFF-time, robust stability.**

I. Introduction

RIPPLE-BASED constant ON/OFF-time control techniques find widespread applications in dc–dc converters [2]–[14], as they offer fast transient response and an improved light-load efficiency [2]–[6]. They often utilize inherent ripple parameters of a practical dc–dc converter [5]. There are primarily two types of modulators: constant ON-time and constant OFF-time modulators. In addition to the voltage regulator loop, they generally require a ramp compensation, which can be the output voltage ripple [dominated by the effective series resistance (ESR)] [5], the inductor current ripple [10], an estimated current ripple

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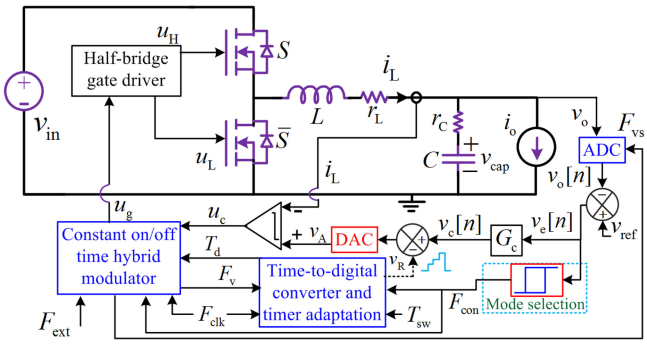


Fig. 1. Schematic of a mixed-signal current-mode synchronous buck converter using the proposed ON/OFF-time hybrid modulation technique; $i_{\rm L}$, v_o, and $v_{\rm ref}$ indicate the inductor current, output voltage, and reference voltage, respectively.

2) To establish fast-scale stability.
3) To derive a discrete-time small-signal model for the direct digital control design.
4) To develop a hybrid modulation technique for fast step-up/down transient performance using a single monoshot timer and a single voltage controller with seamless transition.
5) To develop a direct frequency adaptation method using a TDC for real-time frequency programming.

This paper proposes a digital current-mode architecture with constant ON/OFF-time hybrid modulation. A buck converter prototype is tested, and the benefits of the proposed control are verified experimentally.

This paper is organized as follows. Section II introduces an event-based constant ON/OFF-time hybrid modulation technique in digital current-mode control (CMC). A discrete-time framework is proposed, and stability analysis is carried out in Section III. The design methods are discussed in Section IV. Section V presents hardware implementation of a synchronous buck converter. Section VI concludes this paper.

II. Proposed Constant ON/OFF-Time Hybrid Modulation in Digital CMC

Primary objectives here are to develop: 1) event-based sampling mechanisms for both constant ON-time and OFF-time digital modulators for sampling the output voltage once per switching cycle and 2) a hybrid modulation technique to retain fast step-up/down transient performance. A discrete-time framework is developed in the subsequent section for stability analysis and the digital voltage controller design.

A. Digital Current-Mode Constant ON/OFF-Time Modulation

Fig. 1 shows the schematic of the proposed mixed-signal current-mode constant ON/OFF-time hybrid modulation technique in a synchronous buck converter, in which the outer voltage loop is kept in the digital domain and the inner current loop in the analog domain. The overall schematic consists of three primary blocks, which are discussed later in detail:

1) "constant ON/OFF-time hybrid modulator" block;
2) "time-to-digital converter and timer adaptation" block;
3) "mode selection" block.

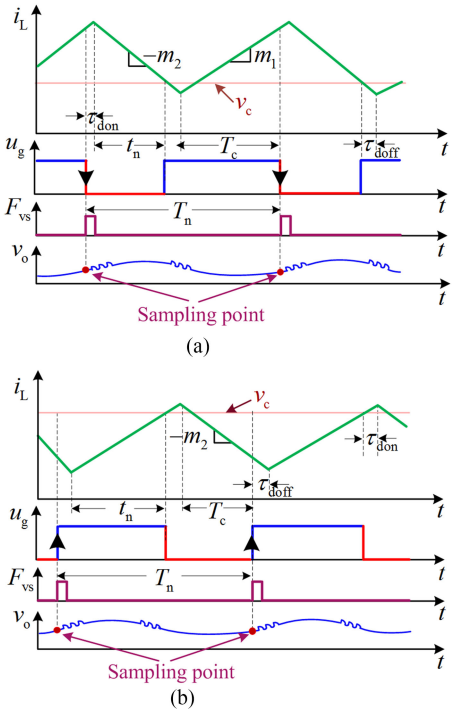


Fig. 2. Control waveforms under the proposed (a) constant ON-time modulation and (b) constant OFF-time modulation.

An analog-to-digital converter (ADC) is used to sample the output voltage v_o using an event-based sampling clock $F_{\rm vs}$, which takes the *falling* (or *rising*) edge of the gate signal $u_{\rm g}$ under constant ON-time (or constant OFF-time) modulation. If the output of the "mode selection" block $F_{\rm con} = 0$, the constant ON-time modulation is enabled; otherwise, the constant OFF-time modulation is enabled. The sampled voltage $v_o[n]$ is subtracted from the reference voltage $v_{\rm ref}$ to generate the error voltage v_e, and the digital voltage controller $G_c(z)$ computes at the same rate using $F_{\rm vs}$. An optional ramp $v_{\rm R}$ may be considered with the controller output $v_c[n]$, and the final output is converted into an equivalent analog voltage $v_{\rm A}$ using a digital-to-analog converter (DAC), as shown in Fig. 1. The DAC output is directly compared with the sensed inductor current using a high-speed analog comparator. The comparator output u_c is used to generate the controllable gate signal u_g by the "constant ON/OFF-time hybrid modulator" block; thereafter, a half-bridge gate driver circuit generates the respective gate signals for the high- and low-side MOSFETs of the synchronous buck converter.

Fig. 2 demonstrates the key control waveforms using the constant ON-time as well as constant OFF-time modulators using the proposed event-based sampling mechanisms. For the former, the output voltage is sampled at the falling edge of the gate signal u_g; thereafter, the high-side MOSFET is turned OFF after a finite delay $\tau_{\rm don}$, as shown in Fig. 2(a). In a practical converter, $\tau_{\rm don}$ is due to sampling, comparator, and driver delays, which helps to capture clean (output) voltage samples without being affected by switching noises. While a small delay $\tau_{\rm don}$ is practically recommended, it is important to investigate how the choice of $\tau_{\rm don}$ affects the output voltage regulation and fast-scale stability. The former can be intuitively perceived by looking at the

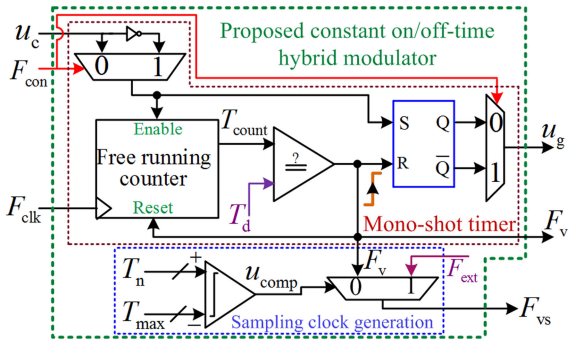


Fig. 3. Schematic of the proposed constant ON/OFF-time hybrid modulation.

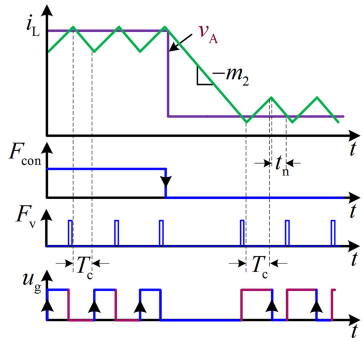


Fig. 4. Timing diagram of the proposed modulation in Fig. 3.

output voltage waveform in Fig. 2(a). This indicates that for a suitable choice of $\tau_{\rm don}$, the sampling point can made close to the average output voltage, which is indeed helpful to make the (output) voltage regulation more or less insensitive to load current and input voltage variations. Thus, the proposed constant ON-time modulation can overcome the voltage regulation problem, which persists in existing constant ON-time modulation techniques [2]. The effect of $\tau_{\rm don}$ on stability is analyzed in the subsequent section. Similarly, for the constant OFF-time modulator, the output voltage is sampled at the rising edge of u_g, after which the high-side switch turns ON after a finite delay $\tau_{\rm doff}$, as shown in Fig. 2(b).

B. Automated Constant ON/OFF-Time Mode Selection

A load step-up (or step-down) transient results in an undershoot (or overshoot) in the output voltage. A hysteretic comparator using the error (output) voltage is used as the "mode selection" block, as shown in Fig. 1. Here $F_{\rm con}$ is set to "logic 1" if the error voltage $v_e[n]$ goes above the hysteresis band $\Delta v_{\rm H}$, and the constant OFF-time modulator is enabled. Similarly, $F_{\rm con}=0$ if $v_e[n]\le -\Delta v_{\rm H}$, when the constant ON-time modulator will be enabled. Due to a large output capacitor, the effect of a load step transient gets reflected in the output voltage after a finite time. Thus, this automated logic block may introduce a (transient) detection delay, which would be shown later using test results. This can be overcome by generating $F_{\rm con}$ using direct feedforward information of the load current. Nowadays, for a smart electronic devices such as mobile processers, the load current information and timing are readily available from the PMBus architecture. For light-emitting diode (LED) drivers, such load current information is readily available from the LED dimming signals.

C. Constant ON/OFF-Time Hybrid Modulator

Fig. 3 shows the schematic of the "constant ON/OFF-time hybrid modulator" block in Fig. 1, in which the constant ON-time modulation is enabled if $F_{\rm con}=0$, else the constant OFF-time modulation is enabled. Here, $F_{\rm con}$ is used as the select line of a digital multiplexer (MUX) of which output is used as the "Enable" signal of a monoshot timer. For $F_{\rm con}=0$, "Enable" is set to "logic 1" when the comparator output u_c becomes high, as shown in Fig. 3. The timer consisting of a free-running

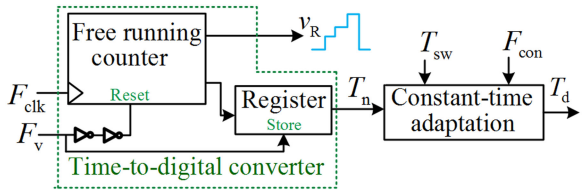


Fig. 5. Schematic of the time-to-digital converter and timer adaptation for the steady-state frequency regulation.

counter starts counting when "Enable" goes high, and the counter is reset when its output $T_{\rm count}$ equals the desired timing parameter T_d. Upon reset, a trigger signal F_v is generated, which is used as an event-based sampling clock. The comparator output and the output of the RS flip-flop are time multiplexed to generate the controllable gate signal $u_{\rm g}$ using $F_{\rm con}$ as the select line, as shown in Fig. 3.

During a large-signal transient recovery, the MOSFET may not change its state for a longer duration when the output voltage samples cannot be updated using the event-driven sampling clock F_v. Thus, F_v is used with an external uniform sampling clock $F_{\rm ext}$ to generate an interrupt-driven sampling clock $F_{\rm vs}$ using a digital MUX, as shown in Fig. 3. If the intersample duration T_n exceeds an upper limit $T_{\rm max}$, $F_{\rm ext}$ is used as the ADC sampling clock; otherwise, F_v is used.

The proposed hybrid modulator uses a single voltage controller $G_c(z)$ and a single monoshot timer, which can be reconfigured based on the modulation technique, and its value can be accordingly updated in real time. After identifying a step-down transient, $F_{\rm con}$ is set to "logic 0," and the constant ON-time modulator is enabled, as shown in Fig. 4. Similarly, the constant OFF-time modulator would be enabled after detecting a step-up transient. Interestingly, an antiwindup mode transition can be inherently achieved because of using a common $G_c(z)$ of which output remains unchanged during a modulator reconfiguration. Also, improved step-up/down transient performance can be retained using the proposed hybrid modulator.

D. TDC and Real-Time Timer Adaptation

Fig. 5 shows the "time-to-digital converter and timer adaptation" block of the proposed hybrid modulation scheme in Fig. 1. The TDC uses the rising edges of the event-based sampling clock F_v and generates an equivalent digital code T_n related to

the instantaneous (switching) time period, which is the interval between two subsequent rising edges of F_v. The value of T_n is stored using a register, which gets updated in every switching cycle before resetting the TDC counter. The "constant-time adaptation" block uses T_n and the desired (switching) time period $T_{\rm sw}$ to generate the desired constant time T_d based on the modulator configuration using $F_{\rm con}$ in Fig. 3. For a given operating point in a synchronous buck converter, the effective duty ratio can be assumed to be more or less constant for a wide variation of the steady-state switching frequency, even considering possible power circuit parasitics. Let T_n be the time period related to a predefined ON-time (or OFF-time) T_c using the constant ON-time (or OFF-time) modulator. Then, the desired ON-time (OFF-time) T_d can be calculated as

$$T_d = (T_{\rm sw}/T_n) \times T_c \tag{1}$$

where the desired time period $T_{\rm sw}$ can be either kept constant or programmed for real-time energy optimization [38], [39] as well as improvement in the light-load efficiency [38]. Thus, a fixed-frequency operation can be achieved by adjusting T_d using (1); however, it is difficult to implement a division operation using fixed-point arithmetic. While an iterative Newton–Raphson method can be used, this would require considerable hardware resources. An alternative method is to piecewise linearize the functional form $f(T_{\rm n}) = T_{\rm sw}/T_n$ in (1), thereafter, multiplying by T_c. Considering a deviation variable ΔT_n as $\Delta T_n = T_{\rm sw} - T_n$, the desired timing parameter T_d can be approximately calculated as

$$\begin{aligned} T_d &= \left[\frac{1}{1-(\Delta T_n/T_{\rm sw})}\right] \times T_c \\ &\approx \left[1+\frac{\Delta T_n}{T_{\rm sw}}\right] \times T_c = \left[2-\frac{T_n}{T_{\rm sw}}\right] \times T_c. \end{aligned} \tag{2}$$

This shows that a division operation in (1) can be replaced by multiplication and addition operations in (2), which can be easily realized using fixed-point arithmetic. This approach is used in this paper. Based on the modulator configuration using $F_{\rm con}$, T_d can be calculated offline using (2) and be stored in a lookup table for various operating points. Alternatively, a feedback PLL arrangement can be used, and available algorithms can be used to speed up the PLL response time [23].

III. Discrete-Time Modeling and Stability Analysis

A. General Perspective of Discrete-Time Modeling

A synchronous buck converter operates in the continuous conduction mode (CCM). It can take two feasible switch configurations, namely Mode 1 when the high-side switch is ON and Mode 2, otherwise. Referring to the buck converter schematic in Fig. 1, the state-space model of these two modes can be derived as follows:

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}-\frac{r_n}{L} & -\frac{1}{L}\\ \frac{1}{C} & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}\frac{u}{L} & \frac{r_c}{L}\\ 0 & -\frac{1}{C}\end{bmatrix}\begin{bmatrix}v_{\rm in}\\ i_o\end{bmatrix} \tag{3}$$

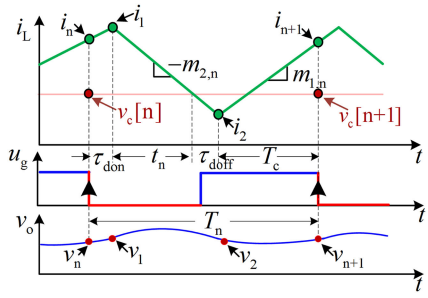


Fig. 6. Control waveforms using the proposed current-mode constant ON-time modulator: $\tau_{\rm on}$ is the MOSFET-driver delay and $\tau_{\rm doff}$ is the delay due to the MOSFET driver and analog comparator.

where states x_1 and x_2 indicate the respective inductor current $i_{\rm L}$ and the capacitor voltage $v_{\rm cap}$, $r_n = r_{\rm on} + r_{\rm L}$, where $r_{\rm on}$ and $r_{\rm L}$ are the MOSFET's ON-resistance and dc series resistance of the inductor, respectively, and r_c is the ESR of the output capacitor. When the control input $u = 1$, the system is said to operate in Mode 1; otherwise, it operates in Mode 2. From the buck converter schematic in Fig. 1, the output voltage v_o can be written as

$$v_o(t) = r_c i_{\rm L} + v_{\rm cap} - i_o r_c. \tag{4}$$

It is reasonable to assume that $i_{\rm L}$ varies linearly with time; thus, $i_{\rm L}$ and $v_{\rm cap}$ can be written using (3) as

$$\begin{aligned} i_{\rm L}(t) &= i_{\rm int} + \left(m_{\rm k} - \frac{r_n}{L} i_{\rm int}\right) t \\ v_{\rm cap}(t) &= v_{\rm c,int} + \frac{(i_{\rm int} - i_o)}{C} t + \left(m_{\rm k} - \frac{r_n}{L} i_{\rm int}\right) \frac{t^2}{2C} \end{aligned} \tag{5}$$

where $i_{\rm int}$ and $v_{\rm c,int}$ are the initial values of $i_{\rm L}$ and $v_{\rm cap}$, respectively, and i_o indicates the load current. The slope of the inductor current, $m_{\rm k}$, can be written as

$$m_{\rm k} = \begin{cases} m_1 = (v_{\rm in} - v_o)/L, & \text{during Mode 1} \\ -m_2 = -v_o/L, & \text{during Mode 2.} \end{cases} \tag{6}$$

Referring to Fig. 6, discrete-time models under the proposed scheme can be derived between two subsequent sampling instants. For constant ON-time modulation, the complete discrete-time model during the nth cycle can be derived using the sequence consisting of Mode 1 followed by Mode 2 followed by Mode 1 along with their respective time intervals. For constant OFF-time modulation, the sequence consists of Mode 2 followed by Mode 1 followed by Mode 2.

B. Discrete-Time Modeling Under Constant ON-Time Modulation

Control waveforms under constant ON-time modulation are shown in Fig. 6. During the nth switching cycle, t_n and T_n represent the respective OFF-time and time period, where T_c is the constant ON-time. The delays during ON-to-OFF and OFF-to-ON transitions are $\tau_{\rm don}$ and $\tau_{\rm doff}$, respectively, which include delays of the MOSFET, the comparator, and the controller. The control sequence begins with Mode 1, where the output voltage v_o is sampled using the falling edge of the gate signal $u_{\rm g}$, however,

before the switch turns OFF, as shown in Fig. 6. Let $i_{\rm L}$ and v_o at the start of the nth switching cycle be i_n and v_n, and those at the end of the switching cycle be i_{n+1} and v_{n+1}, respectively. Let the intermediate values of $\{i_{\rm L},\ v_o\}$ be $\{i_1,\ v_1\}$ at the end of MODE 1 and $\{i_2,\ v_2\}$ at the end of MODE 2, which can be derived using (4)–(6) as

$$\begin{aligned} i_1 &= i_n + \left(m_1 - \frac{r_n}{L} i_n\right) \tau_{\rm don} \\ v_1 &= v_n + \left(\frac{i_n - i_o}{C}\right) \tau_{\rm don} + m_{1,\rm n} \times \left(r_c + \frac{\tau_{\rm don}}{2C}\right) \tau_{\rm don} \quad (7) \\ i_2 &= i_1 - \left(m_2 + \frac{r_n}{L} i_1\right) (t_n + \tau_{\rm doff}) \\ v_2 &= v_1 + \left(\frac{i_1 - i_o}{C}\right) (t_n + \tau_{\rm doff}) \\ &\quad - \left(m_2 + \frac{r_n}{L} i_1\right) \times \left(r_c + \frac{t_n + \tau_{\rm doff}}{2C}\right) (t_n + \tau_{\rm doff}) \quad (8) \end{aligned}$$

where $m_{1,\rm n} = m_1 - \dfrac{r_n}{L} i_n$. Using (4)–(6), the final vector $\{i_{n+1},\ v_{n+1}\}$ under the proposed constant ON-time control can be derived as

$$\begin{aligned} i_{n+1} &= i_2 + \left(m_1 - \frac{r_n}{L} i_2\right) T_c \\ v_{n+1} &= v_2 + \left[\left(\frac{i_2 - i_o}{C}\right) + \left(m_1 - \frac{r_n i_2}{L}\right)\left(r_c + \frac{T_c}{2C}\right)\right] T_c. \end{aligned} \quad (9)$$

Assuming load current i_o to be constant, the term $i_1 - i_o$ in (8) can be written as $i_1 - i_o = [m_2 + (r_n/L) i_1]\,(t_{\rm n} + \tau_{\rm doff})/2$. This indicates that any perturbation in i_1 is immediately reflected in the instantaneous OFF-time t_n. Thus, the expression of i_{n+1} and v_{n+1} in (9) can be further simplified using (7) and (8) as

$$\begin{aligned} i_{n+1} &= \beta\,(v_c\,[n] - m_{21,\rm n}\tau_{\rm doff}) + m_1 T_c \\ v_{n+1} &= v_n + \left(\frac{i_n - i_o}{C}\right) \tau_{\rm don} + (\alpha_{\rm on}\tau_{\rm don} + \alpha\beta_{\rm on} T_c)\, r_c m_{1,n} \\ &\quad - \alpha\beta r_c m_{21,\rm n}\,(t_n + \tau_{\rm doff}) \end{aligned} \quad (10)$$

where $\alpha = 1 + \frac{T_c}{2r_c C}$, $\alpha_{\rm on} = 1 + \frac{\tau_{\rm don}}{2r_c C}$, $\beta = 1 - \frac{r_n}{L} T_c$, $\beta_{\rm on} = 1 - \frac{r_n}{L}\tau_{\rm don}$, $m_{21,\rm n} = m_{2,\rm n} + \frac{r_n}{L} m_{1,\rm n}\tau_{\rm don}$, $m_{2,\rm n} = m_2 + \frac{r_{\rm n}}{L} i_n$, and $v_c[n]$ is the output of the digital voltage controller $G_c(z)$, as shown in Fig. 1.

The proposed constant ON-time digital control is simulated using the SIMPLIS simulation tool. A study comparing the proposed discrete-time models with the SIMPLIS simulation is shown in Fig. 7 using the parameter set in Table I. The simulation results are obtained by using the SIMetrix/SIMPLIS (Ver. 8.10g) analog/mixed-signal simulator, which can simulate the closed-loop mixed-signal circuit with the digital blocks in Verilog and the analog power circuit components. Fig. 7 shows that the sampled inductor current and the output voltage obtained using the discrete-time models using the proposed constant ON-time modulator accurately match with the SIMPLIS simulation.

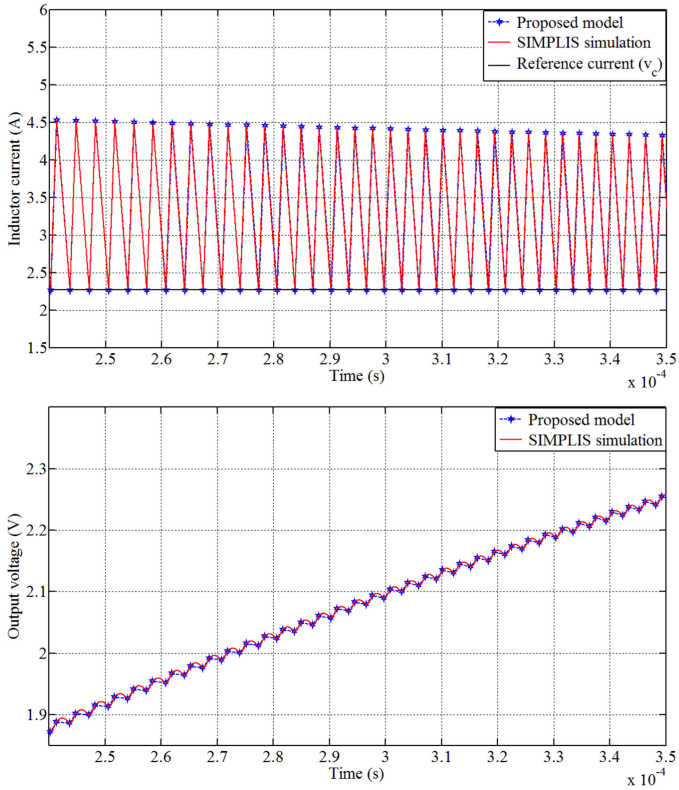


Fig. 7. Discrete-time model verification under the proposed constant ON-time modulation.

C. Discrete-Time Modeling Under Constant OFF-Time Modulation

Fig. 2(b) shows the control waveforms under the proposed constant OFF-time CMC, which is analogous to peak CMC. The output voltage v_o under constant OFF-time modulation is sampled using the rising edge of $u_{\rm g}$, in which the periodic sequence begins with MODE 2. Consider the nth switching cycle with the instantaneous time period T_n, the constant OFF-time T_c, and the ON-time t_n. Let the inductor current and the output voltage at the start of the nth switching cycle be i_n and v_n, and those at the end of the clock period be i_{n+1} and v_{n+1}, respectively. Following the similar methodology in Section III-B, the inductor current and the output voltage at the end of the nth switching cycle can be obtained as

$$\begin{aligned} i_{n+1} &= \beta\,(v_c\,[n] + m_{12,\rm n}\tau_{\rm don}) - m_2 T_c \\ v_{n+1} &= v_n + \left(\frac{i_n - i_o}{C}\right) \tau_{\rm doff} + \alpha\beta r_c m_{12,n}\,(t_n + \tau_{\rm don}) \\ &\quad - (\alpha_{\rm off}\tau_{\rm doff} + \alpha\beta_{\rm off} T_c)\, r_c m_{2,n} \end{aligned} \quad (11)$$

where $\alpha_{\rm off} = 1 + \dfrac{\tau_{\rm doff}}{2r_c C}$, $\beta_{\rm off} = 1 - \dfrac{r_n}{L}\tau_{\rm doff}$, and $m_{12,n} = m_{1,n} + \dfrac{r_n}{L} m_{2,n}\tau_{\rm doff}$.

Using the parameter set in Table I, a study comparing the above discrete-time models under the proposed constant OFF-time control and the SIMPLIS simulation is shown in Fig. 8. The study shows that the sampled inductor current and the out-

TABLE I
SPECIFICATION OF A SYNCHRONOUS BUCK CONVERTER *[as per Datasheet]*

Parameters	$v_{\rm in}$	$v_{\rm o}$	$F_{\rm s}$	$i_{\rm o}$	L	$r_{\rm L}$	C	$r_{\rm C}$
Value	(5 - 12) V	3.3 V	500 kHz	(0.5-7.5) A	2 μH	1.34 mΩ	100 μF	$< 10\ m\Omega$

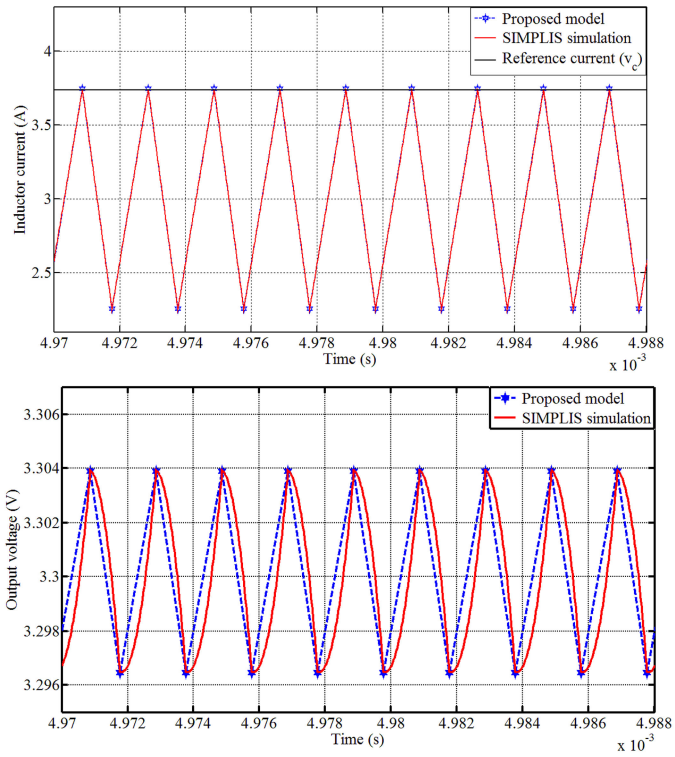


Fig. 8. Discrete-time model verification under the proposed constant OFF-time modulation.

put voltage obtained using the discrete-time models accurately match with the SIMPLIS simulation. Thus, the discrete-time models in (10) and (11) related to the respective constant ON-time and OFF-time modulation techniques can be used for (fast-scale) stability analysis as well as derivation of discrete-time small-signal models for the direct digital control design.

D. Stability Analysis Under Constant ON-Time Modulator

Consider $G_c(z)$ in Fig. 1 as a discrete-time proportional–integral (PI) controller as follows:

$$v_c[n] = k_{\rm p} v_e[n] + u_{\rm I}[n] \tag{12}$$

where $u_{\rm I}[n] = u_{\rm I}[n-1] + k_i v_e[n]$ and $v_e[n] = (v_{\rm ref} - v_n)$; $k_{\rm p}$ and k_i indicate proportional and integral gains in the discrete domain, respectively.

Fig. 1 shows the schematic of the proposed mixed-signal constant ON/OFF-time hybrid CMC, and the key control waveforms of constant ON-time modulation are shown in Fig. 2(a). This considers the falling edge of the gate signal $u_{\rm g}$ for output voltage sampling and controller computation. Under the ideal parametric condition, it can be found from (10) that the current loop $i_{n+1} = v_c[n] + m_1 T_c$ exhibits unconditional zero-input stability using the constant ON-time modulation technique. Furthermore, the closed-loop stability is completely determined by the voltage controller. Thus, the proposed CMC achieves robust stability, whereas conventional fixed-frequency CMC becomes unstable for a duty ratio $D > 0.5$ [30].

Under constant ON-time modulation (shown in Fig. 6), the instantaneous OFF-time t_n during the nth cycle is derived as

$$t_n = \frac{i_1 - (v_c[n]/R_i)}{m_2 + \dfrac{r_n}{L} i_1} \tag{13}$$

where R_i is the current-feedback gain, which is the multiplication of the sensing resistance and the gain of the current sense amplifier. Using (10) and (13), the closed-loop discrete-time state-space model can be derived. In the discrete-time PI controller given in (12), $k_{\rm p}$ is generally much larger than k_i. Thus, the stability boundary, under individual modulation techniques, is primarily decided by the upper limit of $k_{\rm p}$; however, the choice of $k_{\rm p}$ and k_i requires a good tradeoff between the phase margin and the settling time. Thus, for finding the stability boundary in this section, only $k_{\rm p}$ is considered. The perturbed discrete-time state-space model is derived using a proportional controller with $k_i = 0$ in (12) as

$$\begin{bmatrix} \hat{i}_{n+1} \\ \hat{v}_{n+1} \end{bmatrix} = \begin{bmatrix} -\beta\delta & -k_{\rm p}\beta \\ -\alpha r_c\,(1+\beta\delta) + r_1 & 1 - \alpha\beta k_{\rm p} r_c \end{bmatrix} \begin{bmatrix} \hat{i}_n \\ \hat{v}_n \end{bmatrix} \tag{14}$$

$$\text{where}\quad {\rm r_1} = \frac{\tau_{\rm don}}{\rm 2C}\left(1 + \beta_{\rm on} + \frac{\rm r_n}{\rm L}{\rm T_c}\right) \text{ and } \quad \delta = \frac{\rm r_n}{\rm L}\beta_{\rm on}\tau_{\rm doff}.$$

The closed-loop characteristics equation can be obtained applying Z-transformation on (14) [40]; thereafter, the eigenvalues become

$$\lambda_{1,2} = \frac{1}{2}\Big[1 - \beta\left(k_{\rm p} r_c \alpha + \delta\right) \pm \sqrt{\left[1 - \beta\left(k_{\rm p} r_c \alpha + \delta\right)\right]^2 + 4\beta\left[k_{\rm p}(r_c\alpha - r_1) + \delta\right]}\Big]. \tag{15}$$

Since $r_1 \ll r_c\alpha$, the discrete-time eigenvalues in (15) can be obtained as

$$\lambda_1 = 1, \quad \lambda_2 = -\beta\left(k_{\rm p} r_c \alpha + \delta\right). \tag{16}$$

Thus, the stability condition becomes

$$k_{\rm p} < \frac{1 - \dfrac{r_n}{L}\tau_{\rm doff}\left(1 - \dfrac{r_n}{L}T_c\right) \times \left(1 - \dfrac{r_n}{L}\tau_{\rm don}\right)}{r_c \times \left(1 - \dfrac{r_n}{L}T_c\right) \times \left(1 + \dfrac{T_c}{2r_c C}\right)}. \tag{17}$$

Fig. 9 shows simulated stability boundaries for a varying system as well as delay parameters, which indicates considerable effects due to the output capacitor and its ESR.

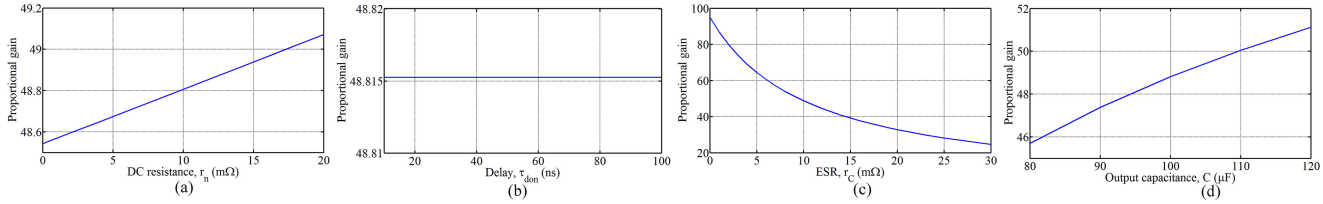


Fig. 9. Effect of parasitics on the stability boundary for constant ON-time modulation; variations in (a) the dc resistance $(r_{\rm on}+r_{\rm L})$, (b) the sampling and the switching delay $(\tau_{\rm don})$, (c) the ESR of the output capacitor (r_c), and (d) the output capacitance (C) using the nominal values given in Table I.

E. Stability Analysis Under Constant OFF-Time Modulator

Under constant OFF-time modulation, T_c is the (constant) OFF-time, and the ON-time t_n [in Fig. 2(b)] during the nth cycle can be derived as

$$t_n=\frac{(v_c[n]/R_i)-i_1}{m_1-\dfrac{r_n}{L}i_1}. \tag{18}$$

Substituting (18) into (11) and incorporating small perturbations, the perturbed closed-loop discrete-time state-space model can be obtained as

$$\begin{bmatrix}\hat{i}_{n+1}\\ \hat{v}_{n+1}\end{bmatrix}=\begin{bmatrix}-\beta\delta_1 & -k_{\rm p}\beta\\ -\alpha r_c\,(1+\beta\delta_1)+r_2 & 1-k_{\rm p}r_c\alpha\beta\end{bmatrix}\begin{bmatrix}\hat{i}_n\\ \hat{v}_n\end{bmatrix} \tag{19}$$

where $r_2=\dfrac{\tau_{\rm doff}}{2C}\left(1+\beta_{\rm off}+\dfrac{r_n}{L}T_c\right)$ and $\delta_1=\dfrac{r_n}{L}\beta_{\rm off}\tau_{\rm don}$.

Following the stability analysis carried out in Section III-D, the stability condition for the constant OFF-time modulation can be obtained as

$$k_{\rm p}<\frac{1-\dfrac{r_n}{L}\tau_{\rm don}\left(1-\dfrac{r_n}{L}T_c\right)\times\left(1-\dfrac{r_n}{L}\tau_{\rm doff}\right)}{r_c\times\left(1-\dfrac{r_n}{L}T_c\right)\times\left(1+\dfrac{T_c}{2r_cC}\right)}. \tag{20}$$

IV. Design of the Proposed Constant ON/OFF-Time Modulator

A. Stability Enhancement Using Ramp Compensation

Fig. 9 shows the effect of variations in the combined dc resistance (r_n), the sampling and the switching delay $(\tau_{\rm don})$, the ESR of the output capacitor (r_c), and the output capacitance (C) on the stability boundary $(k_{\rm p})$ for the proposed constant ON-time modulation. It is clear from Fig. 9 that r_n and $\tau_{\rm don}$ have a negligible effect on the stable range of $k_{\rm p}$, whereas r_c and C significantly affect the stability boundary.

The stability boundary in (17) using the proposed scheme is insensitive to the input voltage, whereas a fixed-frequency CMC technique becomes unstable for the duty ratio $D>0.5$, which requires a compensating ramp for stabilization. A ramp may not be needed in the proposed scheme as long as the controller gains satisfy the criteria given in (17); however, it is important to investigate whether this can help to enhance the stability boundary. Considering a ramp compensation under constant ON-time control, the OFF-time $t_{n,r}$ during the nth cycle becomes

$$t_{n,r}=\frac{i_n-(v_c[n]/R_i)}{m_2+m_c} \tag{21}$$

where m_c is the slope of the ramp. Subsequently, the perturbed model can be derived using (10), (12), and (21) as

$$\begin{bmatrix}\hat{i}_{n+1}\\ \hat{v}_{n+1}\end{bmatrix}=\begin{bmatrix}0 & -k_{\rm p}\\ -\bar{\alpha}r_c & 1-\bar{\alpha}r_ck_{\rm p}\end{bmatrix}\begin{bmatrix}\hat{i}_n\\ \hat{v}_n\end{bmatrix}$$

where $\bar{\alpha}=\alpha m_2/(m_2+m_c)$. Using the similar methodology in Section III-D, the stability boundary with a ramp compensation under constant ON-time CMC can be derived as

$$k_{\rm p}<\left(1+\frac{m_c}{m_2}\right)\times\frac{1}{r_c}\times\left[1+\frac{T_c}{2r_cC}\right]^{-1}. \tag{22}$$

This indicates that the stable range of $k_{\rm p}$ can be enlarged by reducing the ESR and increasing the output capacitor; however, r_c and C cannot be varied after the power stage design. Thus, the stability boundary in (22) using the proposed scheme can be enhanced by additionally considering a ramp compensation $v_{\rm R}$; the gain range is increased by a factor $(1+m_c/m_2)$. However, a higher value of m_c can degrade the closed-loop bandwidth; thus, $v_{\rm R}$ should be considered if needed, and its slope needs to be small enough in order to ensure cycle-by-cycle stability. Similarly, the stability boundary with a ramp compensation using the proposed current-mode constant OFF-time modulator can be derived as

$$k_{\rm p}<\left(1+\frac{m_c}{m_1}\right)\times\frac{1}{r_c}\times\left[1+\frac{T_c}{2r_cC}\right]^{-1}. \tag{23}$$

B. Small-Signal Modeling

The small-signal model of the proposed constant ON-time modulation scheme can be derived using the discrete-time model given in (10). Assuming constant input voltage $(\hat{v}_{\rm in}=0)$ and constant load current $(\hat{i}_o=0)$, the perturbed state-space model under constant ON-time modulation is obtained as

$$\begin{bmatrix}\hat{i}_{n+1}\\ \hat{v}_{n+1}\end{bmatrix}=\begin{bmatrix}k_c & Y_x\\ R_y & k_v\end{bmatrix}\begin{bmatrix}\hat{i}_n\\ \hat{v}_n\end{bmatrix}+\begin{bmatrix}-\beta M_{2,n}\\ -M_{2,n}R_z\end{bmatrix}\hat{t}_n \tag{24}$$

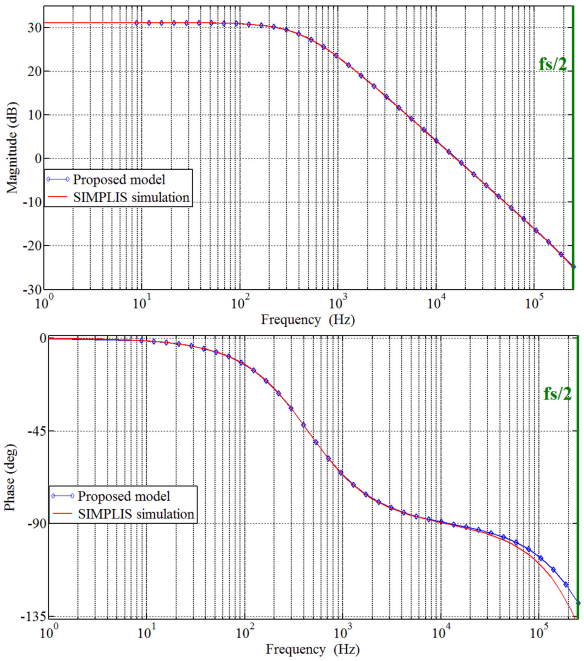


Fig. 10. Frequency-domain verification of the control-to-output transfer function under the proposed constant ON-time modulation using SIMPLIS simulation.

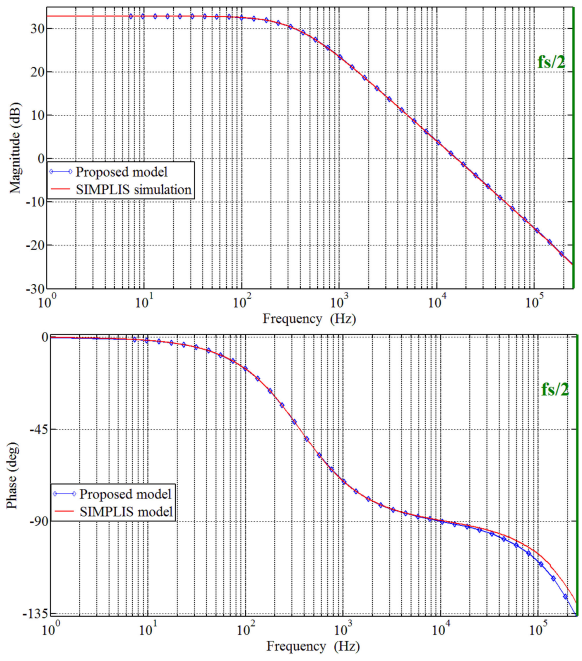


Fig. 11. Frequency-domain verification of the control-to-output transfer function under the proposed constant OFF-time modulation using SIMPLIS simulation.

where

$$k_c = \beta\beta_{\rm on}\left(\beta_{\rm off} - \frac{r_n}{L}T_{\rm off}\right)$$

$$Y_x = -\left[\beta\beta_{\rm on}\left(T_{\rm off}+\tau_{\rm off}\right)+T_c+\beta\tau_{\rm don}\right]/L$$

$$R_y = r_c\left(k_c-1\right)+r_3\beta_{\rm on}+\frac{\tau_{\rm don}}{2C}\left(1+\beta_{\rm on}\right)$$

$$k_v = r_c Y_{\rm x}+\frac{\left(T_{\rm off}+\tau_{\rm doff}\right)R_z-r_3\tau_{\rm don}}{L}-\frac{T_c^2+\tau_{\rm don}^2}{2LC}$$

$$r_3 = \frac{T_c}{2C}\left(1+\beta\right)\times\left(\beta_{\rm off}-\frac{r_n}{L}T_{\rm off}\right)+\frac{\left(T_{\rm off}+\tau_{\rm doff}\right)}{2C}\left(1+\beta_{\rm off}-\frac{r_n}{L}T_{\rm off}\right)$$

$$R_z = \alpha\beta r_c+\frac{T_c+T_{\rm off}+\tau_{\rm doff}}{2C}.$$

From (13), the control law for the proposed constant ON-time modulation is obtained as

$$\hat{t}_n = \frac{\beta_1}{M_{2,n}}\hat{i}_n-\frac{1}{R_i M_{2,n}}\hat{v}_c\left[n\right]-\frac{T_{\rm off}}{LM_{2,n}}\hat{v}_n. \tag{25}$$

Using (25) in (24) and applying Z-transformation, the discrete-time control-to-output transfer function $(\hat{v}_o/\hat{v}_{\rm A})$ of the proposed constant ON-time modulation can be obtained as

$$G_{\rm vc}(z) = K\frac{z+z_1}{z^2+p_1 z+p_2}. \tag{26}$$

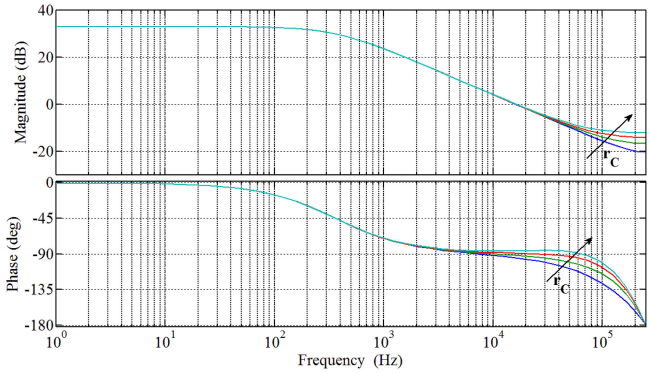


Fig. 12. Effect of variation in output capacitor ESR (r_c) in the control-to-output transfer function $(G_{\rm vc})$ of CMC constant ON-time modulation.

The coefficients of the transfer function z, p_1, and p_1 in (26) are

$$K = \left(R_z/R_i\right)$$

$$z_1 = \left(R_y/R_z\right)\beta-k_c,$$

$$p_1 = \beta\beta_1-\left(k_c+k_v\right)-\frac{T_{\rm off}}{L}R_z,$$

$$p_2 = k_c\left(k_v+\frac{T_{\rm off}}{L}R_z\right)-\beta\left(k_v\beta_1+R_y\frac{T_{\rm off}}{L}\right)-Y_x\left(R_y-\beta_1 R_z\right).$$

Following the same methodology, the control-to-output transfer function under the proposed constant OFF-time modulation can be derived using (11) and (18).

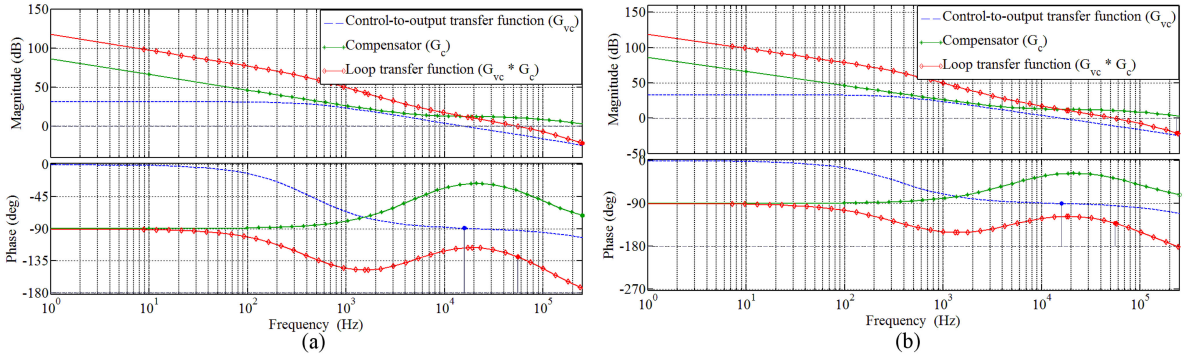


Fig. 13. Bode plot of the control-to-output, compensator, and loop transfer functions of the mixed-signal current-mode synchronous buck converter under (a) constant ON-time modulation and (b) constant OFF-time modulation; the compensator G_c designed achieves a bandwidth of 55 kHz $(f_s/9)$ and the phase margin of around 50°.

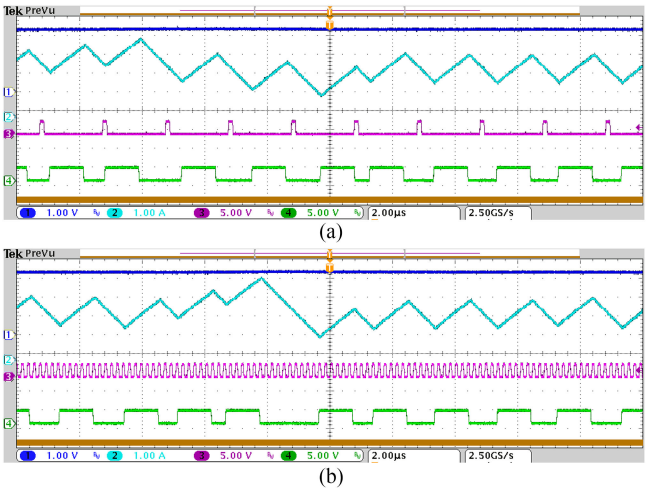


Fig. 14. Steady-state waveform of a CCM buck converter using mixed-signal current-mode constant ON-time control at a load current of 2.5 A with $k_p = 15$, and $k_i = 0.1$: Using an external uniform sampling clock F_{ext} with the rates (a) 500 kHz and (b) 5 MHz: $T_c = 1.12\,\mu$s. Time scale of 2 μs/div. From the top, Ch-1 v_o (1 V/div), Ch-2 i_L (1 A/div), Ch-3 F_{vs} (5 V/div), and Ch-4 u_g (5 V/div).

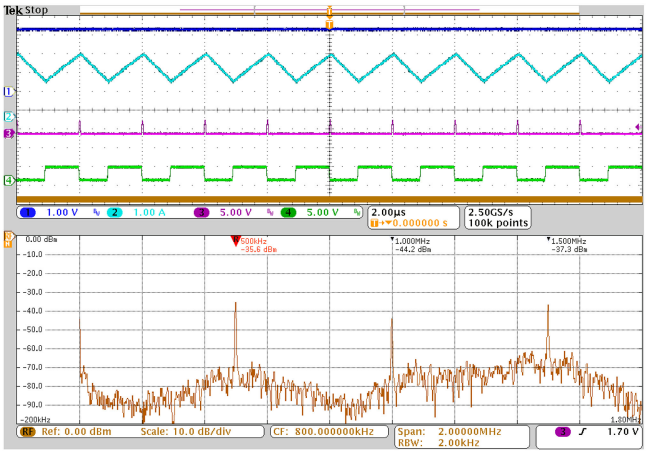


Fig. 15. Steady-state waveform of a CCM buck converter using mixed-signal current-mode constant ON-time control at a load current of 2.5 A with $k_p = 15$, and $k_i = 0.1$: Using the proposed event-driven sampling: $T_c = 1.12\,\mu$ s. Time scale of 2 μ s/div. From the top, Ch-1 v_o (1 V/div), Ch-2 i_L (1 A/div), Ch-3 F_{vs} (5 V/div), Ch-4 u_g (5 V/div), and the FFT trace shows the power spectrum of i_L.

C. Comparative Study of Small-Signal Behavior

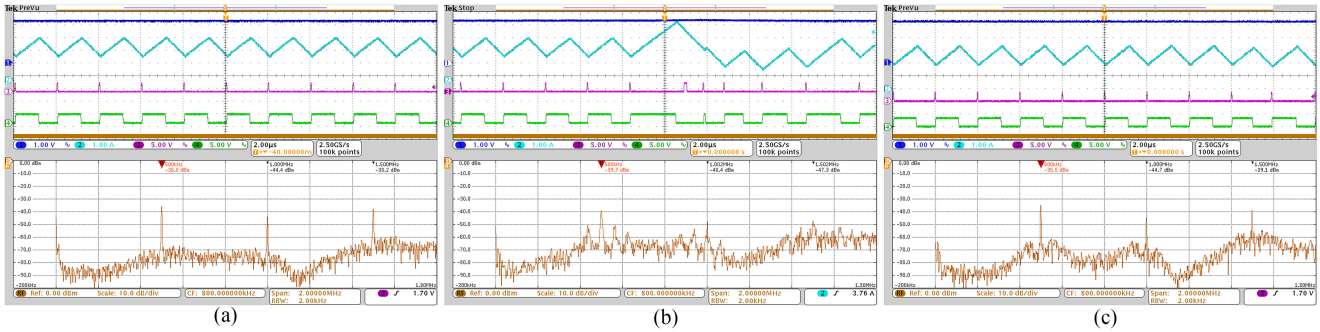
Fig. 10 shows the Bode plots of the control-to-output transfer function G_{vc} under the proposed constant ON-time modulation. The frequency response using the proposed model in (26) is verified using the SIMPLIS simulation with the parameter set given in Table I. The figure shows that G_{vc} results in a 31-dB dc gain and a 16-kHz gain crossover frequency with a phase margin of 89°. Also, the proposed discrete-time model closely matches with the SIMPLIS simulation throughout the Nyquist frequency range, except for nearly 5° phase difference at high frequency. A similar comparative study of frequency response using the constant OFF-time modulator is shown in Fig. 11, which shows close agreements between the proposed model and the SIMPLIS simulation. Thus, the proposed models are accurate enough to carry out digital controller design.

D. Effect of the Capacitor ESR on the Small-Signal Behavior

While a larger ESR significantly limits the stable range of the controller gain, as evident from Fig. 9(b), it is important to investigate the effect of the capacitor ESR in the frequency response using the proposed scheme. Fig. 12 shows Bode plots of G_{vc} in (26) for different ESR values. The effect is consistent with the well-known fact that a larger ESR tends to bring the high-frequency zero inside the Nyquist frequency range, thereby increasing the phase margin and the high-frequency gain. While this would tend to improve closed-loop damping, voltage overshoot/undershoot as well as critical bandwidth during a load step transient would be limited by a large ESR [41]. Also, the voltage ripple significantly increases, and the stability boundary degrades using the proposed scheme, as shown in Fig. 9(b). Thus, a smaller capacitor ESR is useful from a practical standpoint, and the proposed scheme would offer a larger range of stable controller gains.

E. Design of the Discrete-Time Compensator: A Case Study

Considering a nominal switching frequency of $f_{sw} =$ 500 kHz, the sampling time in the discrete-time transfer function is taken as 2 μs in (26) related to the constant ON-time modulation. The controller is designed to achieve the closed-loop bandwidth of nearly $f_{sw}/10$ and 45° phase margin. Using



(a) (b) (c)

Fig. 16. Steady-state waveform of a mixed-signal current-mode constant OFF-time CCM buck converter at a load current of 2.5 A under the proposed event-driven sampling using the discrete-time compensator gains as (a) $k_{\rm p} = 15$, and $k_{\rm i} = 0.1$, (b) $k_{\rm p} = 42$ and $k_{\rm i} = 0.1$, and (c) $k_{\rm p} = 42$ and $k_{\rm i} = 0.1$ with external ramp compensation: $T_c = 850\,ns$. Time scale of 2 μs/div. From the top, Ch-1 v_o (1 V/div), Ch-2 $i_{\rm L}$ (1 A/div), Ch-3 $F_{\rm vs}$ (5 V/div), Ch-4 $u_{\rm g}$ (5 V/div), and the FFT trace shows the power spectrum of $i_{\rm L}$.

MATLAB SISO toolbox, the discrete-time controller gains are found to be $k_{\rm p} = 7$ and $k_i = 0.9$. This achieves the phase margin of 50° with the loop bandwidth of 55.5 kHz and the frequency response of the same, is shown in Fig. 13(a). Similarly, with the same controller gains, the constant OFF-time modulation scheme achieves the phase margin of 48.5° at the bandwidth of 55.5 kHz, and the frequency response of the compensator and the loop transfer functions are shown in Fig. 13(b). These design parameters are later used in test case studies.

V. Hardware Implementation

A synchronous buck converter prototype has been made, and the proposed techniques are implemented using a field-programmable gate array (FPGA) device. For the experimental verification, the nominal parameter set is given in Table I. The time period of the FPGA clock is $t_{\rm clk} = 10$ ns. A 10-bit AD9215 differential pipeline ADC is used to sample the output voltage, which is preceded by an AD8138 single-ended-to-differential driver. A 12-bit AD9762 DAC followed by an AD8130 differential-to-single-ended driver is used to convert the controller output $v_c[n]$ into an analog voltage $v_{\rm A}$, which is compared with the sensed inductor current using a high-speed analog comparator (TLV3501). A 10–mΩ shunt resistor is used to sense the inductor current followed by a high-side current sense amplifier with a gain of 10.

A discrete-time PI voltage controller in (12) is used for all the following experimental results.

A. Steady-State Behavior and Fast-Scale Stability

For all the fast Fourier transform (FFT) traces in Figs. 15 and 16, the x-axis indicates the frequency with 200 kHz/div and the y-axis indicates power spectral density with 10 dB/div.

Figs. 14 and 15 demonstrate experimental results of a CCM buck converter using the proposed mixed-signal current-mode constant ON-time control. The constant ON-time T_c is selected in a way to achieve a nominal switching frequency of 500 kHz. If an external uniform clock $F_{\rm ext}$ of 500 kHz is used to sample the output voltage, Fig. 14(a) clearly indicates the existence of multilimit cycle oscillations [44]. This is because of mismatches in the sampling and switching instants, while using uniform sampling in variable-frequency digital control. Such oscillations eventually increase the root-mean-square (RMS) value of the inductor current, thereby increasing the conduction losses and degrading the efficiency. Although the use of a higher sampling rate of 5 MHz (ten times the nominal switching frequency) reduces timing mismatches, as shown in Fig. 14(b), this cannot completely stabilize the steady-state periodic behavior. Moreover, such a higher sampling requirement increases the cost of an ADC along with its power dissipation, which may not be practically recommended for high-frequency applications.

TABLE II
Stability Boundary Comparison Under Constant OFF-Time Modulation

$v_{\rm in}$ (V)	$T_{\rm off}$ (μs)	Critical stability boundary ($k_{\rm p}$)	
		Theoretical prediction	Experimental validation
6	0.85	48.25	42
8	1.17	44.4	39.25
10	1.3	43.06	38.8

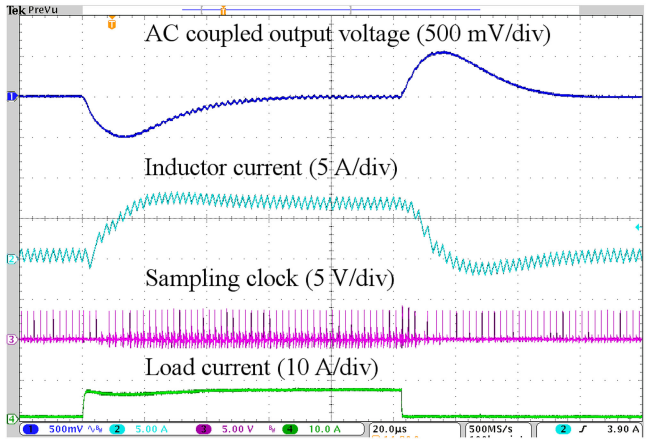


Fig. 17. Transient response of a synchronous buck converter using the proposed hybrid constant ON/OFF-time modulation technique for the load step change from 0.5 to 7.5 A and back at the 6-V input. Time scale of 10 μs/div.

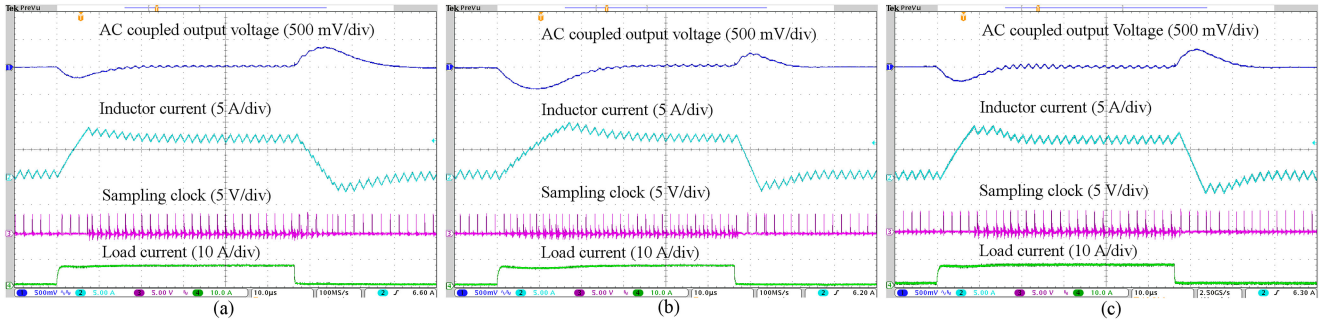


Fig. 18. Transient response of a synchronous buck converter at the 6-V input for the load step from 0.5 to 7.5 A and back with load current feedforward using (a) constant OFF-time modulation technique, (b) constant ON-time modulation technique, and (c) proposed hybrid constant ON/OFF-time modulation. Time scale of 10 μs/div.

The use of the proposed event-driven sampling approach is able to completely stabilize the mixed-signal current-mode constant ON-time modulator control, as shown in Fig. 15. This is also evident from the FFT trace of the inductor current, which indicates that spectral peaks appear at dc as well as the switching frequency and its harmonics. Thus, stable periodic behavior can be achieved by sampling the output voltage once per switching cycle, which drastically reduces the sampling requirement, thereby making it suitable for high-frequency implementation. Similarly, an event-based sampling approach can stabilize the constant OFF-time modulator, as shown in Fig. 16, in which the rising edge of $u_{\rm g}$ is used as the sampling clock for the ADC. However, if the proportional gain is increased to $k_{\rm p} = 42$, the stable gain range in (20) is violated, which results in subharmonic instability, as shown in Fig. 16(b). This is evident from the FFT trace of $i_{\rm L}$, in which sideband spectral peaks exist along the fundamental and harmonic contents. While this may be useful from the spectral spreading perspective, such instabilities may lead to unpredictable inductor current ripple with a considerably higher RMS value. If an optional compensating ramp $v_{\rm R}$ is used of which the slope is calculated using (23) as $m_c = 0.18\,{\rm V}/\mu{\rm s}$, the stability boundary can be further enhanced to $k_{\rm p} = 54.7$ and the stable periodic behavior is restored, as shown in Fig. 16(c), which is also evident from the FFT trace.

Table II compares the analytical stability boundaries $(k_{\rm p})$ with those obtained through experimentation under constant OFF-time modulation for different input voltage conditions. The table shows that the experimental stability boundaries are somewhat smaller than those obtained analytically. This can be attributed to parasitic in a practical converter, such as the effective series inductance, additional delays due to sampling and controller computation, and unmodeled dynamics using off-the-shelf discrete components. Also, it is very difficult to accurately know the capacitor ESR r_c during the runtime of a practical converter, and Fig. 9(c) shows that a small ESR variation can considerably affect the stability boundary. Such practical mismatches can be reduced using power management integrated circuits. Nevertheless, the trend of stability (boundary) enhancement using an additional ramp compensation is clearly visible in the test case [shown in Fig. 16(c)], which is consistent with the analytical study using the proposed constant ON/OFF-time hybrid digital modulator.

B. Transient Response

Fig. 17 shows the transient performance of a CCM buck converter using the proposed hybrid modulator for a step change in the load current from 0.5 to 7.5 A and back. Using the "mode selection" block, as shown in Fig. 1 and discussed in Section II-B, if the error voltage $V_e[n] \geq \Delta v_{\rm H}$ during a (load) step-up transient, $F_{\rm con}$ is set to logic 1, and the constant OFF-time modulator is enabled. As discussed earlier, the use of a voltage hysteresis band introduces a (transient) detection delay which results an initial inverse response in $i_{\rm L}$ during a step-up transient, as shown in Fig. 17. Similarly, a (load) step-down transient is detected using the hysteretic comparator, which sets $F_{\rm con} = 0$ and enables the constant ON-time modulator. The specifications and design criteria in Section IV-E are considered here. This results in 50-μs settling time with 500-mV (output) voltage undershoot during a step-up transient and 44-μs settling time with 550-mV overshoot during a step-down transient. The voltage undershoot/overshoot is within the specified limit, which is generally up to 20% of the nominal output voltage (3.3 V here). Also, the transient performance are found to be consistent with the design specifications in Section IV-E.

The transient performance can be further improved by considering a load current feedforward. This can be directly used in $F_{\rm con}$, instead of a hysteretic comparator, to avoid any (transient) detection delay. A load feedforward is also useful for disturbance rejection and to implement high-performance control [42]. In the rest of the test case studies, a load feedforward is used along with the feedback compensator.

Fig. 18(b) shows the load transient performance in a synchronous buck converter using the constant ON-time modulator throughout. This results in 24-μs settling time and 400-mV voltage undershoot for a step-up transient; however, this results in a faster step-down recovery with 12-μs settling time and 250-mV voltage overshoot. On the other hand, Fig. 18(a) shows that the constant OFF-time modulator achieves a fast step-up recovery with 12-μs settling time and 200-mV voltage undershoot, while the step-down performance is significantly degraded with 20-μs settling time and 350–mV voltage overshoot. It is clear from Fig. 18(a) and (b) that constant ON-time modulator offers fast step-down recovery, whereas constant OFF-time modulator offers fast step-up recovery. A hybrid combination can retain

TABLE III
TRANSIENT PERFORMANCE COMPARISON FOR THE LOAD STEP CHANGE FROM 0.5 TO 7.5 A AND BACK

Load transients	Modulation	Settling time (μs)	Δv_o (mV)
0.5 A – 7.5 A	Constant on-time	24	400
	Constant off-time	12	200
	Proposed hybrid	13	250
7.5 A – 0.5 A	Constant on-time	12	250
	Constant off-time	20	350
	Proposed hybrid	14	300

Δv_o = voltage undershoot/overshoot.

their best features with improved step-up/down performance using the constant OFF- and ON-time modulators, respectively, as shown in Fig. 18(c). The same controller gains in Section IV-E are used for both the cases. A further improvement is possible by adaptively varying the timing parameters for an active modulator. This provides opportunities for implementing high-performance control algorithms with minimized hardware resources.

Table III shows the performance comparison using the proposed modulation techniques under step load transients. The table shows that the proposed hybrid modulator overcomes the difficulty of individual modulation schemes and retains their best features, however, with a small delay due to a modulator reconfiguration. The proposed scheme requires full-current sensing for hybridization. For the applications using only high-side or low-side current sensing, either of the proposed event-based constant OFF-time or ON-time modulator can be used with reduced sampling requirement and with the flexibilities of real-time tuning the controller parameters and adaptation of the constant timing parameter for improved performance.

C. Performance Comparison With Fixed-Frequency Mixed-Signal Current-Mode Control for $D > 0.5$

Fig. 19 shows the transient response of a synchronous buck converter using fixed-frequency mixed-signal peak current-mode control (MCMC) [29] for a step change in the load current from 0.5 to 7.5 A. Using the same controller gains as well as load current feedforward as in Fig. 18, the transient performance using the MCMC technique [shown in Fig. 19(a)] is more or less comparable with the proposed constant OFF-time modulator with 12-μs settling time and 200-mV (output) voltage undershoot for the effective steady-state duty ratio $D = 0.62$. However, the former results in subharmonic (or fast-scale) instability for $D > 0.5$, as evident from Fig. 19(a). This significantly increases the voltage ripple and the RMS value of the inductor current, thereby increasing the conduction losses. An external ramp compensation is needed for stabilizing MCMC [30]. However, this would degrade the closed-loop bandwidth and thereby penalize the transient performance [43]. It is clear from the test result in Fig. 19(b) that a ramp compensation $v_{\rm R}$ degrades the transient performance with a settling time of 16 μs and a voltage undershoot of 320 mV, compared to that without using $v_{\rm R}$ in Fig. 19(a). A comparative study using the MCMC scheme and the proposed scheme is presented in Table IV. This shows that the proposed constant OFF-time modulation offers superior performance and stability compared to that using MCMC.

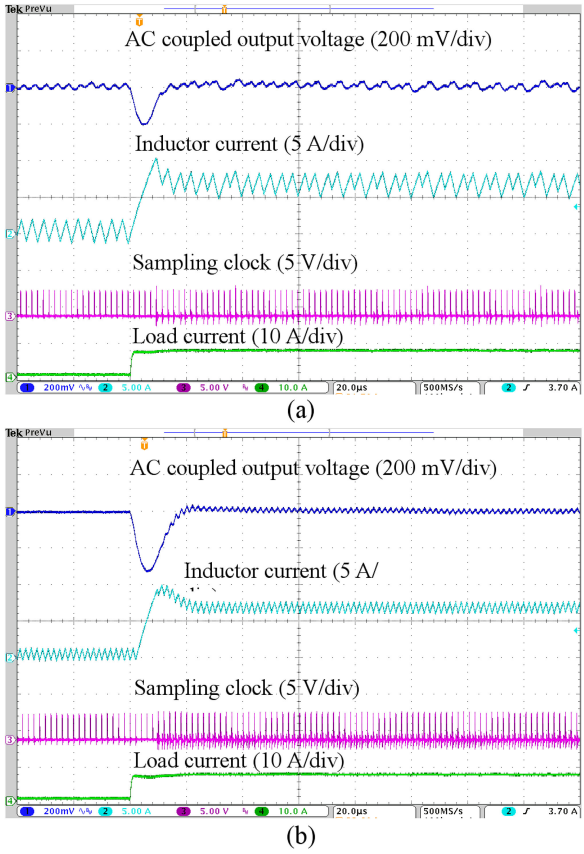


Fig. 19. Transient response of a synchronous buck converter at the 6-V input for the load step from 0.5 to 7.5 A and back operating at $D = 0.62$ under the fixed-frequency MCMC scheme (a) without using and (b) with using a ramp compensation. Time scale of 20 μs/div.

TABLE IV
TRANSIENT PERFORMANCE COMPARISON FOR THE LOAD STEP CHANGE FROM 0.5 TO 7.5 A WITH THE OUTPUT VOLTAGE OF 3.3 V AND THE STEADY-STATE DUTY RATIO $D = 0.62$

Modulation scheme		Settling time	Δv_o
Fixed-frequency MCMC	$m_c = 0$	12 μs	200 mV
	$m_c = 0.36$ V/μs	16 μs	320 mV
Constant off-time MCMC [Referring Fig. 18 (a)]		12 μs	200 mV

Δv_o = voltage undershoot and m_c = Ramp slope.

D. Steady-State Frequency Adaptation and Regulation

Fig. 20 shows the transient performance of a CCM buck converter for a step change in the output voltage from 2.5 to 4 V at the 6-V input using the proposed constant OFF-time

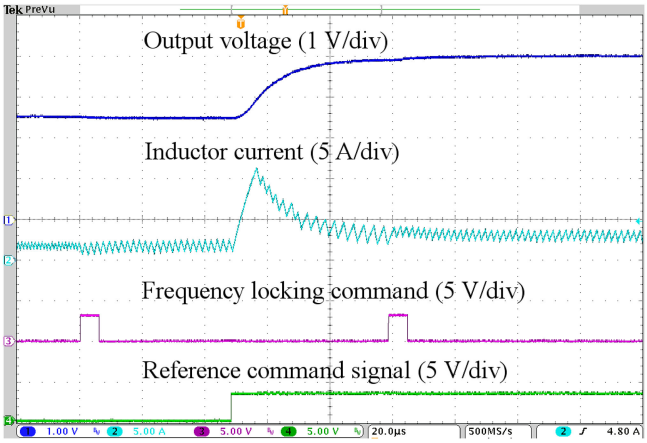


Fig. 20. Transient response of a synchronous buck converter for a step change in the reference voltage from 2.5 to 4 V using the proposed constant OFF-time modulator with $k_{\rm p} = 7$ and $k_{\rm i} = 0.1$ for $R = 1.25\,\Omega$ and $v_{\rm in} = 6$ V. Time scale of 20 μs/div.

mixed-signal CMC. The controller parameters considered for this experimentation are $k_{\rm p} = 7$ and $k_{\rm i} = 0.1$. This results in a settling time of 32 μs and a current overshoot of 11.5 A. At a higher output voltage, the effective ON-time increases, which decreases the effective switching period and increases the current ripple. Thus, the constant OFF-time needs to be decreased in real time in order to achieve a fixed steady-state switching frequency of 500 kHz, as shown in Fig. 20. The proposed scheme achieves stable periodic behavior using one sample per cycle.

E. Wide Duty-Ratio Operation Using the Proposed Hybrid Modulator

Fig. 21 shows the transient response of the synchronous buck converter using the proposed constant hybrid modulation for a step change in the load current from 0.5 to 7.5 A and back for a higher duty ratio $D = 0.73$ and a lower duty ratio $D = 0.28$. Using the same controller gains as in Fig. 18, the proposed hybrid modulator results in a settling time of 22 μs with a voltage undershoot of 350 mV for a (load) step-up transient for $D = 0.73$ [shown in Fig. 21(a)]. For the same step-up transient with $D = 0.28$, it results in a settling time of 14 μs and a voltage undershoot of 200 mV, as shown in Fig. 21(b). This is consistent with the fact that the step-up transient performance is indeed faster using a higher input voltage (or a smaller D). However, for the same output voltage condition, the step-down transient performance is more or less the same for both the cases with a settling time of 16 μs and a voltage undershoot of 250 mV.

The event-based sampling is capable of stabilizing the closed-loop converter using one sample per cycle over a wide duty-ratio range without the need for a ramp compensation, and the proposed hybrid modulator retains the improved step-up/down performance throughout. Thus, the proposed scheme can be an attractive solution for digitally controlled dc–dc converters over the fixed-frequency MCMC technique, particularly for wide duty-ratio operations.

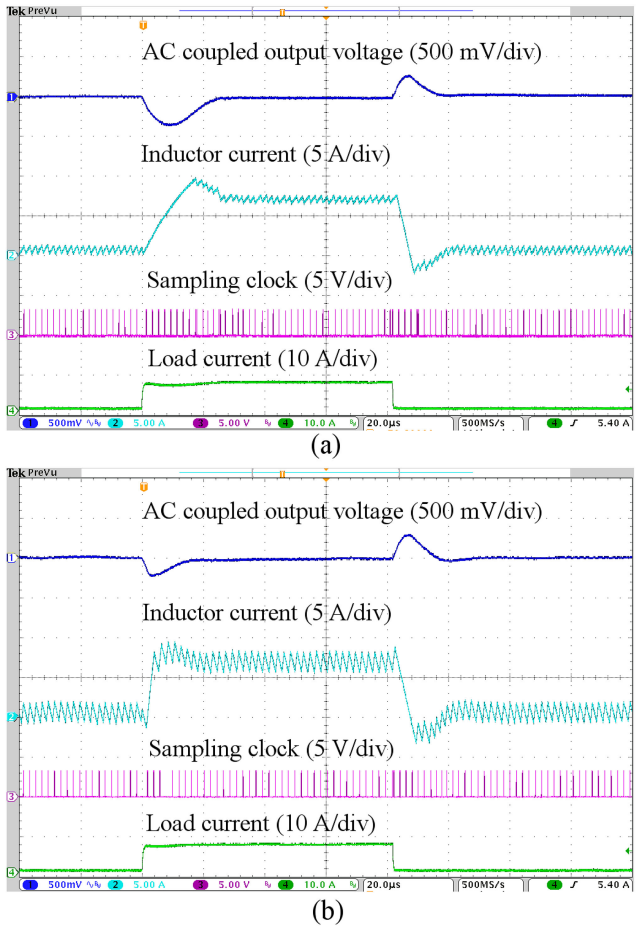


Fig. 21. Transient response of a synchronous buck converter for the load step from 0.5 to 7.5 A and back using the proposed constant ON/OFF-time hybrid modulation with an event-driven sampling mechanism: for duty ratio (a) $D = 0.73$ and (b) $D = 0.28$ at 3.3 V output. Time scale of 20 μs/div.

VI. Conclusion

A hybrid constant ON/OFF-time modulator using an event-driven sampling mechanism was proposed in a digitally current-mode controlled point-of-load converter. This utilizes the best features of the individual modulators and achieves improved load transient performance over a wide operating range. Either of the modulators uses a common digital voltage controller while remaining active; thus, an antiwindup controller transition is inherently achieved, and hardware resource is also minimized. A theoretical framework of discrete-time modeling and stability analysis was presented. Design methods for the enhanced stability boundary and the switching frequency regulation at the steady state were discussed. This achieves robust closed-loop stability and a fixed-frequency operation at the steady state without sensing the input voltage. The proposed method significantly reduces the sampling and computational requirements; thus, this would be useful for high-frequency digital control implementation with fast transient performance.

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