An Integrated Multilevel Converter With Sigma–Delta Control for LED Lighting

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***Abstract*—LEDs have finally emerged as the dominant lighting technology. As such, the lighting industry values power converters that have high efficiency, unity power factor, minimal flicker, dimming, low cost, and a small form factor. This paper presents an integrated circuit (IC) LED driver that is designed to achieve these goals. It introduces multilevel converters with sigma–delta modulation to the power IC space. The driver features a pair of sigma–delta-controlled multilevel converters. The first is a multilevel rectifier responsible for power factor correction and dimming. The second is a bidirectional multilevel inverter used to cancel ac power ripple from the dc bus. The system also contains an output stage that powers the LEDs with dc and provides for galvanic isolation. The IC LED driver has been simulated and prototyped on a silicon fabrication process. Its functional performance indicates that integrated multilevel converters are a viable topology for lighting or other similar applications.**

***Index Terms*—Integrated circuits, inverters, lighting, power electronics, sigma delta modulation.**

I. Introduction and Background

A. Challenge of Driving LEDs

SOLID-STATE lighting is recognized for its efficiency, reliability, and environmental benefits. The combination of efficiency and lifespan makes LEDs the most economic choice for lighting. As such, it is important that the LED driver be equally inexpensive, efficient, and reliable.

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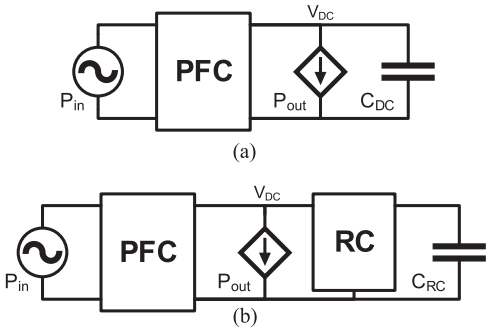

Fig. 1. Methods for reduction or cancellation of the 120-Hz power ripple from the driver's PFC input module. It is desirable for the driver's output to the LEDs, P_{out}, to be constant. (a) Passive RC involves the use of a large dc capacitor C_{DC} to filter the ripple. (b) Active RC strategy that involves the use of a separate power converter for RC. The RC module includes a storage capacitor C_{RC} that can be much smaller than C_{DC}.

cial in improving efficiency, reducing switch stress, and allowing for smaller switches. Quasi-resonant topologies improve on various switched-mode converter topologies by adding a small resonant tank near the power switch. Although the quasi-resonant tank does not regulate the output current, its presence allows for all the benefits of zero-voltage switching. Several quasi-resonant LED drivers have been proposed as soft-switching variations of the flyback [22] or boost [23] drivers.

Switched-capacitor (SC) converters have recently been in the research spotlight for low-to-moderate power conversion. As such, they have naturally been considered in lighting applications [17], [18]. The SC converter uses an array of switches and capacitors as a charge pump. Its major advantage is that no magnetics are required for fixed-ratio voltage conversion, making it very amenable to integration.

B. Power Ripple and Flicker

As mentioned in Section I-A, ac power ripple at the driver input can cause flicker on the LEDs. When a lamp operates with unity power factor, its input current $I\sin(\omega_0 t)$ is sinusoidal and in phase with the line voltage $V\sin(\omega_0 t)$. The resulting input power is

$$P_{\text{in}} = V\sin(\omega_0 t) I\sin(\omega_0 t) = \frac{VI}{2} - \frac{VI}{2}\cos(2\omega_0 t) = P_{\text{out}} + P_{\text{RC}} \quad (1)$$

where ω_0 is $2\pi 60$ in the U.S. The average power P_{out} represents the desired dc output to the LEDs. Since the 120-Hz ripple power P_{RC} contributes directly to 120-Hz flicker, it is desirable to cancel P_{RC} from the driver's output. The IEEE Standard 1789-2015 [24] suggests that 120-Hz flicker can be considered low risk below 10% flicker and has no effect below 4% flicker.

Many LED drivers use passive ripple cancellation (RC). As shown in Fig. 1(a), passive RC methods often require a postrectification dc capacitor bank, which must be large enough to filter the low-frequency ripple power. For high-capacitance and high-voltage applications, electrolytic capacitors are considerably more cost effective than ceramic capacitors. However, electrolytics can be problematic in LED drivers due to their bulk and limited lifespan [6], [25]–[28]. High driver temperatures speed the evaporation of the liquid electrolyte, which can cause the capacitor to fail within five years. Since LEDs last up to 20 years, addressing or removing the electrolytic capacitor can greatly improve the lifespan of the lamp. Additional problems with electrolytics include high resistive loss in aging capacitors and the potential to explode when stressed by a short circuit or hydrogen buildup.

In order to eliminate the electrolytic capacitor, there has been a push toward the research and development of high-quality LED drivers that employ active RC techniques [27]–[32]. Such techniques include multiple power conversion stages, DCM [28]–[30], resonant current control [31], and the addition of a separate RC module or energy buffer [27], [32], [33]. As shown in Fig. 1(b), the LED driver in this work utilizes a separate RC module that transfers the ripple energy to a storage capacitor C_{RC}. As shown in (1), the desired constant output power P_{out} can be achieved if P_{RC} is transferred to the storage capacitor. In order to transfer power to and from the storage capacitor C_{RC}, the active RC module can swing the voltage across C_{RC}, as explained in Section IV-B.

An active RC module has the benefit of greatly reducing the required capacitor size. As shown in Fig. 1, the passive RC strategy requires a central dc capacitor C_{DC}, while the active RC module requires a storage capacitor C_{RC}. Driver specifications often allow for a fractional amount of ripple power F to pass to the LEDs. As such, $P_{\text{RC}}F$ may be transferred to the LEDs, and $P_{\text{RC}}(1-F)$ must be transferred to C_{DC} or C_{RC}. The energy on C_{DC} or C_{RC} is developed from (1) as

$$P_{\text{cap}} = (1-F)P_{\text{RC}} = (1-F)\frac{VI}{2}\cos(2\omega_0 t)$$
$$E_{\text{cap}} = \int P_{\text{cap}} = -(1-F)\frac{VI}{4\omega_0}\sin(2\omega_0 t) + E_{\text{cap,avg}}. \quad (2)$$

The size of a capacitor capable of absorbing P_{cap} can be derived from the capacitor's energy swing as

$$\frac{1}{2}CV_{\text{cap,max}}^2 - \frac{1}{2}CV_{\text{cap,min}}^2 = 2(1-F)\frac{VI}{4\omega_0}$$
$$C(V_{\text{cap,max}} + V_{\text{cap,min}})(V_{\text{cap,max}} - V_{\text{cap,min}}) = (1-F)\frac{VI}{\omega_0}$$
$$C = (1-F)\frac{VI}{\omega_0(2V_{\text{cap,avg}})(V_{\text{cap,swing}})} \quad (3)$$

where $V_{\text{cap,swing}}$ is the maximum allowed peak–peak voltage range the capacitor can swing, and $V_{\text{cap,avg}}$ is the average dc voltage of the capacitor.

With passive RC, the capacitor voltage is coupled to the output voltage, as shown in Fig. 1(a). In this way, $V_{\text{cap,avg}} = V_{\text{DC}}$ and $V_{\text{cap,swing}} = V_{\text{DC}}F$. The required dc capacitor size is thus

$$C_{\text{DC}} = \frac{(1-F)}{2F}\frac{VI}{\omega_0 V_{\text{DC}}^2}. \quad (4)$$

The active RC strategy in Fig. 1(b) has a decoupled storage capacitor whose voltage can swing between ground and V_{DC}. With $V_{\text{cap,avg}} = V_{\text{DC}}/2$ and $V_{\text{cap,swing}} = V_{\text{DC}}$, the required storage capacitor size is

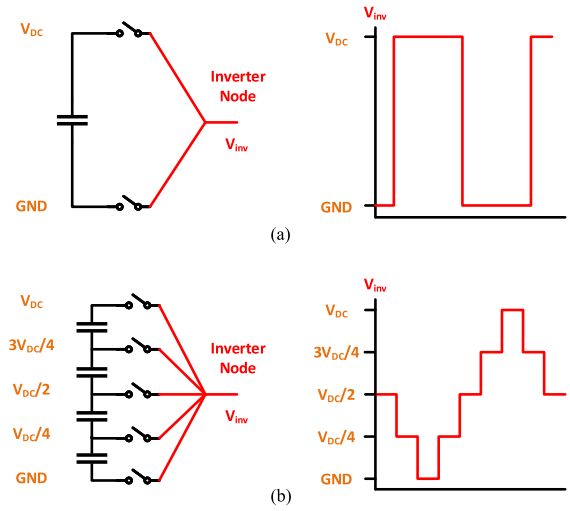

Fig. 2. Theoretical multilevel converters. $V_{\rm inv}$ can be connected to any of the levels of the dc capacitor bus, producing the output waveforms on the right. (a) Two-level inverter or half-bridge. (b) Five-level inverter.

$$C_{\rm RC} = (1-F)\frac{VI}{\omega_0 V_{\rm DC}^2} = (2F)C_{\rm DC}. \tag{5}$$

The result of this analysis shows that the required size of the passive method's dc capacitor $C_{\rm DC}$ is much larger than the required active method's storage capacitor $C_{\rm RC}$. Consider the design of a 20-W LED driver with $V_{\rm DC} = 180$ V and a fractional output ripple of $F = 0.066$, equivalent to an A19 incandescent bulb with 6.6% flicker [2], [3]. The driver requires $C_{\rm RC} = 1.5\ \mu$F or $C_{\rm DC} = 12\ \mu$F for active or passive RC, respectively. It can be shown that the passive driver will need a high-voltage electrolytic capacitor [34]. The required $C_{\rm DC}$ increases very quickly with lower flicker specifications.

C. Integrated Multilevel Converters as LED Drivers

This work introduces multilevel circuit methods to the LED driver space as a means of addressing the challenges in driving LEDs (see Section I-A), while also reducing the volumetric requirements for passive elements. Multilevel converters are a class of power converters that distribute the switching functionality and stress over an array of vertically stacked power switches. As shown in Fig. 2, multilevel converters are capable of connecting their inverter node to one of several dc levels. The dc levels are maintained on a dc bus, which is usually implemented with actively balanced capacitors.

Multilevel inverters have become popular in the last decade as a means to utilize lower voltage solid-state switches in high-voltage applications [35]. They have the advantage of reducing individual switch stress by distributing high voltage over multiple switches. Multilevel inverters also have the ability to output one of several voltage levels, thus allowing for greatly reduced harmonic content compared to the standard two-level inverter. This feature ultimately allows for reduction in a converter's switching frequency or passive filtering requirements. Various multilevel inverter topologies have been proposed, such as the diode-clamped [36], capacitor-clamped [37]–[40], and cascaded topologies [41]. Several multilevel inverter topologies can be simplified to function as rectifiers, such as the Vienna rectifier [42]. Multilevel topologies can also be useful for energy buffer circuits [33], [43].

Since multilevel converters involve many active devices, integrated circuit (IC) technology is a convenient means of producing an efficient low-cost LED driver with small form factor. IC applications often revolve around integrating full systems onto a single chip. However, many silicon processes have device voltage limitations that would present a challenge for the design of fully integrated power systems. As such, it is natural to develop the driver using a multilevel topology so as to reduce voltage stress on each individual power switch. Overall performance may be evaluated with techniques developed in the SC design frameworks [44], [45].

In this work, a multilevel topology allows the IC to interface with the line voltage despite its device voltage limitations. In addition, this topology reduces the requirements on passive elements in the driver. The multilevel circuit function is used in two positions: one to provide PFC rectification and a second to provide bidirectional power flow for RC. The generalized multilevel topology [46] is chosen because it addresses both of these functions and admits a fairly regular gate drive pattern. Other choices may very well be advantageous in optimizing die area.

Several control strategies exist for inverters and active rectifiers. Popular methods include sinusoidal pulsewidth modulation (PWM), space vector modulation [47], and selective harmonic elimination [48]. This work uses sigma–delta modulation [49] because of its simple implementation and direct mapping into the multilevel modulation function.

Sigma–delta modulation is often presented as a cost-effective strategy for analog-to-digital signal conversion in low-bandwidth applications. It is naturally attractive in switching converters, which require converting a low-bandwidth control signal to one of the discrete conduction states present in an H-bridge or multilevel converter. Switch modulation produces quantization noise, which is modeled as a white process with uniform noise power. Sigma–delta modulation invokes closed-loop control to shape the noise power spectrum [50]–[54]. In practice, the sigma–delta loop functions to push the quantization noise to higher frequencies, after which it can easily be filtered out. Intuitively, the output of the sigma–delta modulator attempts to best approximate the input.

Previous work has detailed the construction of diode- or capacitor-clamped multilevel inverters [36], [37], but very few have built a generalized multilevel converter. Sigma–delta control for multilevel inverters has been simulated in other papers [49], [55]–[58] but has seldom been put to practice, especially in rectification. Most importantly, this research introduces multilevel converters to the power IC space. DC–DC circuits such as the SC circuit have had the recent spotlight in the emerging field of power ICs [17], [44], [45], [59]. However, this research is the first to build a fully integrated multilevel converter, thus introducing a number of engineering benefits and challenges to the fields of multilevel converters and power ICs.

II. Full System Architecture

The full system in Fig. 3 contains an input PFC rectifier, an RC circuit, a dc capacitor bus, and an output stage. The PFC

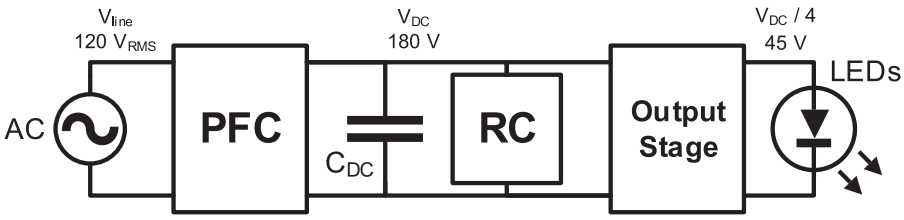

Fig. 3. Block diagram of the LED driver with PFC, RC, and output stage. C_{DC} indicates the dc capacitor bus.

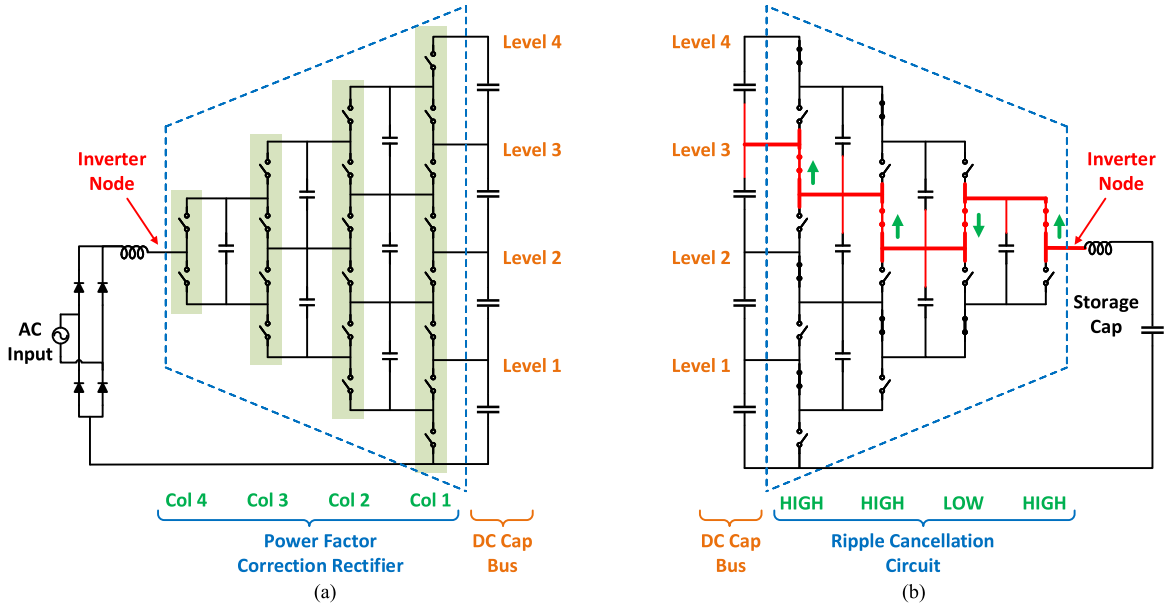

Fig. 4. Generalized multilevel schematic for the PFC rectifier and RC modules. The dc capacitor bus helps define the dc levels, buffers power flow, and connects to the output stage (not shown here). (a) PFC with switching columns highlighted in green. (b) RC module with an example switch configuration for connecting the inverter node to level 3. Note that the dc capacitor bus is shared among (a), (b), and the output stage in Fig. 6.

rectifier converts the ac line voltage to dc with low harmonic current injection and provides for input current regulation and dimming. The dimming level is directly controlled by the input current regulation, since subsequent stages simply convert this current and feed it to the LED string. Voltage regulation is effected by the LED string voltage–current characteristic. The RC circuit cancels ripple on the dc capacitor bus. Finally, the output stage downconverts the dc bus voltage and uses a small transformer to provide for galvanic isolation.

At full power, the system is designed to operate at 20 W, with an input voltage and current of 120 V_{RMS} and 167 mA_{RMS}, respectively. The nominal voltages of the internal dc bus and output LED string are, respectively, 180 and 45 V, but these voltages may vary by application and dimming level.

III. Multilevel Topology for PFC and RC Modules

The PFC rectifier and RC modules use a generalized multilevel topology, as shown in Fig. 4. Each switching column contains transistors that switch synchronously and alternate in complementary pairs. By switching the various columns high or low, the inverter node can be connected to any of the five dc levels. Each column connects to a set of smaller integrated flying capacitors, which assist in rapidly stabilizing the column voltages and serve as a supply for the gate drivers. This topology is bidirectional, allowing the circuit to be configured as a rectifier or inverter, for PFC and RC, respectively. It can also self-balance the dc capacitor bus such that the voltages across the dc capacitors are equal [46].

The PFC rectifier functions to enforce unity power factor and control the input power. As shown in Fig. 4(a), the PFC rectifier can control the voltage at the inverter node. In this way, the PFC rectifier can set the voltage across the input inductor and, thus, control the input current. Fine control over the input current enables harmonic reduction and allows for dimming via current control.

As mentioned in Section I-B, 120-Hz input power ripple can cause LED flicker. The RC module functions to actively cancel ripple from the dc capacitor bus. As shown in Fig. 4(b), the RC circuit is able to transfer ripple energy from the dc capacitor bus to the storage capacitor by precisely swinging the storage capacitor voltage. This allows for a huge reduction in the required dc capacitor size and obviates the need for electrolytics.

IV. Sigma–Delta Control

The multilevel converters in the PFC and RC modules are controlled via sigma–delta modulation. In this context, the

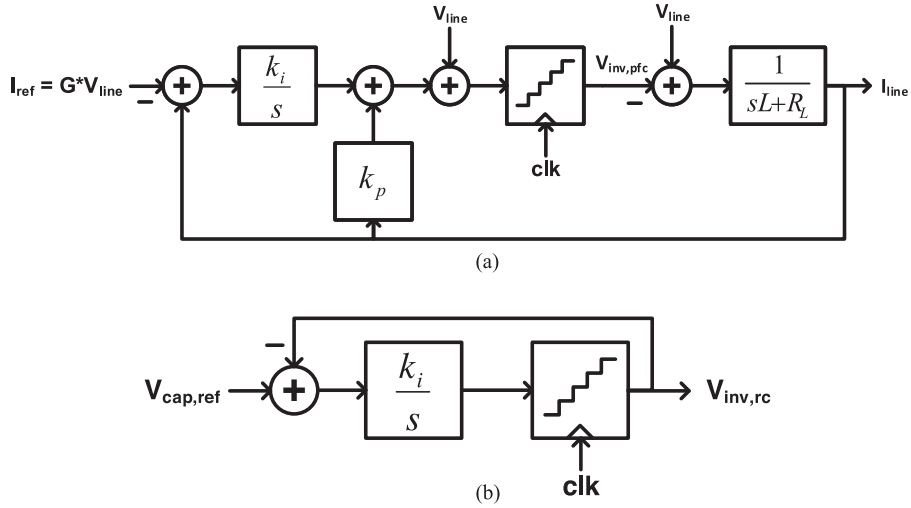

Fig. 5. Sigma–delta control loops for the PFC rectifier and RC modules. Each loop has an integrator and a quantizer clocked at 400 kHz. (a) Second-order sigma–delta loop is used for the PFC rectifier. The first pole is obtained from the input inductor with inductance L and series resistance R_L. The voltage across the inductor is the difference between the line voltage $V_{\rm line}$ and the inverter node of the PFC rectifier $V_{\rm inv,pfc}$. The second pole is obtained from the control blocks with integral gain k_i and proportional gain k_p. Negative feedback causes the input current $I_{\rm line}$ to closely track a reference current $I_{\rm ref}$. Dimming is adjusted via the input gain G, which scales the line voltage waveform to the intended input current level. (b) First-order sigma–delta loop is used for the RC module. This module uses the sigma–delta loop to set the inverter node of the RC circuit $V_{\rm inv,rc}$ to approximate a preprogrammed waveform $V_{\rm cap,ref}$.

multilevel converter behaves like a quantizer, since it can only set the inverter node to one of several quantized levels. Like any quantizer, the multilevel converter produces quantization noise. Sigma–delta modulation invokes closed-loop control to push the quantization noise to higher frequencies, after which it can easily be filtered out [50]. Intuitively, the output of the sigma–delta modulator will attempt to best approximate the input.

As a control scheme, sigma–delta modulation has the distinct advantage of simplicity. Fig. 5(b) suggests that a simple first-order sigma–delta control loop could be implemented with a single integrating operational amplifier. Sigma–delta modulation also has the advantages of closed-loop robustness and stability, assuming that the loop is properly designed. Finally, the quantization behavior of the multilevel converter causes sigma–delta modulation to simply be a very convenient control scheme. PWM is rather difficult and complicated for multilevel converters because a triangle wave must be generated between each level. Techniques such as space vector modulation and selective harmonic elimination all require complicated control.

A. Control for the PFC Rectifier

The PFC rectifier uses a second-order sigma–delta loop to set the line current to best approximate a reference current waveform. As shown in Fig. 5(a), the reference current waveform $I_{\rm ref}$ is nominally sinusoidal and in-phase with the line voltage. Sigma–delta control is especially useful because its ability to shape quantization noise is necessary for meeting the line-current harmonic specifications. The variable current control factor G can modulate the amplitude of $I_{\rm ref}$, which ultimately controls the input power. In this way, LED dimming is achieved by decreasing G and thus choking the driver's input power.

The control loop design in Fig. 5(a) allows for the adjustment of the integral gain k_i and the proportional gain k_p. It is often reasonable to set

$$K = (k_i/f_s)(\Delta/\delta) = 1 \tag{6}$$

where the quantizer is clocked at frequency f_s, and its quantization levels step by Δ at the output and δ at the input [56], [57]. If $K >> 1$, the quantizer may attempt to switch by more than one level at a time. If $K << 1$, the quantizer output may experience dead zones, in which it does not switch when it should. After f_s and k_i are selected, k_p can be chosen to help shape the quantization noise curve. In this work, $L = 10$ mH, $R_L = 2\,\Omega$, $k_i =$ 1e7, and $k_p = 25$. The PFC rectifier samples at $f_s = 400$ kHz.

B. Control for the RC Module

The RC module uses sigma–delta modulation to swing the storage capacitor voltage such that the 120-Hz power ripple is cancelled from the dc bus. The 120-Hz ripple power $P_{\rm RC}$ is previously developed in (1) and does not account for internal driver losses. An ideal active RC module transfers all of $P_{\rm RC}$ to the storage capacitor. As such, the ideal voltage waveform $v_{\rm cap,ref}$ on the storage capacitor is derived from its energy $E_{\rm RC}$ as

$$E_{\rm RC}(t) = \frac{1}{2}C_{\rm RC}v^2_{\rm cap,ref}(t) = \int_{-\infty}^{t} P_{\rm RC}(t) \tag{7}$$

$$v_{\rm cap,ref}(t) = \sqrt{-\frac{VI}{2\omega_0 C_{\rm RC}}\sin(2\omega_0 t) + \frac{V^2_{\max}+V^2_{\min}}{2}} \tag{8}$$

for storage capacitance $C_{\rm RC}$. $V_{\max}$ and $V_{\min}$ are, respectively, the maximum and minimum levels that the storage capacitor voltage should be constrained to.

In this work, the RC module relies on open-loop control with a lookup table parameterized by dimming level command, e.g., power level. Each $v_{\rm cap,ref}$ waveform stored in the lookup table corresponds to one half-period of data. The data are actually the

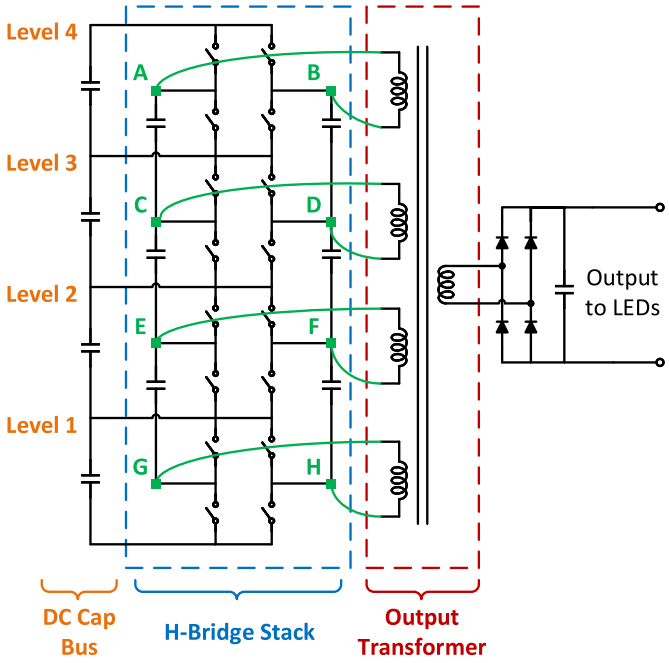

Fig. 6. Output stage is comprised of an integrated H-bridge stack and an output transformer. The H-bridge stack is clocked at 50 kHz. Note that the dc capacitor bus is shared with the circuits in Fig. 4.

modulation waveform, generated with a system, as indicated in Fig. 5(b). In practice, the waveform is triggered by the line voltage zero crossing.

V. Output Stage

As shown in Fig. 6, power is provided to the LEDs through the output stage, which consists of an array of stacked H-bridges and an output transformer. The output stage functions as a fixed-ratio 4:1 series–parallel step-down circuit, which serves to step the 180-V dc capacitor bus voltage down to the 45-V LED output. Another function of the output stage is to facilitate in balancing the voltage levels on the dc capacitor bus, which is crucial for correct operation of the PFC and RC modules.

Each of the inverter nodes in the H-bridge stack is connected to a small isolation transformer. This transformer has four primary windings and one secondary, all of which have the same number of turns. The transformer is useful in galvanically isolating the LEDs from the high-voltage circuits and in facilitating the series–parallel connection of this stage. In addition, it provides soft switching to the H-bridge stack via its leakage and magnetizing inductance. This transformer is not designed to store energy, so it can be substantially smaller than that of an equivalent flyback converter. Its size is determined by the desired switching frequency of the H-bridge stack. Even with a small toroid, the H-bridge stack can be clocked at 50 kHz or lower.

An alternative output stage topology, the hybrid resonant switched-capacitor (HRSC) converter, is discussed in [17]. In the HRSC topology, the H-bridge stack does not require an output transformer, but instead achieves galvanic isolation via capacitive coupling to a resonant tank. Adjusting the switching frequency of the H-bridge stack adjusts the driving frequency of the resonant tank, thereby providing a secondary means of current control to the LEDs. The main disadvantage of the HRSC is that it must switch in the megahertz range in order to leverage a reasonably sized resonant tank for current control. In addition, the coupling capacitors have to withstand the relatively high resonant tank voltage. Although Le *et al.* [17] demonstrate the HRSC as a viable alternative, the LED driver in this work uses the transformer output topology (see Fig. 6) because the PFC rectifier already provides for current regulation.

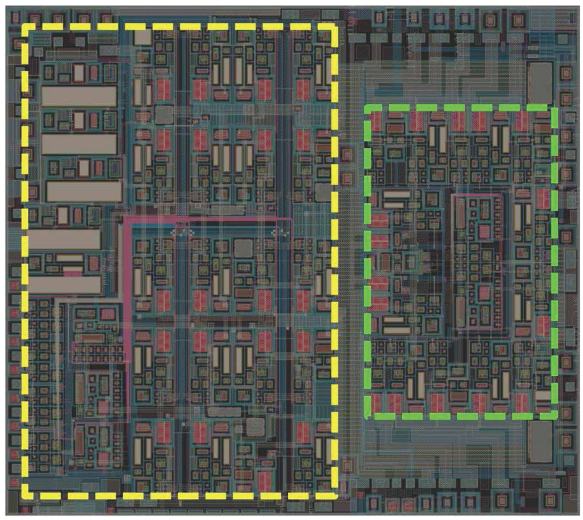

Fig. 7. Prototype IC layout with dimensions of 7.08 mm × 6.28 mm. The multilevel converter is on the left (yellow). The H-bridge stack is on the right (green).

VI. Experimental Results

A. Integration and Testing

The full system from Fig. 3 has been simulated, experimentally tested, and verified. A prototype IC, shown in Fig. 7, was designed and fabricated on an analog–bipolar-CMOS-DMOS (ABCD) high-voltage process. The IC contains the circuitry for a multilevel converter and an H-bridge stack. Both circuits use 100-V n-type LDMOS transistors as their power switches, and every power switch requires an integrated gate driver.

The architecture for the chip's gate driver is shown in Fig. 8. Each gate driver consists of a floating channel supply generator, a level shifter, and a driver. The channel supply uses power from a dc or flying capacitor to create a floating 5-V supply. Its function is to provide power to the level shifter and the driver. The level shifter is responsible for shifting a low-voltage digital signal up to the floating voltage domain. Finally, the driver is an inverter that amplifies the floating digital signal with enough power to drive the gate capacitance of the power switch. Additional details about the design of the gate driving channel are discussed in [17].

The test board in Fig. 9 is implemented on a two-layer printed circuit board, and the system is controlled via off-chip components and a Xilinx Spartan-3 field-programmable gate array (FPGA). These off-chip functions can be readily integrated on a

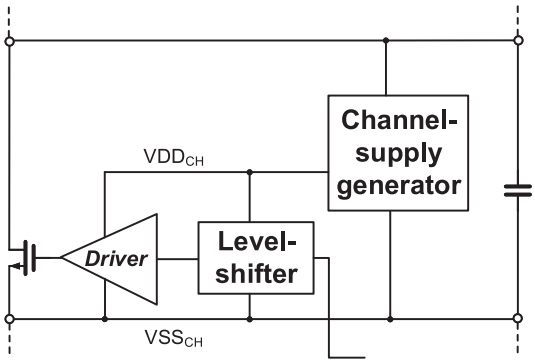

Fig. 8. LDMOS power switch and its gate driving channel. Each channel consists of a floating channel supply, a level shifter, and a driver (inverter). The channel supply bootstraps off a flying capacitor and generates the $\mathrm{VDD_{CH}}$ voltage at 5 V above $\mathrm{VSS_{CH}}$.

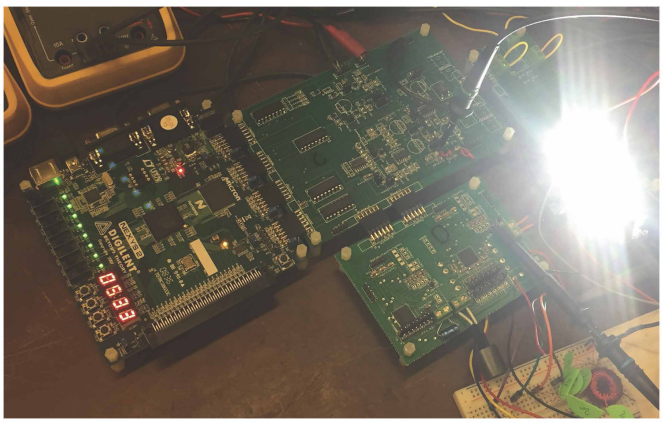

Fig. 9. Board and laboratory setup. The power board (lower left of the LEDs) contains two ICs: one for the PFC rectifier and one for the RC module. The FPGA board (left) attaches to the control board (top center). All of the control logic can be integrated in CMOS on the IC.

TABLE I
POWER COMPONENTS USED IN THE PROTOTYPE LED DRIVER

Component	Part Number	Desc.	Dim. (mm)	Qty.
PFC Inductor	RFS1317-825KL	8.2 mH 0.25 A	13.3x13.3x16	1
Ripple Canc. Inductor	RFB0810-102L	1 mH 0.35 A	9.5x9.5x11.5	1
Transformer Toroid	C055379A2		18.1x18.1x7.1	1
DC Bus Caps	C3216X7R2A 105K160AA	1 uF 100 V	3.2x1.6x1.3	4
Ripple Canc. Storage Cap	SK052E475ZAR	4.7 uF 200 V	12.7x5.1x14.2	1-2
Input Bridge	DF02S-E3/45	200 V	8.5x6.5x3.3	1
Output Bridge	PD3S160-7	60 V	1.9x1.3x0.7	4

subsequent design turn and require very small die area. Table I shows a full list of required external components (not including the pair of multilevel converter chips).

B. Data and Results

The waveforms in Fig. 10 demonstrate functionality. The PLECS simulation waveforms shown in Fig. 10(a) and (b) can be compared to the experimental scope waveforms shown in Fig. 10(c) and (d). Fig. 10(a) and (c) shows that the PFC rectifier can limit harmonics on the line current (green) and ensure that it is in phase with the line voltage (yellow). The PFC inverter node (blue) of the PFC is shown to utilize all four levels. Fig. 10(a) and (b) shows that the RC module can cancel the ac ripple from the dc capacitor bus. Swinging the storage capacitor voltage (purple) allows the dc voltage at level 4 (green) to be almost entirely devoid of ripple.

Fig. 11 shows a fast Fourier transform (FFT) of the line-current input. Standards such as IEC 61000-3-2 (US) and EN 61000-3-2 (Europe) specify the acceptable limitations on specific line-current harmonics [60]. For lighting applications, these standards specify that the fifth harmonic must be less than 10% of the fundamental. In this work, the fifth harmonic is 4.6% of the fundamental. Higher harmonics are required to be less than 3% of the fundamental, and these specifications are also met.

The test part did not function at the full rated voltage, but was testable to approximately half of the rated voltage. This was due to an unfixable process error with the metal finger capacitors in the channel supply generator (see Fig. 8). High-voltage swings would cause $\mathrm{VDD_{CH}}$ to latch below $\mathrm{VSS_{CH}}$. The leakage current due to this defect would drain the flying bootstrap capacitor and lead to catastrophic failure at higher voltage. As such, data are only reported for operation at input voltages up to 45 $\mathrm{V_{RMS}}$.

Fig. 12 shows how the efficiency varies over input voltage and current. A comparative analysis with modeled performance is given in Fig. 13 to inform understanding of the results. For the lower input voltages, the modeled loss (multicolored bar) can be compared with the actual measured loss (dark blue bar). The measured losses were well modeled, though slightly higher than predicted in modeling.

C. Applicability of an Integrated Multilevel LED Driver

The prototype LED driver is functional in dimming, regulating the line-current harmonics, and canceling the input ripple power without an electrolytic capacitor. However, it fails to meet the desired specifications of input voltage range and efficiency. As mentioned above, the input voltage is limited because of a process error. The ABCD process nominally supports up to 220 V on die, which would have otherwise allowed up to a 120-$\mathrm{V_{RMS}}$ input. Most of the conduction losses decrease with the square of the voltage ($P = V^2/R$), and the loss model in [61] and [62] predicts the efficiency to approach 90% with a 120-$\mathrm{V_{RMS}}$ input.

Despite these shortcomings, industrially developed integrated multilevel LED drivers could have the potential to greatly improve on cost and size compared to the industry standard flyback driver. First, the multilevel nature of the PFC rectifier allows the input inductor to be smaller than the inductor in a flyback driver's EMI filter. In addition, the toroidal isolation transformer at the

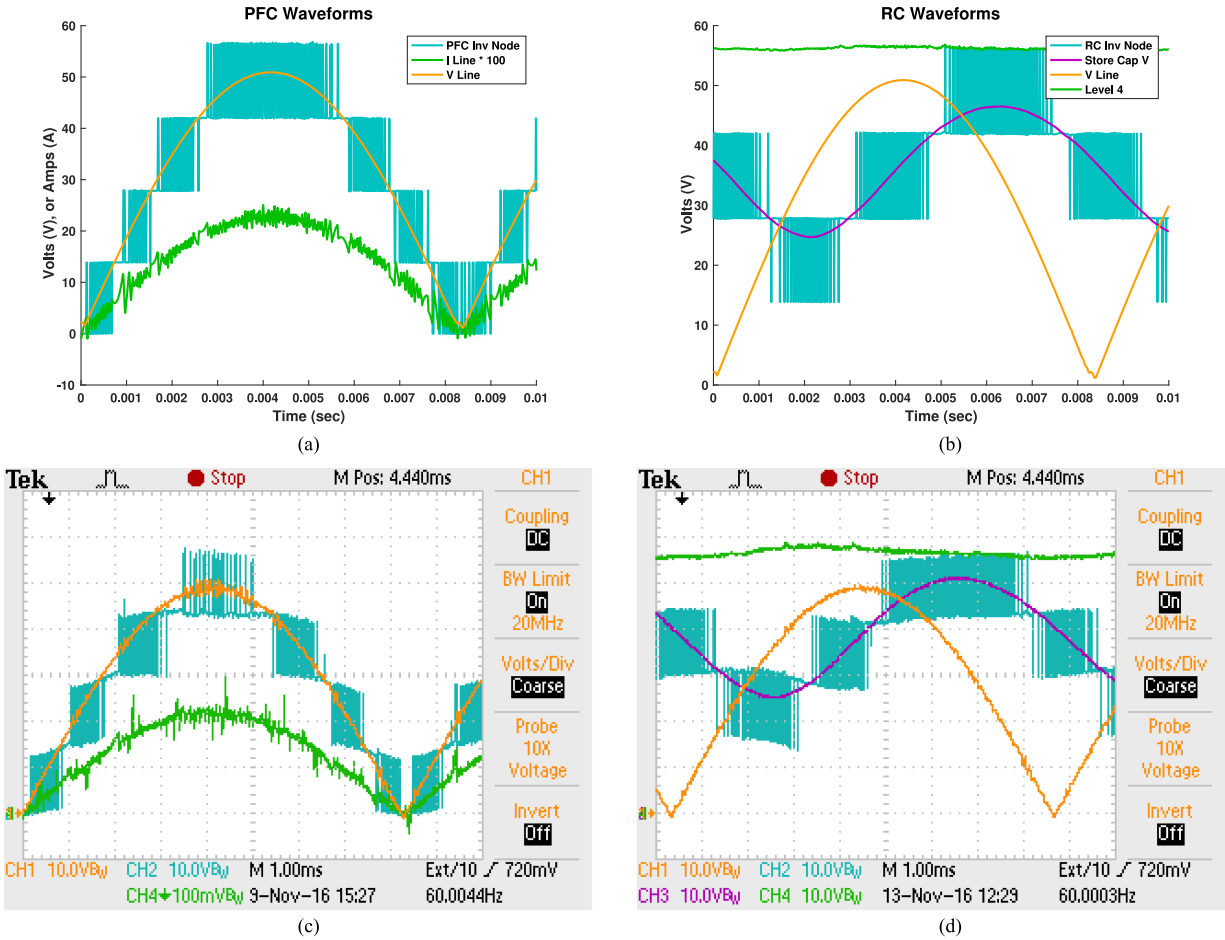

Fig. 10. Simulated and experimental waveforms that demonstrate the functionality of the PFC rectifier and RC modules. (a) Simulated PFC waveforms with the line voltage (yellow), line current (green), and the PFC rectifier inverter node of Fig. 4(a) (blue). The line current is scaled by 100 for visibility. (b) Simulated RC module waveforms. Waveforms include the line voltage (yellow), the voltage at level 4 of the dc capacitor bus (green), the voltage across the storage capacitor (purple), and the RC module inverter node from Fig. 4(b) (blue). (c) Experimental PFC rectifier waveforms from oscilloscope; waveforms correspond to (a). The line current (green) is measured as the voltage across a 1-Ω current sense resistor, and the amperage is directly equal to the measured voltage. Horizontal divisions are 1 ms. Vertical divisions are 10 V for the line voltage (yellow) and PFC rectifier inverter node (blue) and are 100 mV for the line current (green). (d) Experimental RC module waveforms; waveforms correspond to (b). Horizontal divisions are 1 ms and vertical divisions are all 10 V.

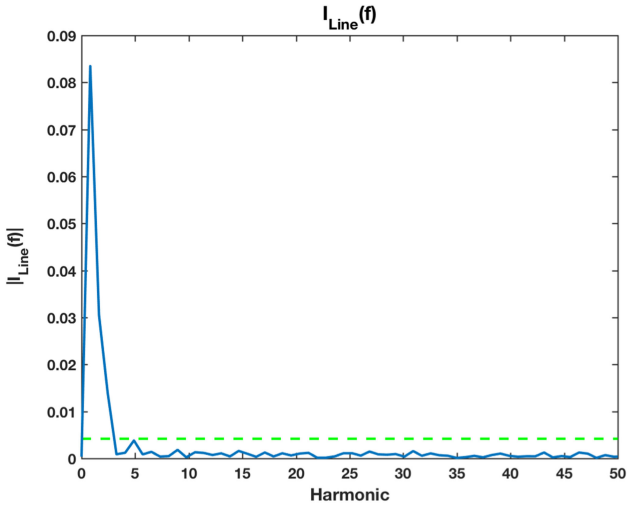

Fig. 11. FFT of the line-current input I_{Line}. Line-current harmonics are all less than 5% of the fundamental (indicated by green-dashed line). Data are obtained at an ac input voltage of 36 V_{RMS} and an ac input current of 68.5 mA_{RMS}.

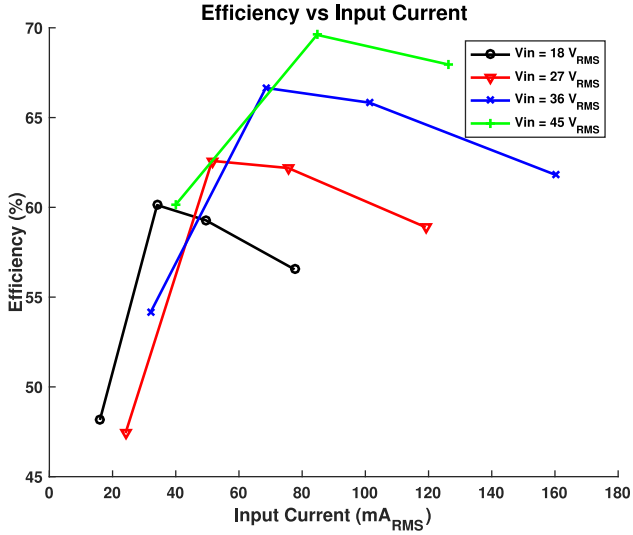

Fig. 12. Efficiency versus input current. The output voltage was set at the optimal value using an electronic load. In general, the output voltage and current are determined by the total voltage drop of the series LED string.

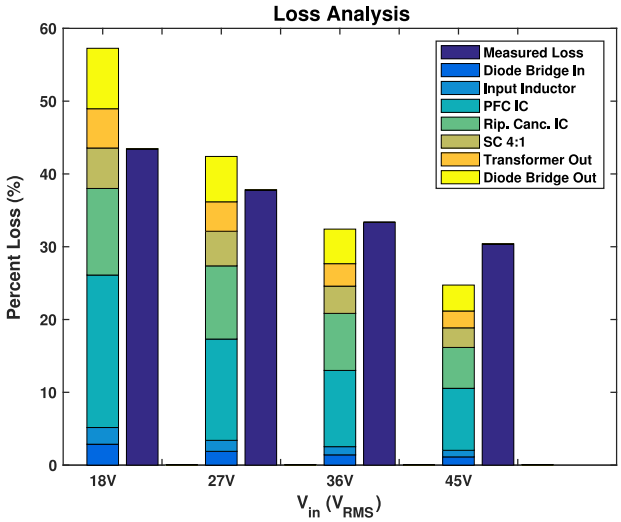

Fig. 13. Loss versus input voltage at an input current of 80 mA. The lower voltages each compare a loss model (left bar) to the actual measured loss (right dark blue bar). The loss model can provide an indicative projection of how the driver would perform at higher input voltage.

output stage is not designed to store energy and, thus, can be much smaller than a flyback transformer. In theory, the total switch die area in an integrated multilevel converter should be less than the single switch in the flyback converter [44], [45]. However, the gate drive circuitry became unexpectedly large due to the isolation requirements in supporting floating gate drivers. Finally, it is important to reiterate that the active RC module is crucial in obviating the electrolytic capacitor and increasing the driver's lifespan.

Integrated multilevel circuits have many potential benefits, and further research in the area is recommended. The authors suggest two main ways to improve this work, and a more detailed discussion is presented in [62]. First, a capacitor-clamped multilevel topology should be used instead of the generalized multilevel topology. The capacitor-clamped topology has fewer switches, and the power density demonstrated in [38]–[40] suggests the potential for a die area reduction (although larger flying capacitors would be required). In addition, this topology alleviates many of the robustness issues present in the generalized topology that arise because of the floating gate drivers in columns 2, 3, and 4. Second, the authors recommend substituting every other NMOS power switch for an equivalent PMOS. PMOS switches, in conjunction with a capacitor-clamped topology, have the potential to eliminate the need for floating gate drivers altogether. Fixed gate drivers are far more robust and require less die area.

VII. Conclusion

This paper documents the design, fabrication, and testing of an IC LED driver based on a multilevel topology. The multilevel PFC rectifier converts ac to dc, cancels line-current harmonics, and controls the input power. The multilevel RC module swings the voltage on a storage capacitor in order to cancel ripple from the dc capacitor bus. Both modules are controlled via sigma–delta modulation.

While multilevel converters have proven to be practical for high-voltage electronics, this work demonstrates their potential to be practical in the IC space. The multilevel topology was shown to be particularly useful for expanding the capabilities of any IC process that has devices with a relatively low drain–source breakdown voltage ($V_{\mathrm{DS,max}}$). With careful and robust design, integrated multilevel converters show great promise for lighting and household electronics.

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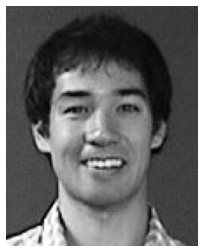

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