Advanced Single-Phase DSC-Based PLLs

Saeed Golestan, *Senior Member, IEEE*, Josep M. Guerrero, *Fellow, IEEE*, Juan C. Vasquez, *Senior Member, IEEE*, Abdullah M. Abusorrah, *Senior Member, IEEE*, and Yusuf Al-Turki, *Senior Member, IEEE*

***Abstract*—In three-phase systems, using the delayed signal cancelation (DSC) operators is one of the most popular approaches for designing advanced phase-locked loops (PLLs), particularly for applications where a high disturbance rejection ability is demanded. In single-phase systems, however, they have not received a considerable attention. The aim of this paper is to develop advanced DSC-based PLLs for single-phase applications. To this end, three PLLs are designed and presented. The first is based on adaptive DSC operators, and the other two are based on nonadaptive operators. The design aspects of these PLLs are discussed in detail, and their performances are evaluated using experimental results.**

***Index Terms*—Delayed signal cancelation (DSC), filters, frequency estimation, phase detection, phase-locked loop (PLL), single-phase systems, synchronization.**

I. Introduction

THE high flexibility (customizability), implementation simplicity, and effectiveness of the delayed signal cancelation (DSC) operator, which is a finite impulse response (FIR) filter, have made it an interesting option for signal processing purposes in power and energy applications, particularly for designing synchronization techniques [1]. This operator has two different types: the first is often employed in the *dq* frame and, therefore, is referred to as the *dq*-frame DSC (*dq*DSC) operator, while the second is utilized in the $\alpha\beta$ frame and, hence, is called the $\alpha\beta$-frame DSC ($\alpha\beta$DSC) operator. It is worth mentioning here that, regardless of the working frame of the DSC operators, typically, multiple operators are cascaded, and a chain is formed because a single operator has a limited ability in rejecting disturbances. A chain of cascaded DSC (CDSC) operators in the *dq* and $\alpha\beta$ frames are briefly referred to as the *dq*CDSC and $\alpha\beta$CDSC operators, respectively. In what follows, a brief review of the historical development of the DSC operator and its

Manuscript received January 18, 2018; revised March 9, 2018 and May 6, 2018; accepted June 29, 2018. Date of publication July 17, 2018; date of current version February 20, 2019. This work was supported by by the Deanship of Scientific Research (DSR), King Abdulaziz University, Jeddah, under Grant 264-135-D1435. Recommended for publication by Associate Editor M. S. El-Moursi. *(Corresponding author: Saeed Golestan.)*

S. Golestan, J. M. Guerrero, and J. C. Vasquez are with the Department of Energy Technology, Aalborg University, Aalborg DK-9220, Denmark (e-mail:

In [10], a study on *dq*CDSC-PLLs is conducted. This study includes a systematic design approach for selecting the control parameters of *dq*CDSC-PLLs, presenting a method for enhancing the dynamic performance of these PLLs, analyzing the advantage/disadvantages of the *dq*CDSC-PLLs, and proving the equivalence of *dq*CDSC-PLLs and moving-average-filter-based PLLs (MAF-PLLs) [11] under certain conditions.

In [12], an efficient implementation of an SRF-PLL with a chain of $\alpha\beta$DSC operators in its input is suggested. In this work, it is proposed to remove the frequency feedback loop and keep the $\alpha\beta$DSC operators nonadaptive. The phase offset and amplitude scaling errors caused by these nonadaptive operators are then corrected in the SRF-PLL output using simple yet efficient compensators. This idea results in a great simplicity compared to the structures proposed in [5]–[7]. The problem is that the nonadaptive operators may not effectively reject the disturbances (particularly the FFNS component) when the grid frequency deviation from the nominal value is very large. This PLL structure is called the enhanced GDSC-PLL.

In [13], an axis drift control (ADC) for adapting the $\alpha\beta$DSC operators in the PLL input is presented. This ADC acts like a parallel frequency detector and synchronizes the operators to the grid frequency changes. The modeling and tuning procedure of the resultant PLL, which is called the ADC-PLL, are also discussed in [13].

In [14], a research on three-phase PLLs with a chain of variable-length (frequency-adaptive) DSC operators in their input is conducted. This study mainly includes a general approach for the small-signal modeling of these PLLs and tuning their control parameters. The GDSC-PLL [5] and CDSC-PLL [7] are considered as the case studies of this research, and a performance comparison between them is also conducted. The obtained results in [14] demonstrate no large performance difference between these structures. Based on this finding and the lower computational burden of the CDSC-PLL, it is concluded in [14] that the CDSC-PLL is a better choice than the GDSC-PLL.

Combining the DSC operators and fuzzy controllers to enhance the PLL dynamic performance [15], [16], cascading a DSC operator and a second-order-generalized-integrator-based filter before the PLL input to improve its filtering capability [17], using a DSC operator, a MAF, and a phase lead compensator inside the PLL control loop to achieve a satisfactory speed/accuracy/simplicity tradeoff [18], and the simultaneous application of DSC operators before and inside the PLL control loops [19] are also worth pointing out here. These approaches are not described in detail to save the space.

All these works reviewed so far were about three-phase PLLs. It, however, does mean that the DSC operators are only applicable to three-phase PLLs. Indeed, some attempts for enhancing the performance of single-phase PLLs using the DSC operators have also been made. For example, to deal with the double-frequency oscillatory ripple in a power-based PLL (pPLL), which is a standard PLL in single-phase applications [20], including two cascaded *dq*DSC operators with $1/4$ cycle delay length in the pPLL control loop is suggested in [21]. These *dq*DSC operators effectively reject the double-frequency oscillatory ripples but at the cost of creating a large phase delay in the pPLL control loop and, hence, considerably slowing down its dynamic response. In [22], an enhanced PLL (EPLL) structure [23] is considered as the basic unit, and a combination of $\alpha\beta$DSC and *dq*DSC operators is included in its structure to enhance its filtering ability. To be more exact, an $\alpha\beta$DSC operator with $1/2$ cycle delay length is included in the EPLL input to remove the dc offset and all even-order harmonics up to the aliasing point, and four *dq*DSC operators with $1/4$, $1/8$, $1/16$, and $1/32$ cycle delay length are included in the phase and amplitude estimation loops to remove the rest of the harmonics. These *dq*DSC operators, however, as mentioned before, make the EPLL dynamic response slow.

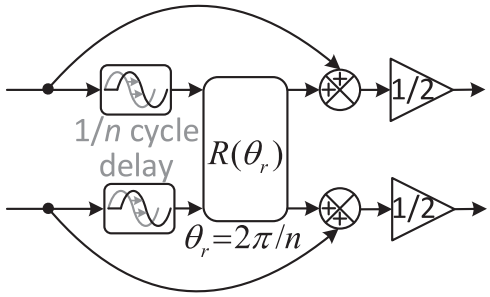

Fig. 1. Implementation of an $\alpha\beta$DSC operator.

In summary, the DSC filters offer a great potential for designing advanced PLLs. The focus of researchers, however, has been mainly on three-phase applications, and limited works have been conducted for single-phase applications. The aim of this paper is covering this gap and presenting advanced single-phase DSC-based PLLs.

The rest of this paper is organized as follows. In Section II, a review on the $\alpha\beta$DSC operator is conducted. In Section III, an advanced single-phase PLL using frequency-adaptive $\alpha\beta$DSC operators is designed. In Section IV, two advanced single-phase PLLs using nonadaptive $\alpha\beta$DSC operators are designed. In Section V, a performance comparison among all designed PLLs is carried out. Section VI concludes this paper.

II. $\alpha\beta$DSC Operator

The $\alpha\beta$DSC operator, as mentioned before, is an FIR filter. When extracting the FFPS component is intended, this operator is defined in the Laplace domain as [7]

$$\alpha\beta\mathrm{DSC}_n(s) = \frac{1}{2}\left[1 + e^{\frac{j2\pi}{n}} e^{-\frac{T}{n}s}\right] \tag{1}$$

where n is called the delay factor and T is the grid fundamental period. Fig. 1 illustrates the implementation of an $\alpha\beta$DSC operator, in which the rotation matrix $R(\theta_r)$ is

$$R(\theta_r) = \begin{bmatrix} \cos(\theta_r) & -\sin(\theta_r) \\ \sin(\theta_r) & \cos(\theta_r) \end{bmatrix}. \tag{2}$$

Notice that $\theta_r = 2\pi/n$.

Using (1), the frequency response of the $\alpha\beta$DSC operator can be expressed as

$$\alpha\beta\mathrm{DSC}_n(j\omega) = \left|\cos\left(\frac{T\omega - 2\pi}{2n}\right)\right| \angle -\left(\frac{T\omega - 2\pi}{2n}\right). \tag{3}$$

Based on (3), the following observations are made.

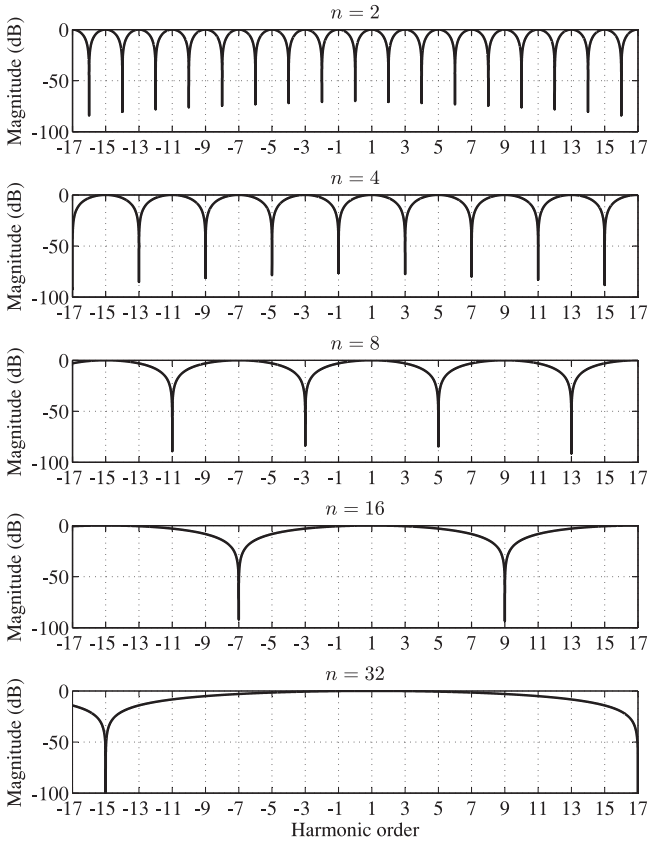

Fig. 2. Magnitude-frequency response of the $\alpha\beta$DSC operator for different values of the delay factor n.

1) For any value of the delay factor n, the operator passes the FFPS component.
2) The delay factor n determines those disturbances that the operator blocks.
3) A single operator may not be good enough to deal with the grid voltage disturbances in most of the practical scenarios, and a chain of operators with different delay factors is required.

These facts can be better visualized from Fig. 2, which illustrates the magnitude-frequency response of the $\alpha\beta$DSC operator for different values of the delay factor n.

III. Designing an Advanced Single-Phase PLL Using Frequency-Adaptive $\alpha\beta$DSC Operators

Fig. 3 illustrates the block diagram of the CDSC-PLL [7], which has been proposed for three-phase applications. The CDSC-PLL includes a chain of five $\alpha\beta$DSC operators with delay factors 2, 4, 8, 16, and 32, a standard SRF-PLL, and a frequency feedback loop for adjusting the length of delays of operators. This combination of operators is able to reject the dc offset and all harmonics of the grid voltage of both the positive and negative sequences up to the aliasing point, except for those of order -31, $+33$, -63, $+65$, etc. Fig. 4 illustrates the frequency response of this chain. A powerful yet relatively simple single-phase synchronization tool can be made from Fig. 3 by applying some modifications/simplifications to it. These modifications/simplifications are as follows.

1) The Clarke's transformation is removed as there is only one input signal.
2) The single-phase signal v_g is multiplied by 2 and is considered as the α-axis input signal of the operators, and the β-axis input signal is set to zero. Notice that the $\alpha\beta$DSC operators are basically complex (as opposed to real) filters, and from their point of view, the single-phase input signal is an imbalanced signal. Multiplying this signal by 2 causes an FFPS component with the same amplitude as that of the single-phase signal v_g in the input of operators. This fact is clear from (4), in which $v_g(t) = V\cos(\theta)$ (V and θ denote the amplitude and the phase angle, respectively) is the single-phase input signal

$$\begin{aligned} v_\alpha(t) &= 2v_g(t) = 2V\cos(\theta) = V\cos(\theta) + V\cos(-\theta) \\ v_\beta(t) &= 0 = V\sin(\theta) + V\sin(-\theta). \end{aligned} \tag{4}$$

3) The first operator has a delay factor equal to 2. Therefore, according to (2), its rotation matrix has -1 on the main diagonal and zeros elsewhere. It means that there is no coupling between the α- and β-axis of this operator. Considering that the β-axis input of this operator is equal to zero, its β-axis output will be equal to zero too. This results in some simplifications in the implementation. Further simplifications can be applied by understanding that the β-axis input of the second $\alpha\beta$DSC operator, which has a delay factor equal to 4, and the diagonal elements of its rotation matrix are all equal to zero.
4) As shown in Fig. 3, the output of the proportional–integral (PI) controller is considered as an estimate of the frequency. This signal is then passed through a low-pass filter (LPF) and used for calculating the grid voltage period. This LPF is mainly responsible for filtering high-frequency noise and avoiding a large transient in the feedback signal. The same objectives can be achieved by considering the PI controller integrator output as the estimated frequency [23], [24]. Therefore, for the sake of implementation simplicity, the LPF is removed, and the output of the integrator of the PI regulator is considered as the estimated frequency.
5) Selecting the PI controller integrator output as the estimated frequency means that the input of this integrator is an estimation of the rate of change of frequency. Therefore, a controllable phase lead in the feedback loop may be provided by adding a factor of this signal to the frequency feedback signal. This phase lead is useful in enhancing the PLL dynamic performance.

Applying the above-mentioned modifications/simplifications to Fig. 3 results in Fig. 5. This structure is briefly referred to as the adaptive 1ϕ-CDSC-PLL, where *adaptive* indicates that this PLL uses frequency-adaptive operators, and 1ϕ means that it is for the single-phase applications.

Considering the modeling procedure presented in [14], the small-signal modeling of the adaptive 1ϕ-CDSC-PLL is quite straightforward. The model of this PLL is shown in Fig. 6.

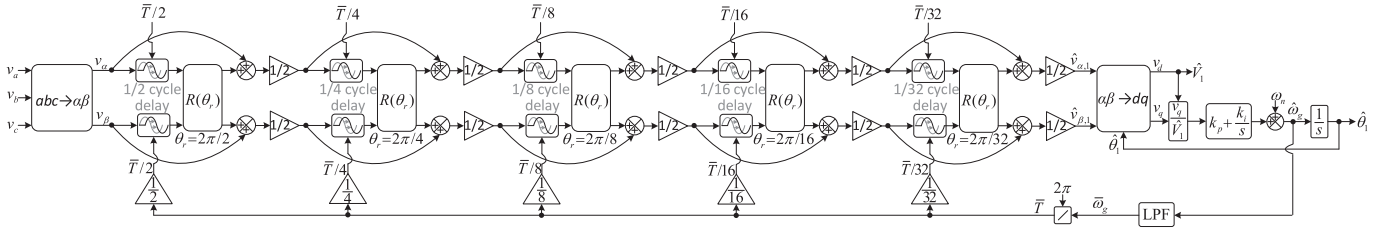

Fig. 3. Block diagram of the CDSC-PLL.

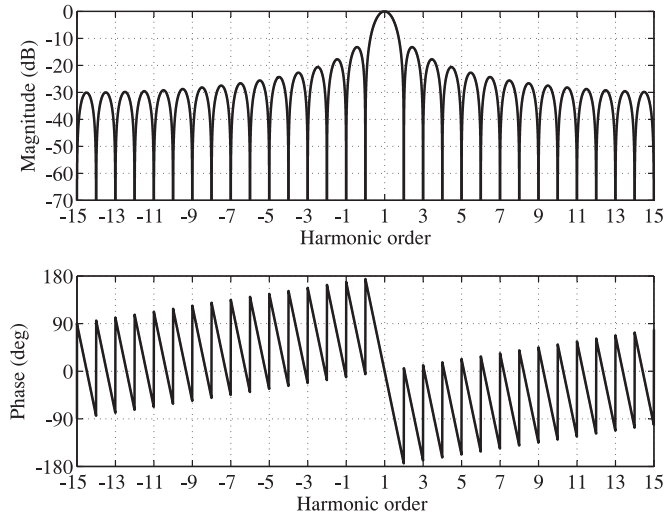

Fig. 4. Frequency response of a chain of five $\alpha\beta$DSC operators with delay factors 2, 4, 8, 16, and 32.

Based on this model, the closed-loop transfer function of the adaptive 1ϕ-CDSC-PLL can be obtained as

$$G_{cl}(s)=\frac{\Delta\hat{\theta}(s)}{\Delta\theta(s)}=\frac{1+e^{-\frac{T}{2}s}}{2}\frac{1+e^{-\frac{T}{4}s}}{2}\frac{1+e^{-\frac{T}{8}s}}{2}\frac{1+e^{-\frac{T}{16}s}}{2}\frac{1+e^{-\frac{T}{32}s}}{2}\frac{k_ps+k_i}{s^2+[k_p-k_i(1+k_ds)H(s)]\,s+k_i} \tag{5}$$

where $H(s)$ is

$$H(s)=\frac{T}{64}\left[1+\left(1+e^{-\frac{T}{32}s}\right)+\left(1+e^{-\frac{T}{16}s}\right)\left(1+e^{-\frac{T}{32}s}\right)+\left(1+e^{-\frac{T}{8}s}\right)\left(1+e^{-\frac{T}{16}s}\right)\left(1+e^{-\frac{T}{32}s}\right)+\left(1+e^{-\frac{T}{4}s}\right)\left(1+e^{-\frac{T}{8}s}\right)\left(1+e^{-\frac{T}{16}s}\right)\left(1+e^{-\frac{T}{32}s}\right)\right]. \tag{6}$$

It can be shown that $H(s)$ in the low-frequency range can be approximated by [14]

$$H(s)\approx\frac{\overbrace{31T/64}^{k_{dc}}}{\underbrace{(10T/64)}_{\tau}s+1}. \tag{7}$$

Therefore, by selecting $k_d=\tau=10T/64$, a pole-zero cancelation is achieved, and (5) can be simplified as

$$G_{cl}(s)\approx\frac{1+e^{-\frac{T}{2}s}}{2}\frac{1+e^{-\frac{T}{4}s}}{2}\frac{1+e^{-\frac{T}{8}s}}{2}\frac{1+e^{-\frac{T}{16}s}}{2}\frac{1+e^{-\frac{T}{32}s}}{2}\frac{k_ps+k_i}{s^2+[k_p-k_ik_{dc}]\,s+k_i}. \tag{8}$$

The characteristic polynomial of (8) is a second-order polynomial as

$$s^2+\underbrace{[k_p-k_ik_{dc}]}_{2\zeta\omega_n'}s+\underbrace{k_i}_{(\omega_n')^2}=0 \tag{9}$$

in which ζ and ω_n' denote the damping factor and the natural frequency of the closed-loop poles, respectively. Therefore, k_p and k_i can be determined by choosing appropriate values for these parameters. This process, of course, involves some tradeoff decisions, which have been well discussed in the literature [12], [14]. Therefore, they are not repeated here to save the space. In this work, $\zeta=1$ and $\omega_n'=2\pi35$ rad/s are chosen, which, according to (9), are corresponding to $k_p=908$ and $k_i=48361$.

IV. Designing Advanced Single-Phase PLLs Using Nonadaptive $\alpha\beta$DSC Operators

In this section, two advanced single-phase PLLs using nonadaptive $\alpha\beta$DSC operators are designed and presented.

A. First Design Approach

The nonadaptive version of Fig. 5, which is shown in Fig. 7(a), is considered as the basic structure for developing an efficient PLL. From Fig. 7(a), the transfer functions relating the output signals $\hat{v}_\alpha$ and $\hat{v}_\beta$ to the grid voltage signal can be obtained as

$$G_\alpha(s)=\frac{\hat{v}_\alpha(s)}{v_g(s)}=\frac{1}{16}\sum_{m=0}^{31}\cos\left(\frac{2\pi m}{32}\right)e^{-\frac{mT}{32}s} \tag{10}$$

$$G_\beta(s)=\frac{\hat{v}_\beta(s)}{v_g(s)}=\frac{1}{16}\sum_{m=0}^{31}\sin\left(\frac{2\pi m}{32}\right)e^{-\frac{mT}{32}s} \tag{11}$$

or equivalently as (see the Appendix for the proof)

$$G_\alpha(s)=\frac{1}{16}\frac{\left(1-\cos(2\pi/32)e^{-\frac{Ts}{32}}\right)\left(1-e^{-Ts}\right)}{1-2\cos(2\pi/32)e^{-\frac{Ts}{32}}+e^{-\frac{2Ts}{32}}} \tag{12}$$

$$G_\beta(s)=\frac{1}{16}\frac{\left(\sin(2\pi/32)e^{-\frac{Ts}{32}}\right)\left(1-e^{-Ts}\right)}{1-2\cos(2\pi/32)e^{-\frac{Ts}{32}}+e^{-\frac{2Ts}{32}}}. \tag{13}$$

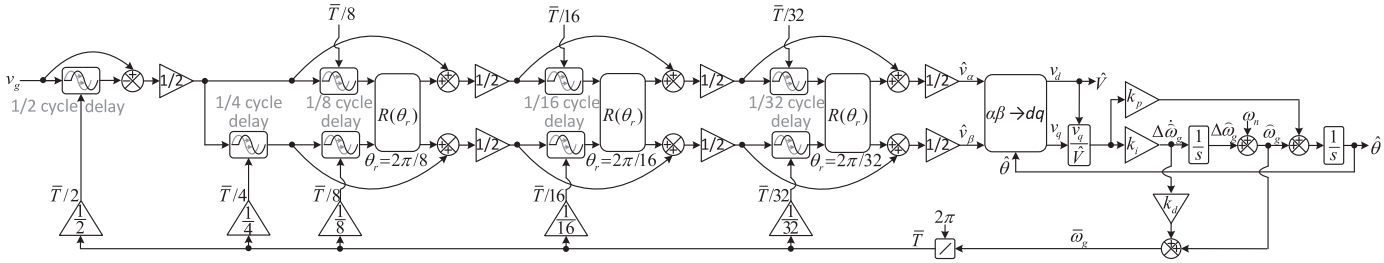

Fig. 5. Block diagram of the adaptive 1ϕ-CDSC-PLL.

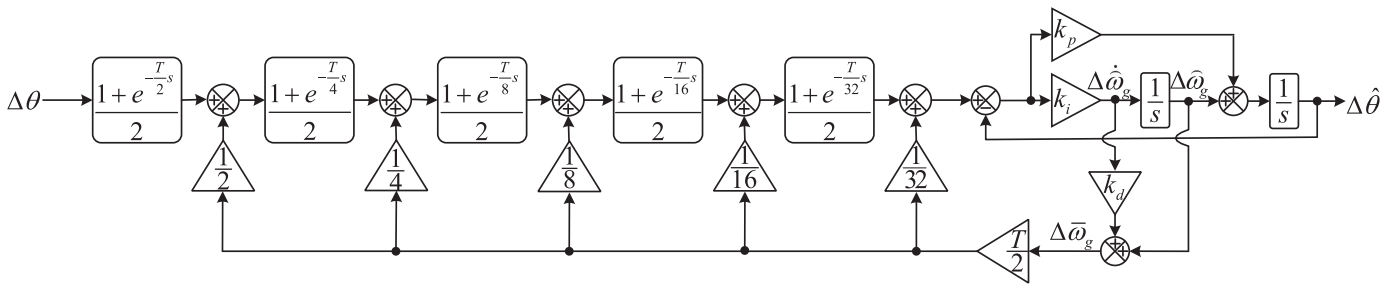

Fig. 6. Small-signal model of the adaptive 1ϕ-CDSC-PLL. $T = 0.02$ s.

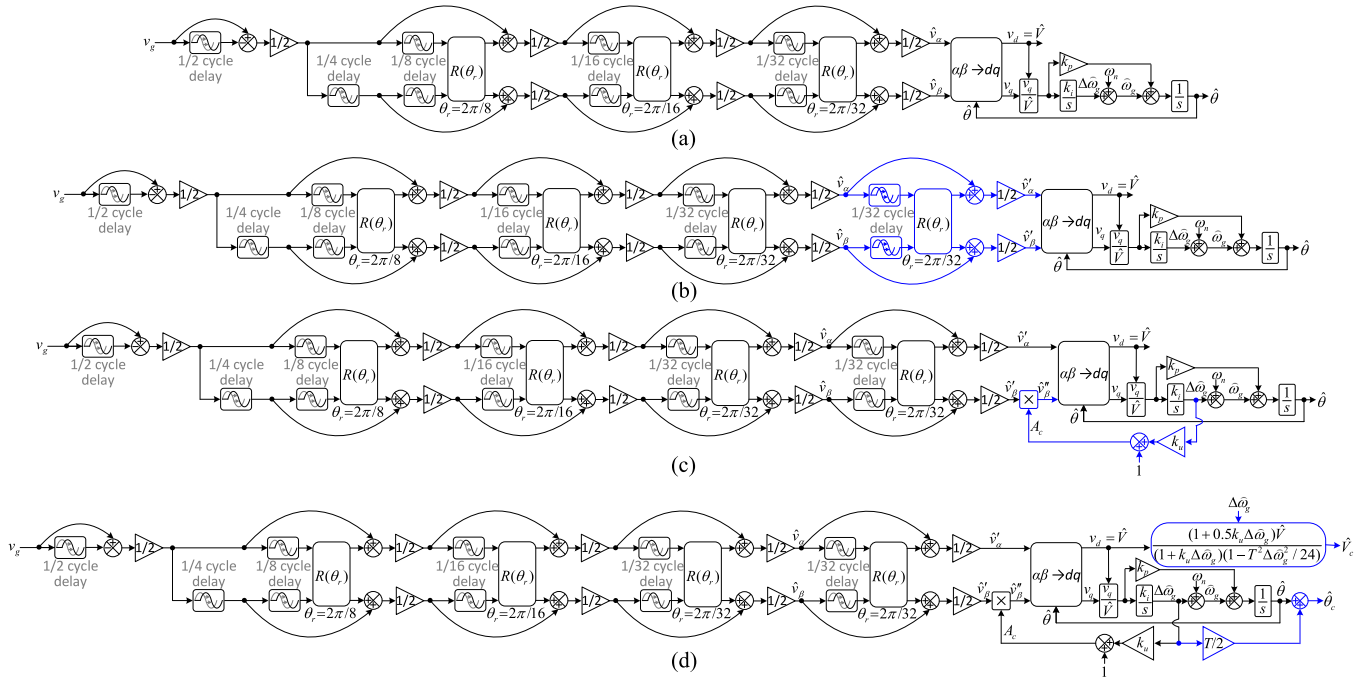

Fig. 7. Step-by-step procedure toward designing the first PLL structure with nonadaptive $\alpha\beta$DSC operators. (a) Nonadaptive version of Fig. 5. (b) Adding an extra $\alpha\beta$DSC operator with the delay factor 32 to the chain operators to ensure a 90° phase difference between its α- and β-axis outputs under both nominal and off-nominal frequencies. (c) Correcting the amplitude imbalance in the SRF-PLL input under off-nominal frequencies [$k_u = (T/32)\cot(2\pi/32) = 0.00314$]. (d) Correcting the phase offset and amplitude scaling errors by adding the phase and amplitude error compensators to the SRF-PLL. This final product is briefly called the nonadaptive 1ϕ-CDSC-PLL$_1$.

Fig. 8 illustrates the frequency response of these transfer functions, and Fig. 9 shows the frequency response of their ratio around the fundamental frequency. From these plots, the following observations are made.

1) When the grid frequency is at its nominal value, the α- and β-axis output signals (i.e., $\hat{v}_\alpha$ and $\hat{v}_\beta$) in Fig. 7(a) have the same amplitude as the fundamental component of the grid voltage signal. In this condition, the signal $\hat{v}_\alpha$ is in-phase with the fundamental component of the grid voltage, and the signal $\hat{v}_\beta$ is orthogonal to it.
2) When the grid frequency deviates from its nominal value, the α- and β-axis output signals have different amplitudes compared to each other and also compared to the funda-

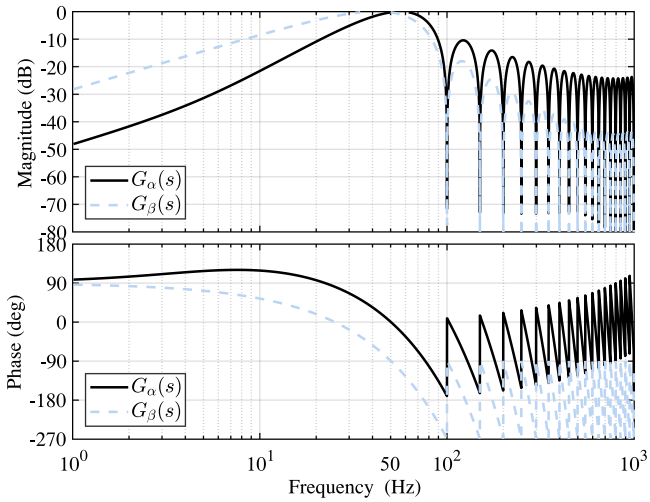

Fig. 8. Frequency response of (12) and (13).

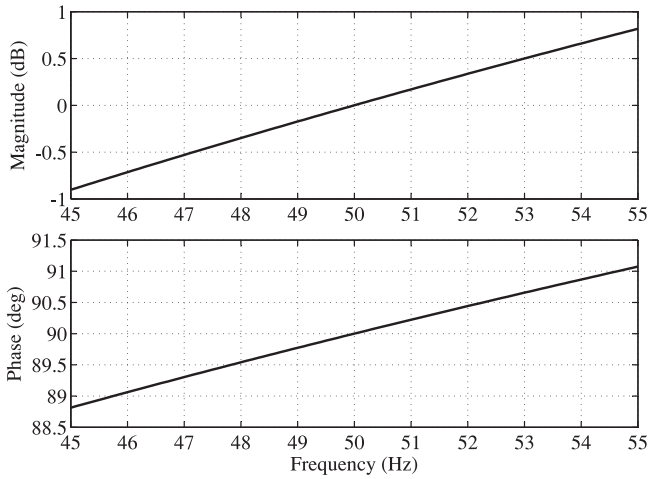

Fig. 9. Frequency response of the ratio of (12) and (13) around the fundamental frequency.

mental component of the grid voltage. In this condition, the signal $\hat{v}_\alpha$ is no longer in-phase with the fundamental component of the grid voltage, and the signal $\hat{v}_\beta$ is not orthogonal to it. Besides, the phase difference between $\hat{v}_\alpha$ and $\hat{v}_\beta$ is no longer 90°.

In addition to the phase offset and amplitude scaling errors, these problems result in large double-frequency oscillatory errors in the estimated quantities by the SRF-PLL under off-nominal frequencies as they make the SRF-PLL input unbalanced. The dark solid lines in Fig. 10, which demonstrate the performance of Fig. 7(a) in response to a +2-Hz step change in the grid frequency, clearly show these errors.

The first step to deal with these issues is finding an approach to preserve the orthogonality (90° phase difference) between the α- and β-axis output signals under off-nominal frequencies. In this paper, adding an extra $\alpha\beta$DSC operator with the delay factor 32 to the chain of operators in Fig. 7(a) is suggested. Fig. 7(b) illustrates this idea, and (14) and (15) describe the input–output

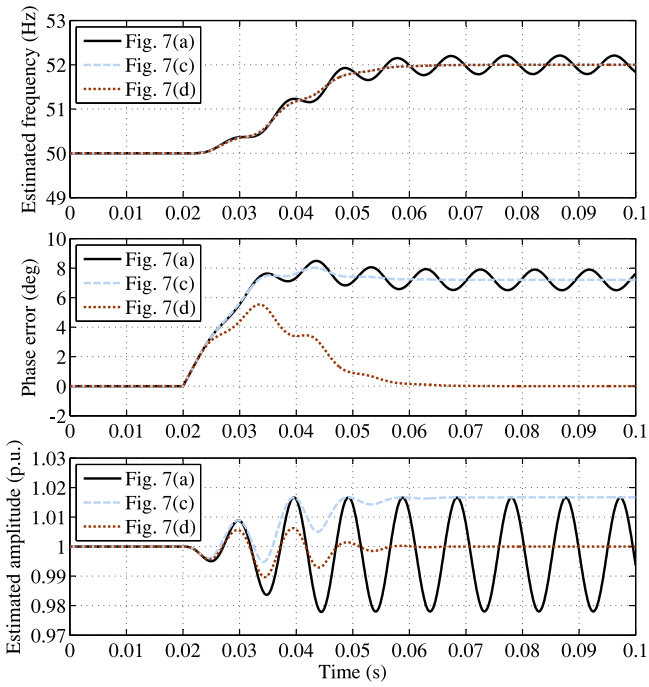

Fig. 10. Performance of the PLL structures shown in Fig. 7(a), (c), and (d) in response to a +2-Hz step change in the grid frequency.

transfer functions of the chain of operators in this figure

$$G'_\alpha(s) = \frac{\hat{v}'_\alpha(s)}{v_g(s)} = \frac{1+\cos(2\pi/32)e^{-\frac{Ts}{32}}}{2}G_\alpha(s) - \frac{\sin(2\pi/32)}{2}e^{-\frac{Ts}{32}}G_\beta(s) = \frac{1}{32}\frac{\left(1-e^{-\frac{2Ts}{32}}\right)\left(1-e^{-Ts}\right)}{1-2\cos(2\pi/32)e^{-\frac{Ts}{32}}+e^{-\frac{2Ts}{32}}} \quad (14)$$

$$G'_\beta(s) = \frac{\hat{v}'_\beta(s)}{v_g(s)} = \frac{1+\cos(2\pi/32)e^{-\frac{Ts}{32}}}{2}G_\beta(s) + \frac{\sin(2\pi/32)}{2}e^{-\frac{Ts}{32}}G_\alpha(s) = \frac{1}{32}\frac{2\sin(2\pi/32)e^{-\frac{Ts}{32}}\left(1-e^{-Ts}\right)}{1-2\cos(2\pi/32)e^{-\frac{Ts}{32}}+e^{-\frac{2Ts}{32}}}. \quad (15)$$

Using (14) and (15), their frequency response can be expressed as

$$G'_\alpha(j\omega) = \frac{1}{16}\frac{\boldsymbol{|\sin(T\omega/32)|}\,|\sin(T\omega/2)|}{|\cos(T\omega/32)-\cos(2\pi/32)|}\angle(\pi - T\omega/2) \quad (16)$$

$$G'_\beta(j\omega) = \frac{1}{16}\frac{\boldsymbol{\sin(2\pi/32)}\,|\sin(T\omega/2)|}{|\cos(T\omega/32)-\cos(2\pi/32)|}\angle(\pi/2 - T\omega/2). \quad (17)$$

According to these equations and Figs. 11 and 12, which show the frequency response of (14) and (15) and their ratio, it can be concluded that the SRF-PLL input signals in Fig. 7(b) are

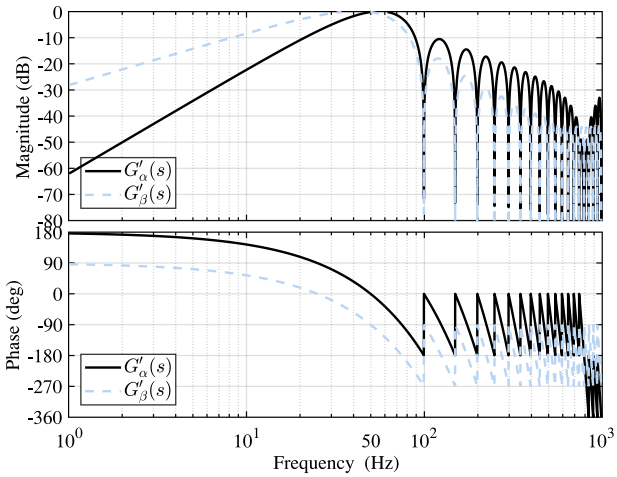

Fig. 11. Frequency response of (14) and (15).

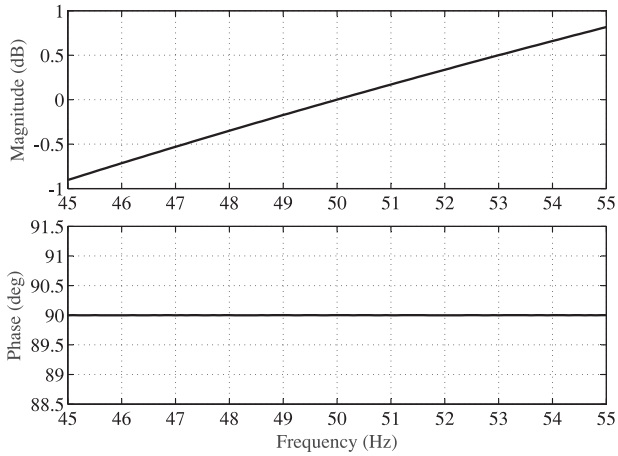

Fig. 12. Frequency response of the ratio of (14) and (15) around the fundamental frequency.

always orthogonal. However, they still have different amplitudes under off-nominal frequencies.

This amplitude difference is because of the highlighted terms in (16) and (17). Therefore, it can be corrected by multiplying the β-axis output signal by an estimation of the ratio of these terms at the fundamental frequency, i.e.,

$$\begin{aligned} A_c &= \frac{\sin(T\omega_g/32)}{\sin(2\pi/32)} \\ &= \frac{\sin(\overbrace{T\omega_n/32}^{2\pi/32})\cos(T\Delta\omega_g/32)+\cos(T\omega_n/32)\sin(T\Delta\omega_g/32)}{\sin(2\pi/32)} \\ &= \overbrace{\cos(T\Delta\omega_g/32)}^{\approx 1}+\cot(2\pi/32)\overbrace{\sin(T\Delta\omega_g/32)}^{\approx (T\Delta\omega_g/32)} \\ &\approx 1+\overbrace{\left(\frac{T\cot(2\pi/32)}{32}\right)}^{k_u}\Delta\omega_g. \end{aligned} \tag{18}$$

This idea has been highlighted in Fig. 7(c). Notice that in obtaining (18), the definition $\omega_g = \omega_n + \Delta\omega_g$ has been considered, in which ω_g is the grid fundamental frequency, and $\omega_n = 2\pi/T$ is the nominal value of the grid frequency. Notice also that in implementing this idea in Fig. 7(c), the output of the integrator of the PI controller is considered as an estimation of $\Delta\omega_g$.

With the aforementioned modifications, the SRF-PLL input signals have the same amplitude and 90° phase difference under both nominal and off-nominal frequencies. Therefore, the double-frequency problem is completely solved. The dashed lines in Fig. 10 confirm this fact. Now, the phase offset and amplitude scaling errors need to be corrected.

According to (16), the phase difference between the fundamental component of the grid voltage and the α-axis output of the chain of the operators is equal to

$$\angle G'_\alpha(j\omega_g) = \pi - T\omega_g/2 = -T\Delta\omega_g/2 \tag{19}$$

where ω_g is the grid frequency and $\Delta\omega_g = \omega_g - \omega_n$. Therefore, this phase error can be simply corrected by adding $T\Delta\widehat{\omega}_g/2$, which is an estimation of (19) with an opposite sign, to the SRF-PLL output. This idea is highlighted in Fig. 7(d).

In a similar manner, it can be shown using (16) that the amplitude scaling error between the fundamental component of the grid voltage and the SRF-PLL inputs can be well approximated by

$$\begin{aligned} &|G'_\alpha(j\omega_g)| \\ &\quad\approx \left|\frac{\sin(2\pi/32)+\cos(2\pi/32)(T\Delta\omega_g/32)}{\sin(2\pi/32)+0.5\cos(2\pi/32)(T\Delta\omega_g/32)}\right. \\ &\quad\quad \left.\left(1-\frac{T^2}{24}\Delta\omega_g^2\right)\right| \end{aligned} \tag{20}$$

or equivalently by

$$|G'_\alpha(j\omega_g)| \approx \left|\frac{1+k_u\Delta\omega_g}{1+0.5k_u\Delta\omega_g}\left(1-\frac{T^2}{24}\Delta\omega_g^2\right)\right| \tag{21}$$

where the definition k_u can be found in (18). Therefore, as highlighted in Fig. 7(d), this scaling error can be corrected by multiplying the estimated amplitude by an estimation of the inverse of (21).

Fig. 7(d) illustrates the final product. It is briefly referred to as the nonadaptive 1ϕ-CDSC-PLL$_1$, where *nonadaptive* denotes that this PLL uses nonadaptive $\alpha\beta$DSC operators, 1ϕ (as mentioned before) means that it is for single-phase applications, and the subscript 1 is used to discriminate it from the second PLL structure, which is going to be designed and presented in the next section. The dotted lines in Fig. 10 show the performance of the nonadaptive 1ϕ-CDSC-PLL$_1$ in response to the frequency jump. It can be observed that the estimated quantities by this PLL are free from any error.

From Fig. 7(d) and using the guidelines presented in [25], the small-signal model of the nonadaptive 1ϕ-CDSC-PLL$_1$ can be derived, as shown in Fig. 13. Based on this model, the closed-

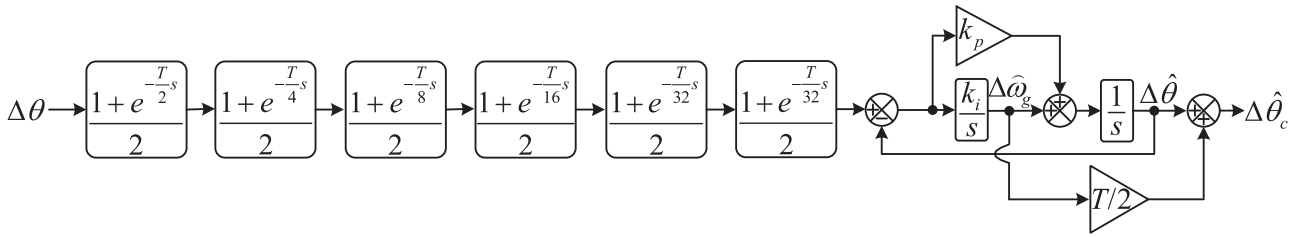

Fig. 13. Small-signal model of the nonadaptive 1ϕ-CDSC-PLL$_1$.

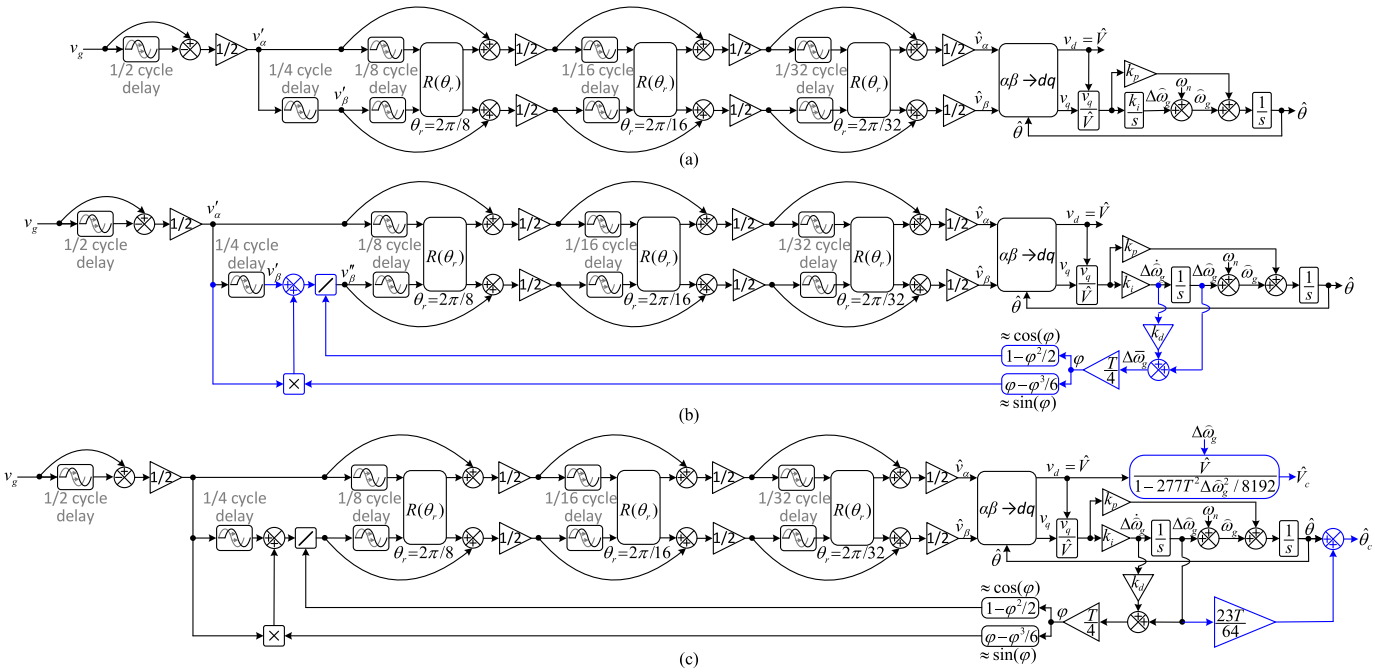

Fig. 14. Step-by-step procedure toward designing the second PLL structure with nonadaptive $\alpha\beta$DSC operators. (a) Nonadaptive version of Fig. 5. (b) Correcting the double-frequency problem using a nonlinear frequency feedback scheme. (c) Correcting the phase offset and amplitude scaling errors by adding phase and amplitude error compensators to the SRF-PLL. This final product is briefly called the nonadaptive 1ϕ-CDSC-PLL$_2$.

loop transfer function of this PLL can be obtained as

$$G_{cl}(s) = \frac{\Delta\hat{\theta}_c(s)}{\Delta\theta(s)}$$

$$= \frac{1+e^{-\frac{T}{2}s}}{2}\frac{1+e^{-\frac{T}{4}s}}{2}\frac{1+e^{-\frac{T}{8}s}}{2}\frac{1+e^{-\frac{T}{16}s}}{2}\left(\frac{1+e^{-\frac{T}{32}s}}{2}\right)^2 \frac{(k_p+k_iT/2)\,s+k_i}{s^2+k_ps+k_i}. \tag{22}$$

The characteristic polynomial of (22) is as

$$s^2 + \underbrace{k_p}_{2\zeta\omega_n'}\,s + \underbrace{k_i}_{(\omega_n')^2} = 0 \tag{23}$$

in which ζ and ω_n', as defined before, are the damping factor and natural frequency of the closed-loop poles, respectively. To have a fair comparison, the same damping factor and natural frequency as those selected for the adaptive 1ϕ-CDSC-PLL, i.e., $\zeta = 1$ and $\omega_n' = 2\pi 35$ rad/s, are chosen here. These selections result in $k_p = 439.8$ and $k_i = 48361$.

B. Second Design Approach

Again, as shown in Fig. 14(a), the nonadaptive version of Fig. 5 is considered as the basic structure for developing an efficient single-phase PLL with nonadaptive $\alpha\beta$DSC operators. It was discussed in Section IV-A that this structure suffers from a phase offset error, an amplitude scaling error, and double-frequency oscillatory errors under off-nominal frequencies. The solid lines in Fig. 15 illustrate this fact again. All delays in the SRF-PLL input play a part in generating the phase offset/amplitude scaling errors. But, only one of them, i.e., the delay with the $1/4$-cycle length, is responsible for creating the double-frequency oscillatory error. Notice that this delay is not able to create exactly a 90° phase shift under off-nominal frequencies. This results in a nonorthogonality between its input and output signals [i.e., the signals v_α' and v_β' in Fig. 14(a)] in this condition. As none of the operators after this delay are able to block the FFNS component, the SRF-PLL input signals will be unbalanced under off-nominal frequencies, which results in a double-frequency oscillatory error in the estimated quantities by the SRF-PLL. Consequently, an approach to solve the double-

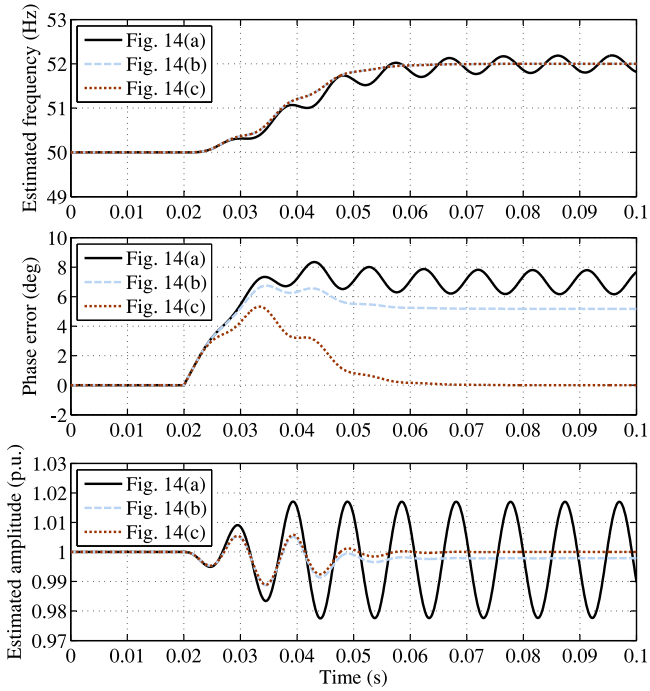

Fig. 15. Performance of the PLL structures shown in Fig. 14(a)–(c) in response to a +2-Hz step change in the grid frequency.

frequency problem is to ensure that the input and output signals of the quarter cycle delay are always orthogonal.

Assume that the input signal of the quarter cycle delay in Fig. 14(a) is

$$v'_\alpha(t) = V' \cos\overbrace{(\omega_g t + \varphi')}^{\theta'} \tag{24}$$

where V' and φ' are the amplitude and initial phase angle of this signal, respectively, which may not be necessarily equal to those of the grid voltage v_g. In this case, the output signal of the quarter cycle delay may be expressed as

$$\begin{aligned} v'_\beta(t) &= v'_\alpha(t - T/4) = V' \cos(\theta' - T\omega_g/4) \\ &= V' \sin(\theta' - T\Delta\omega_g/4) \\ &= \overbrace{V' \sin(\theta')}^{v''_\beta(t)} \cos(T\Delta\omega_g/4) - \overbrace{V' \cos(\theta')}^{v'_\alpha(t)} \sin(T\Delta\omega_g/4). \end{aligned} \tag{25}$$

The term $v''_\beta(t) = V' \sin(\theta')$ on the right-hand side of (25) is orthogonal to the input signal of the quarter cycle delay, and therefore, it is what we are looking for. This term can be expressed as [26]

$$v''_\beta(t) = \frac{v'_\beta(t) + v'_\alpha(t) \sin(T\Delta\omega_g/4)}{\cos(T\Delta\omega_g/4)}. \tag{26}$$

Fig. 14(b) illustrates the resultant structure of applying (26) for correcting the nonorthogonality between the input and output signals of the quarter cycle delay under off-nominal frequencies. Notice that the terms $\sin(T\Delta\omega_g/4)$ and $\cos(T\Delta\omega_g/4)$, which are calculated using an estimation of the grid frequency, are approximated by the first two terms of their Taylor series expansions.

The dashed lines in Fig. 15 illustrate the performance of Fig. 14(b) in response to a step change in the grid frequency. It can be seen that the double-frequency oscillatory errors are totally removed. Besides, a reduction in the phase offset error compared to that of Fig. 14(a) is observed.

With removing the double-frequency errors, the phase offset and amplitude scaling errors should to be corrected now. These errors are because of the operators with the delay factor 2, 8, 16, and 32. Therefore, using (1) and (3), these errors can be calculated as

$$\begin{aligned} \sum_{n=2,8,16,32} \angle\alpha\beta\mathrm{DSC}_n(j\omega_g) &= -\sum_{n=2,8,16,32} \frac{T\omega_g - 2\pi}{2n} \\ &= -\sum_{n=2,8,16,32} \frac{T\Delta\omega_g}{2n} \\ &= -\frac{23T}{64}\Delta\omega_g \end{aligned} \tag{27}$$

$$\begin{aligned} \prod_{n=2,8,16,32} |\alpha\beta\mathrm{DSC}_n(j\omega_g)| &= \prod_{n=2,8,16,32} \left|\cos\left(\frac{T\omega_g - 2\pi}{2n}\right)\right| \\ &= \prod_{n=2,8,16,32} \left|\cos\left(\frac{T\Delta\omega_g}{2n}\right)\right| \\ &\approx \prod_{n=2,8,16,32} \left|1 - 0.5\left(\frac{T\Delta\omega_g}{2n}\right)^2\right| \\ &\approx 1 - \frac{277T^2}{8192}\Delta\omega_g^2. \end{aligned} \tag{28}$$

The phase offset error can now be corrected by calculating (27) using the estimated frequency and adding it with an opposite sign to the phase angle estimated by the SRF-PLL. In a similar manner, the amplitude scaling error can be corrected by calculating (28) and multiplying the estimated amplitude by its inverse. Applying these corrections to Fig. 14(b) is shown in Fig. 14(c). This structure is briefly referred to as the nonadaptive 1ϕ-CDSC-PLL$_2$.

The dotted lines in Fig. 15 illustrate the performance of the nonadaptive 1ϕ-CDSC-PLL$_2$ in response to a frequency jump. It can be observed that it is free from any error under off-nominal frequencies.

Using Fig. 14(c) and based on the guidelines presented in [25] and [26], the small-signal model of the nonadaptive 1ϕ-CDSC-PLL$_2$ can be obtained, as depicted in Fig. 16. According to this model, the closed-loop transfer function can be expressed as

$$\begin{aligned} G_{cl}(s) &= \frac{\Delta\hat{\theta}_c(s)}{\Delta\theta(s)} \\ &= \frac{1 + e^{-\frac{T}{2}s}}{2} \frac{1 + e^{-\frac{T}{4}s}}{2} \frac{1 + e^{-\frac{T}{8}s}}{2} \frac{1 + e^{-\frac{T}{16}s}}{2} \frac{1 + e^{-\frac{T}{32}s}}{2} \\ &\quad \frac{(k_p + 23Tk_i/64)\, s + k_i}{s^2 + [k_p - k_i(1 + k_d s)H'(s)]\, s + k_i} \end{aligned} \tag{29}$$

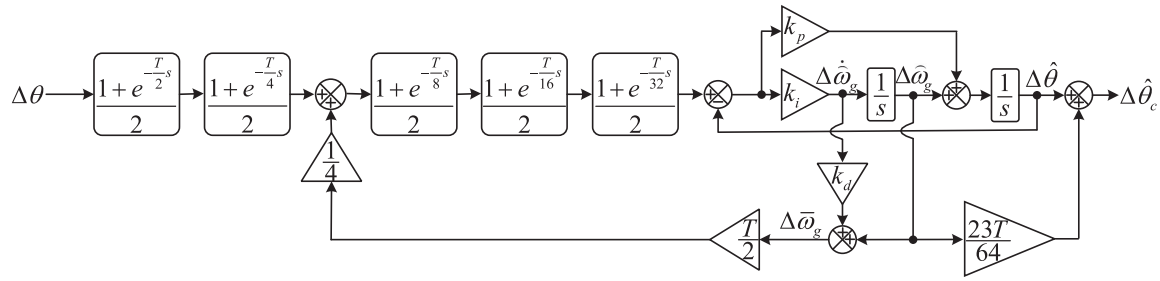

Fig. 16. Small-signal model of the nonadaptive 1ϕ-CDSC-PLL$_2$.

TABLE I
CONTROL PARAMETERS ($T = 0.02$ s)

	Adaptive 1ϕ-CDSC-PLL	nonadaptive 1ϕ-CDSC-PLL$_1$	nonadaptive 1ϕ-CDSC-PLL$_2$
Proportional gain k_p	908	439.8	560.7
Integrator gain k_i	48361	48361	48361
Gain k_d	$10T/64$	——	$7T/64$

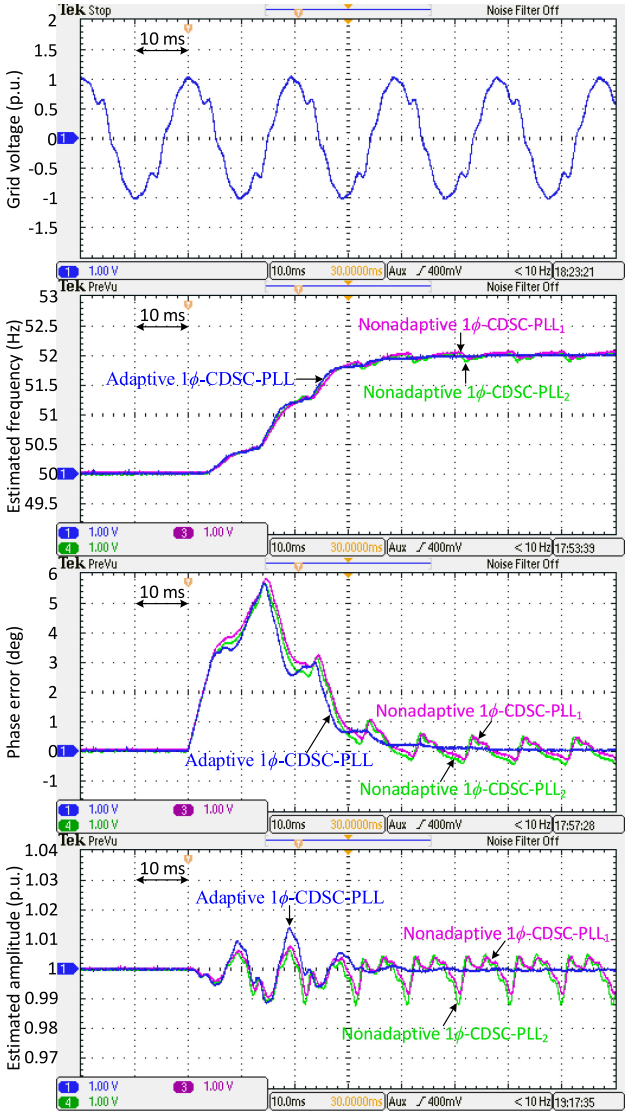

Fig. 17. Results of Test 1.

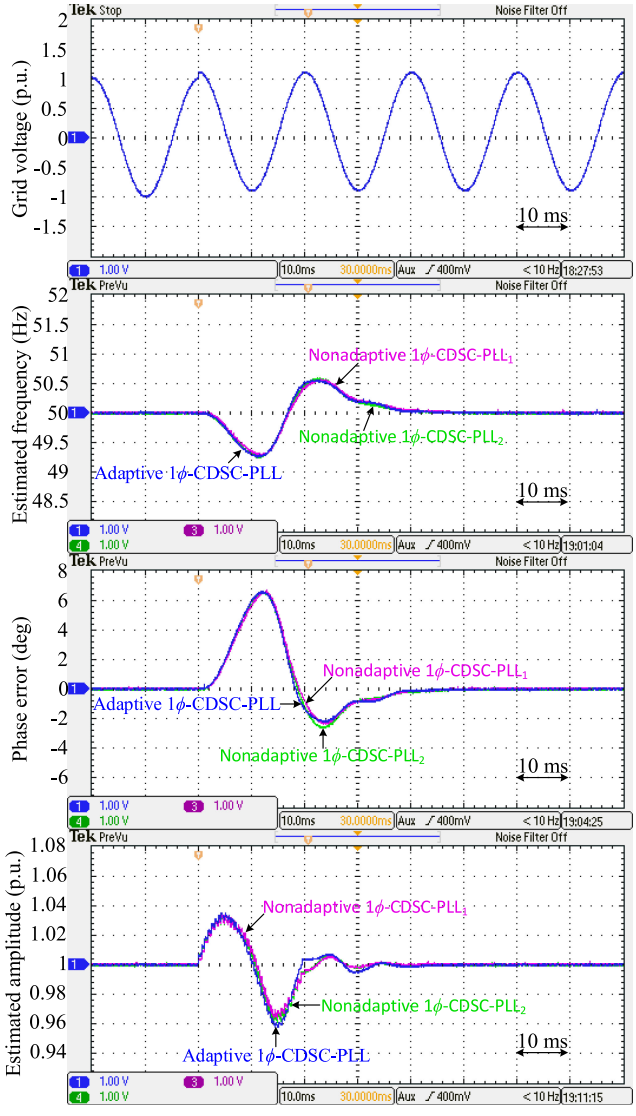

Fig. 18. Results of Test 2.

where

$$H'(s) = \frac{T}{8}\frac{1+e^{-\frac{T}{8}s}}{2}\frac{1+e^{-\frac{T}{16}s}}{2}\frac{1+e^{-\frac{T}{32}s}}{2}$$
$$\approx \frac{T}{8}\frac{1}{(T/16)\,s+1}\frac{1}{(T/32)\,s+1}\frac{1}{(T/64)\,s+1}$$
$$\approx \frac{T/8}{(7T/64)\,s+1}. \quad (30)$$

According to (30), it can be concluded that a pole-zero cancelation can be achieved in (29) by selecting $k_d = 7T/64$. With this pole-zero cancelation, (29) can be simplified as

$$G_{cl}(s) \approx \frac{1+e^{-\frac{T}{2}s}}{2}\frac{1+e^{-\frac{T}{4}s}}{2}\frac{1+e^{-\frac{T}{8}s}}{2}\frac{1+e^{-\frac{T}{16}s}}{2}\frac{1+e^{-\frac{T}{32}s}}{2}$$
$$\frac{(k_p + 23Tk_i/64)\,s + k_i}{s^2 + (k_p - Tk_i/8)\,s + k_i}. \quad (31)$$

The characteristic polynomial of (31) is as follows:

$$s^2 + \underbrace{(k_p - Tk_i/8)}_{2\zeta\omega_n'}\,s + \underbrace{k_i}_{(\omega_n')^2} = 0 \quad (32)$$

in which, as mentioned before, ζ is the damping factor and ω_n' is the natural frequency. Again, to have a fair comparison, the same damping factor and the natural frequency as those selected for the adaptive 1ϕ-CDSC-PLL and the nonadaptive 1ϕ-CDSC-PLL$_1$, i.e., $\zeta = 1$ and $\omega_n' = 2\pi 35$ rad/s, are chosen here. These selections result in $k_p = 560.7$ and $k_i = 48361$.

V. Performance Comparison

In this section, the performance of the adaptive 1ϕ-CDSC-PLL (see Fig. 5), the nonadaptive 1ϕ-CDSC-PLL$_1$ [see Fig. 7(d)], and the nonadaptive 1ϕ-CDSC-PLL$_2$ [see Fig. 14(c)] is compared using the dSPACE 1006 platform. To provide a high flexibility in performing comparative tests, the single-phase input signal of PLLs is also generated using the dSPACE platform. The following tests are considered for the comparison.

1) *Test 1:* A +2-Hz frequency jump under a harmonically distorted grid condition occurs. The grid voltage in this test contains 0.07 p.u. third harmonic, 0.05 p.u. fifth harmonic, 0.06 p.u. seventh harmonic, and 0.05 p.u. ninth harmonic.
2) *Test 2:* A 0.1 p.u. dc offset is superimposed to the grid voltage signal.
3) *Test 3:* A 40° phase jump and 0.5 p.u. voltage sag happen.

Table I summarizes the control parameters of all PLLs. The sampling frequency and the nominal frequency, throughout this study, are 8 kHz and 50 Hz, respectively.

Fig. 17 demonstrates the performance of three PLLs in response to Test 1. All PLLs completely reject the harmonics before the frequency step change (i.e., when the grid frequency is at its nominal value). Besides, no large difference between the transient behavior of PLLs is observed. The only difference between them lies in their harmonic rejection ability after the deviation of the grid frequency from its nominal value. It can be observed that the adaptive 1ϕ-CDSC-PLL, thanks to the frequency-adaptive operators in its input, still completely rejects the harmonics. The nonadaptive 1ϕ-CDSC-PLL$_1$ and the nonadaptive 1ϕ-CDSC-PLL$_2$, however, suffer from some rather small oscillatory ripples in their estimated quantities in this condition. This is because these two PLLs use nonadaptive operators in their input.

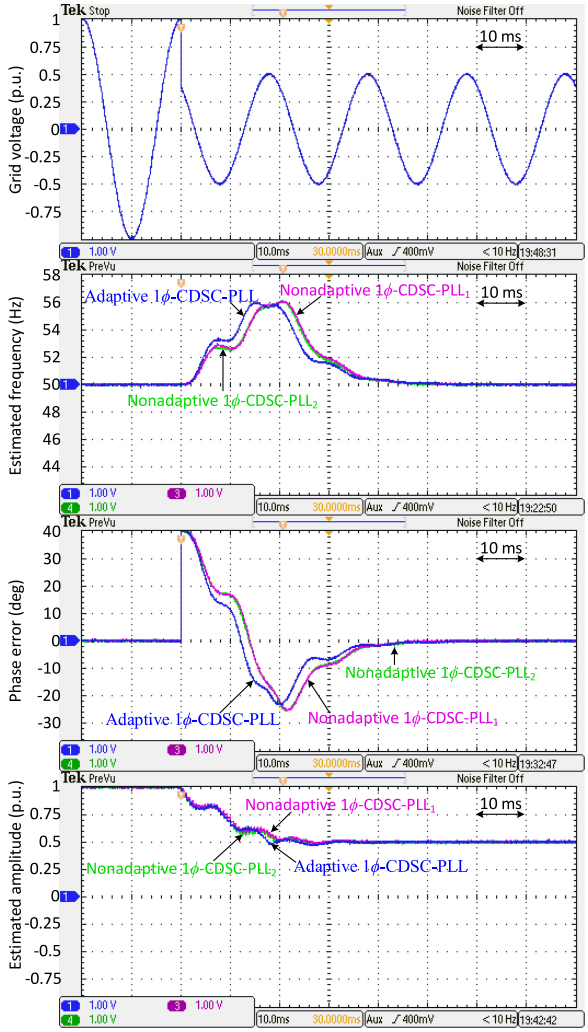

Fig. 19. Results of Test 3.

The response of PLLs to adding a dc component to their input can be observed in Fig. 18. All PLLs completely reject the dc component, and no large difference in their transient behaviors is observed.

Fig. 19 shows the behavior of PLLs under Test 3. All PLLs demonstrate a fast dynamic response and reach the steady state in around two cycles of the nominal frequency.

In summary, all PLLs demonstrate a good performance. The only noticeable difference between them lies in the more efficient operation of the adaptive 1ϕ-CDSC-PLL in rejecting harmonics under off-nominal frequencies. This advantage is of course at the cost of a rather higher implementation complexity of this PLL compared to the others. Notice that, as mentioned before, the adaptive 1ϕ-CDSC-PLL uses frequency-adaptive operators in its input, which involves adjusting the length of its delays according to the grid frequency variations. This task almost always involves using interpolation techniques [27].

VI. Conclusion

In this paper, some advanced single-phase PLLs using $\alpha\beta$DSC operators were designed. One of these PLLs uses frequency-adaptive operators and the rest of them employ non-adaptive operators. The design procedures of these PLLs were described in detail, their small-signal models were presented, and their tuning procedures were explained. Finally, a performance comparison between them was conducted. From the obtained results, the following conclusions can be made.

1) All PLLs completely reject the grid voltage dc component.
2) All PLLs have a fast dynamic response (a response time around two cycles of the nominal frequency). And there is no large difference between their transient behaviors.
3) They all completely block the grid voltage harmonics when the grid frequency is at its nominal value. Under off-nominal frequency, nevertheless, it is only the adaptive 1ϕ-CDSC-PLL that can still perfectly block harmonics. This advantage of the adaptive 1ϕ-CDSC-PLL is of course at the cost of its higher implementation complexity compared to the other structures. Notice that realizing variable-length delays in this structure involve using interpolation techniques.

Appendix
Procedure of Obtaining (12) and (13)

By substituting $\cos\left(\frac{2\pi m}{32}\right)=\frac{e^{j\frac{2\pi m}{32}}+e^{-j\frac{2\pi m}{32}}}{2}$ and $\sin\left(\frac{2\pi m}{32}\right)=\frac{e^{j\frac{2\pi m}{32}}-e^{-j\frac{2\pi m}{32}}}{2j}$ into (10) and (11), they can be rewritten as

$$G_\alpha(s)=\frac{1}{32}\sum_{m=0}^{31}e^{-\frac{m}{32}(Ts-j2\pi)}+\frac{1}{32}\sum_{m=0}^{31}e^{-\frac{m}{32}(Ts+j2\pi)} \tag{33}$$

$$G_\beta(s)=\frac{1}{32j}\sum_{m=0}^{31}e^{-\frac{m}{32}(Ts-j2\pi)}-\frac{1}{32j}\sum_{m=0}^{31}e^{-\frac{m}{32}(Ts+j2\pi)}. \tag{34}$$

Both (33) and (34) contain two geometric progressions with common ratios $e^{-\frac{Ts-j2\pi}{32}}$ and $e^{-\frac{Ts+j2\pi}{32}}$. Therefore, they can be rewritten as

$$\begin{aligned}G_\alpha(s)&=\frac{1}{32}\frac{1-\overbrace{e^{-(Ts-j2\pi)}}^{=e^{-Ts}}}{1-e^{-\frac{1}{32}(Ts-j2\pi)}}+\frac{1}{32}\frac{1-\overbrace{e^{-(Ts+j2\pi)}}^{=e^{-Ts}}}{1-e^{-\frac{1}{32}(Ts+j2\pi)}}\\&=\frac{1}{16}\frac{\left(1-\cos(2\pi/32)e^{-\frac{Ts}{32}}\right)\left(1-e^{-Ts}\right)}{1-2\cos(2\pi/32)e^{-\frac{Ts}{32}}+e^{-\frac{2Ts}{32}}}\end{aligned} \tag{35}$$

$$\begin{aligned}G_\beta(s)&=\frac{1}{32j}\frac{1-e^{-(Ts-j2\pi)}}{1-e^{-\frac{1}{32}(Ts-j2\pi)}}-\frac{1}{32j}\frac{1-e^{-(Ts+j2\pi)}}{1-e^{-\frac{1}{32}(Ts+j2\pi)}}\\&=\frac{1}{16}\frac{\left(\sin(2\pi/32)e^{-\frac{Ts}{32}}\right)\left(1-e^{-Ts}\right)}{1-2\cos(2\pi/32)e^{-\frac{Ts}{32}}+e^{-\frac{2Ts}{32}}}.\end{aligned} \tag{36}$$

Acknowledgment

This project was funded by the Deanship of Scientific Research (DSR), King Abdulaziz University, Jeddah, under grant no. (264-135-D1435). The Authors, therefore, acknowledge with thanks DSR technical and financial support.

References

[1] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1894–1907, Mar. 2017.
[2] T.-N. Le, "Kompensation schnell veränderlicher blindströme eines drehstromverbrauchers," *ETZ-Archiv*, vol. 11, no. 8, pp. 249–253, 1989.
[3] H. Awad, J. Svensson, and M. Bollen, "Mitigation of unbalanced voltage dips using static series compensator," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 837–846, May 2004.
[4] H. Awad, J. Svensson, and M. J. Bollen, "Tuning software phase-locked loop for series-connected converters," *IEEE Trans. Power Del.*, vol. 20, no. 1, pp. 300–308, Jan. 2005.
[5] F. A. S. Neves, H. E. P. de Souza, M. C. Cavalcanti, F. Bradaschia, and E. J. Bueno, "Digital filters for fast harmonic sequence component separation of unbalanced and distorted three-phase signals," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3847–3859, Oct. 2012.
[6] Y. F. Wang and Y. W. Li, "Analysis and digital implementation of cascaded delayed-signal-cancellation PLL," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1067–1080, Apr. 2011.
[7] Y. F. Wang and Y. W. Li, "Grid synchronization PLL based on cascaded delayed signal cancellation," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1987–1997, Jul. 2011.
[8] J. Svensson, M. Bongiorno, and A. Sannino, "Practical implementation of delayed signal cancellation method for phase-sequence separation," *IEEE Trans. Power Del.*, vol. 22, no. 1, pp. 18–26, Jan. 2007.
[9] M. Bongiorno, J. Svensson, and A. Sannino, "Effect of sampling frequency and harmonics on delay-based phase-sequence estimation method," *IEEE Trans. Power Del.*, vol. 23, no. 3, pp. 1664–1672, Jul. 2008.
[10] S. Golestan, M. Ramezani, J. M. Guerrero, and M. Monfared, "dq-frame cascaded delayed signal cancellation-based PLL: Analysis, design, and comparison with moving average filter-based PLL," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1618–1632, Mar. 2015.
[11] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Performance analysis and design guidelines," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2750–2763, Jun. 2014.
[12] S. Golestan, F. D. Freijedo, A. Vidal, A. G. Yepes, J. M. Guerrero, and J. Doval-Gandoy, "An efficient implementation of generalized delayed signal cancellation PLL," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1085–1094, Feb. 2016.
[13] H. A. Hamed, A. F. Abdou, E. H. E. Bayoumi, and E. E. EL-Kholy, "Frequency adaptive CDSC-PLL using axis drift control under adverse grid condition," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2671–2682, Apr. 2017.
[14] S. Golestan, J. M. Guerrero, J. Vasquez, A. M. Abusorrah, and Y. A. Al-Turki, "Research on variable-length transfer delay and delayed signal cancellation based PLLs," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8388–8398, Oct. 2018.
[15] H. A. Hamed, A. F. Abdou, E. E. El-Kholy, and E. H. E. Bayoumi, "Adaptive cascaded delayed signal cancelation PLL based fuzzy controller under grid disturbances," in *Proc. IEEE 59th Int. Midwest Symp. Circuits Syst.*, Oct. 2016, pp. 1–4.
[16] H. A. Hamed, A. F. Abdou, E. H. E. Bayoumi, and E. E. EL-Kholy, "A fast recovery technique for grid-connected converters after short dips using a hybrid structure PLL," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3056–3068, Apr. 2018.
[17] J. C. Alfonso-Gil, J. J. Vague-Cardona, S. Orts-Grau, F. J. Gimeno-Sales, and S. Segui-Chilet, "Enhanced grid fundamental positive-sequence digital synchronization structure," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 226–234, Jan. 2013.
[18] Q. Huang and K. Rajashekara, "An improved delayed signal cancellation PLL for fast grid synchronization under distorted and unbalanced grid condition," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4985–4997, Sep. 2017.

[19] F. Wu and X. Li, "Multiple DSC filter-based three-phase EPLL for non-ideal grid synchronization," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 1396–1403, Sep. 2017.

[20] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Single-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9013–9030, Dec. 2017.

[21] A. Elrayyah, Y. Sozer, and M. Elbuluk, "Robust phase locked-loop algorithm for single-phase utility-interactive inverters," *IET Power Electron.*, vol. 7, no. 5, pp. 1064–1072, May 2014.

[22] F. Wu, D. Sun, L. Zhang, and J. Duan, "Influence of plugging DC offset estimation integrator in single-phase EPLL and alternative scheme to eliminate effect of input DC offset and harmonics," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4823–4831, Aug. 2015.

[23] M. Karimi-Ghartemani and M. R. Iravani, "A method for synchronization of power electronic converters in polluted and variable-frequency environments," *IEEE Trans. Power Syst.*, vol. 19, no. 3, pp. 1263–1270, Aug. 2004.

[24] M. Ramezani, S. Golestan, S. Li, and J. M. Guerrero, "A simple approach to enhance the performance of complex-coefficient filter-based PLL in grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5081–5085, Jun. 2018.

[25] S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes, J. Doval-Gandoy, and F. D. Freijedo, "Small-signal modeling, stability analysis and design optimization of single-phase delay-based PLLs," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3517–3527, May 2016.

[26] S. Golestan, J. M. Guerrero, A. Abusorrah, M. M. Al-Hindawi, and Y. Al-Turki, "An adaptive quadrature signal generation-based single-phase phase-locked loop for grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2848–2854, Apr. 2017.

[27] T. I. Laakso, V. Valimaki, M. Karjalainen, and U. K. Laine, "Splitting the unit delay [FIR/all pass filters design]," *IEEE Signal Process. Mag.*, vol. 13, no. 1, pp. 30–60, Jan. 1996.

Authors' photographs and biographies not available at the time of publication.