

# A Novel Solid-State Circuit Breaker With Self-Adapt Fault Current Limiting Capability for LVDC Distribution Network

Bin Li , Member, IEEE, Jiawei He , Ye Li, and Ruisheng Li

**Abstract**—DC fault current limitation is important for the low-voltage dc distribution network, because the existing dc selective protection cannot act fast enough. However, the typical dc fault current limiting method—installing dc reactors directly in the dc system—will lead to negative influence on the system normal operation and dc circuit breaker (DCCB) fast isolation. This paper proposed a novel solid-state circuit breaker (SSCB) with self-adapt fault current limiting capability, namely, no negative influence on the dc distribution network normal operation, swift fault current limiting response to the dc fault, and efficient cooperation between the fault current limitation and isolation. The hybrid configuration strategy of the proposed SSCB and mechanical DCCB for multiterminal dc distribution network is proposed to reduce the conducting power loss and investment from the scale of the whole system. Finally, the experiment tests and simulation cases are carried out to verify the working principle and superiorities of the proposed SSCB.

**Index Terms**—DC fault ride-through, fault current limitation, low-voltage dc (LVDC) distribution network, solid-state circuit breaker (SSCB).

## I. INTRODUCTION

WITH the development of the voltage source converter (VSC) technique, more flexible control and better power quality of the dc system can be obtained [1], [2]. The low-voltage dc (LVDC) distribution network gradually becomes an important subject in the research of the distribution system, because it is beneficial to integrate the continuously increasing dc loads and dc distributed generators, e.g., the data centers, the electric vehicles, and the photovoltaic generators [3]–[5].

However, for engineering application, several key technical problems need to be solved first, one of which is the dc fault handling. In the LVDC distribution network, the VSCs will be widely applied, leading the dc fault current to increase extremely fast [6]. For the operation security and power supply reliability,

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an LCL–VSC converter composed of a VSC converter and a passive inductor–capacitor–inductor (LCL) circuit, which can limit the ac-side current and converter current effectively during dc faults. In the multiterminal dc system, it is very important to limit the dc line current and prevent the dc voltage dropping; however, the LCL–VSC converter does not have this ability. The superconducting fault current limiter (SFCL) has been proved to have a wide application prospect in the dc system [16]. And, it is worth conducting further researches on the dc-system-used SFCL, especially including the fast quench after dc faults, fast recovery after isolation, and so on. In addition, it has been proved that installing dc reactors is an effective way to limit dc fault current for the flexible HVDC transmission system [17]. It is obvious that the reactive fault current limiting method can also play a significant role in the LVDC distribution network, including limiting the fault current and preventing the dc voltage collapsing after dc faults. Moreover, the larger the installed reactor, the better the fault current limiting effect.

However, large dc reactors are not allowed to be installed in the dc system directly, because of the following negative influences.

- 1) *Influence on normal operation of the dc system:* As we know, the dc reactor will limit the current change rate, so it is not beneficial to the fast transient response of the dc system during power flow shifting [18], and may even lead to system instability. That is to say, it is necessary that the dc reactors are not connected into the circuit during normal operation.
- 2) *Slow down the isolating speed of the DCCB:* According to the working principle of the typical SSCB, the fault energy is dissipated by the arrester after the IGBTs are turned off (namely the SSCB is tripped). If the dc reactor is still connected in the fault circuit after that, the fault current clearing time of the arrester will be very long, because the energy stored in the dc reactor is mixed together with that of the dc line. In other words, the real isolating speed of the SSCB is prolonged drastically, which is detrimental to the fast recovery of the healthy network, and the fast recovery of the fault line insulation characteristic. Therefore, it is also expected that the dc reactor can be bypassed from the fault circuit after the SSCB is tripped.

The hybrid current-limiting circuit (HCLC) proposed in [19] can accelerate the DCCB isolating speed by connecting an energy dissipation circuit (EDC) in parallel with the reactor. Furthermore, this paper proposed a novel SSCB with self-adapt fault current limiting capability, which not only can accelerate the fault isolating speed but also can avoid the negative influences of the reactor on the system normal operation. This paper is organized as follows. In Section II, the novel SSCB with self-adapt fault current limiting capability is proposed. Then, the parameter design principle and hybrid configuration strategy are discussed in Section III. In Section IV, experiment tests are carried out to verify the working principle and superiority of the proposed SSCB. The advantages of the proposed SSCB for application in the multiterminal dc distribution network are further proved by the simulation cases in Section V. Finally, in Section VI, conclusions of this paper are given.

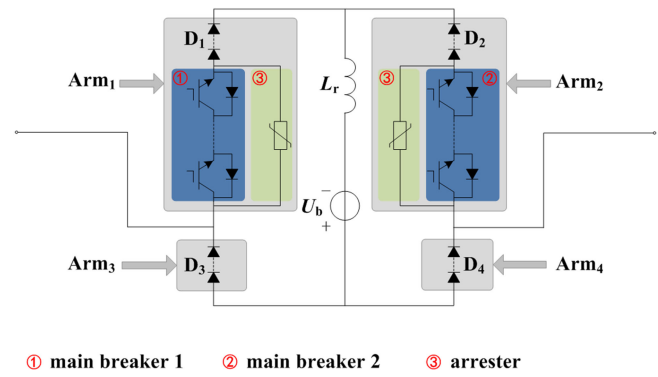


Fig. 1. Topology of the proposed SSCB.

## II. PROPOSED SOLID-STATE CIRCUIT BREAKER

### A. Topology and Working Principle of the Proposed SSCB

For lowering the requirement on the action speed of the dc fault handling (including fault detection, location, and isolation), effective dc fault current limiting measures must be taken in the dc distribution network. To eliminate the negative influences of installing the dc reactors directly, a novel SSCB that integrates self-adapt fault current limiting capability is proposed in this section. Here, the self-adapt fault current limiting capability refers to that the dc reactor for fault current limitation in the proposed SSCB can be bypassed from or connected into the dc line adaptively with different operation states.

The topology of the proposed SSCB is shown in Fig. 1. It consists of an H-bridge and a branch in which a dc reactor and a dc biased power supply are placed in series. In the H-bridge, the main breaker 1 composed of series IGBTs is connected with an arrester in parallel, and with the series diode group  $D_1$  in series, to constitute the Arm<sub>1</sub>, while the structure of Arm<sub>2</sub> is the same. For the other two arms (Arm<sub>3</sub> and Arm<sub>4</sub>), they are all composed of series diodes ( $D_3$  and  $D_4$ ). The branch composed of the dc reactor and dc biased power supply is placed between the common cathode point of  $D_1$ ,  $D_2$  and the common anode point of  $D_3$ ,  $D_4$ . The dc line is connected with the SSCB through the junctions between Arm<sub>1</sub> and Arm<sub>3</sub>, and Arm<sub>2</sub> and Arm<sub>4</sub>, respectively.

There are four operation states of the proposed SSCB, namely, the normal operation state, fault current limiting state, fault current clearing state, and recovery state.

1) *Normal Operation State:* During the system normal operation, all the IGBTs in the SSCB are in ON state. The dc biased power supply provides a dc biased current  $I_b$ . With different dc line current  $i_{dc}$ , the proposed SSCB has two operation modes during this state.

- 1)  $0 < i_{dc} < I_b(R_u + R_d)/2R_u$ : According to the Kirchhoff's current law theorem,  $I_b$  is averagely distributed to Arm<sub>1</sub> and Arm<sub>2</sub>, as well as Arm<sub>3</sub> and Arm<sub>4</sub>, because the conducting resistances of Arm<sub>1</sub> and Arm<sub>2</sub> are equal, and the resistances of Arm<sub>3</sub> and Arm<sub>4</sub> are also equal. In addition,  $i_{dc}$  is distributed to Arm<sub>1</sub> and Arm<sub>3</sub> at their junction. But, considering that the devices in Arm<sub>1</sub> and Arm<sub>3</sub> are different, which means their conducting

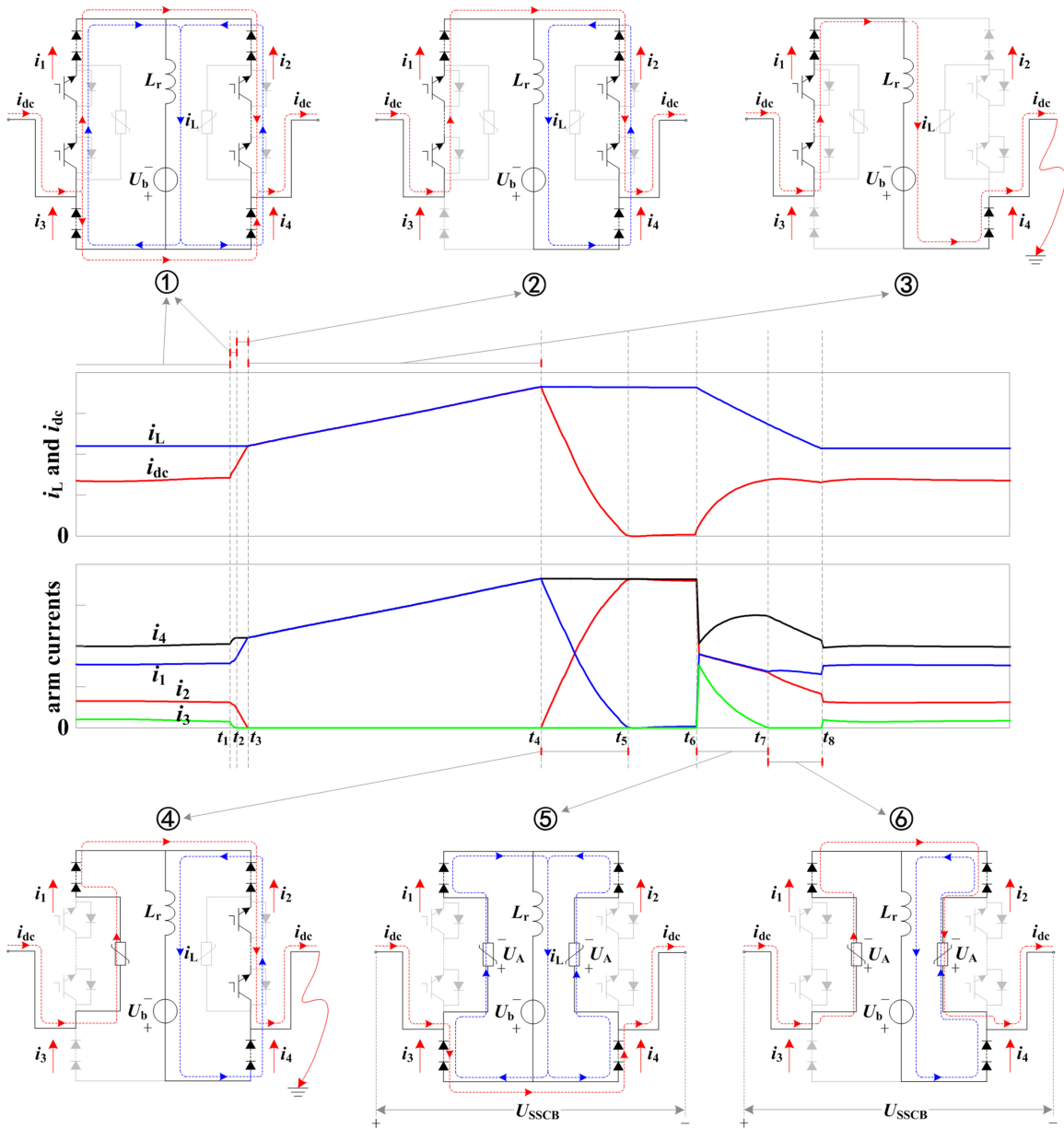


Fig. 2. Working principle of the proposed SSCB.

resistances are different, the distributed currents are also different. According to the current distribution theory of the parallel circuits, the current distributed to Arm<sub>1</sub> from  $i_{dc}$  is  $i_{dc}R_d/(R_u + R_d)$ , and the current distributed to Arm<sub>3</sub> from  $i_{dc}$  is  $i_{dc}R_u/(R_u + R_d)$ , where  $R_u, R_d$  are the conducting resistances of the upper arms (Arm<sub>1</sub> and Arm<sub>2</sub>) and down arms (Arm<sub>3</sub> and Arm<sub>4</sub>), respectively. Therefore, as shown in Fig. 2①, the currents of Arm<sub>1</sub> – Arm<sub>4</sub> ( $i_1 - i_4$ ) can be expressed as

$$\begin{cases} i_1 = \frac{1}{2}I_b + \frac{R_d}{R_u + R_d}i_{dc}, & i_2 = \frac{1}{2}I_b - \frac{R_d}{R_u + R_d}i_{dc} \\ i_3 = \frac{1}{2}I_b - \frac{R_u}{R_u + R_d}i_{dc}, & i_4 = \frac{1}{2}I_b + \frac{R_u}{R_u + R_d}i_{dc}. \end{cases} \quad (1)$$

Obviously,  $i_1$  and  $i_4$  are larger than 0. In addition, because  $i_{dc} < I_b(R_u + R_d)/2R_u$  and  $R_d < R_u$ , and  $i_3$  and  $i_2$  are also larger than 0. As shown in Fig. 2,  $i_1 - i_4$  are all

larger than 0 (corresponding to the arm current schematic waveforms before  $t_1$ ), meaning that Arm<sub>1</sub> – Arm<sub>4</sub> are all conducting. Therefore, it can be considered that the dc reactor is bypassed from the dc line by the conducting Arm<sub>1</sub> – Arm<sub>4</sub>.

- 2)  $I_b(R_u + R_d)/2R_u \leq i_{dc} < I_b$ : Obviously, according to (1), D<sub>3</sub> cannot conduct under this condition because  $I_b/2 - i_{dc}R_u/(R_u + R_d) \leq 0$ . Therefore, the biased current  $I_b$  can only flow through Arm<sub>4</sub> and Arm<sub>2</sub>, and the dc line current  $i_{dc}$  flows to Arm<sub>1</sub> completely at the junction between Arm<sub>1</sub> and Arm<sub>3</sub>. As shown in Fig. 2②, the arm currents can be expressed as

$$\begin{cases} i_1 = i_{dc}, & i_2 = I_b - i_{dc} \\ i_3 = 0, & i_4 = I_b. \end{cases} \quad (2)$$

Obviously,  $i_1$  and  $i_4$  are all larger than 0. Considering that  $i_{dc} < I_b$ , and  $i_2$  is also larger than 0. Therefore, Arm<sub>1</sub>, Arm<sub>2</sub>, and Arm<sub>4</sub> are conducting under this condition, and it can also be concluded that the dc reactor is bypassed from the dc line by the conducting arms Arm<sub>1</sub> and Arm<sub>2</sub>.

In conclusion, as long as the dc line current  $i_{dc}$  does not exceed the dc biased current  $I_b$ , the dc reactor is always bypassed from the dc line, thus having no influence on the normal operation of the dc system.

2) *Fault Current Limiting State*: When a dc fault happens, the dc fault current rises [6]. Supposing that the dc line current satisfies  $0 < i_{dc} < I_b(R_u + R_d)/2R_u$  before the fault, the arm currents  $i_2$  and  $i_3$  will decrease with  $i_{dc}$  rising according to (1), as the current schematic waveforms shown in Fig. 2. And,  $i_3$  reaches 0 first, because  $R_u > R_d$ . This means that Arm<sub>3</sub> is turned OFF automatically, and the operation mode of the proposed SSCB gets into Fig. 2② from ①. According to (2),  $i_2$  continues to decrease. As long as  $i_{dc}$  increases to exceed  $I_b$ ,  $i_2$  reaches 0 and Arm<sub>2</sub> is turned OFF automatically. As shown in Fig. 2③, the dc line current  $i_{dc}$  can only flow through Arm<sub>1</sub>, the dc reactor branch, and Arm<sub>4</sub>, which means that the dc reactor is connected into the fault circuit instantaneously and automatically, working to limit the fault current. Similarly, when  $i_{dc} < 0$ , once  $|i_{dc}| > I_b$ , only Arm<sub>2</sub> and Arm<sub>3</sub> will conduct, so the dc reactor is also connected into the fault circuit instantaneously and automatically to limit the fault current. In sum, the proposed SSCB has an automatic (without any change of the SSCB control) and bidirectional fault current limiting capability. Moreover, this fault current limiting response to dc faults can be very fast as long as  $I_b$  is properly set.

In addition, it should be noted that in Fig. 2, the current schematic waveforms before the fault correspond to the condition  $0 < i_{dc} < I_b(R_u + R_d)/2R_u$ . After the dc fault, the proposed SSCB will get into the fault current limiting state from the normal operation state, as shown in Fig. 2①, passing the transition state, as shown in Fig. 2②. Differently, if  $I_b(R_u + R_d)/2R_u \leq i_{dc} < I_b$  before the dc fault, the proposed SSCB will get into the fault current limiting state directly from the normal operation state, as shown in Fig. 2②.

3) *Fault Current Clearing State*: As shown in Fig. 1, the proposed SSCB has two main breakers. When the tripping signal from the protection is received, the corresponding main breaker should be turned OFF, with the other one still in ON state. For example, as shown in Fig. 2④, if the fault is located at the Arm<sub>2</sub> side, the main breaker 1 in Arm<sub>1</sub> should be turned OFF, while the main breaker 2 in Arm<sub>2</sub> is still in ON state (taking the SSCB on the positive pole for instance). On the contrary, if the fault is located at the Arm<sub>1</sub> side, the main breaker 2 in Arm<sub>2</sub> should be turned OFF, and the main breaker 1 in Arm<sub>1</sub> is still in ON state.

As shown in Fig. 2④, once one of the main breakers is turned OFF (main breaker 1 for instance), the corresponding arrester will be connected into the fault circuit, and thus, the fault current begins to decrease. In this state, the freewheeling current of dc reactor will produce a reverse electromotive force to make Arm<sub>2</sub> and Arm<sub>4</sub> conduct, and Arm<sub>3</sub> is turned OFF by the reverse clamping voltage from the arrester in Arm<sub>1</sub>. So, the freewheeling current of the dc reactor will only flow through Arm<sub>2</sub> and Arm<sub>4</sub>.

It indicates that the dc reactor in the proposed SSCB is bypassed from the fault circuit again after turning OFF one of the main breakers. That is to say, the arrester need not dissipate the energy stored in the dc reactor, because the freewheeling current of the dc reactor can flow in the SSCB itself, and it can be considered that the energy in the reactor is separated from the dc line. So, the arrester only needs to dissipate the fault energy of the line during the fault current clearing period, as the current schematic waveforms during  $t_4 - t_5$ , as shown in Fig. 2. According to the calculation method proposed in [20], the fault current clearing time under this condition can be expressed as

$$T_{\text{clear}} = I_{\text{trip}} L_l / (U_A - U_{dc}/2) \quad (3)$$

where  $I_{\text{trip}}$  is the dc fault current at the moment when the main breaker is turned OFF,  $L_l$  is the equivalent inductance of the fault line,  $U_A$  is the clamping voltage of the arrester, and  $U_{dc}$  is the dc voltage of the dc system. Obviously,  $T_{\text{clear}}$  of the proposed SSCB is much smaller compared with the condition that the dc reactors are directly installed, because when the dc reactors are directly installed,  $T_{\text{clear}}$  is

$$T_{\text{clear}} = I_{\text{trip}} (L_l + L_r) / (U_A - U_{dc}/2) \quad (4)$$

where  $L_r$  is the value of the directly installed dc reactor. Generally,  $L_r$  is much larger than  $L_l$ .

Therefore, the isolating speed of the proposed SSCB is much faster compared with the condition that the dc reactors are directly installed in the dc system. This important feature is beneficial to guarantee the fast recovery of the healthy network and the fast recovery of the fault line insulation characteristic.

4) *Recovery State*: After the fault point has disappeared or been removed, the fault line should be reconnected into the system. Meanwhile, the freewheeling current of the dc reactor (namely  $i_L$ ) in the proposed SSCB is also required to recover to the set value  $I_b$ . It should be noted that the definitions of  $i_L$  and  $I_b$  are different in this paper.  $I_b$  is the dc biased current set value required to be provided by the biased power supply during system normal operation, which is a constant (neglecting the change of the power electronic switch conducting resistance), and  $i_L$  refers to the current flowing through the dc reactor. During system normal operation, the dc line current does not flow through the dc reactor, and the dc reactor current  $i_L$  is dependent on the dc biased power supply, which means  $i_L = I_b$ . But, when the proposed SSCB gets into the fault current limiting state, shown in Fig. 2③, the dc reactor is connected into the fault circuit; therefore,  $i_L = i_{dc}$  in this state.  $i_L$  is not equal to  $I_b$  anymore, because the current flowing through the dc reactor branch is not dependent on the dc-biased power supply. Then, during the fault current clearing state,  $i_{dc}$  decreases very quickly due to the arrester. But,  $i_L$  only flows through Arm<sub>2</sub> and Arm<sub>4</sub>, being not exposed to the arrester, which means it decreases very slowly. Therefore,  $i_L$  will have a large value before the recovery state, which is much larger than  $I_b$ .

For the recovery of  $i_L$ , namely the recovery of the proposed SSCB, the other main breaker still in ON state is turned off first, as shown in Fig. 2⑤. Therefore, the stored energy in the dc reactor can be dissipated by the arresters, and the freewheeling current  $i_L$  of the reactor will decay rapidly. Then, both the main

breakers 1 and 2 are turned ON synchronously when  $i_L$  decays to near  $I_b$ , which means that the proposed SSCB is recovered completely, to prepare for handling the next fault.

In addition, the recovery state of the proposed SSCB also has two operation modes, as shown in Fig. 2⑤ and ⑥.

- 1)  $i_{dc} < i_L/2$ : Before the recovery state, the dc line current  $i_{dc} = 0$ , because it has been cleared by the arrester in the fault current clearing state. Therefore, as long as the proposed SSCB gets into the recovery state, the dc reactor current  $i_L$  is equally distributed to the branch composed of Arm<sub>1</sub> and Arm<sub>3</sub>, and the branch composed of Arm<sub>2</sub> and Arm<sub>4</sub>, and the dc line current  $i_{dc}$  can flow through Arm<sub>3</sub> and Arm<sub>4</sub> directly as long as  $i_{dc} < i_L/2$ , as shown in Fig. 2⑤. So,  $i_{dc}$  begins to recover quickly as the current schematic waveforms shown in Fig. 2. Moreover, the clamping voltages on the two arresters respectively in Arm<sub>1</sub> and Arm<sub>2</sub> are so polarity-opposite that they just cancel each other out from the dc line, namely, the voltage across the proposed SSCB  $U_{SSCB} \approx U_A - U_A = 0$ . Therefore, it can be considered that the arresters almost do not function to the dc system. In other words, the fault line is re-connected into the system at the moment when the other main breaker is turned OFF, and the fault part of the system can recover immediately. This means the recovery of the proposed SSCB almost has no influence on the recovery of the dc system.
- 2)  $i_{dc} \geq i_L/2$ : During the recovery state,  $i_L$  decreases quickly and  $i_{dc}$  increases. If  $i_{dc}$  increases to exceed  $i_L/2$ , Arm<sub>3</sub> will not conduct anymore, and  $i_L$  can only flow through Arm<sub>2</sub> and Arm<sub>4</sub>. As shown in Fig. 2⑥, the voltage across the proposed SSCB still satisfies  $U_{SSCB} \approx U_A - U_A = 0$ . So, under this condition, it can still be considered that the recovery of the SSCB almost has no influence on the recovery of the dc system.

### B. Comparison With the Existing Methods

Obviously, the method of installing the dc reactor directly is the simplest dc fault current limiting method, which, however, has negative influences on the system normal operation and DCCB isolating speed. The HCLC method proposed in [19] turns ON the thyristors after opening the DCCB, to make the resistor in the EDC dissipate the fault energy together with the arrester in the DCCB, and thus, the current clearing speed can be accelerated significantly. However, during system normal operation, the reactor in the HCLC is always connected in the dc line, even when the power flow shifts. This means that the HCLC method cannot avoid the negative influence of the reactor on the system normal operation. Differently, the proposed method can bypass or connect the large dc reactor from or into the dc line adaptively with different operation states of the SSCB, namely, the self-adapt fault current limiting. The detailed advantages of the proposed SSCB are listed as follows.

- 1) During normal operation, the dc reactor in the proposed SSCB is bypassed from the dc line, thus having no negative influence on the system, including transient response speed, stability, and so on.
- 2) After dc faults, the dc reactor is connected into the fault circuit very quickly and automatically. It can limit the fault

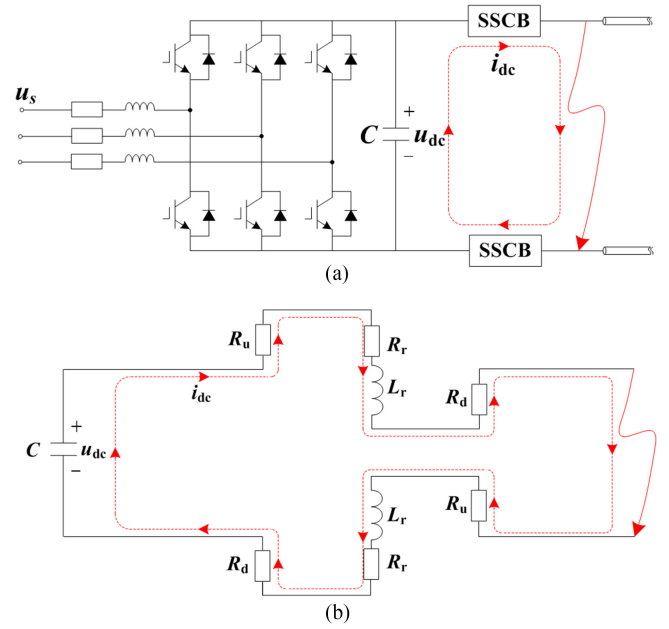


Fig. 3. DC pole-to-pole fault. (a) Equivalent circuit of the dc pole-to-pole fault at the converter output position. (b) Equivalent circuit of the capacitor discharge stage with the proposed SSCB.

current and slow the dc voltage dropping, guaranteeing the fault ride-through of the healthy network, and thus creating enough time for the protection and isolation.

- 3) During the fault current clearing state, the dc reactor is bypassed from the fault circuit again, also instantaneously and automatically. It can accelerate the fault isolation drastically, guaranteeing the fast recovery of the healthy network and the fast recovery of the fault line insulation characteristic.
- 4) The fault part of the system can recover quickly after the fault point has disappeared or been removed, and the SSCB itself can also recover quickly, preparing for handling the next fault.

## III. PARAMETER DESIGN AND HYBRID CONFIGURATION FOR THE MULTITERMINAL DC DISTRIBUTION NETWORK

### A. Parameter Design of the Proposed SSCB

The design of the proposed SSCB key parameters, mainly including the value of required dc reactor, withstand voltage and current of the power electronic devices, dc biased current, and arrester capacity, is discussed in this section, for the purpose of healthy network fault ride-through and gaining enough time for the protection. In the dc distribution system, the proposed SSCB can be installed at the dc output positions of the converters, and the parameters should be determined according to the most serious condition, i.e., the metallic pole-to-pole fault at the converter output position, as shown in Fig. 3(a).

1) *Required DC Reactor*: After dc faults, the dc reactor in the proposed SSCB is connected into the fault circuit very quickly to slow the fault propagation, and gain enough time for the protection. Two factors should be considered when determining the value of the required dc reactor.

As shown in Fig. 3(b), with the dc reactor being connected, the fault process will stay in the capacitor discharge stage chronically. In this stage, the overcurrent mainly occurs at the dc side [6]. Therefore, the main target of the fault current limitation is to limit the dc current  $i_{dc}$  below the permitted level, namely,  $i_{dc} \leq I_{set}$ , before the protection acts to trip the corresponding DCCBs.

In addition, during the capacitor discharge stage, the dc voltage decays. If the dc voltage decays to below  $2U_m$  (ac phase voltage amplitude), the converter will be blocked due to over-modulation. Hence, the dc voltage  $u_{dc}$  should remain above the permitted value, namely,  $u_{dc} \geq U_{set}$ .

The transient characteristic shown in Fig. 3(b) is a second-order process. In addition, the fault current limiting effect of conducting resistances ( $R_u$ ,  $R_d$ ,  $R_r$ ) of the power electronic devices and dc reactor is tiny; thus, it is neglected when calculating the required dc reactor. Therefore, the dc voltage and dc current during the capacitor discharge stage can be expressed as

$$u_{dc} = U_0 \cos \omega t - \frac{I_0}{\omega C} \sin \omega t \quad (5)$$

$$i_{dc} = U_0 \omega C \sin \omega t + I_0 \cos \omega t \quad (6)$$

where  $U_0$  and  $I_0$  are the initial values of the dc voltage and dc current,  $L_r$  is the value of the dc reactor, and  $\omega = \sqrt{1/2L_r C}$ .

Therefore, the required value  $L_r$  of the dc reactor in the proposed SSCB can be calculated by solving the following equations:

$$U_0 \cos \omega t_{trip} - \frac{I_0}{\omega C} \sin \omega t_{trip} = U_{set} \quad (7)$$

$$U_0 \omega C \sin \omega t_{trip} + I_0 \cos \omega t_{trip} = I_{set} \quad (8)$$

where  $t_{trip}$  is the needed time from the fault moment to the moment when the DCCB is tripped. Because (7) and (8) are both the transcend equations, so the iterative algorithm, such as the dichotomy algorithm, based on the computer is used to solve these equations, and the larger solution of these two equations is selected as the required value of the dc reactor.

2) *Withstand Voltages and Currents of the Power Electronic Devices*: For the proposed SSCB, IGBTs and diodes are used, whose maximum voltages and currents should be estimated for type selection. According to the working principle of the proposed SSCB, the maximum currents flowing through the IGBTs and diodes are both the same as its breaking current. Generally, in the dc system, the breaking current of the SSCB should be determined according to the overcurrent tolerance of the key equipment, such as the converter, the dc cable, and so on. Therefore, the current parameter of the IGBTs and diodes can also be determined according to this experience. In addition, the IGBTs of the main breakers in the SSCB only need to withstand the clamping voltage of the arrester, namely  $U_A$ , so the withstand voltage of the IGBTs can be determined correspondingly. Differently, as shown in Fig. 2③ and ④, the series diodes group should withstand the clamping voltage of the arrester or the voltage of the dc reactor. Therefore, the withstand voltage of the series diodes groups D<sub>1</sub>–D<sub>4</sub> is selected as the larger one between  $U_A$  and  $U_{L\_max}$ , where  $U_{L\_max}$  is the largest voltage drop on the dc reactor. According to Fig. 3(b),  $U_{L\_max}$  can be

estimated as  $L_r \times di_{dc}/dt|_{t=0} = 0.5U_0$ . Based on the analysis presented above, the type and the number of IGBTs and diodes in the proposed SSCB can be determined.

3) *DC Biased Current*: According to the working principle of the proposed SSCB,  $I_b$  should not be smaller than the normal operation dc current  $i_{dc}$ , preventing the dc reactor from adversely affecting the system normal operation, especially the fast transient response and stability of the dc system during power flow shifting. In addition,  $I_b$  should also not be too large, for the fast current-limiting response to the faults. Therefore,  $I_b$  is designed as the largest dc load current or a little larger. In particular, it is also feasible to set  $I_b$  as the largest dc load current. Under this condition, although the dc reactor is connected into the dc line similar to Fig. 2③ when the converter operates at the largest dc load current, it will be bypassed from the dc line instantaneously and automatically during the power flow shifting, because  $i_{dc}$  will only decrease under this critical condition and the operation state of the proposed SSCB will come back to Fig. 2②. For the required dc biased current, the voltage of the biased power supply should be estimated according to the conducting resistance of the biased current flowing path, mainly including the conducting resistance of the dc reactor and the conducting resistances of the power electronic switches in the SSCB arms. But, it may be hard to calculate the conducting resistances of the power electronic switches accurately in the practical engineering, which may change with different flowing currents and temperatures. Therefore, the influence of the variety of the switch resistance on the feeding biased current and corresponding improved biased power supply design method will be researched in the future work.

4) *Arrester Capacity*: The capacity of the arrester, referring to the energy the arrester needs to absorb, should be selected when design the proposed SSCB. According to the working principle, the arrester needs to dissipate the fault energy of the line during the fault current clearing state and part of the reactor energy (from  $I_{trip}$  to  $I_b$ ) during the recovery state. During the fault current clearing state, the fault energy in the dc line is dissipated by the connected arrester as shown in Fig. 4(a), which can be mathematically equivalent to

$$2U_A + 2L_l \frac{di_{dc}}{dt} = U_{dc}. \quad (9)$$

Therefore, the dc line current  $i_{dc}$  can be expressed as

$$i_{dc} = I_{trip} - \frac{U_A - U_{dc}/2}{L_l} t. \quad (10)$$

Based on (10), the energy absorbed by the arrester in one SSCB thus can be calculated as

$$\begin{aligned} W_{A1} &= \int_0^{\frac{I_{trip} L_l}{U_A - U_{dc}/2}} U_A \cdot \left( I_{trip} - \frac{U_A - U_{dc}/2}{L_l} t \right) dt \\ &= U_A \cdot \left( I_{trip} t - \frac{U_A - U_{dc}/2}{2L_l} t^2 \right) \Big|_{t=0}^{t=\frac{I_{trip} L_l}{U_A - U_{dc}/2}} \\ &= \frac{1}{2} \frac{U_A}{U_A - U_{dc}/2} L_l I_{trip}^2. \end{aligned} \quad (11)$$

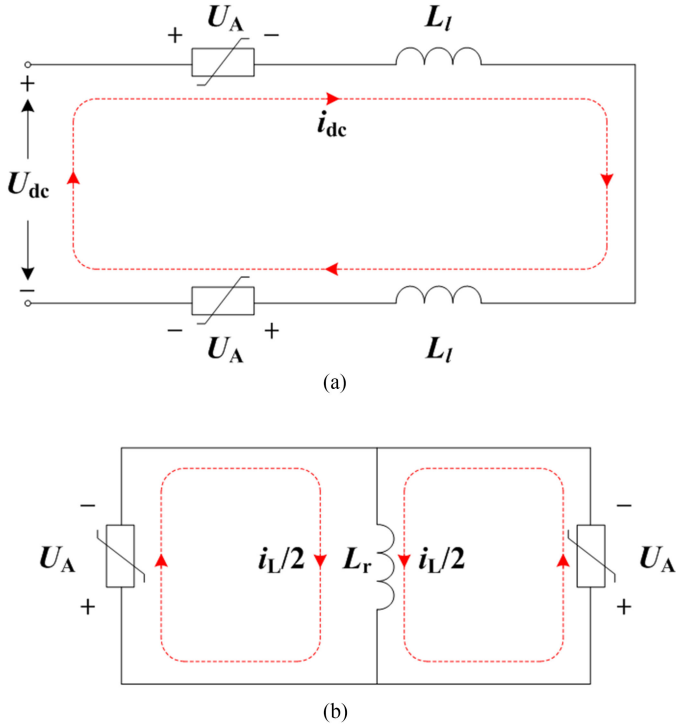


Fig. 4. Equivalent circuit of the fault current clearing state and recovery state. (a) Equivalent circuit of the fault current clearing state. (b) Equivalent circuit of the recovery of the proposed SSCB.

In addition, according to Fig. 4(b), the energy stored in the reactor should be dissipated to make  $i_L$  decay from  $I_{trip}$  (neglecting the decay of  $i_L$  due to the conducting resistors of the devices in the SSCB) to  $I_b$ . In Fig. 4(b), the biased power supply is also neglected because its output voltage is very small compared with  $U_A$ . Obviously, this part of energy is completely absorbed by the two arresters on Arm<sub>1</sub> and Arm<sub>2</sub> on average. Therefore, the energy absorbed in each arrester can be calculated by

$$W_{A2} = \frac{1}{4} L_r (I_{trip}^2 - I_b^2). \quad (12)$$

Finally, the largest energy may absorbed by one arrester  $W_A = W_{A1} + W_{A2}$ , namely

$$W_A = \frac{1}{2} \frac{U_A}{U_A - U_{dc}/2} L_l I_{trip}^2 + \frac{1}{4} L_r (I_{trip}^2 - I_b^2). \quad (13)$$

According to (13), the capacity of the arrester can thus be selected.

### B. Hybrid Configuration of the DCCBs in the Multiterminal DC Distribution Network

The dc fault propagation in dc system is extremely fast, so it requires the action speed of the protection and DCCB can be quick enough, e.g., 2–4 ms (including the action time of the protection and DCCB) [4], [7]. Therefore, the high-speed SSCBs should be installed widely in the dc system [13], including the converter output positions and each terminal of the dc lines. Obviously, it is not economical because the conducting power loss and investment will be very high. Installing dc reactors in the dc system can slow the fault propagation effectively and, thus, lower the requirement on the action speed of

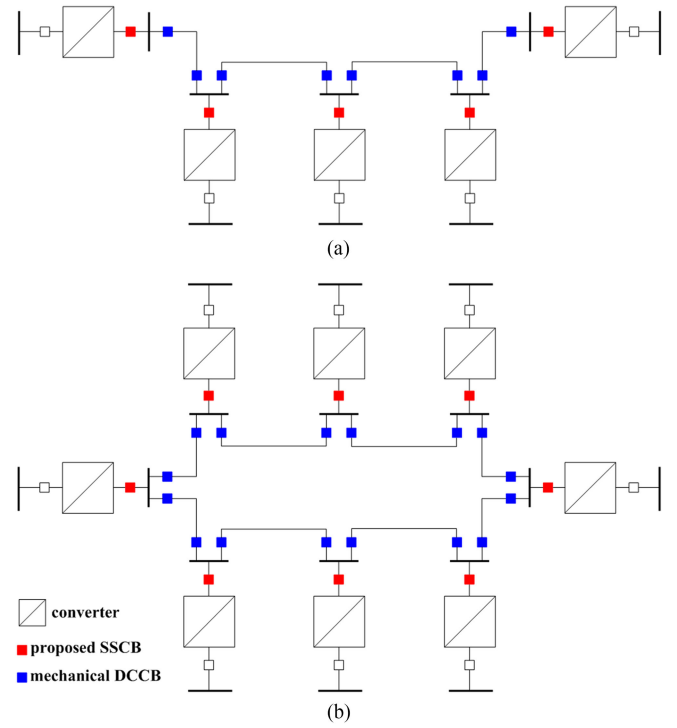


Fig. 5. Hybrid configuration idea of the proposed SSCB and mechanical DCCB in the multiterminal dc distribution network. (a) Radial dc system. (b) Meshed dc system.

the protection and DCCB. However, as analyzed in Section I, the large dc reactors directly installed in the dc system have negative influences on the normal operation of the system and isolating speed of the DCCB, thus being not feasible for the dc distribution network. Differently, the proposed SSCB with self-adapt fault current limiting capability has no negative influences described above, so it has outstanding application prospect in the dc distribution network.

Furthermore, considering that the negative influences of the dc reactor have been avoided, a large enough reactor can be installed in the proposed SSCB to limit the fault current thoroughly. In addition, according to the dc fault transient characteristic, the fault current is mainly provided by converter capacitors [6]. Therefore, as long as the proposed SSCB is installed at each converter output position, the fault current of the whole dc system is limited effectively, wherever the dc fault position is. Under this condition, the other positions of the dc system, mainly referring to the dc line terminals, can be configured with the mechanical DCCBs to replace the SSCBs, because the fault current has been limited by the proposed SSCBs installed at the converter output positions and it is not necessary to isolate the fault very fast (e.g., 2–4 ms) anymore. According to the analysis presented above, the hybrid configuration strategy of the proposed SSCB and mechanical DCCB for the multiterminal dc distribution network is proposed, i.e., installing the proposed SSCB at each converter output position and installing the mechanical DCCBs at the dc line terminals. Taking the radial dc system shown in Fig. 5(a) for instance, without the proposed SSCB, 26 typical SSCBs (positive and negative poles) should be installed. When the proposed SSCBs are installed at

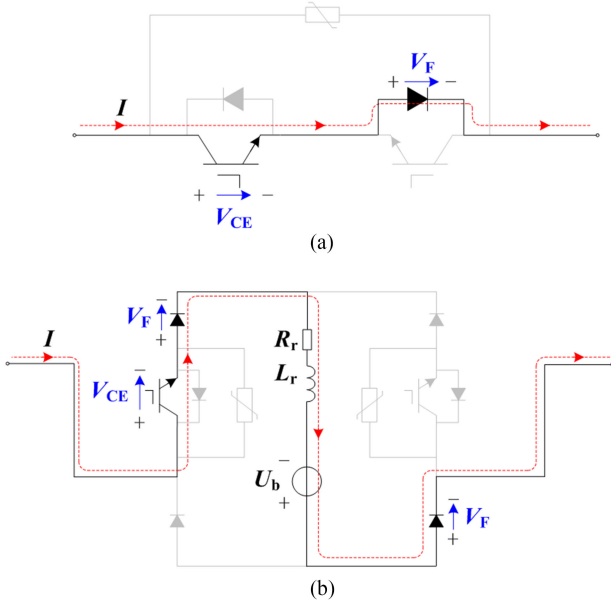


Fig. 6. Equivalent circuit for calculating the conducting power loss. (a) Typical SSCB. (b) Proposed SSCB.

the converter output positions, the remaining 16 SSCBs on the dc lines can be replaced by the mechanical DCCBs. Considering that the conducting power loss and investment of the mechanical DCCB is much smaller than the SSCB, it is obvious that this hybrid configuration strategy can reduce economic cost significantly. With the system scale increasing, this advantage will become more evident. Such as the meshed dc system shown in Fig. 5(b), 32 SSCBs can be replaced by the mechanical DCCBs.

### C. Power Loss Analysis

The conducting power loss of DCCBs is one of the key factors for engineering application, because it is directly related to the economic cost. Therefore, the power loss of installing the typical SSCBs is analyzed to be compared with that of the hybrid configuration strategy from the scale of the whole system, taking the dc voltage 1.5 kV and dc current 0.1 kA for instance.

For the typical SSCBs, the clamping voltage  $U_A$  of the arrester in each SSCB (installed on the positive and negative poles respectively) should be larger than 0.75 kV, to realize reliable fault isolation. Here, Infineon IGBT FF200R12kS4 (1.2 kV and 0.2 kA rated) is selected for instance, and two IGBTs (bidirectional isolation) are needed for one SSCB. As shown in Fig. 6(a), during normal operation, the current flows through one IGBT and one antiparallel diode. According to the datasheet of FF200R12kS4,  $V_{CE}$  at  $I = 0.1$  kA is about 2.7 V and  $V_F$  at  $I = 0.1$  kA is about 1.3 V, so the conducting power loss of one typical SSCB can be calculated as

$$P_{\text{loss\_typical\_SSCB}} = 100 \times 2.7 + 100 \times 1.3 = 0.4 \text{ kW}. \quad (14)$$

For the proposed SSCB, the required number of IGBTs is the same with the typical SSCB, and, according to Section A, the required number of diodes is 4.  $I_b$  is set as 0.1 kA. Under

this condition, the current flowing path in the proposed SSCB is shown as Fig. 6(b) at the largest load current 0.1 kA. According to Fig. 6(b), the conducting power loss of the proposed SSCB is composed of three parts, namely, the conducting loss of the power electronic switches, the conducting loss of the reactor, and the conducting loss of the biased power supply. The method to calculate the conducting loss of the power electronic switches is the same as the typical SSCB. For the dc reactor conducting loss, the equivalent resistor of a 50-mH dc reactor produced by a manufacturer in China is about 0.0072  $\Omega$ . In the 1.5 kV, 0.1-kA dc system, a 75-mH reactor in the proposed SSCB is enough (seeing the detailed system parameters in simulation), namely, with an equivalent resistor about 0.011  $\Omega$ . So, the corresponding conducting loss can be calculated as  $100 \text{ A} \times 100 \text{ A} \times 0.011 \Omega = 0.11 \text{ kW}$ . In addition, the dc biased power supply is generally also based on the power electronic switches, but it is obvious that the voltage rating of the switches in the biased power supply is much smaller than that of the switches in the SSCB arms. This means that the conducting loss of the biased power supply is much smaller than that of the switches in the arms and, thus, can be neglected. In conclusion, the conducting power loss of the proposed SSCB can be calculated as

$$P_{\text{loss\_pro\_SSCB}} = 100 \times 2.7 + 2 \times 100 \times 1.3 + 0.11 \text{ kW} = 0.64 \text{ kW}. \quad (15)$$

Due to the additional diodes and dc reactor, the conducting power loss of one proposed SSCB is slightly larger than one typical SSCB. However, for the multiterminal dc distribution network, when the proposed SSCBs are installed at converter output positions, only the mechanical DCCBs are required to be installed at other positions, as described in the hybrid configuration strategy in Section B. Differently, if the typical SSCBs are applied, they should be installed at each position in the system. Under this condition, the advantage of hybrid configuration strategy is highlighted, because power loss of the mechanical DCCB is extremely small (can be neglected). Taking the radial dc system shown in Fig. 5(a) for instance, the power losses of using typical SSCB and the hybrid configuration strategy are

$$P_{\text{loss\_typical}} = 0.4 \times 26 = 10.4 \text{ kW} \quad (16)$$

$$P_{\text{loss\_hybrid}} = 0.64 \times 10 = 6.4 \text{ kW}. \quad (17)$$

According to (16) and (17), 4 kW power is saved by the hybrid configuration strategy. With the system scale increasing, this advantage is more evident. For example, for the meshed dc system shown in Fig. 5(b), the corresponding power losses are

$$P_{\text{loss\_typical}} = 0.4 \times 48 = 19.2 \text{ kW} \quad (18)$$

$$P_{\text{loss\_hybrid}} = 0.64 \times 16 = 10.24 \text{ kW}. \quad (19)$$

According to (18) and (19), 8.96 kW power is saved.

## IV. EXPERIMENT TEST

### A. Test Setup

The proposed SSCB is built according to the topology described above, and a scaled-down test circuit is also constructed

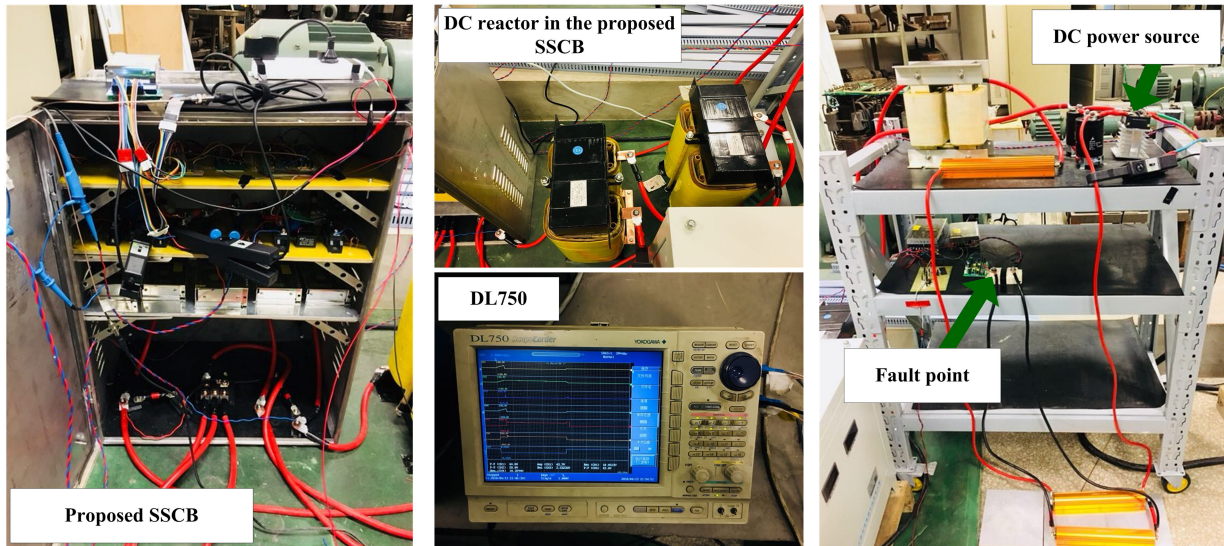
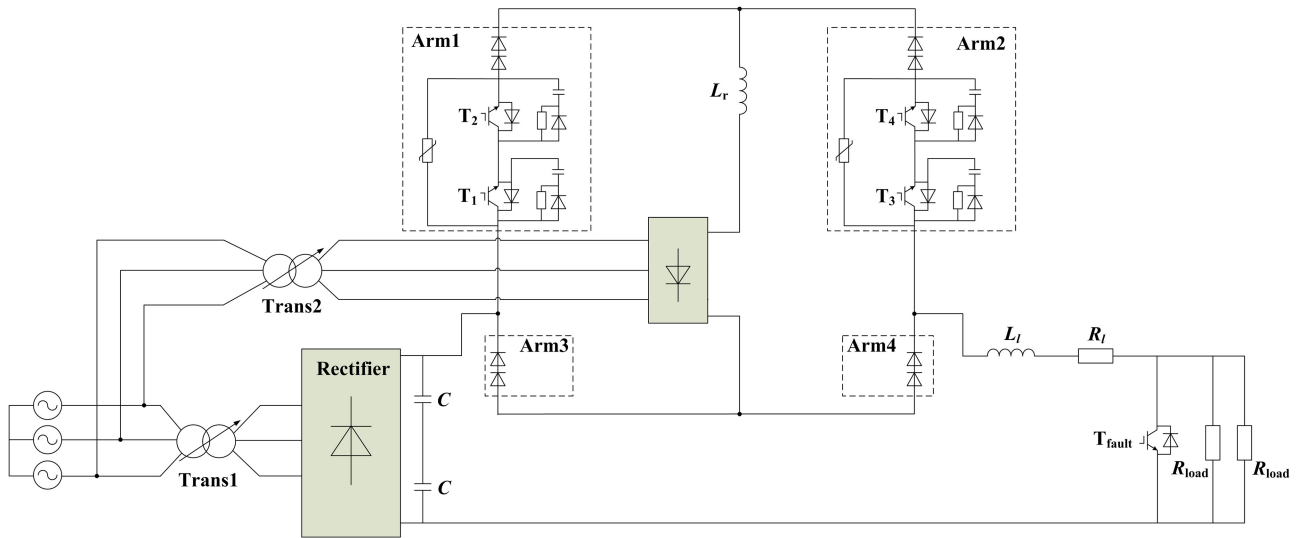


Fig. 7. Experiment test circuit of this paper.

as shown in Fig. 7, to verify the working principle and superiority of the proposed SSCB.

Fig. 7 illustrates the proposed SSCB experiment test circuit, whose parameters have been listed in Table I. Two series capacitors are connected with a rectifier in parallel to build up the desired voltage. The dc line is imitated by a resistor and a reactor. Particularly, the dc biased power supply is simply designed as an uncontrolled rectifier, and the required dc biased current can be obtained by regulating the input ac voltage of the rectifier. Obviously, this kind of dc biased power supply is very simple to be realized in the practical engineering. It should be noted that the IGBT and arrester of the typical SSCB in the comparative experiments are the same as the proposed SSCB. Considering that the largest energy absorbed by the arrester may be larger than the tolerated energy of one MYG 20D241K, two MYG 20D241Ks are connected in parallel for the SSCBs in the experiment tests.

## B. Test Results

1) *Performance of the Designed DC Biased Power Supply:* As shown in Fig. 7, the dc biased power supply in the proposed SSCB is designed as an uncontrolled rectifier, and the required dc biased current is obtained by regulating the input ac voltage. According to the experiment results shown in Fig. 8, with a little dc voltage ( $< 7$  V), the current flowing through the reactor branch  $i_L$  is approximately equal to the designed dc biased current 15 A, which is always larger than the dc line current  $i_{dc}$ . It should be noted that, although the output voltage of the designed dc biased power supply has a fluctuation on the basis of the dc voltage, the waveform quality of the biased current is very good, because of the reactor filtering effect. This means the designed biased power supply can satisfy the requirement of the proposed SSCB.

2) *Power Flow Shifting:* In this case, the load resistor is changed from  $40 \Omega$  to  $20 \Omega$  at  $t = 0$  s with different fault handling

TABLE I  
PARAMETERS OF THE EXPERIMENT TEST CIRCUIT

PARAMETER	VALUE
Rated dc voltage (V)	200
Rated dc current (A)	10
Capacitor $C$ (mF)	4.7
IGBT of the SSCB	FF200R12kS4
Diode of the SSCB	MD200A1600V
Arrester	MYG 20D241K
DC reactor $L_r$ (mH)	40
DC biased current (A)	15
Equivalent dc line resistor $R_l$ ( $\Omega$ )	0.3
Equivalent dc line inductor $L_l$ (mH)	3

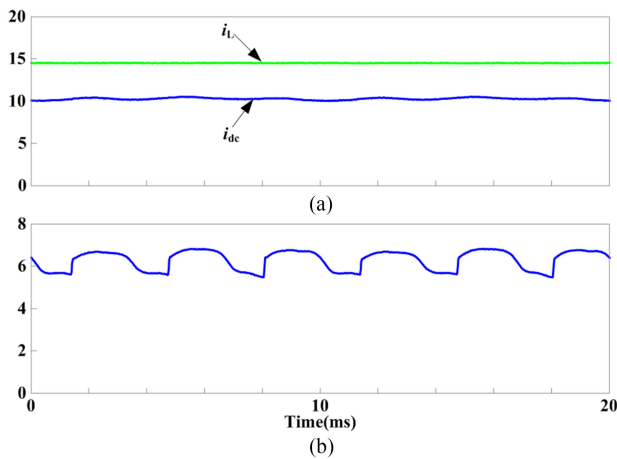


Fig. 8. Performance of the designed dc biased power supply in the proposed SSCB. (a) Current flowing through the reactor branch  $i_L$  and the dc line current  $i_{dc}$  (A). (b) Output voltage of the designed dc biased power supply (V).

strategies, and the corresponding experimental results are shown in Fig. 9. According to the experimental results, when the dc reactor is directly installed, the dc current changes very slowly. It needs about 10 ms to change to the new load current (about 10 A). This transient response speed is much slower than the condition without the dc reactor. In fact, in the VSC-based dc distribution system, this phenomenon may even lead to system instability, because the PI control is applied. Differently, when the proposed SSCB is installed, the dc current changes to the new load current very quickly (about 1 ms), which is very close to the condition without dc reactor. Fig. 9(b) shows the arm currents of the proposed SSCB during the power flow shifting. As the experimental results show, the currents of Arm<sub>1</sub>, Arm<sub>2</sub>, and Arm<sub>4</sub> ( $i_{arm1}$ ,  $i_{arm2}$ , and  $i_{arm4}$ , respectively) are always larger than 0, which means that the dc reactor is always bypassed from the dc line by the conducting Arm<sub>1</sub> and Arm<sub>2</sub>. This is the reason why the proposed SSCB has no influence on the transient response speed of the system, which is very important for the stability of the dc distribution network. Additionally, in this case, it should be noted that the dc current has a wave, except the condition that the dc reactor is installed directly. This

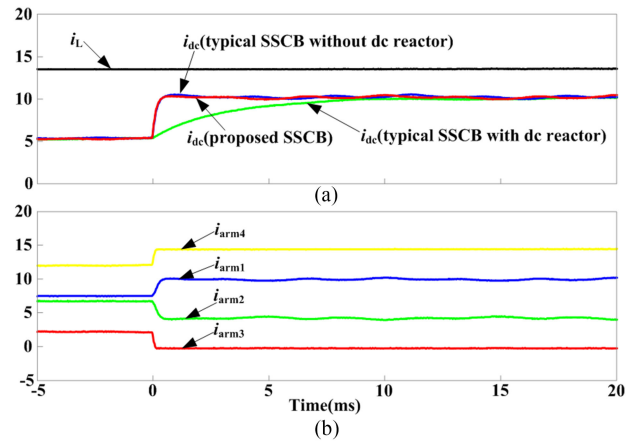


Fig. 9. Experimental results of the power flow shifting with different fault handling strategies. (a) DC line current  $i_{dc}$  and the current flowing through the reactor branch  $i_L$  (A). (b) Arm currents of the proposed SSCB.

is because the uncontrolled rectifier, which produces six-pulse wave, is used as the dc power source for the experiment circuit. In fact, in the dc distribution network, the converters are mainly the VSCs. So, the waveform quality will be very good, and a large dc reactor for the function of filtering is not required.

3) *DC Fault Current Limiting and Clearing*: In this case, a dc pole-to-pole fault is set to occur at  $t = 0$  s. Different fault handling strategies are applied, and the corresponding experimental results are shown in Fig. 10. For the strategy “typical SSCB without dc reactor,” the SSCB is set to be tripped 1 ms after the fault. As the experimental results show, the dc current quickly increases from about 10 to about 70 A in 1 ms. When the 40-mH dc reactor is installed directly with the typical SSCB, the fault current is limited significantly (limited at around 40 A in 10 ms after the fault). However, when the SSCB is tripped 10 ms after the fault, the fault clearing time is prolonged drastically (about 20 ms). Differently, when the proposed SSCB is applied, it can also limit the fault current before the tripping signal, and being tripped 10 ms after the fault, the fault current is cleared very quickly (smaller than 2 ms, close to the strategy “typical SSCB without dc reactor”). This is because the Arm<sub>2</sub> conducts instantaneously after tripping the SSCB, to bypass the dc reactor combing with the conducting Arm<sub>4</sub>, as shown in Fig. 10(d). This means that the proposed SSCB can limit the fault current quickly and automatically after the dc fault, to create adequate action time for the protection. After the protection acts to trip the SSCB, it can isolate the fault very quickly, which will benefit the fast recovery of the healthy network and the fast recovery of the fault line insulation characteristic. In addition, according to Fig. 10(b) and (c), the energy absorbed by the arrester during the fault current clearing period of the proposed SSCB is only about 6 J, which is much smaller than that of the condition that the reactor is directly installed (about 117 J). In other words, the capacity of the arrester for the proposed SSCB can be much smaller than that for the strategy “typical SSCB with dc reactor.”

4) *Recovery After the Fault Disappears*: For the nonpermanent fault, the fault line should be reconnected after the fault disappears. Suppose that the time for the fault line to recover

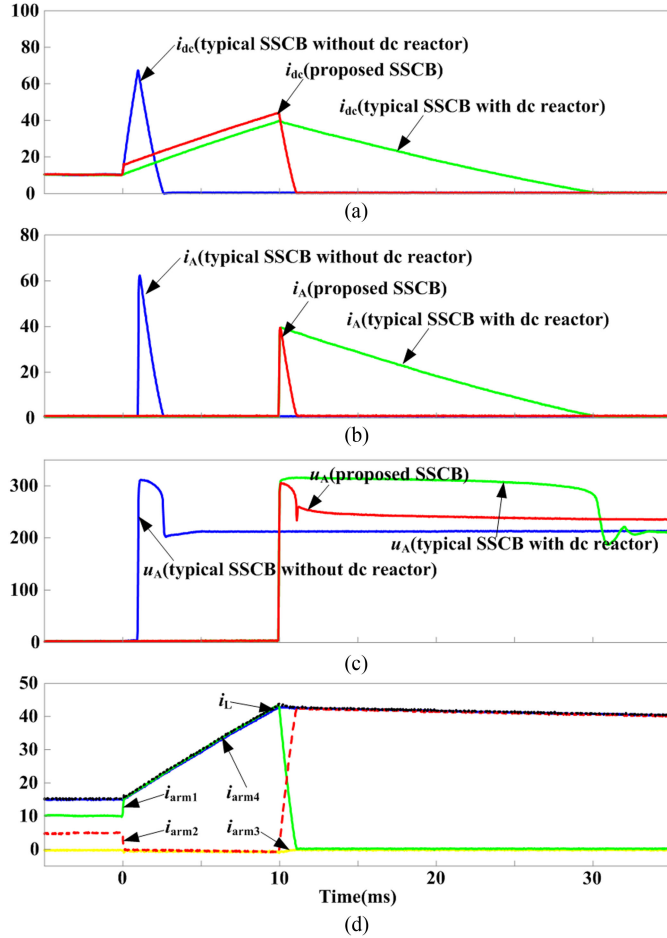


Fig. 10. Experimental results of the dc fault current limiting and clearing with different handling strategies. (a) DC line current (A). (b) Arrester current (A). (c) Arrester voltage (V). (d) Arm currents and the current flowing through the reactor branch (A).

the insulation characteristic is  $t_{rec}$ , and the time to identify the fault property is  $t_{pro}$ , the strategy “typical SSCB with dc reactor” can reclose the SSCB in about  $t_{trip} + 20 \text{ ms} + t_{rec} + t_{pro}$  after the fault (in this case,  $t_{trip}$  is set as 10 ms,  $t_{rec}$  is set as 80 ms and  $t_{pro}$  is set as 1 ms). Considering that about another 15 ms is needed for the dc current to recover to the load current value after the SSCB is reclosed [see Fig. 11(a)], it takes  $t_{trip} + 20 \text{ ms} + t_{rec} + t_{pro} + 15 \text{ ms}$  from the fault moment to the moment the whole system is recovered. When the proposed SSCB is installed, the dc biased current can be recovered to nearby the required value  $I_b$  quickly with the proposed recovery strategy, as shown in Fig. 11(b). Furthermore, as the experimental results show, the recovery of the SSCB itself has slight influence on the recovery of the system. The dc current can recover to the load current in 1 ms. The essential reason is that the clamping voltages of the two arresters respectively in Arm1 and Arm2 of the proposed SSCB are polarity-opposite for the dc line, and thus, the actual voltage exerted on the dc line by the DCCB is very small, as shown in Fig. 11(e). Therefore, with the proposed SSCB, only  $t_{trip} + 2 \text{ ms} + t_{rec} + t_{pro} + 1 \text{ ms}$  is needed from the fault moment to the system completely re-

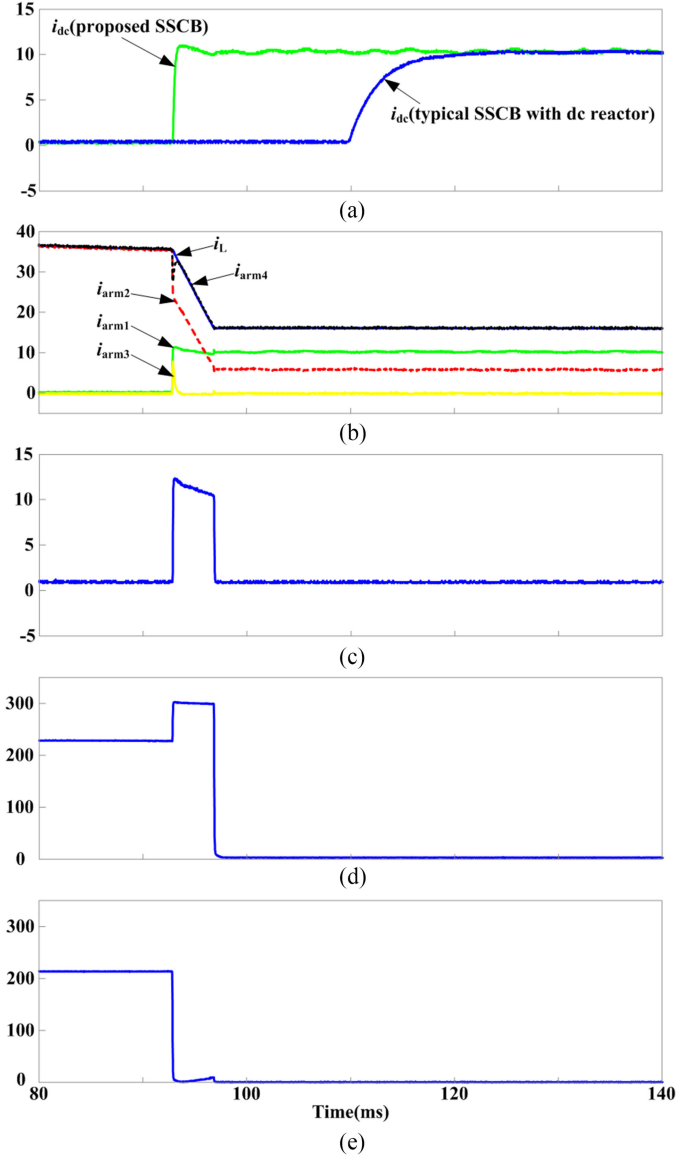


Fig. 11. Experimental results of the recovery after the fault disappears with different handling strategies. (a) DC line current (A). (b) Arm currents and the current flowing through the reactor branch (A). (c) Arrester current (A). (d) Arrester voltage (V). (e) DCCB voltage (V).

covered moment. In total, 32 ms are saved compared with the strategy “typical SSCB with dc reactor.”

## V. SIMULATION CASE STUDY

The working principle of the proposed SSCB has been proved by the experiment test in the scaled-down test circuit. To further verify the advantages of the proposed SSCB for application in the multiterminal dc distribution network, a four-terminal VSC-based dc system model, as shown in Fig. 12, is built on PSCAD/EMTDC, where the frequency-dependent model is used for the dc cables, and the detailed parameters of the simulation model are listed in Table II. In the simulation cases,  $I_{set}$  and  $U_{set}$  are set as  $4I_{dcN}$  and  $M \times U_{dcN}$  respectively, where  $I_{dcN}$  is the rated dc current of each converter station,  $U_{dcN}$  is the

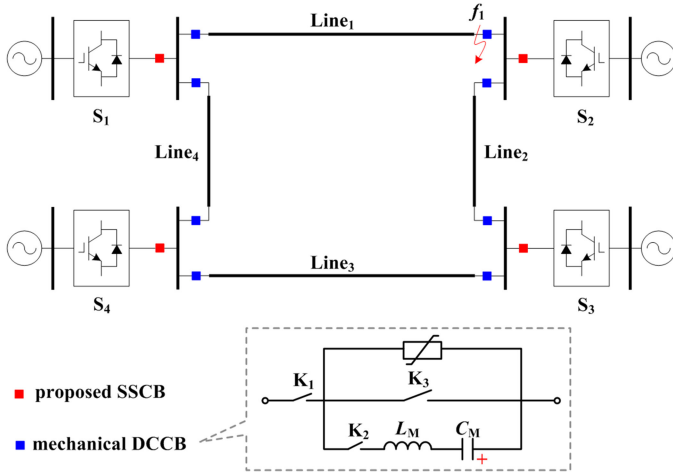


Fig. 12. Topology of the simulation four-terminal VSC-based dc distribution system model.

TABLE II  
PARAMETERS OF THE SIMULATION FOUR-TERMINAL VSC-BASED  
DC DISTRIBUTION SYSTEM

PARAMETER	VALUE
Rated dc voltage(kV)	1.5
Rated ac voltage(kV)	0.75
Modulation ratio $M$	0.816
DC capacitors of $S_1 \sim S_4$ (mF)	10
AC reactors of $S_1 \sim S_4$ (mH)	10
Parameters of the current commutation branch	$L_M$ : 0.01mH; $C_M$ : 0.1mF, 1.5kV
Rated capacity of $S_1 \sim S_4$ (kW)	75, 150, 75, 75
Length of the dc cables(km)	2, 1, 2, 1

rated dc voltage and  $M$  is the modulation ratio of the converter. Therefore, according to (7) and (8), the required dc reactors for  $S_1$ ,  $S_2$ , and  $S_3$  are all 79 mH (each pole, and a reliability factor of 1.1 is introduced), while that for  $S_4$  is 75mH, where  $t_{\text{trip}}$  is set as 15 ms.

### A. Power Flow Shifting

In the experiment tests, it has been proved that the transient response speed will be slowed down when the dc reactor is installed directly. Its further influence on the stability of the system is observed in this case, where the reference value of the active power of  $S_3$  is set to change from 75 to  $-75$  kW at  $t = 10$  s.

As shown in Fig. 13, for the condition that no dc reactors are installed, the dc current can change from about 0.05 to about  $-0.05$  kA quickly, and the dc voltage can also recover to a stable value (about 1.5 kV) quickly after an acceptable fluctuation. However, when the dc reactors are directly installed in the dc system, in this case, two 79 mH reactors are respectively installed at the positive and negative poles of the  $S_3$  output position, an oscillation occurs during the change process of the dc current and voltage. What is worse, the oscillation amplitude

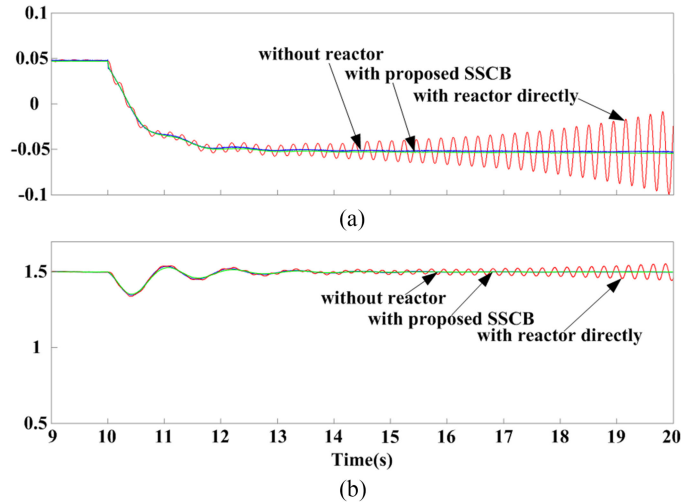


Fig. 13. Simulation results of the power flow shifting. (a) DC current (kA). (b) DC voltage (kV).

increases gradually, finally leading to the system instability. This is one of the main reasons why the large dc reactors are not allowed to be installed in the dc system directly. Differently, when the proposed SSCBs are applied (installed at the output position of each converter station), the transient response characteristic during the power flow shifting is almost the same with the condition that no dc reactors are installed. This means that the proposed SSCB has no negative influence on the transient response characteristic and system stability.

### B. Fault Ride-Through of the Healthy Part of the System

To verify the reliable fault ride-through capability of the healthy part of the system with the hybrid configuration strategy described in Section III, the proposed SSCBs are installed at each converter output position, and the mechanical DCCBs are installed on each dc line terminal in this case. In this paper, the mechanical DCCB based on the active oscillating current commutation technique is modeled in the simulation, and the detailed parameters of the current commutation branch are listed in Table II.

A dc pole-to-pole fault  $f_1$ , shown in Fig. 12, is set to occur at  $t = 10$  s. As shown in Fig. 14(a), the fault line is isolated about 15 ms after the fault (15 ms is for the protection and mechanical DCCBs on Line1). In addition, the dc current and dc voltage of  $S_2$  are observed because it is the nearest converter to  $f_1$ . As shown in Fig. 14(b), during the action period of the protection and mechanical DCCB, the dc current of  $S_2$  is limited below the setting upper limit value ( $4I_{\text{dcN}} = 0.4$  kA), and the dc voltage is also kept above the lower limit value ( $M \times U_{\text{dcN}} = 1.224$  kV). Then, after the fault line is isolated, the dc system voltage, healthy line currents, converter currents, and powers can all recover to the stable values, as shown in Fig. 14(b)–(h). This means that the designed SSCB can limit the fault current effectively, and the healthy network can ride-through the dc fault successfully with the proposed hybrid configuration strategy.

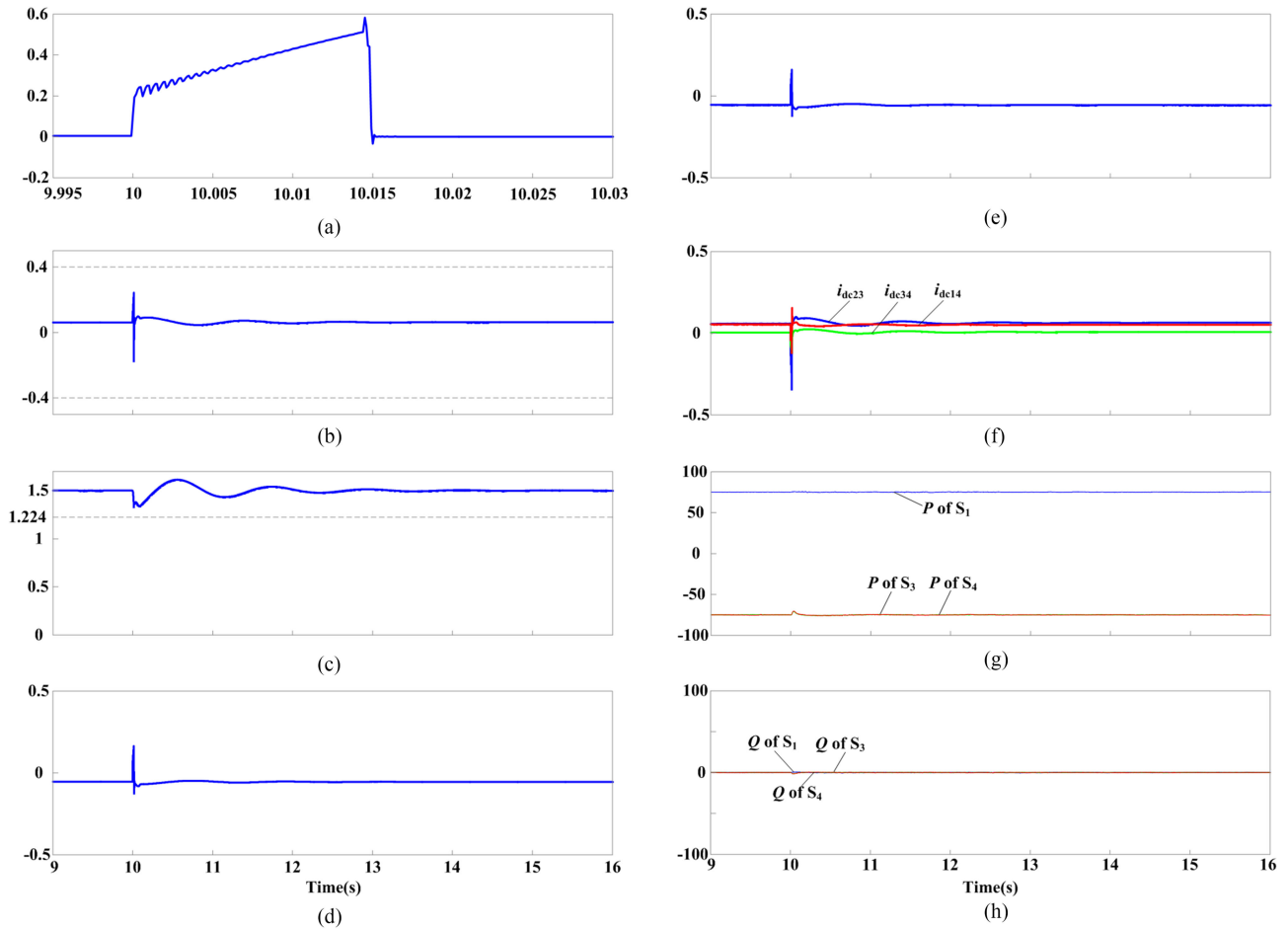


Fig. 14. Simulation results of dc pole-to-pole fault. (a) DC fault line current (kA). (b) DC current of  $S_2$  (kA). (c) DC voltage of  $S_2$  (kV). (d) DC current of  $S_3$  (kA). (e) DC current of  $S_1$  (kA). (f) DC currents of Line<sub>2</sub>–Line<sub>4</sub> (kA). (g)  $P$  of the converters (kW). (h)  $Q$  of the converters (kVar).

## VI. CONCLUSION

Effective fault current limiting methods are beneficial to lower the requirement on the acting speed of the dc fault protection and isolation for LVDC distribution network. This paper proposed a novel SSCB that can limit the dc fault current quickly and automatically before the tripping signal from the protection is received. To reduce the conducting power loss and investment, the hybrid configuration strategy of the proposed SSCB and mechanical DCCB for the multiterminal dc distribution network is proposed as well. The experiment tests and simulation cases verify that, compared with the typical fault current limiting method—by installing dc reactor directly, the proposed method has two appealing advantages: First, during normal operation, the dc reactor in the SSCB is not connected into the dc line, so the transient response speed and stability of the dc system, especially during the power flow shifting, are not deteriorated. Second, after the SSCB is tripped, the reactor in the SSCB is bypassed again from the fault circuit automatically and instantaneously, guaranteeing the fast fault current clearing. Considering that the proposed SSCB is more complex than the typical SSCB, its feasibility in the engineering fields still needs to be verified by a practical application. In addition, for application in HVDC grid, the improved topology should also be researched in the future works.

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