Letters

A New Half-Bridge Impedance Source Inverter With High Voltage Gain

Xiaoquan Zhu, Bo Zhang, *Senior Member, IEEE*, and Dongyuan Qiu, *Member, IEEE*

***Abstract*—In this letter, a new half-bridge impedance source inverter (HBISI) with high voltage conversion ratio is developed. Compared with other well-known existed HBISIs (HB-qZSIs/HB-qSBIs), the proposed HBI can increase the voltage boost factor significantly. Only a very small shoot-through (ST) duty cycle (D_{sh}) is required to produce a higher voltage gain. The upper and lower switches of the inverter bridge can be turned ON simultaneously, and no dead time is needed for the control scheme. So the reliability of the inverter system can be improved. The produced square-waveform output voltage not only has positive and negative voltage levels like the traditional HB-ZSI but also has a zero voltage level, and the *n*th harmonic of the output voltage can be eliminated by choosing $D_{\mathrm{sh}} = 1/n$, which implies that it would be applicable for the electrochemical and electroplating applications. The topological configuration, operating principle, power loss analysis, and performance comparison with other high-boost HBISIs are presented. Finally, both simulations and the experimental results are presented to validate the effectiveness of the proposed topology.**

***Index Terms*—Half-bridge inverter (HBI), high voltage gain, impedance network, Z-source inverter (ZSI).**

I. Introduction

THE two active power switches in the conventional half-bridge inverters (HBIs) are connected in series, which may cause mis-gating on at the same time due to the electromagnetic interference (EMI). Then the inverter bridge is short-circuit and operates in the shoot-through (ST) state, resulting in a high current flow through the inverter bridge and breaking down of the power switches. Moreover, the peak ac output voltage of the conventional HBIs is limited to lower than the dc input voltage, which is undesirable for many practical applications [1]. To overcome the ST problem and improve the limited output voltage gain, a novel and efficient design of the impedance source network, known as Z-network, was first proposed in [2]. The original Z-network is composed of one diode, two inductors, and two capacitors. By cascading the Z-network between the dc

Manuscript received May 14, 2018; revised June 23, 2018 and July 28, 2018; accepted August 13, 2018. Date of publication August 23, 2018; date of current version February 20, 2019. This work was supported in part by the Team Program of Natural Science Foundation of Guangdong Province, China, under Grant 2017B030312001 and in part by the Key Program of National Natural Science Foundation of China under Grant 51437005. *(Corresponding author: Bo Zhang.)*

The authors are with the School of Electric Power, South China University of Technology, Guangzhou 510640, China (e-mail:

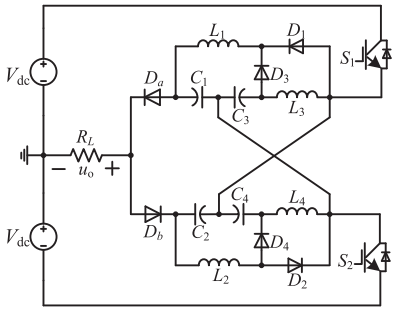

Fig. 1. Topological configuration of the proposed HBISI.

voltage gain, that is, $1/(1-2D)$. Similarly, by combining two conventional quasi-switched-boost network with the traditional HBI topology, two kinds of half-bridge quasi-SBIs (HB-qSBIs) were proposed in [17] and [18], respectively. And both of them have the same voltage boost factor $(1-D)/(1-3D)$, which is higher than the HB-(q)ZSIs. In [19], another two new half-bridge and full-bridge SBIs were presented, which can provide continuous input current, use lower number of passive components, and have a much higher voltage boost factor $1/(1-3D)$ than those of the HB-(q)ZSIs and HB-(q)SBIs mentioned earlier. In addition, these half-bridge and full-bridge (q)ZSIs and (q)SBIs are also applicable for the photovoltaic applications and the galvanically isolated dc/dc power conversion fields [20].

In this letter, a new half-bridge impedance source inverter (HBISI) is proposed, which has a much higher voltage boost factor than those of the existing HB-(q)ZSIs and HB-(q)SBIs. The proposed method can not only output positive and negative voltages like the traditional HB-ZSI but also produces a zero voltage level at the output. By controlling the switching frequency and the shoot-through duty ratio for this HBI, the amplitude and frequency of the output voltage can be low or high. Then, the current densities and directions can be regulated according to the electroplating technology; the metal ions in the electrolyte can cover the negative electrode surface evenly and smoothly. Therefore, the proposed HBI is suitable for the electroplating and electrochemical power supply applications [11].

In the following sections, the steady-state operating principle of the proposed HBI is analyzed. Then, the comprehensive performance comparison between the proposed and the conventional HBISIs is discussed. Finally, both simulation and experimental results are conducted to verify the theoretical analysis.

II. Operating Principle Analysis of the Proposed HBI

Fig. 1 shows the topological configuration of the proposed HBI, which has two improved quasi-Z-source networks. The upper qZS network consists of inductors L_1 and L_3, capacitors C_1 and C_3, and diodes D_1, D_3, and D_a. The lower qZS network consists of inductors L_2 and L_4, capacitors C_2 and C_4, and diodes D_2, D_4, and D_b. Active power switches S_1 and S_2, output load, and two identical dc input sources with the same amplitude of $V_{\rm dc}$ are the other components of the proposed half-bridge inverter.

For the sake of analysis, all the components used in the proposed circuit are considered to be lossless and ideal. In order to produce the symmetrical square-waveform voltage at the output, the load type of the proposed inverter cannot be inductive or capacitive. Thus, in the following steady-state analysis, the output load is assumed to be resistive. In addition, due to the symmetry of the proposed impedance network, all the inductors and capacitors are assumed to have the same values, i.e., $L_1 = L_2 = L_3 = L_4, C_1 = C_2 = C_3 = C_4$.

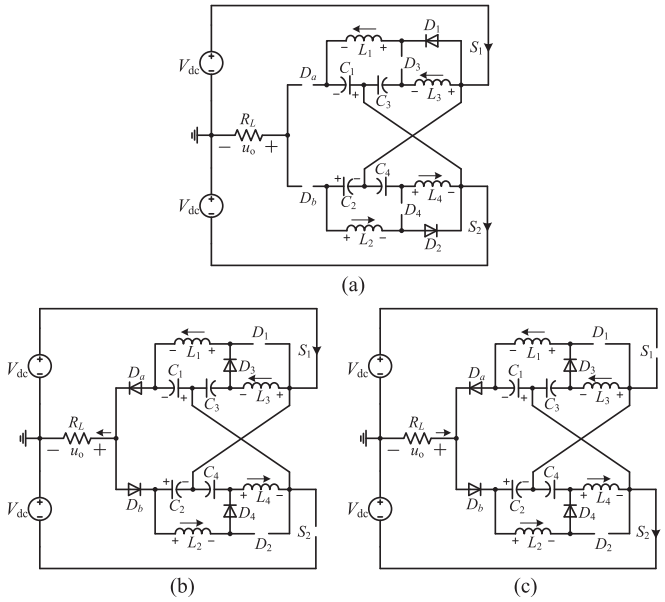

Fig. 2. Equivalent circuit schematic diagrams of the proposed HBI in different operating modes. (a) Operating mode 1 and operating mode 3. (b) Operating mode 2. (c) Operating mode 4.

A. Operating Modes Analysis of the Proposed HBI

The operating modes of the proposed HBI during a switching period are determined by the ON and OFF states of diodes $(D_1$–$D_4,\ D_a,\ D_b)$ and switches $(S_1,\ S_2)$. Here, $D_{\rm sh}$ is the ST duty ratio of the proposed inverter, which is defined as the ratio of the ST time interval $D_{\rm sh}T_{\rm s}$ to the switching period $T_{\rm s}$.

1) Operating Mode 1 ($0 < t < 0.5D_{sh}T_s$): The equivalent circuit of this operating mode is shown in Fig. 2(a). Both of the active switches S_1 and S_2 are turned ON at the same time. Diodes $D_3,\ D_4,\ D_a$, and D_b are OFF due to the reverse parallel connection with capacitors. Inductors $L_1,\ L_2,\ L_3,\ L_4$ are charged by capacitors $C_1,\ C_2,\ C_3,\ C_4$, respectively. The output voltage is zero due to the output load is in the open-circuit situation. Based on the Kirchhoff's voltage law for the circuit in Fig. 2(a), we have

$$\begin{cases} u_{L1} = V_{C1} + 2V_{\rm dc} & u_{L2} = V_{C2} + 2V_{\rm dc} \\ u_{L3} = V_{C3} + 2V_{\rm dc} & u_{L4} = V_{C4} + 2V_{\rm dc} \\ V_{Da} = -V_{\rm dc} - V_{C2} & V_{D3} = -u_{L3} \\ V_{Db} = -V_{\rm dc} - V_{C1} & V_{D4} = -u_{L4} \\ i_{C1} = -i_{L1}\, i_{C2} = -i_{L2} & i_{C3} = -i_{L3}\, i_{C4} = -i_{L4}. \end{cases} \tag{1}$$

2) Operating Mode 2 ($0.5D_{sh}T_s < t < 0.5T_s$): During this state, as shown in Fig. 2(b), switch S_1 is ON, S_2 is OFF, diodes D_3, D_4, D_a, and D_b are turned ON, while D_1 and D_2 are reverse blocking. Then the inductors discharge the stored energy

and transfer it to the capacitors. Here, C_1 is charged by L_2 and L_4, C_2 is charged by L_1 and L_3; C_3 is charged by L_1, L_2, and L_4; and C_4 is charged by L_1, L_2, and L_3. Due to the open circuit of the lower dc input source, only the upper dc power supply is involved in the whole circuit operation. Thus, the positive output voltage can be produced at the load resistance, that is, $V_o = V_{\rm dc} + V_{C1}$. Therefore

$$\begin{cases} u_{L1} = V_{C1} - V_{C3} \quad u_{L3} = -V_{C1} - V_{C2} + V_{C3} \\ V_{D1} = -u_{L3} \\ u_{L2} = V_{C2} - V_{C4} \quad u_{L4} = -V_{C1} - V_{C2} + V_{C4} \\ V_{D2} = -u_{L4} \\ i_{C1} = i_{L3} + i_{L4} - i_{L1} - i_o \quad i_{C3} = i_{L1} - i_{L3} \\ i_{C2} = i_{L3} + i_{L4} - i_{L2} \qquad\quad i_{C4} = i_{L2} - i_{L4}. \end{cases} \tag{2}$$

3) Operating Mode 3 ($0.5T_s < t < 0.5(1 + D_{sh})T_s$): In this state, the equivalent circuit is same as that of operating mode 1. Inductors (L_1, L_2, L_3, L_4) are charged by capacitors (C_1, C_2, C_3, C_4), respectively. And they both have the same voltage and current relationships of passive and active components.

4) Operating Mode 4 ($0.5(1 + D_{sh})T_s < t < T_s$): The equivalent circuit of this operating state is shown in Fig. 2(c). Switch S_1 is turned OFF, while S_2 is turned ON. Diodes D_a, D_b, D_3, and D_4 are forward biased, while D_1 and D_2 are reverse blocking. The inductors discharge and transfer the stored energy to capacitors. Therefore, inductor currents decrease from their maximum value to the minimum value, respectively. And the upper dc input source is shut down due to the open circuit. The negative output voltage will be produced by the lower dc power supply, which can be expressed as $V_{\rm o} = -V_{\rm dc} - V_{C2}$. By applying KVL, one can obtain

$$\begin{cases} u_{L1} = V_{C1} - V_{C3} & u_{L3} = -V_{C1} - V_{C2} + V_{C3} \\ u_{L2} = V_{C2} - V_{C4} & u_{L4} = -V_{C1} - V_{C2} + V_{C4} \\ i_{C1} = i_{L3} + i_{L4} - i_{L1} & i_{C3} = i_{L1} - i_{L3} \\ i_{C2} = i_{L3} + i_{L4} - i_{L2} + i_o & i_{C4} = i_{L2} - i_{L4}. \end{cases} \tag{3}$$

B. Derivation of Capacitor Voltages and Voltage Gain

According to the volt–second balance principle of inductors, the steady-state average inductor voltage over one switching period is zero. Thus, based on (1)–(3), the steady-state capacitor voltages can be derived as

$$\begin{aligned} V_{C1} = V_{C2} &= \frac{2D_{\rm sh}\left(2 - D_{\rm sh}\right)}{1 - 4D_{\rm sh} + 2D_{\rm sh}^2} V_{\rm dc} \\ V_{C3} = V_{C4} &= \frac{2D_{\rm sh}\left(3 - 2D_{\rm sh}\right)}{1 - 4D_{\rm sh} + 2D_{\rm sh}^2} V_{\rm dc}. \end{aligned} \tag{4}$$

Therefore, the output voltage of the proposed HBI is

$$\begin{aligned} V_{\rm o\_postive} = -V_{\rm o\_negative} &= V_{\rm dc} + V_{C1} \\ &= \frac{1}{1 - 4D_{\rm sh} + 2D_{\rm sh}^2} V_{\rm dc} = BV_{\rm dc} \end{aligned} \tag{5}$$

where B is the output voltage gain of the proposed inverter. Then, the corresponding diode voltage stress and active switching voltage stress can be obtained as

$$\begin{aligned} V_{D1} = V_{D2} &= \frac{2D_{\rm sh}}{1 - 4D_{\rm sh} + 2D_{\rm sh}^2} V_{\rm dc} \\ V_{D3} = V_{D4} &= \frac{2\left(1 - D_{\rm sh}\right)}{1 - 4D_{\rm sh} + 2D_{\rm sh}^2} V_{\rm dc} \\ V_{Da} = V_{Db} &= \frac{1}{1 - 4D_{\rm sh} + 2D_{\rm sh}^2} V_{\rm dc} \end{aligned} \tag{6}$$

$$V_{S1} = V_{S2} = \frac{2}{1 - 4D_{\rm sh} + 2D_{\rm sh}^2} V_{\rm dc}. \tag{7}$$

C. Harmonic Analysis of the Output Voltage

Considering the symmetrical output voltage waveform of the proposed HBI, the corresponding Fourier series of the output voltage can be expressed as

$$v_o\left(t\right) = \sum_{n=1,3,5\ldots}^{\infty} V_n \sin\left(n\omega t\right). \tag{8}$$

Due to the characteristic of half-wave symmetry of the output voltage waveform, V_n in (8) can be calculated by $V_n = [4v_{o,\max}\cos\left(n\pi D_{\rm sh}/2\right)n/\pi]$, where $v_{o,\max} = BV_{\rm dc} = V_{\rm dc}/(1 - 4D + 2D^2)$. Then, the harmonic amplitude V_n can be obtained as

$$V_n = \frac{4\cos\left(0.5n\pi D_{\rm sh}\right)}{n\pi\left(1 - 4D + 2D^2\right)} V_{\rm dc}. \tag{9}$$

It can be found from (9) that the harmonic amplitude V_n can be controlled by the ST duty cycle $D_{\rm sh}$. For example, the fourth and fifth harmonic amplitude will be zero ($V_4 = V_5 = 0$) when $D_{\rm sh}$ equals 0.25 and 0.2, respectively. Therefore, the *n*th harmonic will be eliminated by choosing $D_{\rm sh} = 1/n$. Then, based on [19], the total harmonic distortion (THD) for the proposed inverter can be calculated by

$$\begin{aligned} {\rm THD} &= \frac{\sqrt{2B^2V_{\rm dc}^2\left(1 - D_{\rm sh}\right)\pi - \pi V_1^2}]}{\sqrt{\pi} V_1} \\ &= \frac{\sqrt{2\left(1 - D_{\rm sh}\right)\pi^2 - 16\cos^2\left(0.5\pi D_{\rm sh}\right)}}{4\cos\left(0.5\pi D_{\rm sh}\right)} \end{aligned} \tag{10}$$

where V_1 is the amplitude of the fundamental harmonic, $V_1 = 4BV_{\rm dc}\cos\left(0.5\pi D_{\rm sh}\right)/\pi$.

D. Passive Elements' Design Guideline

In order to make the parameter design of inductance and capacitance values more appropriate, it is necessary to calculate the inductor current ripple and capacitor voltage ripple in advance. Based on (2), (4), and the equation of $u_L = L(di_L/dt)$, the inductor current ripples can be expressed as

$$\begin{aligned} \left|\Delta i_{L1,2}\right| &= \frac{D_{\rm sh}\left(1 - D_{\rm sh}\right)^2 T_s V_{\rm dc}}{L_1\left(1 - 4D_{\rm sh} + 2D_{\rm sh}^2\right)} \\ \left|\Delta i_{L3,4}\right| &= \frac{D_{\rm sh}\left(1 - D_{\rm sh}\right) T_s V_{\rm dc}}{L_3\left(1 - 4D_{\rm sh} + 2D_{\rm sh}^2\right)}. \end{aligned} \tag{11}$$

Similarly, based on the Kirchhoff's current law (KCL), (2), and equation $i_C = C(du_C/dt)$, the capacitor voltage ripples can be obtained as follows:

$$|\Delta u_{C1,2}| = \frac{(1-D_{\rm sh})\,T_s}{2C_1}\,(2I_{L3}-I_{L1})$$
$$|\Delta u_{C3,4}| = \frac{(1-D_{\rm sh})\,T_s}{2C_3}\,(I_{L1}-I_{L3})\,. \tag{12}$$

According to the ampere–second balance property of capacitors, the average capacitor current during a switching period is zero. Thus, based on (1)–(3), the average inductor current can be derived as

$$I_{L1,2} = \frac{(1-D_{\rm sh})\,V_{\rm dc}}{2(1-4D_{\rm sh}+2D_{\rm sh}^2)^2 R_L}$$
$$I_{L3,4} = \frac{(1-D_{\rm sh})^2 V_{\rm dc}}{2(1-4D_{\rm sh}+2D_{\rm sh}^2)^2 R_L}. \tag{13}$$

Substituting the current and voltage expressions of $\Delta i_L = x_L\%I_L$ and $\Delta u_C = x_C\%V_C$, where $x_L\%$ and $x_C\%$ is the permitted fluctuation range of inductor current and capacitor voltage, into the (11) and (12). Then, the nominal value of inductances and capacitances can be expressed as

$$\begin{cases} L_1 = L_2 = \frac{2D_{\rm sh}(1-D_{\rm sh})\left(1-4D_{\rm sh}+2D_{\rm sh}^2\right)R_L}{x_L\%\cdot f_s} \\ L_3 = L_4 = \frac{2D_{\rm sh}\left(1-4D_{\rm sh}+2D_{\rm sh}^2\right)R_L}{x_L\%\cdot(1-D_{\rm sh})f_s} \end{cases} \tag{14}$$

$$\begin{cases} C_1 = C_2 = \frac{(1-D_{\rm sh})^2(1-2D_{\rm sh})T_s}{8D_{\rm sh}(2-D_{\rm sh})\left(1-4D_{\rm sh}+2D_{\rm sh}^2\right)x_L\%R_L} \\ C_3 = C_4 = \frac{(1-D_{\rm sh})^2 T_s}{8(3-2D_{\rm sh})\left(1-4D_{\rm sh}+2D_{\rm sh}^2\right)x_L\%R_L}. \end{cases} \tag{15}$$

In order to produce a symmetric output voltage waveform for the proposed converter in the whole switching period, the current flow through diode D_a at the end of time interval $0.5(1+D_{\rm sh})T_s \le t \le T_s$ and the current flow through D_b at the end of $0.5D_{\rm sh}T_s \le t \le 0.5T_s$ should be greater than or equal to zero. Then

$$i_{Da(t=Ts)} = i_{L3} + i_{L4} + i_o \ge 0$$
$$i_{Db(t=0.5Ts)} = i_{L3} + i_{L4} - i_o \ge 0. \tag{16}$$

Substituting (13) and the load current $I_o = BV_{\rm dc}/R_L$ into (16), the critical inductance can be calculated as

$$L_3 = L_4 \ge \frac{(1-D)\left(1-4D+2D^2\right)R_L}{(2-D)\,f_s}. \tag{17}$$

Due to the symmetry of the impedance network, $L_1 = L_2 = L_3 = L_4$ is assumed in the proposed half-bridge converter. Based on (17), the relationship between the normalized critical inductance and the ST duty cycle $D_{\rm sh}$ is plotted and shown in Fig. 3.

III. Performance Comparison With Other Conventional High-Boost HBISIs

This section presents the performance comparison between the proposed HBI and the other conventional high-boost HBIs

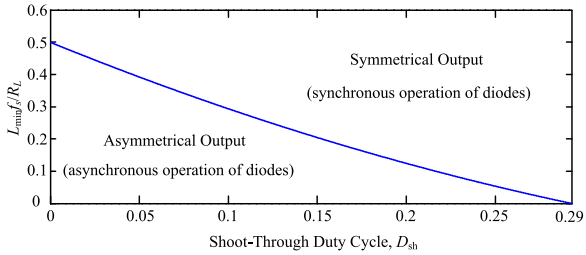

Fig. 3. Relationship between the normalized inductance $L_{\rm min}$ and the ST duty ratio $D_{\rm sh}$.

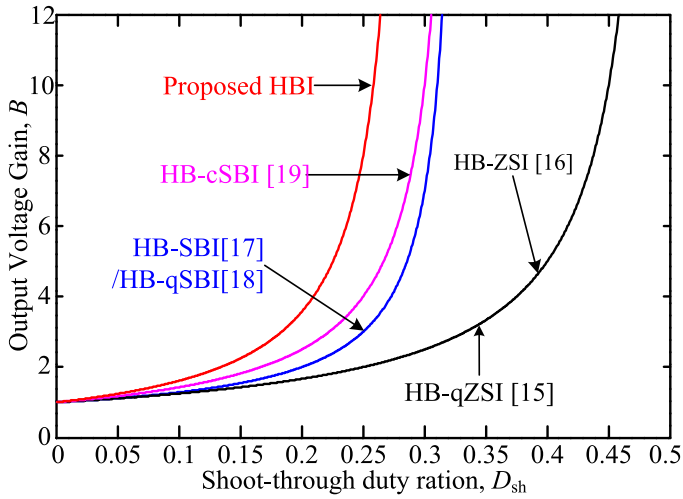

Fig. 4. Output voltage gain B comparison for these high-boost HBISIs.

[15]–[19]. The comparisons are mainly focused on the boost abilities, power losses, inverters' efficiency, volume size, and voltage stresses of passive and active components.

A. Comparison of Boost Abilities

The expressions of the output voltage gains of these high-boost HBIs are tabulated in Table I. The corresponding relationship between the output voltage gain B and the ST duty ratio $D_{\rm sh}$ is plotted and compared in Fig. 4. From this figure, it can be seen that the proposed HBI has the strongest boost ability than those of the other five topologies through the whole ST duty ratio range.

B. Voltage Stresses Comparison of Passive and Active Components

The voltage stresses of passive and active devices for these six inverters have been tabulated in Table I and compared in Fig. 5. From Fig. 5(a), although the capacitor voltage stresses (V_{C3} and V_{C4}) of the proposed inverter is higher when B is larger than 3, the capacitor voltage stresses of $V_{C1}(=V_{C2})$ is same as the HB-ZSI [16] and HB-qSBI [18] and lower than the HB-SBI [17], [19]. As shown in Fig. 5(b), although the diode voltage stresses of $V_{D3}(=V_{D4})$ is higher than those of the other HBIs, the diode voltage stress of $V_{D1}(=V_{D2})$ is much lower than them. In addition, the diodes' total peak switching device power (SDP) [1] has been calculated and compared in Fig. 5(c).

TABLE I
PERFORMANCE COMPARISON BETWEEN THE PROPOSED HBI AND THE OTHER CONVENTIONAL HBIS

	HB-ZSI [16]	HB-SBI[17]	HB-qSBI[18]	HB-cSBI[19]	HB-qZSI [15]	Proposed HBI
Output Voltage Gain (B)	$\frac{1}{1-2D}$	$\frac{1-D}{1-3D}$	$\frac{1-D}{1-3D}$	$\frac{1}{1-3D}$	$\frac{1}{1-2D}$	$\frac{1}{1-4D+2D^2}$
Inductor	2	2	2	1	4	4
Capacitor	2	2	2	2	4	4
Diode	2	4	4	4	2	6
Switch	2	4	4	4	2	2
Capacitor Voltage Stresses (V_C/V_{dc})	$2DB$ ($V_{C1}=V_{C2}$)	B ($V_{Cp}=V_{Cn}$)	$2DB/(1\text{-}D)$ ($V_{Cp}=V_{Cn}$)	B ($V_{Cp}=V_{Cn}$)	DB ($V_{C1p}=V_{C1n}=V_{C2p}=V_{C2n}$)	$2D(2\text{-}D)B$ ($V_{C1}=V_{C2}$) $2D(3\text{-}2D)B$ ($V_{C3}=V_{C4}$)
Diode Voltage Stresses (V_D/V_{dc})	B ($V_{Da}=V_{Db}$)	B ($V_{D1}=V_{D2}$) $2DB/(1\text{-}D)$ ($V_{Dp}=V_{Dn}$)	B ($V_{Dp}=V_{Dn}$) $2DB/(1\text{-}D)$ ($V_{D1}=V_{D2}$)	B ($V_{D1}=V_{D2}=V_{Dp}=V_{Dn}$)	B ($V_{Dp}=V_{Dn}$)	B ($V_{Da}=V_{Db}$) $2DB$ ($V_{D1}=V_{D2}$) $2(1\text{–}D)B$ ($V_{D3}=V_{D4}$)
Voltage Stress of switches (V_S/V_{dc})	$2B$ ($V_{S1}=V_{S2}$)	$2B$ ($V_{S1}=V_{S2}$) $2DB/(1\text{-}D)$ ($V_{Sp}=V_{Sn}$)	$2B$ ($V_{S1}=V_{S2}$) $2DB/(1\text{-}D)$ ($V_{Sp}=V_{Sn}$)	B ($V_{Sp}=V_{Sn}$) $2B$ ($V_{S1}=V_{S2}$)	$2B$ ($V_{S1}=V_{S2}$)	$2B$ ($V_{S1}=V_{S2}$)

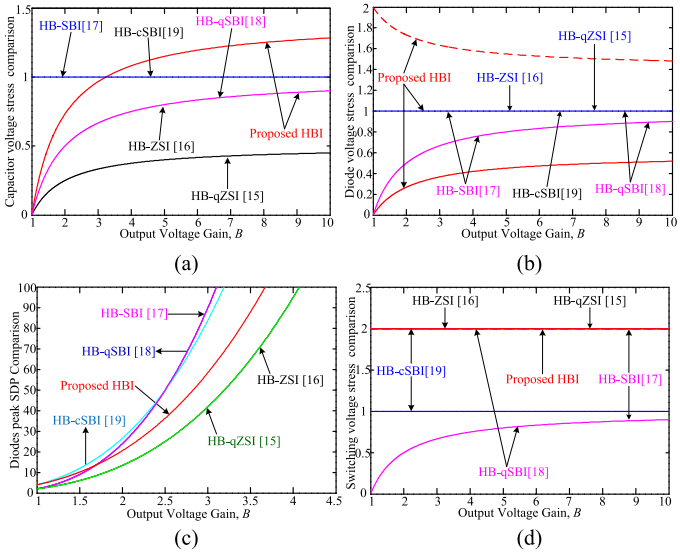

Fig. 5. Voltage stress comparison between the proposed HBI and the other conventional HBIs. (a) Capacitor voltage stress comparison. (b) Diode voltage stress comparison. (c) Diodes' total peak SDP comparison. (d) Active switching voltage stress comparison.

It can be seen that the total diodes' peak SDP of the proposed HBI is only higher than the HB-qZSI [15] and the HB-ZSI [16] but lower than that of the HB-SBI [17], HB-qSBI [18], and the HB-cSBI [19]. As shown in Fig. 5(d), the total active MOSFETs' voltage stresses of the proposed HBI is the same as that of the HB-ZSI and HB-qZSI but lower than the HB-(q)SBIs due to two less power switches used in the proposed topology.

C. Volume Size Comparison of Passive Components

Generally, the volume of a converter is determined by the size of its passive components. Since the size and weight of inductors and capacitors are directly proportional to their numbers and the amount of energy they stored in the converter, so the total volume of inductors is proportional to [$L \times {I_{\rm L}}^2 \times$ (inductors' number)] and the total volume of capacitors is proportional to [$C \times {V_{\rm C}}^2 \times$ (capacitors' number)]. Then, for the proposed HBI, the total inductors' volume and capacitors' volume can be expressed as

$$L_{\rm total} = \frac{4D(1-D)^2 R_L + 4DR_L}{x_L\%\,(1-D)\,Bf_s} \cdot \left[\frac{(1-D)\,B^2 V_{\rm dc}}{2R_L}\right]^2 = \frac{2D(1-D)^3 B^3 V_{\rm dc}^2}{x_L\% f_s R_L} \tag{18}$$

$$C_{\rm total} = \frac{2(1-D)^2\,(1-2D)\,BV_{C_1}^2}{8D\,(2-D)\,x_C\%\,f_s R_L} + \frac{2(1-D)^2 BV_{C_3}^2}{8\,(3-2D)\,x_C\%\,f_s R_L} = \frac{(1-D)^2\left(5-7D+2D^2\right)B^3 V_{\rm dc}^2}{x_C\% f_s R_L}. \tag{19}$$

Therefore, based on (18) and (19), by choosing the same parameters of $V_{\rm dc} = 48\,{\rm V}$, $f_s = 10\,{\rm kHz}$, $R_L = 50\,\Omega$ and the permitted fluctuation range of the inductor current and capacitor voltage $x_L\% = 40\%$ and $x_C\% = 1\%$ for these six high-boost HBIs, the relationship between the total inductors'/capacitors' volume and the output voltage gain B has been plotted and shown in Fig. 6.

From Fig. 6(a), it can be seen that the total inductors' volume of the proposed HBI is only higher than the HB-qZSI [15] and the HB-ZSI [16] but lower than that of the HB-SBI [17], HB-cSBI [19], and HB-qSBI [18]. Meanwhile, it can be observed from Fig. 6(b) the total capacitors' volume of the proposed HBI is only higher than the HB-qZSI [15] and HB-ZSI [16] but much lower than those of the HB-cSBI [19], HB-qSBI [18], and HB-SBI [17].

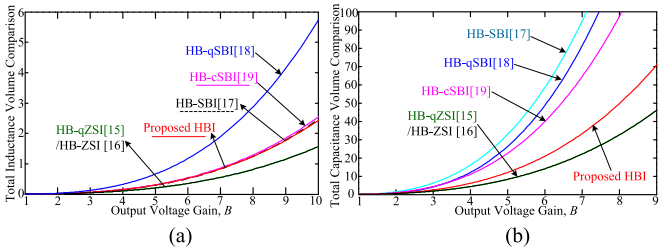

Fig. 6. Volume size comparison. (a) Total inductors' volume comparison. (b) Total capacitors' volume comparison.

D. Power Loss Analysis and Efficiency Comparison

In order to calculate the power losses of passive and active components for these high boost HBIs. Inductors and capacitors are represented by the ideal passive elements with their parasitic resistances r_L and r_C, respectively. MOSFETs are considered as the ideal semiconductor switches in series with the equivalent drain-to-source resistance $r_{\rm DS}$. Diodes are represented by the ideal diodes in series with the forward voltage drop V_F and the parasitic resistance r_D. Therefore, the inductor power loss of the proposed inverter can be calculated by

$$P_{rL} = 2I_{L1}^2 r_L + 2I_{L3}^2 r_L = 2\left(2 - 2D + D^2\right) I_{L1}^2 r_L. \quad (20)$$

The capacitor power loss of the proposed inverter can be expressed as

$$\begin{aligned} P_{rC} &= 2I_{C_{1-\rm RMS}}^2 r_C + 2I_{C_{3-\rm RMS}}^2 r_C \\ &= \left[4D - 2D^2 + (1-D)(1-2D)^2\right] I_{L1}^2 r_C \\ &\quad + (1-D)\, r_C \left[(1-2D)\, I_{L1} - \frac{BV_{\rm dc}}{R_L}\right]^2. \end{aligned} \quad (21)$$

The total diode power loss of the proposed HBI can be calculated by

$$\begin{aligned} P_{D-\rm loss} &= P_{V_F} + P_{rD} \\ &= V_F \left[\left(6 - 8D + 4D^2\right) I_{L1} - \frac{(1-D)\, BV_{\rm dc}}{R_L}\right] \\ &\quad + \left[2 + 4(1-D)^3\right] I_{L1}^2 r_D \\ &\quad + (1-D)\, r_D \left[2(1-D)\, I_{L1} - \frac{BV_{\rm dc}}{R_L}\right]^2. \end{aligned} \quad (22)$$

The MOSFET power loss can be classified into switching power loss during ON and OFF switching states and the ohmic conduction power loss. Then, the total MOSFET loss of the proposed HBI can be derived as

$$\begin{aligned} P_{\rm MOSFET} &= \left[1 + 2D(1-D)(2-D)^2 B^2\right] \left(\frac{BV_{\rm dc}}{R_L}\right)^2 (1-D)\, r_{\rm DS} \\ &\quad + 4(2-D)\, BV_{\rm dc}\left(t_{\rm on} + t_{\rm off}\right) I_{L1} f_s \end{aligned} \quad (23)$$

where $t_{\rm on}$ and $t_{\rm off}$ are the turn-ON and turn-OFF delay times of the power switches and f_s is the switching frequency.

Similarly, the power losses of other conventional high-boost HBIs can be calculated by using the same method. Based on (20)–(23), and the loss-related parameters in Table II. The power loss comparison of passive and active components for these six half-bridge inverters are shown in Fig. 7.

TABLE II
PARAMETERS USED FOR POWER LOSS CALCULATION

Diode	MOSFET	ESR of inductors	ESR of capacitors
RURG3060CC (600V,30A,$V_{F(\max)}$=1.3V)	FCH040N65S3 (650V,65A,r_{DS}=35.4mΩ)	0.22Ω (core:KS300125A142nH/N^2)	120mΩ

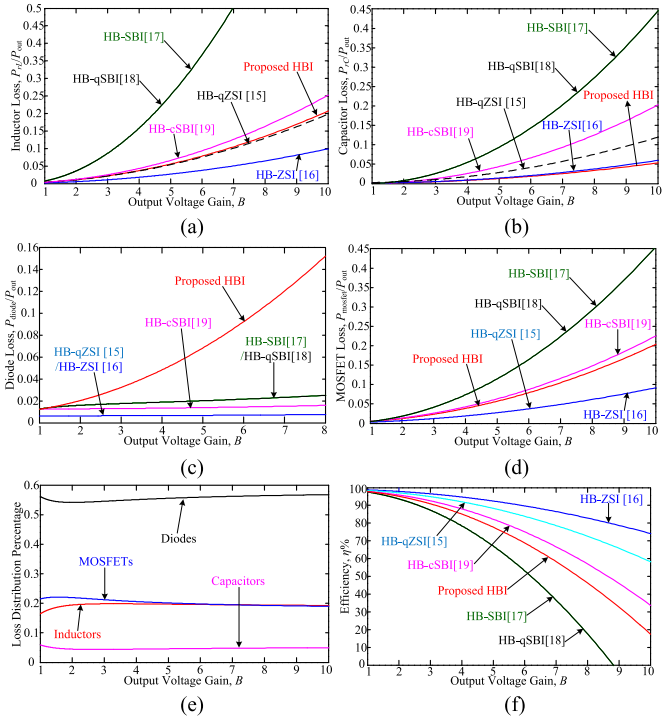

Fig. 7. Power loss and efficiency comparison. (a) Inductor loss comparison. (b) Capacitor loss comparison. (c) Diode loss comparison. (d) MOSFET loss comparison. (e) Loss distribution percentage of the proposed topology. (f) Efficiency comparison for these six HBIs.

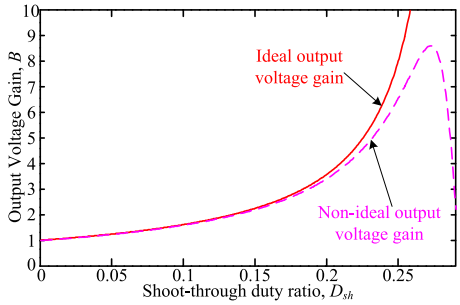

Fig. 8. Nonideal voltage gain B' versus the ST duty ratio $D_{\rm sh}$.

From Fig. 7(a), it can be found that the inductor power loss of the proposed inverter is slightly higher than the HB-qZSI [15] and HB-ZSI [16] but lower than that of the HB-cSBI [19], HB-qSBI [18], and HB-SBI [17]. The capacitor power loss comparison is shown in Fig. 7(b). It can be seen from this figure that the proposed HBI has the lowest capacitor loss than those of the other five conventional topologies [15]–[19]. As shown in Fig. 7(c), for obtaining the same output voltage gain B, the

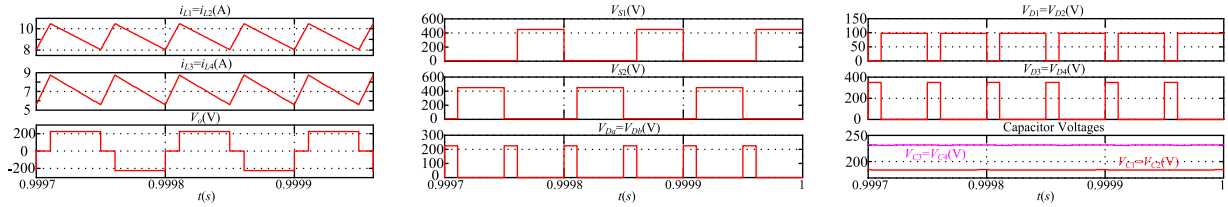

Fig. 9. Simulation results of the proposed half-bridge inverter when $V_{\rm dc} = 48$ V, $D_{\rm sh} = 0.22$. From top to bottom, (a) Inductor currents i_L and output voltage V_o, (b) Voltage stresses of switches S_1, S_2 and diodes D_a and D_b, (c) Diode voltage stress $V_{D1} \sim V_{D4}$, and capacitor voltage stress $V_{C1} \sim V_{C4}$.

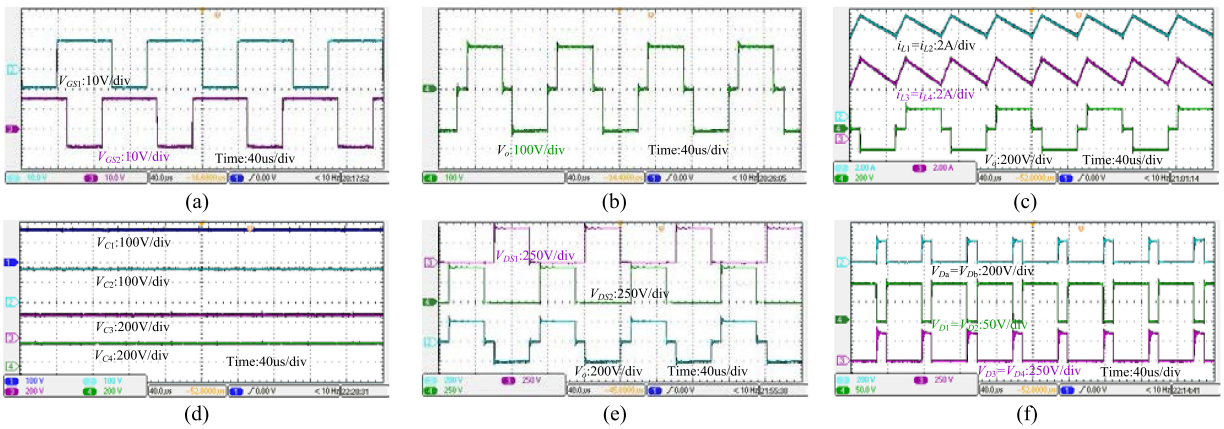

Fig. 10. Experimental results of the proposed half-bridge inverter when $V_{\rm dc} = 48$ V, $D_{\rm sh} = 0.22$. From top to bottom, (a) Gate drive signals G_{S1} and G_{S2}, (b) output voltage V_o, (c) Inductor currents i_L and the output voltage V_o, (d) Capacitor voltages $V_{C1} \sim V_{C4}$, (e) Active switching voltage stress of switches S_1, S_2 and the output voltage V_o, (f) Diode voltage stress V_{Da}, V_{Db} and $V_{D1} \sim V_{D4}$.

proposed inverter has the highest diode power loss due to a little bit more number of diodes used in the power circuit. The MOSFET power loss of the proposed HBI, which is shown in Fig. 7(d), is higher than the HB-qZSI [15] and HB-ZSI [16] but lower than that of the HB-SBI [17], HB-qSBI [18], and HB-cSBI [19].

Based on the earlier power loss analysis, the total power loss in the proposed converter can be expressed as $P_{\text{total-loss}} = P_{rL} + P_{rC} + P_{D-\text{loss}} + P_{\text{mosfet}}$. Then, the efficiency of the proposed HBI can be calculated by

$$\eta = \frac{P_{\rm in} - P_{\rm total-loss}}{P_{\rm in}} = \frac{P_{\rm out} - P_{\rm total-loss}}{P_{\rm out}} = 1 - \frac{P_{\rm total-loss}}{P_{\rm out}}$$
$$= 1 - \left[\frac{P_{rL}}{P_{\rm out}} + \frac{P_{rC}}{P_{\rm out}} + \frac{P_{D-\rm loss}}{P_{\rm out}} + \frac{P_{\rm MOSFET}}{P_{\rm out}}\right] \quad (24)$$

where, in the ideal case, the input power is equal to the output power $P_{\rm in} = P_{\rm out}$.

Therefore, based on (20)–(24), the relationship between efficiency η and the output voltage gain B of the proposed inverter is plotted and compared with other conventional HBIs in Fig. 7(f). Although the inductor loss, the capacitor loss, and the MOSFET loss of the proposed inverter are not very high, the diode power loss is too much higher. And from the loss distribution percentage of the proposed HBI, as shown in Fig. 7(e), the power losses are mainly contributed by diodes. As a result, the overall efficiency of the proposed method, as shown in Fig. 7(f), is lower than the HB-ZSI [16], HB-qZSI [15], and HB-cSBI [19] but higher than that of the HB-SBI [17] and the HB-qSBI [18]. In view of this, by selecting the high-performance diodes with low forward voltage drop V_F and low conduction resistance r_D in the power circuit, the efficiency of the proposed inverter would be further improved.

In addition, by taking the parasitic parameters into consideration, the nonideal output voltage gain of the proposed HBI can be derived as

$$B' = \frac{V'_o}{V_{\rm dc}} = \left(1 - \frac{2V_F}{V_{\rm dc}}\right) \cdot \frac{BR_L}{R_L - (1-D)\,B\cdot P + (2-D)\,B\cdot Q + M} \quad (25)$$

where $P = 3(1-D)r_C + D(1-D)Br_L/2 - (1-D)(3-11D+7D^2)Br_C/2$, $M = [(1-D)(1-2D)Br_C - 2r_C + 2r_{\rm DS}]/2$, $Q = (1-D)r_C + 2D(2-D)(1-D)\,Br_{\rm DS} + (1-D)\,Br_L/2 - (1-D)(1-5D+3D^2)Br_C/2$. And B is the ideal output voltage gain, $B = 1/(1-4D+2D^2)$.

From (25), it can be seen that if $r_L = r_C = r_{\rm DS} = V_F = 0$, B' will become the ideal gain B. The relationship between the nonideal gain B' and the ST duty cycle $D_{\rm sh}$ is plotted in Fig. 8. From this figure, it can be seen that the output voltage gain will not be monotonically increasing when losses are taken into consideration and will be reduced with increase in the parasitic parameters.

IV. Simulation and Experimental Verifications

A. Simulation Results

To validate the features of the proposed half-bridge inverter, simulations based on MATLAB/Simulink software are performed. And the simulation parameters are selected as $V_{\rm dc} = 48$V, $L_1 = L_2 = L_3 = L_4 = 1$ mH, $C_1 = C_2 = C_3 = C_4 = 560\,\mu$F, the shoot-through duty ratio $D_{\rm sh} = 0.22$, the switching frequency $f_s = 10$ kHz, and the load resistance $R_L = 50\,\Omega$. The simulation results are shown in Fig. 9. It can be seen from Fig. 9(a) that the output voltage V_o has three voltage levels—positive voltage 221 V, negative voltage -221 V, and zero voltage 0 V. The capacitor voltages $V_{C1}(= V_{C2})$ and $V_{C3}(= V_{C4})$ are pumped up to 173 and 249 V, respectively. In addition, the active switching voltage stresses and diode voltage stresses are presented in Fig. 9(b) and (c), respectively, which has a good accordance with theoretical results.

B. Experimental Verifications

To verify the effectiveness of the aforementioned simulation and theoretical analysis, a laboratory prototype of the proposed HBI in Fig. 1 was built and tested. The experimental parameters are same as that of the simulation part. Two FCH040N65S3 power MOSFETs are used for the active power switches, both of them are driven by the 2BB0108T basic board with driver 2SC0108T. And all the diodes selected are of the RURG3060CC type.

Fig. 10 shows the corresponding experimental results when $V_{\rm dc} = 48$ V and $D_{\rm sh} = 0.22$. The gate drive signals G_{S1} and G_{S2} of these two MOSFETs are shown in Fig. 10(a). Fig. 10(b) shows the output voltage of the proposed HBI, the positive and negative output voltages are boosted from 48 V to 208 and -208 V, which are slightly lower than the theoretical values. It can be seen from Fig. 10(c) that the inductor currents increase during ST state and decrease during non-ST state. As shown in Fig. 10(d), the capacitor voltages $V_{C1}(= V_{C2})$ and $V_{C3}(= V_{C4})$ are pumped up to 164 and 238 V, respectively, which are less than the calculated values 173.4 and 249.4 V due to the voltage reduction on passive/active elements. The active switching voltage stress (V_{DS1}, V_{DS2}) and the diode voltage stresses are measured and presented in Fig. 10(e) and (f), which also show a good agreement with the simulation results in Fig. 9.

V. Conclusion

In this letter, a new Z-source impedance network-based half-bridge inverter is proposed, which can increase the output voltage gain significantly by using a very small ST duty cycle. Compared with other well-known existed HB-qZSIs/HB-qSBIs, although the proposed topology has a little bit more number of components, the total volume size of passive elements are no higher than them. Moreover, the produced square-waveform output voltage not only has positive and negative voltage levels like traditional HB-ZSI but also has a zero voltage level, and the *n*th harmonic of the output voltage can be eliminated by choosing $D_{\rm sh} = 1/n$, which makes it very suitable for the electroplating and electrochemical power supply applications. Due to the high power loss of diodes, the efficiency of the proposed HBI is limited to some extent and not very high, which can be further improved by selecting high-performance diodes with low forward voltage drop V_F and low parasitic resistance r_D in the power circuit. In addition, the operating principle, passive elements' design guideline, power loss analysis, and voltage stresses comparison of passive/active components are also presented. Finally, both simulation and experimental results are given to verify the features of the proposed topology.

References

[1] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1453–1463, Jul. 2007.

[2] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.

[3] Y. Tang, S. Xie, C. Zhang, and Z. Xu, "Improved Z-source inverter with reduced Z-source capacitor voltage stress and soft-start capability," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 409–415, Feb. 2009.

[4] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2008, pp. 2743–2749.

[5] C. J. Gajanayake, F. L. Luo, H. B. Gooi, P. L. So, and L. K. Siow, "Extended-boost Z-source inverters," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2642–2652, Oct. 2010.

[6] M. Zhu, K. Yu, and F. L. Luo, "Switched-inductor Z-source inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2150–2158, Aug. 2010.

[7] R. Adda, S. Mishra, and A. Joshi, "Analysis and PWM control of switched boost inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5593–5602, Dec. 2013.

[8] S. S. Nag and S. Mishra, "Current-fed switched inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4680–4690, Sep. 2014.

[9] M. K. Nguyen, T. V. Le, S. J. Park, and Y. C. Lim, "A class of quasi switched boost inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1526–1536, Mar. 2015.

[10] P. C. Loh, F. Blaabjerg, and C. P. Wong, "Comparative evaluation of pulse width modulation strategies for Z-source neutral-point-clamped inverter," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 1005–1013, May 2007.

[11] G. Zhang, Z. Li, B. Zhang, D. Qiu, W. Xiao, and W. A. Halang, "A Z source half-bridge inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1269–1279, Mar. 2014.

[12] D. Vinnikov, A. Chub, O. Husev, and T. Jalakas, "Quasi-Z-source half bridge dc–dc converter for photovoltaic applications," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2015, Seville, Spain, pp. 2935–2940.

[13] D. Vinnikov, A. Chub, and L. Liivik, "Asymmetrical quasi-Z-source half-bridge dc–dc converters," in *Proc. 9th Int. Conf. Compat. Power Electron.*, 2015, Lisbon, Portugal, pp. 369–372.

[14] D. Vinnikov, I. Roasto, R. Strzelecki, and M. Adamowicz, "Step-up dc/dc converters with cascaded quasi-Z-source network," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3727–3736, Oct. 2012.

[15] E. Babaei and E. Shokati Asl, "A new topology for Z-source half-bridge inverter with low voltage stress on capacitors," *Elsevier Electr. Power Syst. Res.*, vol. 140, pp. 722–734, Nov. 2016.

[16] E. Babaei and E. Shokati Asl, "High voltage gain half-bridge Z-source inverter with low voltage stress on capacitors," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 191–197, Jan. 2017.

[17] E. Babaei, E. Shokati Asl, and M. H. Babayi, "Steady-state and small-signal analysis of high-voltage gain half-bridge switched boost inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3546–3553, Jun. 2016.

[18] E. Shokati Asl, E. Babaei, and M. Sabahi, "High voltage gain half bridge quasi-switched boost inverter with reduced voltage stress on capacitors," *IET Power Electron*., vol. 10, no. 9, pp. 1095–1108, Jul, 2017.

[19] E. Shokati Asl, E. Babaei, and M. Sabahi, "New half-bridge and full-bridge topologies for a switched-boost inverter with continuous input current," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3188–3197, Apr. 2018.

[20] A. Chub, D. Vinnikov, F. Blaabjerg, and F. Z. Peng, "A review of galvanically isolated impedance-source dc–dc converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2808–2828, Apr. 2016.