Quadratic Boost DC–DC Converter With High Voltage Gain and Reduced Voltage Stresses

Sin-Woo Lee and Hyun-Lark Do

***Abstract*—This paper proposes a quadratic boost dc–dc converter with a high voltage gain and reduced voltage stresses. The conventional quadratic boost converter has a limited voltage gain, which is not suitable for high-step-up applications with various microgrids. In the proposed converter, to improve the voltage gain beyond that of a quadratic converter, a coupled inductor is adopted. Additionally, passive clamping circuits are applied to reduce the high voltage stresses caused by leakage inductance of the coupled inductor. Hence, additional power losses from the snubber circuit do not occur, and low-voltage-rating switching devices can be utilized for the main switch and output diode. Moreover, the reverse-recovery problem of the output diode can be alleviated by the leakage inductance. Therefore, the total power efficiency is improved. The theoretical analysis of the proposed converter is verified with a 300-V, 120-W prototype.**

***Index Terms*—Clamping circuit, coupled inductor, high-step-up converter, quadratic boost converter.**

I. Introduction

RECENTLY, dc microgrid systems for self-sufficiency in small areas have been receiving attention as the next generation of power systems. In particular, renewable power sources such as photovoltaic (PV), wind turbine, waves, and geothermal sources have been adopted for dc power generators in a microgrid system [1]–[3]. Additionally, fuel cells, batteries, and ultracapacitors are also used as backup power sources for the renewable power sources. However, these power sources generate a very low voltage, and a high-step-up dc–dc converter is required to operate loads that require high operating voltages [4].

For step-up applications, a conventional boost dc–dc converter is normally adopted. It has simple structure and low cost. However, its voltage gain is not enough for high-step-up applications [5]–[7]. Moreover, it is not suitable for high-power applications because only two power devices are used to process the load power and it has high voltage and current stresses [8]. As the simplest method to obtain high

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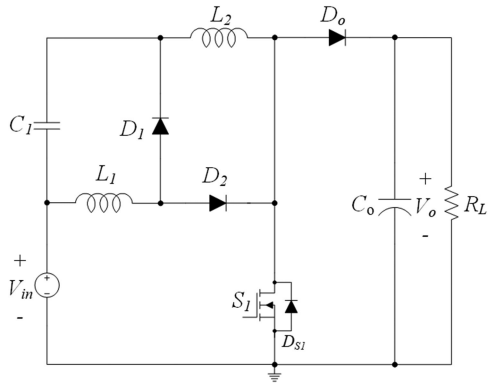

Fig. 1. Conventional quadratic boost dc–dc converter.

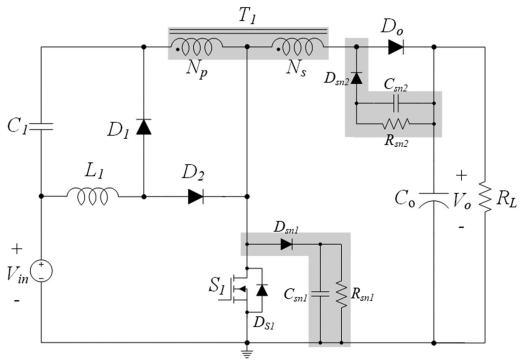

Fig. 2. Convectional quadratic boost dc–dc converter using a coupled-inductor with RCD snubber circuits.

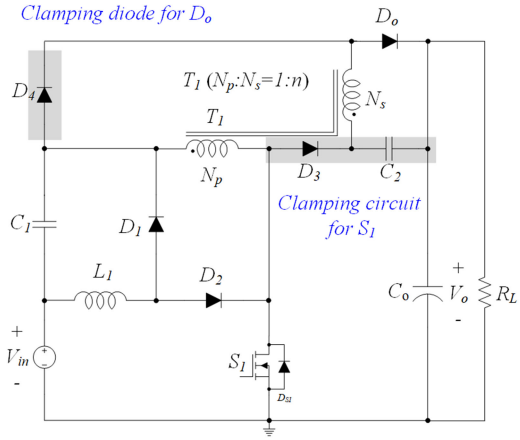

Fig. 3. Circuit diagram of the proposed converter.

by the leakage inductance. Thus, the total power efficiency is improved. In this paper, the theoretical analysis and experimental results of the proposed converter are presented in detail, and the proposed converter is tested by a 300-V, 120-W prototype circuit.

II. Circuit Description

The circuit diagram of the proposed converter is shown in Fig. 3. In the proposed converter, the clamping circuit

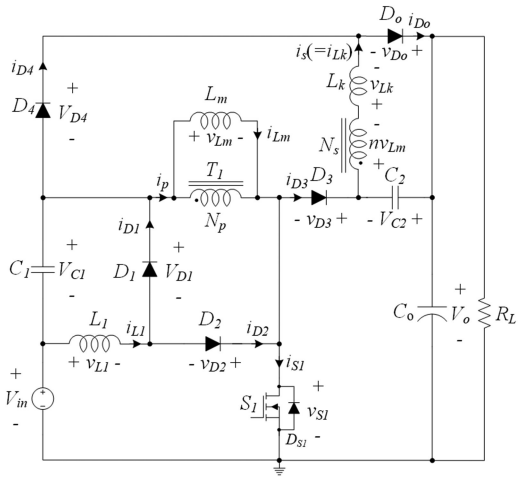

Fig. 4. Equivalent circuit diagram of the proposed converter.

(clamping diode D_3 and clamping capacitor C_2) for S_1 and clamping diode D_4 for D_o are added to the conventional quadratic boost dc–dc converter with a coupled inductor. The other components are the same as those of the conventional quadratic boost dc–dc converter with a coupled inductor. Fig. 4 shows the equivalent circuit diagram of the proposed converter. The coupled inductor T_1 has magnetizing inductance L_m and leakage inductance L_k with a turn ratio of $1:n(n = N_p/N_s)$. L_k is assumed to be much smaller than L_m. The capacitances C_1, C_2, and C_o are considered large enough that their voltages are constant. Because the average inductor voltage should be zero at steady state, according to the volt-second balance law, the voltages across C_1, C_2, and C_o should be equal to V_{C1}, V_{C2}, and V_o.

III. Mode Analysis

The key waveforms and operating modes of the proposed converter are shown in Figs. 5 and 6, respectively. A switching period T_s can be divided into four operating modes. It is assumed that the proposed converter operates in continuous-conduction mode. Before t_0, the main switch S_1 is turned ON and the output diode D_o is conducting by leakage inductance L_k of T_1.

Mode 1 $[t_0, t_1]$*:* The main switch S_1 is conducting, and the output diode D_o is reverse-biased. Energy is stored in inductors L_1 and L_m. Because the voltage v_{L1} across L_1 is $V_{\rm in}$, the current i_{L1} increases linearly with a slope of $V_{\rm in}/L_1$, as follows:

$$i_{L1}(t) = \frac{V_{\rm in}}{L_1}(t - t_0) + I_{L1.\min}. \tag{1}$$

Because the voltage v_{Lm} across L_m is $V_{\rm in} + V_{C1}$, the current i_{Lm} increases linearly with a slope of $(V_{\rm in} + V_{C1})/Lm_1$, as follows:

$$i_{Lm}(t) = \frac{V_{\rm in} + V_{C1}}{L_m}(t - t_0) + I_{Lm.\min}. \tag{2}$$

The clamping diode D_4 is forward-biased because $(1 + n)(V_{\rm in} + V_{C1})$ is greater than $V_o - V_{C2}$. Hence, the current $-i_{D4}$ is same as the secondary current $i_s(=i_{Lk})$ which

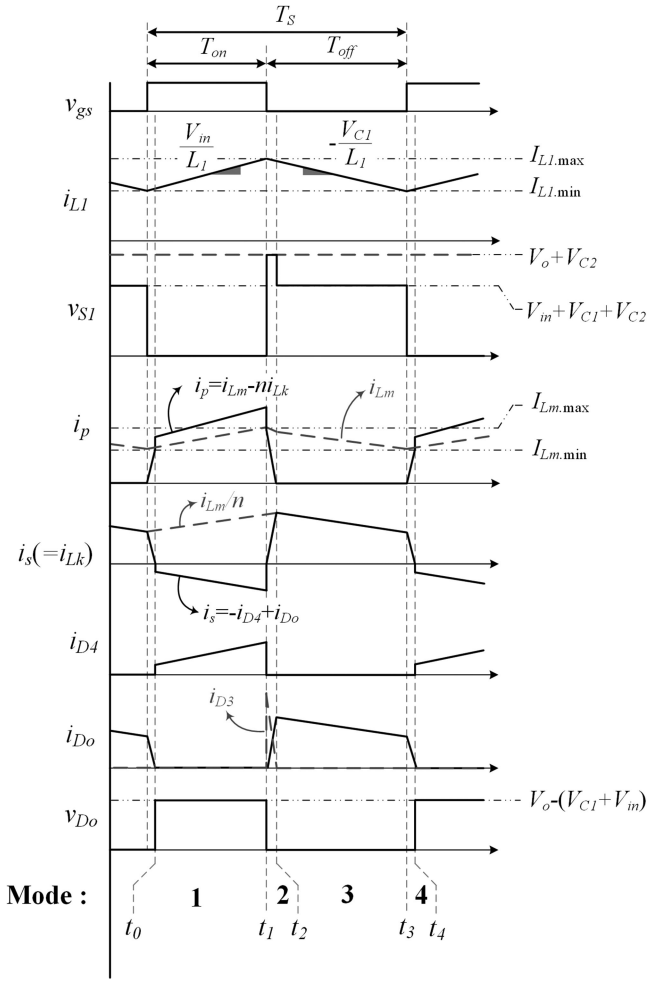

Fig. 5. Key waveforms of the proposed converter.

decreases linearly

$$i_s(t) = \frac{V_o - V_{C2} - (1+n)(V_{\text{in}} + V_{C1})}{L_k}(t - t_0) + i_s(t_0). \tag{3}$$

From (2) and (3), the primary current i_p can be obtained as follows:

$$\begin{aligned} i_p(t) &= i_{Lm}(t) - ni_s(t) \\ &= \left[\frac{v_{Lm}}{L_m} + \frac{n\left[(1+n)v_{Lm} - V_o + V_{C2})\right]}{L_k}\right] \\ &\quad \times (t - t_0) + I_{Lm.\min} - ni_s(t_0) \end{aligned} \tag{4}$$

$$v_{Lm} = V_{\text{in}} + V_{C1}. \tag{5}$$

Mode 2 $[t_1, t_2]$*:* At t_1, the main switch S_1 is turned OFF and the output diode D_o is turned ON. Through diode D_1, the stored energy of L_1 is transferred to C_1.

Because the voltage v_{L1} across L_1 is $-V_{C1}$, the current i_{L1} decreases linearly with a slope of $-V_{C1}/L_1$

$$i_{L1}(t) = \frac{-V_{C1}}{L_1}(t - t_1) + I_{L1.\max}. \tag{6}$$

Because the voltage v_{Lm} across L_m is $(V_o - V_{\text{in}} - V_{C2} - V_{C1})$, the current i_{Lm} decreases linearly, as follows:

$$i_{Lm}(t) = -\frac{V_o - V_{\text{in}} - V_{C1} - V_{C2}}{L_m}(t - t_1) + I_{Lm.\max}. \tag{7}$$

In this mode, the switch voltage V_{S1} is clamped to $V_o - V_{C2}$ because the clamping diode D_3 is turned ON. The output diode current i_{Do} is the same as i_s because the clamping diode D_4 is turned OFF. Because the voltage v_{Lk} across L_k is $-(V_{C2} + nv_{Lm})$, the current $i_s(=i_{Lk})$ decreases linearly as follows:

$$i_s(t) = i_{Do}(t) = \frac{-V_{C2} + n(V_o - V_{\text{in}} - V_{C1} - V_{C2})}{L_k}(t - t_1). \tag{8}$$

In this mode, the primary current i_p is equal to the diode current i_{D3}, which is obtained as follows:

$$\begin{aligned} i_p(t) &= i_{D3}(t) \\ &= I_{Lm.\max} - \tfrac{n[n(V_o - V_{\text{in}} - V_{C1} - V_{C2}) - V_{C2}]}{L_k}(t - t_1). \end{aligned} \tag{9}$$

At the end of this mode, the current i_{D3} reaches to zero. From (9), the time interval between t_2 and t_1 can be obtained by the following:

$$t_2 - t_1 = \frac{I_{Lm.\max} L_k}{n^2(V_o - V_{\text{in}} - V_{C1}) - (1+n^2)V_{C2}}. \tag{10}$$

Mode 3 $[t_2, t_3]$*:* When the primary current i_p reaches zero, this mode starts. The clamping diode D_3 is turned OFF and the current i_{Lm} is the same as ni_s. Because the voltage v_{Lm} across L_m is $-nV_{C2}/(n^2 + L_k/L_m)$, the current i_{Lm} decreases linearly, as follows:

$$\begin{aligned} i_{Lm}(t) &= ni_s(t) \\ &= \frac{-nV_{C2}/(n^2 + L_k/L_m)}{L_m}(t - t_2) + i_{Lm}(t_2). \end{aligned} \tag{11}$$

Because L_k is assumed to be much smaller than L_m, the voltage v_{Lm} can be simplified as

$$v_{Lm} = -\frac{nV_{C2}}{n^2 + L_k/L_m} \approx -V_{C2}/n. \tag{12}$$

Mode 4 $[t_3, t_4]$*:* At t_3, the main switch S_1 is turned ON, but the output diode D_o is not turned OFF due to L_k. The reverse-recovery problem of the output diode can be alleviated because the current i_{Do} decreases linearly with a limited slope by the leakage inductance as follows:

$$i_s(t) = i_{Do}(t) = I_{Lm.\min}/n - \frac{n(V_{\text{in}} + V_{C1}) + V_{C2}}{L_k}(t - t_3). \tag{13}$$

At the end of this mode, the current i_{Do} reaches to zero. From (13), the time interval between t_4 and t_3 can be obtained by the following:

$$t_4 - t_3 = \frac{I_{Lm.\min} L_k/n}{n(V_{\text{in}} + V_{C1}) + V_{C2}}. \tag{14}$$

IV. Characteristic and Design Parameter

In this section, to simplify the mathematical analysis, the leakage inductance L_k is not considered because it is assumed

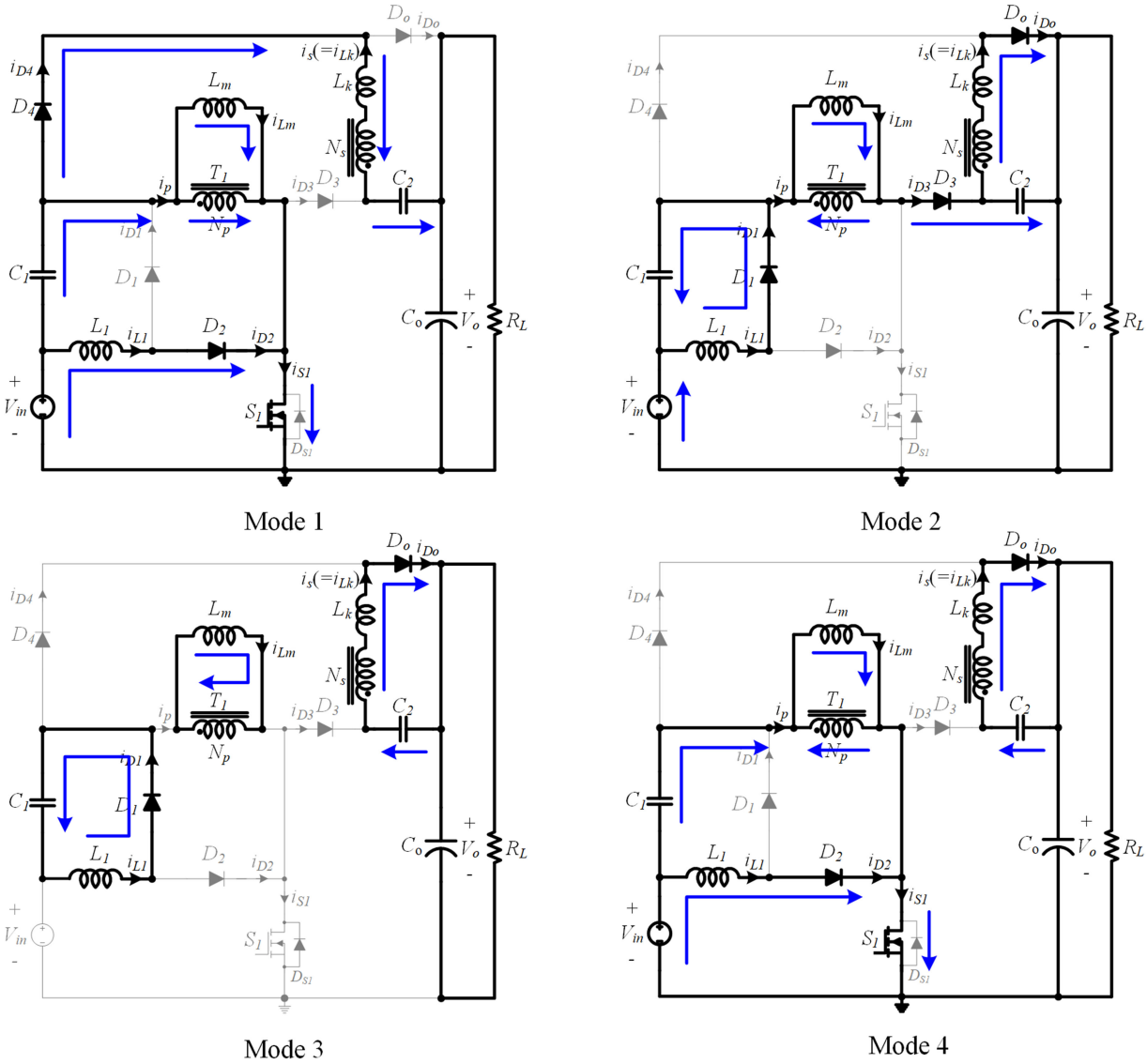

Fig. 6. Operating modes of the proposed converter.

to be much smaller than L_m. To validate the steady-state performance and theoretical analysis of the proposed converter, the design parameters are selected with the following specifications.

1) Input voltage range $V_{\text{in}} = 36 - 48$ V.
2) Output voltage $V_o = 300$ V.
3) Maximum output power $P_o = 120$ W.
4) Switching frequency $f_S = 50$ kHz.

A. Voltages of V_{C1}, and V_{C2}

By applying the voltage-second balance to voltage v_{L1} across L_1, the following equation can be obtained:

$$V_{\text{in}} DT_s - V_{C1}(1-D)T_s = 0. \tag{15}$$

From (15), the voltage V_{C1} can be obtained as follows:

$$V_{C1} = \frac{D}{1-D} V_{\text{in}}. \tag{16}$$

In Mode 1, because it is assumed that the voltage across the capacitors is constant, the following equation can be obtained:

$$(1+n)(V_{\text{in}} + V_{C1}) + V_{C2} - V_o = 0. \tag{17}$$

From (16) and (17), the voltage V_{C2} can be easily obtained as follows:

$$V_{C2} = V_o - \frac{(1+n)V_{\text{in}}}{1-D}. \tag{18}$$

Considering the leakage inductance, the voltage V_{C2} can be obtained as follows:

$$V_{C2} = \frac{V_o - \frac{(1+n)V_{\text{in}}}{1-D}}{1 + (1-k)\left(1 - \frac{1}{D}\right)} \tag{19}$$

$$k = \frac{L_m}{L_k/n^2 + L_m}. \tag{20}$$

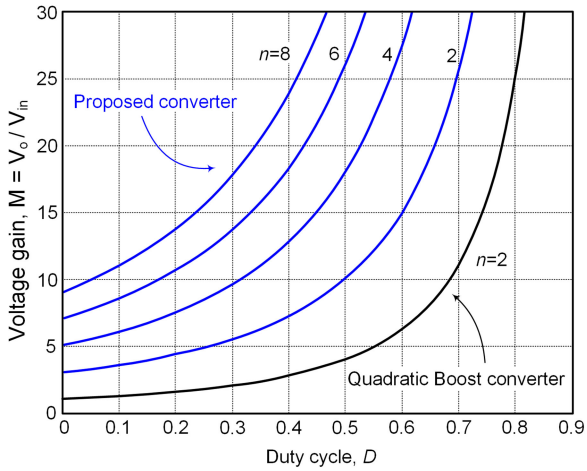

Fig. 7. Voltage gain of the proposed converter.

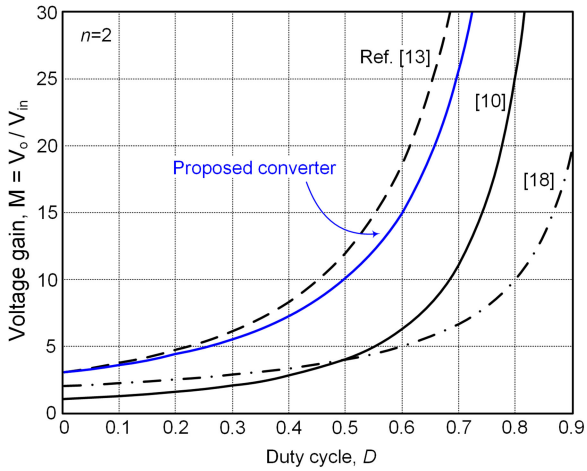

Fig. 8. Comparison of the voltage gain with the high-step-up converter (turn ratio $n = 2$).

B. Voltages Gain M

By applying the voltage-second balance to voltage v_{Lm} across L_m, the following equation can be obtained:

$$(V_{\text{in}} + V_{C1})\, DT_s - \frac{V_{C2}}{n}(1-D)T_s = 0. \tag{21}$$

From (16), (18), and (21), the voltage gain *M* of the proposed converter can be obtained by the following:

$$M = \frac{V_o}{V_{\text{in}}} = \frac{1+n-D}{(1-D)^2}. \tag{22}$$

To achieve the desired voltage, gain *M* (about 6.25–8.33) from (22) for the proposed converter, the duty ration *D* can be calculated as about 0.35–0.45 for the selected turn ratio $n = 2$.

The voltage gain according to the duty cycle is shown in Fig. 7. The voltage gain of the proposed converter is improved over that of the conventional quadratic boost dc–dc converter in Fig. 8. The type of boost-based high-step-up converter is chosen to fairly compare the voltage gain with the proposed converter. The quadratic boost converters were presented in [10] and [13], and the boost convert with a coupled inductor was presented in [18]. These high-step-up converters and the graph of the voltage gain according to the duty cycle are shown in Fig. 8.

Considering the leakage inductance, the voltage gain *M* of the proposed converter can be obtained by the following:

$$M = \frac{V_o}{V_{\text{in}}} = \frac{1+n-D}{(1-D)^2} + \frac{nDk\left[1+(1-k)\left(1-\frac{1}{D}\right)\right]-nD}{(1-D)^2}. \tag{23}$$

Because the voltage gain can be reduced with low coupling coefficient, the coupling coefficient of the coupled inductor should be designed to be tight in order to obtain fine voltage gain.

C. Maximum and Minimum Currents of L_1 and L_m

The average current of L_1 is equal to I_{in}. From (1), the maximum and minimum currents of L_1 can be calculated by the following:

$$I_{L1.\max} = I_{\text{in}} + \frac{V_{\text{in}}}{2L_1} DT_S \tag{24}$$

$$I_{L1.\min} = I_{\text{in}} - \frac{V_{\text{in}}}{2L_1} DT_S. \tag{25}$$

As in a flyback converter, the stored energy of L_m is transferred by T_1 to the secondary side N_s. Therefore, the average current of L_m is equal to $nI_o/(1\text{-}D)$

$$I_{Lm.\text{avg}} = \frac{nI_o}{(1-D)}. \tag{26}$$

From (2) and (26), the maximum and minimum currents of L_1 can be calculated by the following:

$$I_{Lm.\max} = \frac{nI_o}{(1-D)} + \frac{V_{\text{in}} + V_{C1}}{2L_m} DT_S \tag{27}$$

$$I_{Lm.\min} = \frac{nI_o}{(1-D)} - \frac{V_{\text{in}} + V_{C1}}{2L_m} DT_S. \tag{28}$$

D. Selection of Inductors L_1 and L_m

From (24) and (25), the current ripple of L_1 can be calculated by the following:

$$\Delta I_{L1} = I_{L1.\max} - I_{L1.\min} = \frac{V_{\text{in}} DT_S}{L_1}. \tag{29}$$

From (29), to obtain the required ripple component ΔI_{L1}, the inductance of L_1 should satisfy the following condition:

$$L_1 > \frac{V_{\text{in}} D}{\Delta I_{L1} f_s} \tag{30}$$

where $V_{\text{in}} = 48$ V, $D = 0.35$, and $\Delta I_{L1} = 1.5$ A, and (30) gives $L_1 > 224\,\mu$H. Therefore, the inductance of L_1 is selected as 240 μH.

From (27) and (28), the current ripple of L_1 can be calculated by the following:

$$\Delta I_{Lm} = I_{Lm.\max} - I_{Lm.\min} = \frac{V_{\text{in}} DT_S}{(1-D)L_m}. \tag{31}$$

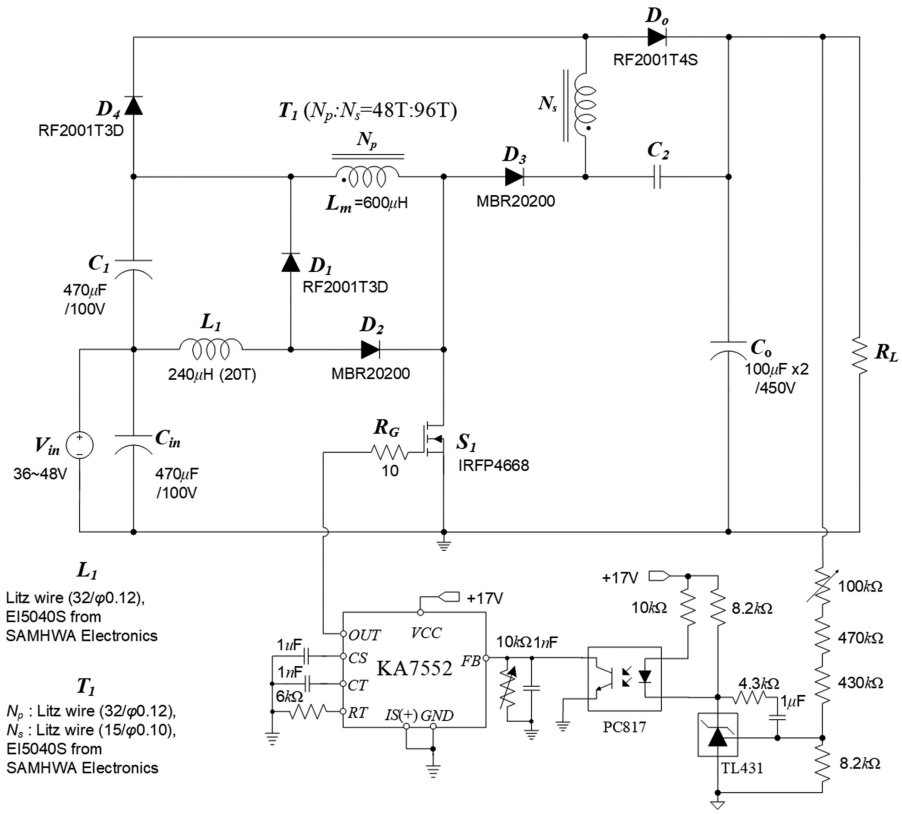

Fig. 9. Laboratory prototype circuit diagram of the proposed converter.

From (31), to obtain the required ripple component ΔI_{Lm}, the inductance of L_m should satisfy the following condition:

$$L_m > \frac{V_{\rm in} D}{(1-D)\Delta I_{Lm} f_s} \tag{32}$$

where $V_{\rm in} = 48$ V, $D = 0.35$, and $\Delta I_{Lm} = 1$ A. Equation (32) gives $L_m > 516\,\mu$H. Therefore, the inductance of L_m is selected as 600 μH.

E. Voltage Stress of Devices

In Mode 2, the maximum voltage across S_1 is clamped to $-V_{C2} + V_{\rm o}$. Therefore, the surge voltage of S_1 is significantly reduced without a dissipative snubber circuit. From (18), the maximum voltages across S_1 can be obtained by

$$V_{S1.\max} = -V_{C2} + V_o = \frac{(1+n)V_{\rm in}}{1-D}. \tag{33}$$

In Mode 1, the maximum voltage across D_o is clamped to $V_o - V_{\rm in} - V_{C1}$. Therefore, the surge voltage of D_o is also significantly reduced. From (16), the output diode D_o can be calculated by the following:

$$V_{Do} = V_o - V_{\rm in} - V_{C1} = \frac{nV_{\rm in}}{(1-D)^2}. \tag{34}$$

The maximum voltages across diodes D_1 and D_2 can be obtained by the following:

$$V_{D1.\max} = V_{\rm in} + V_{C1} = \frac{V_{\rm in}}{1-D} \tag{35}$$

$$V_{D2.\max} = V_o - V_{\rm in} - V_{C1} - V_{C2} = \frac{nV_{\rm in}}{1-D}. \tag{36}$$

V. Experimental Results

To verify the theoretical analysis and the effectiveness of the proposed quadratic boost dc–dc converter with high voltage gain and reduced voltage stresses, a laboratory prototype of the proposed circuit is implemented and tested based on the results of the previous section. The laboratory prototype circuit diagram is shown in Fig. 9. The designed parameters and selected components of the laboratory prototype are shown in Fig. 8. In the control circuit of the proposed converter, KA7552 is used as a pulsewidth modulation IC, and PC817 and TL431 are used for the feedback circuit.

Figs. 10 and 11 show the experimental waveforms of the proposed converter at 36 and 48 V, respectively. Fig. 10(a) and 11(a) show the experimental waveforms of v_{gs} and i_{L1}. These figures demonstrate that the duty ratio is changed according to the input voltage. Figs. 10(b) and 11(b) show the experimental waveforms of v_{gs}, v_{S1}, and i_p. The maximum switch voltage is clamped to $-V_{C2} + V_{\rm o}$. Therefore, low-voltage-rating switching devices are used for a reduction in voltage stress. Figs. 10(c) and 11(c) show the experimental waveforms of v_{gs}, i_s, and v_o.

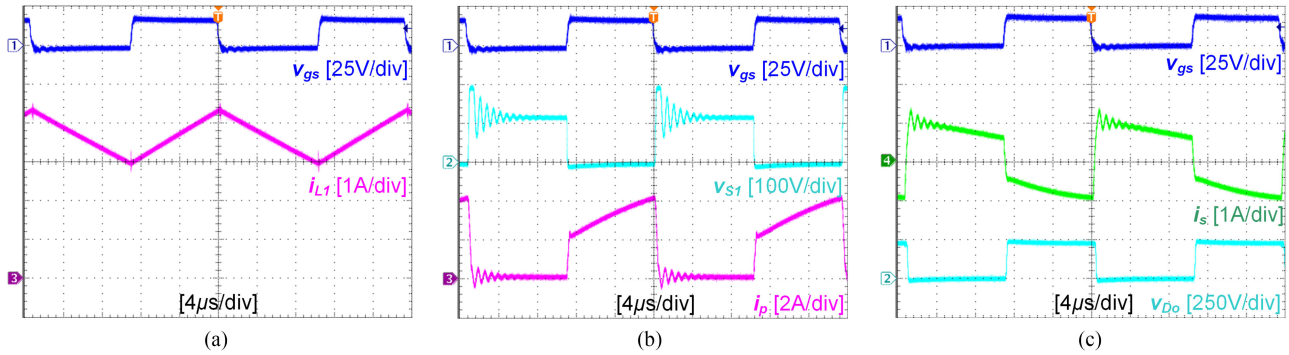

Fig. 10. Experimental waveforms of the proposed converter at $V_{\rm in} = 36$ V. (a) v_{gs} and i_{L1}. (b) v_{gs}, v_{S1}, and i_p. (c) v_{gs}, i_s, and v_{Do}.

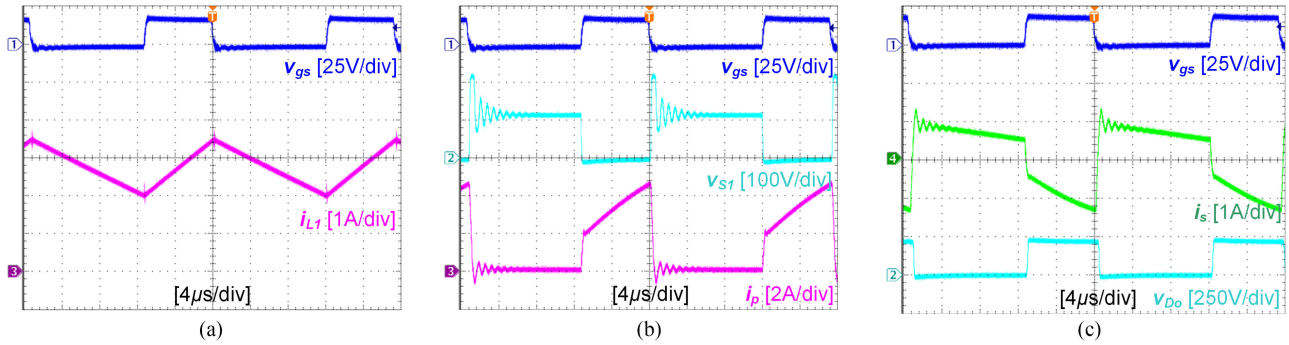

Fig. 11. Experimental waveforms of the proposed converter at $V_{\rm in} = 48$ V. (a) v_{gs} and i_{L1}. (b) v_{gs}, v_{S1}, and i_p. (c) v_{gs}, i_s, and v_{Do}.

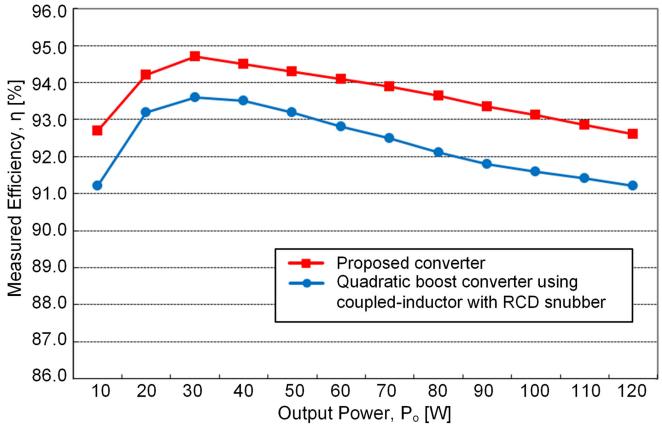

Fig. 12. Measured efficiency of the proposed converter.

These figures show that the maximum output diode voltage is clamped to $V_o - V_{\rm in} - V_{C1}$.

Fig. 12 shows the measured efficiency of the proposed converter compared with the conventional quadratic coupled-inductor converter with a snubber circuit, which is shown in Fig. 2. The efficiency was measured with a WT230 digital power meter from YOKOGAWA.

For a fair comparison, the conventional converter was designed with the same switching frequency, and the other components are all the same except for the lossless passive snubber circuit. In the case of a passive snubber for the main switch, $R_{sn1} = 47$ kΩ and $C_{sn1} = 0.1$ μF are selected for minimum power loss on the passive snubber. The passive snubber circuit (R_{sn2}, C_{sn2}, and D_{sn2}) for the output diode is not used for minimum power loss, although the high-voltage-rating output diode is used.

The efficiency of the proposed converter is higher than the conventional converter because the power losses of the snubber circuit are reduced and low-voltage-rating switching devices are used.

VI. Conclusion

A quadratic boost dc–dc converter with a high voltage gain and reduced voltage stresses is introduced in this paper. In the proposed converter, a coupled inductor is adopted to improve the voltage gain over that of a quadratic converter. Additionally, passive clamping circuits are applied to reduce the high voltage stresses by the leakage inductance of the coupled inductor. Hence, additional power losses of the snubber circuit do not occur and low-voltage-rating switching devices can be utilized for the main switch and output diode. Moreover, the reverse-recovery problem of the output diode can be alleviated by the leakage inductance. Therefore, the total power efficiency is improved.

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