# MagCap DC–DC Converter Utilizing GaN Devices: Design Consideration and Quasi-Resonant Operation

Jong-Won Shin, Masanori Ishigaki, Ercan M. Dede, and Jae Seung Lee

***Abstract*—A MagCap DC–DC converter using GaN semiconductor devices is presented to improve the efficiency and modularity of the vehicular power system. While the topology is as simple as the flyback converter, all the semiconductor switches turn ON and OFF with soft switching. A design guideline to transformer and capacitor is suggested considering the conduction loss and voltage stress of the switches. A quasi-resonant (QR) operation for low output-power condition is also explained. The switches turn ON at the valley of the drain-source waveform to secure soft switching and maximize the efficiency. A 180-W prototype hardware was populated on 63 mm × 31 mm printed circuit board using 200-V GaN FET devices. Peak efficiency was 97.1% at 155-W output power and 1.2-MHz switching frequency. Another prototype was built for the QR operation and demonstrated 91.6% peak efficiency by maintaining the soft switching and avoiding excessive switching frequency.**

***Index Terms*—DC–DC converter, GaN FET, high efficiency, high-frequency switching, quasi-resonant (QR) operation, soft switching.**

## I. INTRODUCTION

POWER system in electrified vehicle (EV) requires high power density and high efficiency. Converters with high volumetric density achieve more freedom for the passengers and other components of the vehicle. High gravimetric density of the converter reduces the weight of the vehicle and improves the driving range. Improved efficiency of the power system enables smaller, lighter, and simpler thermal management devices thanks to its low heat dissipation.

The recent development of widebandgap semiconductors, such as gallium nitride (GaN), is improving the power density and efficiency. Compared with the conventional silicon (Si) MOSFET, the low ON-state resistance of GaN FET decreases the conduction loss, and the small input capacitance and ON-state gate voltage save driving loss. As the device high dv/dt and di/dt

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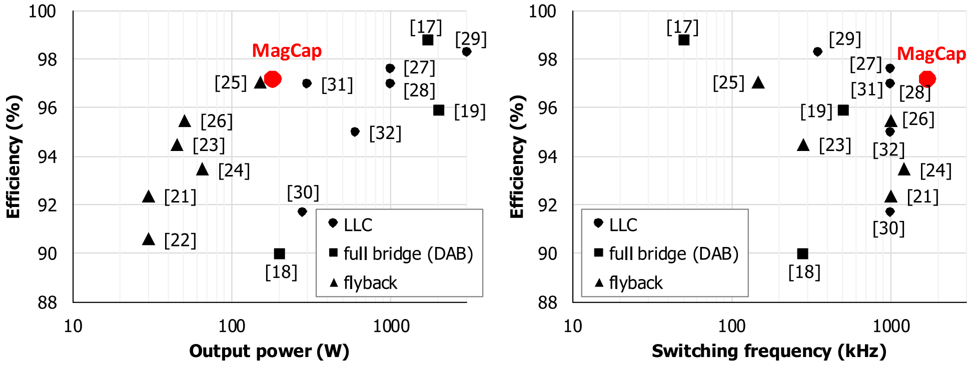


(a) (b)

Fig. 1. Comparison of MagCap converter with other isolated DC–DC converters using GaN FETs [17]–[32] by (a) the rated output power and (b) the maximum switching frequency.

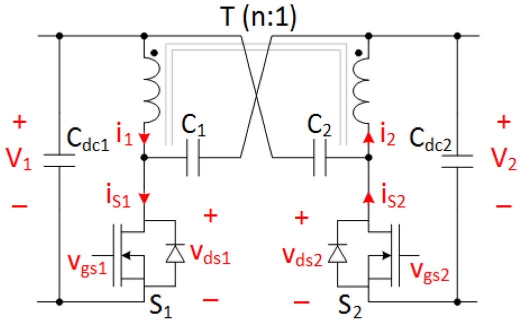


Fig. 2. MagCap converter.

The rest of this paper is structured as follows. Section II articulates the application, circuit topology, and operation principles. Section III explains how the output power is controlled by modulating the ON time of the switch. The QR operation by discrete OFF-time modulation is also presented. Design procedures considering conduction loss and voltage stress of the switch devices are shown in Section IV. Section V reveals the experimental setup and test results of the MagCap converter. Two different prototype circuits verify the peak efficiency such as 97.1% at high power with monotonic ON-time control and 91.6% at low power with QR OFF-time control.

## II. MagCap CONVERTER

### A. Application and Circuit Topology

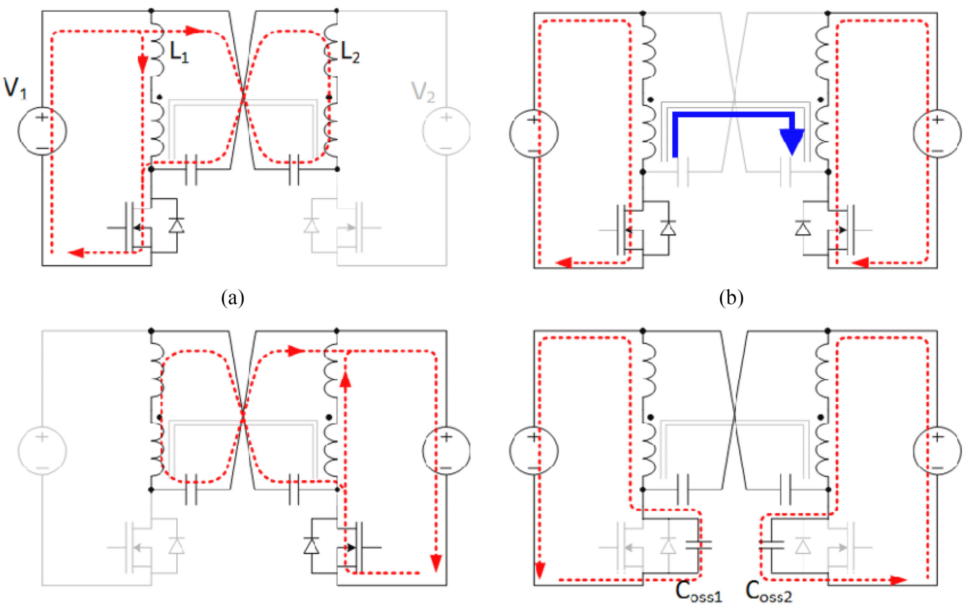
The low-voltage dc system in an EV is described in [15] and [16]. The DC–DC converters in this system should provide high efficiency and power density, and be capable of bidirectional power transfer if connected to batteries. The proposed MagCap converter is shown in Fig. 2 with its key voltages and currents. The converter is designed, implemented, and tested to manage the energy flow between the dc voltage sources $V_1$ and $V_2$. They have the same or similar amplitude such as battery cells. The MagCap converter consists of semiconductor switches $S_1$ and $S_2$, series-connected capacitors $C_1$ and $C_2$, and a transformer $T$. Turn ratio of the primary (left-hand side) and the secondary side (right-hand side) windings is $n$: 1. Decoupling capacitors $C_{\mathrm{dc1}}$ and $C_{\mathrm{dc2}}$ stabilize $V_1$ and $V_2$ by absorbing the high-frequency ac current. The converter is capable of bidirectional power transfer. Switch $S_1$ operates as an active switch and $S_2$ works as a synchronous rectifier (SR) when power flows from $V_1$ to $V_2$. Switch $S_2$ becomes an active switch and $S_1$ an SR when power is drawn from $V_2$ and transferred to $V_1$. Details of the bidirectional power flow are presented in [15, Section IV].

As mentioned in [15], the MagCap converter has a simpler structure than the other bidirectional converters, such as full-bridge or DAB converters and a Ćuk converter, since it employs only two switches without any filter inductors. Comparing with a flyback converter, the MagCap converter has several unique features. It has series-connected capacitors $C_1$ and $C_2$ to enable capacitive power transfer and ZVS. These can be implemented by ceramic capacitors and have negligible effect on the converter volume and weight. The MagCap converter does not need any snubbers to suppress voltage or current spike, because it utilizes the energy stored in the leakage inductances of $T$.

A similar topology was derived by Dai and Ludois by modifying the buck–boost converter [33]. It was named as switch—inductor—inductor—diode (SLLD) converter and used as a capacitive wireless battery charger. Two major differences between the SLLD and MagCap converter are the magnetic coupling and snubber capacitor. The MagCap converter includes a transformer with a single coil, while the SLLD employs two discrete inductors without magnetic coupling. The SLLD converter employs a snubber capacitor across the active switch to guarantee the zero-voltage turn OFF. The MagCap converter utilizes parasitic capacitances of switches only, and no external capacitors are required to achieve the soft switching. This will be explained in detail in Section II-B. Another difference between the two converters is the control method: the MagCap converter operates with variable frequency with modulated constant (monotonic ON-time control) ON time or discrete (QR OFF-time control) OFF time; the SLLD is controlled by fixed-frequency pulsewidth modulation.

### B. Principle of Operation

The operation of the MagCap converter when the power flows from $V_1$ to $V_2$ is explained with the circuit diagrams in Fig. 3 and the key waveforms in Fig. 4. Voltages $v_{gs1}, v_{gs2}, v_{ds1},$



(a) (b)

(c) (d)

Fig. 3. Four operational states of the MagCap converter in a switching cycle. (a) Interval 1 ($t_0 - t_1$). (b) Interval 2 ($t_1 - t_2$). (c) Interval 3 ($t_2 - t_3$). (d) Interval 4 ($t_3 - t_4$).

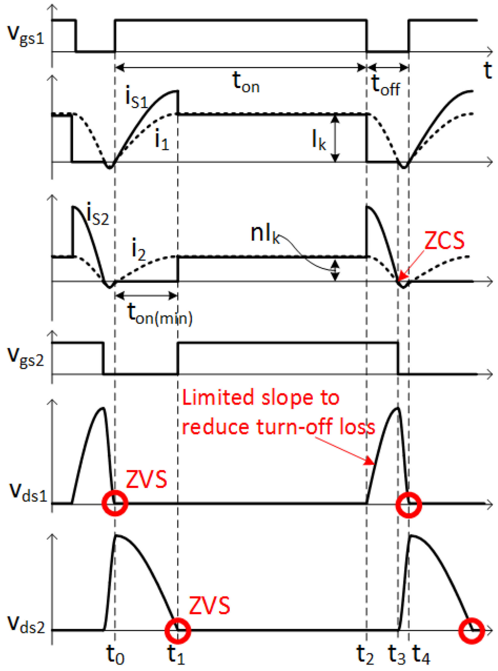


Fig. 4. Key waveforms of the MagCap converter when power is transferred from $V_1$ to $V_2$ ($V_1$ is equal to $nV_2$).

and $v_{ds2}$ are the gate-source voltage of $S_1$, gate-source voltage of $S_2$, drain-source voltage of $S_1$, and drain-source voltage of $S_2$, respectively. Currents $i_1, i_2, i_{S1}$, and $i_{S2}$ flow through the primary-side winding, secondary-side winding, $S_1$, and $S_2$, respectively. $C_{\mathrm{dc1}}$ and $C_{\mathrm{dc2}}$ are neglected in Fig. 3. The transformer $T$ has leakage inductance $L_1$ at the primary side and $L_2$ at the secondary side. Its magnetizing inductance is neglected by assuming that it is sufficiently larger than $L_1$ and $L_2$ and carries negligible current during the operation. Dotted arrows indicate the current flow. A solid arrow in Fig. 3(b) represents the magnetic power transfer from the primary to secondary side.

*Interval 1* ($t_0 - t_1$): $S_1$ turns ON and the currents flows through $T$, $C_1$, and $C_2$. $L_1$ and $L_2$ resonate with $C_1$ and $C_2$ and store energy from $V_1$. Current $i_1$ increases from zero in sinusoidal way according to

$$i_1(t) = I_k \sin \frac{t - t_0}{\sqrt{L_e C_e}} \tag{1}$$

where $L_e = \frac{L_1}{n^2} + L_2$ and $\frac{1}{C_e} = \frac{1}{C_1} + \frac{1}{C_2}$. The coefficient $I_k$ is shown as

$$I_k = \frac{1}{n}\sqrt{\frac{C_e}{L_e}}\left(v_{C1}(t_0) - v_{C2}(t_0) + \frac{n+1}{n}V_1\right). \tag{2}$$

Voltage $v_{C1}(t_0) - v_{C2}(t_0)$ in (2) is determined by output power and other circuit parameters as described in the Appendix. Currents $i_2$ and $i_{S1}$ are shown as

$$i_2(t) = n i_1(t) = n I_k \sin \frac{t - t_0}{\sqrt{L_e C_e}} \tag{3}$$

$$i_{S1}(t) = i_1(t) + i_2(t) = (n+1) I_k \sin \frac{t - t_0}{\sqrt{L_e C_e}}. \tag{4}$$

Voltage $v_{ds2}$ is expressed in (5). $S_1$ turns ON softly at $t_0$ since $v_{ds1}(t_0)$ is zero

$$v_{ds2}(t) = \left(V_2 - \frac{V_1}{n}\right) + n\sqrt{\frac{L_e}{C_e}} I_k \cos \frac{t - t_0}{\sqrt{L_e C_e}}. \tag{5}$$

The interval 1 ends when $v_{ds2}$ touches zero at $t_1$. Duration of interval 1 is equal to a quarter of the resonant period as

$$t_1 - t_0 = \frac{\pi\sqrt{L_e C_e}}{2}. \tag{6}$$

The ON time of $S_1$ $t_{\text{on}}$ should be equal to or longer than this duration to maintain the ZVS of $S_2$ at $t_1$.

*Interval 2* $(t_1 - t_2)$*:* $S_1$ is still turned ON. $S_2$ can be turned ON after $t_2$ as SR to steer $i_2$ from its virtual body diode to junction to reduce the conduction loss. Precise control of the turn ON instant of $S_2$ is critical to the system efficiency because the forward voltage drop of a GaN FET is generally larger than that of Si counterpart. $C_1$ and $C_2$ carry no current in this interval since $V_1$ and $V_2$ hold the voltages of *T* and prohibit resonance. Power is transferred from $V_1$ to $V_2$ through the magnetic coupling of *T*. The slopes of $i_1$ and $i_2$ are

$$\frac{di_1}{dt} = \frac{V_1 - nV_2}{n^2 L_e} \tag{7}$$

$$\frac{di_2}{dt} = n\frac{di_1}{dt} = \frac{V_1 - nV_2}{nL_e}. \tag{8}$$

The slopes of $i_1$ and $i_2$ are zero, i.e., $i_1$ and $i_2$ are constant during the interval 2 when $V_1 = nV_2$. If $V_1 \neq nV_2$, $i_1$ and $i_2$ present finite slope. This interval ends when $S_1$ turns OFF at $t_2$.

*Interval 3* $(t_2 - t_3)$*:* Another resonance occurs at $t_2$. Current flows through $L_1, L_2, C_1$, and $C_2$ which is similar to the interval 1. Energy in $L_1$ and $L_2$ is released to $V_2$ via $C_1$ and $C_2$. The mathematical expressions of current $i_1$ are as follows:

$$\begin{aligned} i_1(t) &= i_1(t_2)\cos\frac{t - t_2}{n\sqrt{L_e C_e}} \\ &\quad - \frac{n + 1}{n}\sqrt{\frac{C_e}{L_e}}\left(V_2 - \frac{V_1}{n}\right)\sin\frac{t - t_2}{n\sqrt{L_e C_e}}. \end{aligned} \tag{9}$$

Using (9) and (2), current $i_{S2}$ is derived as

$$\begin{aligned} i_{S2}(t) &= (n+1)i_1(t_2)\cos\frac{t - t_2}{n\sqrt{L_e C_e}} \\ &\quad - \frac{(n + 1)^2}{n}\sqrt{\frac{C_e}{L_e}}\left(V_2 - \frac{V_1}{n}\right)\sin\frac{t - t_2}{n\sqrt{L_e C_e}}. \end{aligned} \tag{10}$$

If $V_1 = nV_2$, (9) and (10) are simplified as

$$i_1(t) = I_k \cos\frac{t - t_2}{n\sqrt{L_e C_e}} \tag{11}$$

$$i_{S2}(t) = (n + 1)\, I_k \cos\frac{t - t_2}{n\sqrt{L_e C_e}} \tag{12}$$

where $I_k = i_1(t_2)$.

Voltage $v_{ds1}$ is calculated as

$$\begin{aligned} v_{ds1}(t) &= n\sqrt{\frac{L_e}{C_e}}\, i_1(t_2)\sin\frac{t - t_2}{n\sqrt{L_e C_e}} \\ &\quad + (n+1)\sqrt{\frac{L_e}{C_e}}\left(V_2 - \frac{V_1}{n}\right)\left(\cos\frac{t - t_2}{n\sqrt{L_e C_e}} - 1\right) \end{aligned} \tag{13}$$

and if $V_1 = nV_2$, the equation can be written as

$$v_{ds1}(t) = n\sqrt{\frac{L_e}{C_e}}\, I_k \sin\frac{t - t_2}{n\sqrt{L_e C_e}}. \tag{14}$$

Duration of interval 3 is equal to a quarter of the resonant period as in (15), which is $n$ times of interval 1. Note that it is solely determined by $L_e$ and $C_e$, and not affected by $V_1, V_2$, or the output power.

$$t_3 - t_2 = n(t_1 - t_0) = \frac{n\pi\sqrt{L_e C_e}}{2} \tag{15}$$

This interval ends when the currents becomes zero at $t_3$.

*Interval 4* $(t_3 - t_4)$*:* Output parasitic capacitances $C_{\text{oss1}}$ of $S_1$ and $C_{\text{oss2}}$ of $S_2$ resonate with $L_1$ and $L_2$. Duration of interval 4 is half of the resonant period among $C_{\text{oss1}}, C_{\text{oss2}}, L_1$, and $L_2$ as

$$t_4 - t_3 = n\pi\sqrt{L_e C_{e4}} \tag{16}$$

where $\frac{1}{C_{e4}} = \frac{1}{C_{\text{oss1}}} + \frac{n^2}{C_{\text{oss2}}}$. Similar with interval 3, the duration of interval 4 does not depend on $V_1, V_2$, or the output power. Currents through $C_1$ and $C_2$ are zero, and, thus, their voltages are constant during interval 4. $S_1$ turns ON softly after $v_{ds1}$ decreases to zero at $t_4$. Interval 4 is shorter enough than intervals 1 or 2 because $C_{e4}$ is much smaller than $C_e$. If the OFF time is not controlled precisely due to low resolution of $v_{gs1}$, ZVS of $S_1$ may be lost. External capacitors can be added parallel to $S_1$ and $S_2$ to solve this issue.

Intervals 1 and 3 are capacitive since $C_1$ and $C_2$ are involved in the power transfer. Interval 2 is magnetic because the magnetic coupling of *T* transfers power.

All turn-ON and turn-OFF transitions of $S_1$ and $S_2$ are soft switching. Both $S_1$ and $S_2$ turn ON with zero voltage: $S_1$ turns ON at $t_0$ or $t_4$ when $v_{ds1}$ is zero; $S_2$ turns ON at $t_1$ while $\mathrm{v}_{ds2}$ is zero. Though $S_1$ turns OFF at $t_2$ with nonzero current, $v_{ds1}$ does not jump abruptly after $t_2$. The increasing slope of $v_{ds1}$ is limited by the resonance of $C_1, C_2, L_1$, and $L_2$. This minimizes the overlap of $v_{ds1}$ and $i_{d1}$ to make the turn-OFF switching loss of $S_1$ still small. $S_2$ turns OFF with zero current at $t_3$. These soft-switching operations enable the high efficiency presented in Section V.

## III. POWER CONTROL OF A MAGCAP CONVERTER

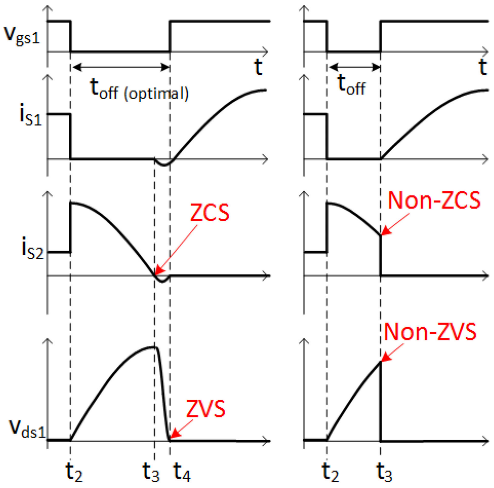
### A. *Monotonic On-Time Control When* $P_o \geq P_{\text{cap}}$

The MagCap converter adjusts its magnetic power by modulating the ON time of $S_1$ $t_{\text{on}}$ while the capacitive power remains constant by the fixed OFF time of $S_1$ $t_{\text{off}}$. They are defined as

$$t_{\text{on}} = t_2 - t_0 \tag{17}$$

$$t_{\text{off}} = t_4 - t_2. \tag{18}$$

*1) Capacitive Power Transfer:* Inductances $L_1$ and $L_2$ store energy from $V_1$ during interval 1, and release the energy to $V_2$ during interval 3 through $C_1$ and $C_2$. The average power delivered by these capacitors in a switching period $P_{\text{cap}}$ is calculated



(a) (b)

Fig. 5. Comparison of switching behavior with (a) optimal $t_{\text{off}}$ to secure the soft switching and (b) shorter $t_{\text{off}}$ that loses soft switching.

from interval 3 as

$$P_{\text{cap}} = \frac{1}{t_4 - t_0}\int_{t_2}^{t_3} i_{S2} V_2 dt = \frac{n\,(n\ +\ 1)\sqrt{L_e} I_k V_2}{t_4 - t_0} \quad (19)$$

assuming that $i_2$ is constant during interval 2 as $nI_k$. The power $P_{\text{cap}}$ is hardly controllable because the quantities in (19) are predetermined by the component design. One way to control $P_{\text{cap}}$ is to adjust $t_{\text{off}}$ to modulate $t_3 - t_2$, the integral interval in (19). However, decreasing $t_{\text{off}}$ should be avoided because $S_1$ and $S_2$ will lose the soft switching. Fig. 5 compares the switching behavior between optimal $t_{\text{off}}$ and shorter $t_{\text{off}}$. If $t_{\text{off}}$ is not long enough and $i_{d2}$ does not reach zero at $t_3$ as shown in Fig. 5(b), $S_2$ turns OFF with nonzero current and $S_1$ turns ON with nonzero voltage. These hard switching generates considerable power loss and noise. $t_{\text{off}}$ and $P_{\text{cap}}$ should therefore be fixed for soft switching. The optimal $t_{\text{off}}$ is expressed in

$$t_{\text{off (optimal)}} = n\pi\left(\frac{\sqrt{L_eC_e}}{2} + \sqrt{L_eC_{e4}}\right). \quad (20)$$

*2) Magnetic Power Transfer:* $P_{\text{mag}}$ is transferred from $V_1$ to $V_2$ through the magnetic coupling of $T$ during interval 2 as

$$P_{\text{mag}} = \frac{1}{t_4 - t_0}\int_{t_1}^{t_2} i_2 V_2 dt = \frac{nI_kV_2\,(t_2 - t_1)}{t_4 - t_0}. \quad (21)$$

$P_{\text{mag}}$ can be controlled by adjusting $t_2 - t_1$. The soft switching of $S_1$ is not interfered if the minimum $t_{\text{on}}$ in (6) is guaranteed. In other words, $S_1$ maintain zero-voltage turn ON if following equation is met

$$t_{\text{on}} \geq t_{\text{on(min)}} = \frac{\pi\sqrt{L_eC_e}}{2}. \quad (22)$$

Fig. 6 plots the normalized output power $P_o = P_{\text{cap}} + P_{\text{mag}}$ with respect to the normalized $t_{\text{on}}$ when (23)–(26) are satisfied. Base quantities of power and time for the normalization are the maximum output power and $t_{\text{on(min)}}$, respectively

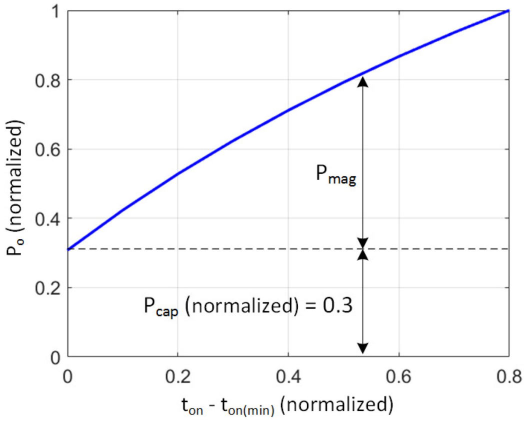


Fig. 6. Normalized output power versus normalized $t_{\text{on}} - t_{\text{on(min)}}$ in monotonic region.

$$t_{\text{on(min)}} \leq t_{\text{on}} - t_{\text{on(min)}} \leq 1.8t_{\text{on(min)}} \quad (23)$$

$$\frac{P_{\text{cap}}}{P_o(\max)} = 0.3 \quad (24)$$

$$V_1 = V_2 \quad (25)$$

$$n = 1. \quad (26)$$

where $P_o$ as well as $P_{\text{mag}}$ increases monotonically as $t_{\text{on}}$ increases. $P_{\text{cap}}$ remains constant regardless of the variation of $t_{\text{on}}$.

### *B. QR Off-Time Control When $P_o < P_{cap}$*

For the output power smaller than $P_{\text{cap}}$, $t_{\text{off}}$ is increased discretely to turn ON $S_1$ at the valley of the $v_{ds1}$ waveform to minimize the switching loss. The waveform in Fig. 7 describes how $t_{\text{off}}$ is controlled in a discrete way as $P_o$ decreases. Note that the hashed area emphasizes the variation of $t_{\text{off}}$. The wave shape of $i_{S2}$ is same with that of $P_o$ since $V_2$ is assumed to be constant. Fig. 7(a) presents the situation where $t_2 - t_1 = P_{\text{mag}} = 0$ and $P_o = P_{\text{cap}}$. In Fig. 7(b), $t_{\text{off}}$ increases to skip one more valley of $v_{ds2}$ waveform and maintain the ZVS of $S_2$. During the valley skipping (from $t_x$ to $t_y$), power circulates through $C_{\text{oss1}}$, $C_{\text{oss2}}$, and $T$ and the net power delivered from $V_1$ to $V_2$ is zero. The QR operation extends interval 4 to increase the switching period and decrease the average power delivered to $V_2$. $t_{\text{off}}$ is further increased and skips two valleys if even smaller output power is requested, as shown in Fig. 7(c).

The OFF-time $t_{\text{off}}$ in (20) is extended as

$$t_{\text{off}} = n\pi\left\{\frac{\sqrt{L_eC_e}}{2} + (m\ +\ 1)\sqrt{L_eC_{e4}}\right\} \quad (27)$$

where $m$ is number of the skipped valleys. The MagCap converter operates in monotonic control when $m = 0$. If $m$ is 1 or larger, the converter is in QR operation. Mathematical

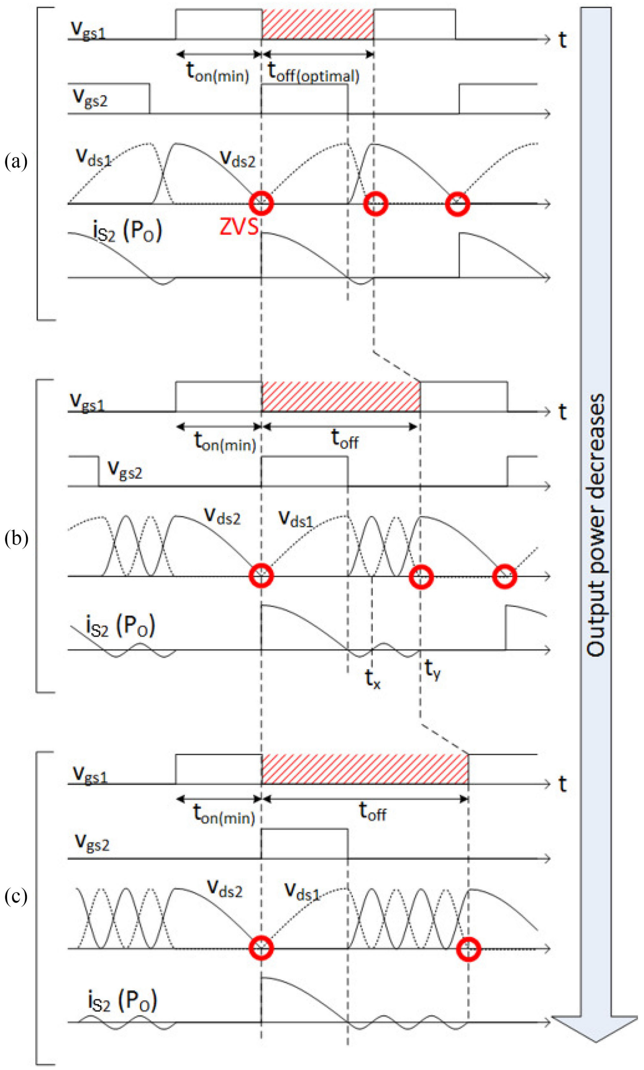


Fig. 7. Control of $t_{\text{off}}$ when output power is smaller than $P_{\text{cap}}$ to achieve valley switching of $S_2$. $t_{\text{off}}$ jumps to larger values and skips more valleys as the output power decreases from (a) to (c). (a) No valley skipping ($m = 0$). (b) One additional valley is skipped ($m = 1$). (c) Two additional valleys are skipped ($m = 2$).

expression of $P_o$ in the QR operation is shown as

$$P_o = P_{\text{cap}} \frac{t_{\text{on}} + t_{\text{off (optimal)}}}{t_{\text{on}} + t_{\text{off (optimal)}} + 2\pi m n \sqrt{L_e C_{e4}}} \tag{28}$$

where $t_{\text{off (optimal)}}$ is as shown in (20) and Fig. 7(a). Skipping more valleys means the larger denominator in (28), and, thus, smaller $P_o$. This QR operation is similar to the conventional converters employing valley switching, such as flyback converter [34], [35] and boost converter in critical-conduction mode [6], [7]. Circulating current during the valley skipping was ignored because the conduction and core losses are negligible.

Fig. 8 visualizes $t_{\text{off}}$ and $t_{\text{on}} - t_{\text{on(min)}}$ in both monotonic and QR regions when $P_o$ varies. Base quantities of the normalization are the same with that used for Fig. 6. $t_{\text{off}}$ jumps discretely to higher values as $P_o$ decreases beyond $P_{\text{cap}}$, as displayed in Fig. 8(a). Fig. 8(b) shows that $t_{\text{on}} - t_{\text{on(min)}}$ is still modulated in the QR region to compensate the power difference between the discretized $P_o$. Note that the plot of the monotonic region in Fig. 8(b) is equal to Fig. 6 with the *x*- and *y*-axes transposed.

## IV. DESIGN CONSIDERATIONS

### A. Minimizing Conduction Loss

Most of the power loss of the MagCap converter is from the transformer, especially the conduction loss in windings (see the loss breakdown shown in Fig. 15), because the switching losses are suppressed by soft switching as explained in Section II-B. In this section, design parameters, such as n, $L_e$, and $C_e$, are considered to minimize the root-mean-square (rms) currents.

*1) Symmetry of Waveform:* The transformer turns ratio $n$ designated by (29) makes the currents $i_1$ and $i_2$ flat during interval 2, and equalizes the current and voltage stress of $S_1$ and $S_2$ in a switching period

$$n = \frac{V_1}{V_2}. \tag{29}$$

The peak voltage of both switches is $n\sqrt{\frac{L_e}{C_e}} I_k$ from (5) and (14) if (29) is satisfied. The peak current of the switches becomes $(n + 1) I_k$ from (4) and (12). Also, the rms $i_1$, $i_2$, $i_{S1}$, and $i_{S2}$ become smaller when (29) is satisfied.

*2) Ratio Between Capacitive and Magnetic Intervals:* The wave shape or "form factor" of the current waveform is determined by the ratio between the capacitive interval (intervals 1 and 3) and magnetic interval (interval 2) in monotonic ON-time control. Interval 4 is neglected since it is much shorter than the other intervals. The ratio of the capacitive interval to the unit switching period $T_n$ is defined as

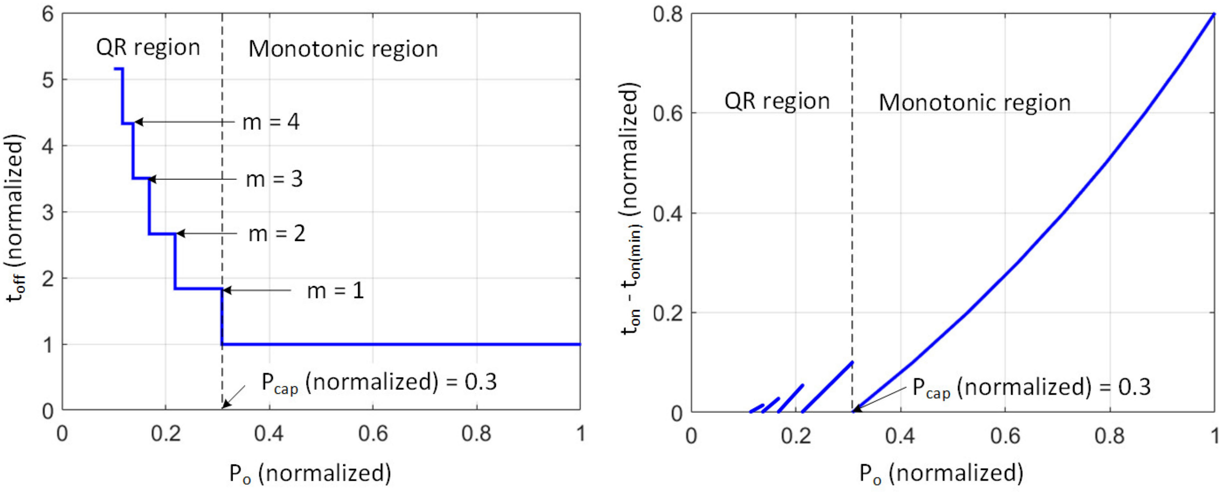
$$T_n = \frac{\text{(capacitive interval)}}{\text{(unit switching period)}} = \frac{(t_1 - t_0) + (t_3 - t_2)}{t_3 - t_0} \tag{30}$$

$T_n$ ranges between zero and unity. The case $T_n = 1$ means that there is no interval 2 and all the power is capacitively transferred within a switching period, as shown in Fig. 7(a). Considering (6) and (15) and defining $T_s$ as the unit switching period, $T_n$ is rearranged, as per

$$T_n = \frac{(n + 1)\pi\sqrt{L_e C_e}}{2T_s}. \tag{31}$$

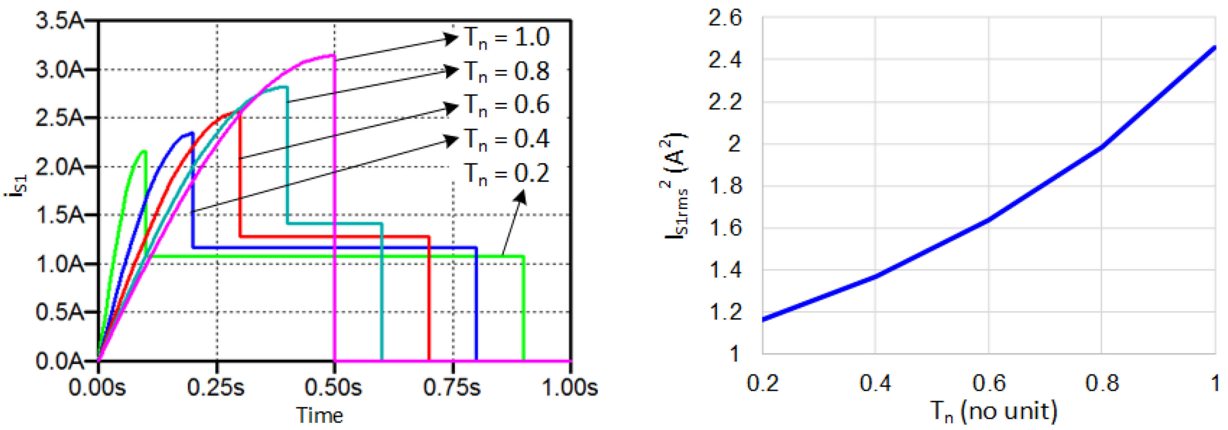
Fig. 9(a) shows the $i_{S1}$ waveform with various $T_n$ when its average current, $n$, and switching period are fixed as 1 A, 1, and 1 s, respectively. The same average $i_{S1}$ means that the same power is drawn from $V_1$. The rms $i_{S1}$ increases as $T_n$ decreases. Fig. 9(b) shows the squared rms $i_{S1}$ versus $T_n$, which is directly proportional to the conduction loss of $S_1$. Other currents such as $i_1$, $i_2$, and $i_{S2}$ have the same tendency. It is, therefore, beneficial to design $T_n$ as small as possible to suppress the conduction loss in the MagCap converter.

The switches will experience high-voltage stress, however, if $T_n$ is excessively small. When (29) is true, the maximum voltage



(a) (b)

Fig. 8. (a) $t_{\mathrm{off}}$ versus $P_o$ (normalized). $t_{\mathrm{off}}$ increases discretely as $P_o$ decreases to skip the valleys and obtain ZVS of $S_2$. (b) $t_{\mathrm{on}} - t_{\mathrm{on(min)}}$ versus $P_o$ (normalized).



(a) (b)

Fig. 9. (a) Waveform of $i_{S1}$ with various $T_n$, while its average value is fixed as 1 A. (b) Squared rms $i_{S1}$.

stress of switches $v_{ds\max}$ is shown as

$$v_{ds\max} = \frac{P_O}{V_2} \frac{1}{\sqrt{\frac{C_e}{L_e}} - \frac{\pi(n+1)C_e}{2T_s}\left(1 - \frac{2}{\pi}\right)}. \tag{32}$$

Detailed derivation of (32) is presented in the Appendix. Fig. 10 shows $v_{ds\max}$ calculated by (32) (solid line) and simulated by LTspice XVII using the parameters defined in Table I (dots with broken line). Several $L_e$ and $C_e$ values were selected to vary $T_n$ while their resonant period $\sqrt{L_e C_e}$ and the capacitive intervals remain constant. $v_{ds\max}$ increases as $T_n$ decreases. Therefore, the minimum $T_n$ should be selected to utilize switch devices with reasonable rated voltage. For example, $T_n$ should be larger than 0.44 to limit the voltage stress as 120 V. There is roughly 5-V error between the calculation and simulation in Fig. 10 since interval 4 was neglected. This error does not significantly affect the selection of the rated voltage of the semiconductor devices.

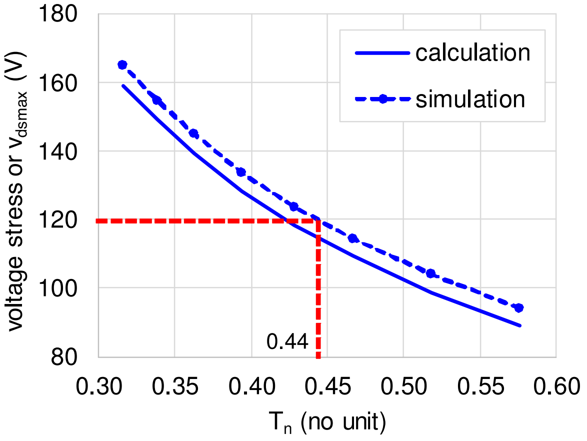


Fig. 10. Voltage stress versus $T_n$ using the parameters defined in Table I.

### *B. Design Procedure*

$L_e$ and $C_e$ can be designed to minimize $T_n$ if the voltage stress remains small enough. Fig. 11 shows the switching period $T_s$,

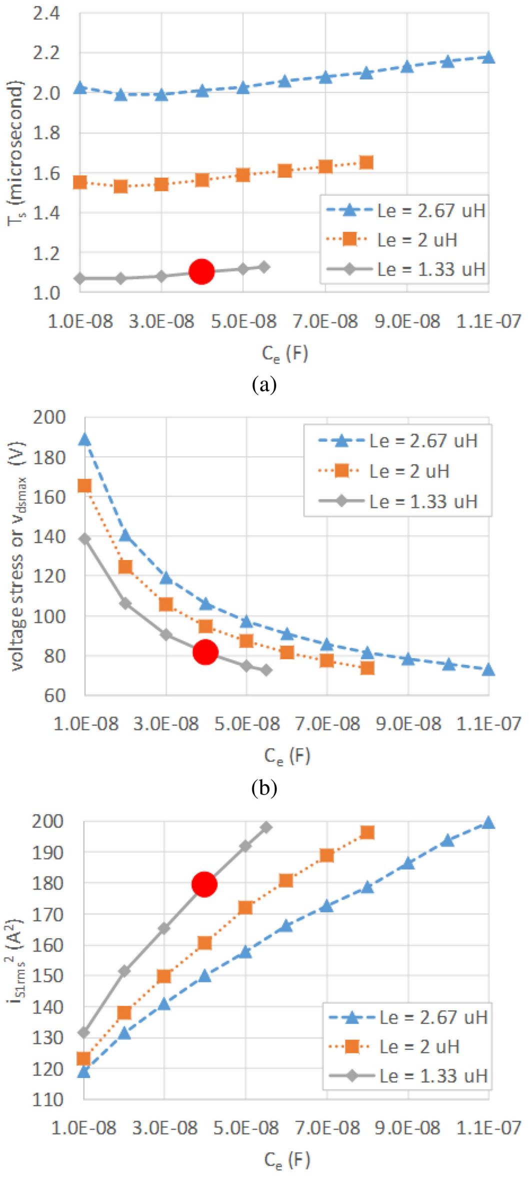
TABLE I
SIMULATION PARAMETERS OF THE MAGCAP CONVERTER

| Parameter | Description | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $S_1$ | MOSFET model<br>On-state resistance $R_{on}$ = 5 mΩ<br>(two EPC2034 in parallel)<br>Off-state resistance $R_{off}$ = 1 MΩ<br>$C_{oss1}$ = 700 pF | | | | | | | |
| $S_2$ | Diode model<br>$R_{on}$ = 5 mΩ<br>$R_{off}$ = 1 MΩ<br>Forward voltage drop $V_f$ = 0 V<br>$C_{oss2}$ = 700 pF | | | | | | | |
| $V_1$, $V_2$ | 20 V | | | | | | | |
| $P_o$ | 200 W | | | | | | | |
| $n$ | 1 | | | | | | | |
| $L_1$, $L_2$ | $0.5L_e$ | | | | | | | |
| $C_1$, $C_2$ | $2C_e$ | | | | | | | |
| $\sqrt{L_e C_e}$ | 330 ns | | | | | | | |
| $L_e$ (μH) | 2.31 | 2.64 | 2.97 | 3.30 | 3.63 | 3.96 | 4.29 | 4.62 |
| $C_e$ (nF) | 47.1 | 41.3 | 36.7 | 33.0 | 30.0 | 27.5 | 25.4 | 23.6 |
| $T_s$ (μs) | 1.80 | 2.00 | 2.22 | 2.42 | 2.63 | 2.86 | 3.06 | 3.28 |
| $T_n$ | 0.58 | 0.52 | 0.47 | 0.43 | 0.39 | 0.36 | 0.34 | 0.32 |
| Simulation time | 3 ms (long enough to guarantee steady-state operation) | | | | | | | |
| Time step | 1 ns | | | | | | | |

voltage stress of the switch $v_{ds\,\max}$, and squared rms $i_{S1}$. All data were obtained by simulating the MagCap converter with 200-W output and 20 V for $V_1$ and $V_2$ in LTspice XVII. Larger $L_e$ results in longer $T_s$, as per Fig. 11(a), and higher voltage stress, as per Fig. 11(b). Smaller $C_e$ is recommended to reduce the conduction loss when $L_e$ is fixed as in Fig. 11(c).

One of the design procedures is to determine $T_s$, $L_e$, and $C_e$ as shown in the flowchart in Fig. 12. The maximum $T_s$ at the rated power is determined first by various external factors such as the input and output filters, voltage- and current-sensing dynamics, performance of digital controller, etc. Lower $T_s$ may decrease $L_e$, voltage stress, and $C_e$, while it may increase the volume and weight of the filters. Either $L_e$ or $C_e$ may be designed after $T_s$ is set. In this procedure, $L_e$ is fixed first by the transformer design because the capacitance is easier to tune than the leakage inductance of a transformer. Smaller $L_e$ is generally preferred to relieve the voltage stress of the switches, as shown in Fig. 11(b). The conduction loss increases with smaller $L_e$, but this may be compensated for by choosing smaller $C_e$ as highlighted in Fig. 11(c). The minimum $C_e$ value is limited by $v_{ds\max}$.

In this paper, $L_e$, $C_e$, and $T_s$ were selected as 1.3 $\mu$H, 44 nF, and 1.1 $\mu$s, respectively. As indicated by the filled red circles in Fig. 11, this design prioritizes both the high switching frequency (1.1–1.7 MHz) and low-voltage stress of the switches by trading off the conduction loss. Increased switching loss and excessive EMI are two typical problems of high-frequency switching. Soft switching of $S_1$ and $S_2$ explained in Section II relieves these issues. Note that the design procedure explained in this paper is not the only possible approach to optimize the MagCap converter. The priority among the $L_e$, $C_e$, and $T_s$ parameters may be interchanged depending upon the application or design objective.



(a)

(b)

(c)

Fig. 11. (a) Switching period $T_s$. (b) Voltage stress $v_{ds\max}$. (c) Squared rms current of switches with various $L_e$ and $C_e$ values. Circles indicate the design example verified in Section V-A.

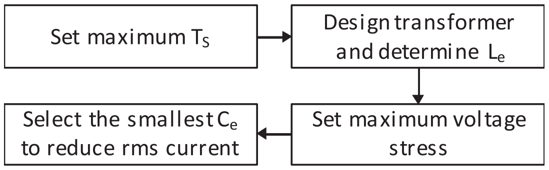
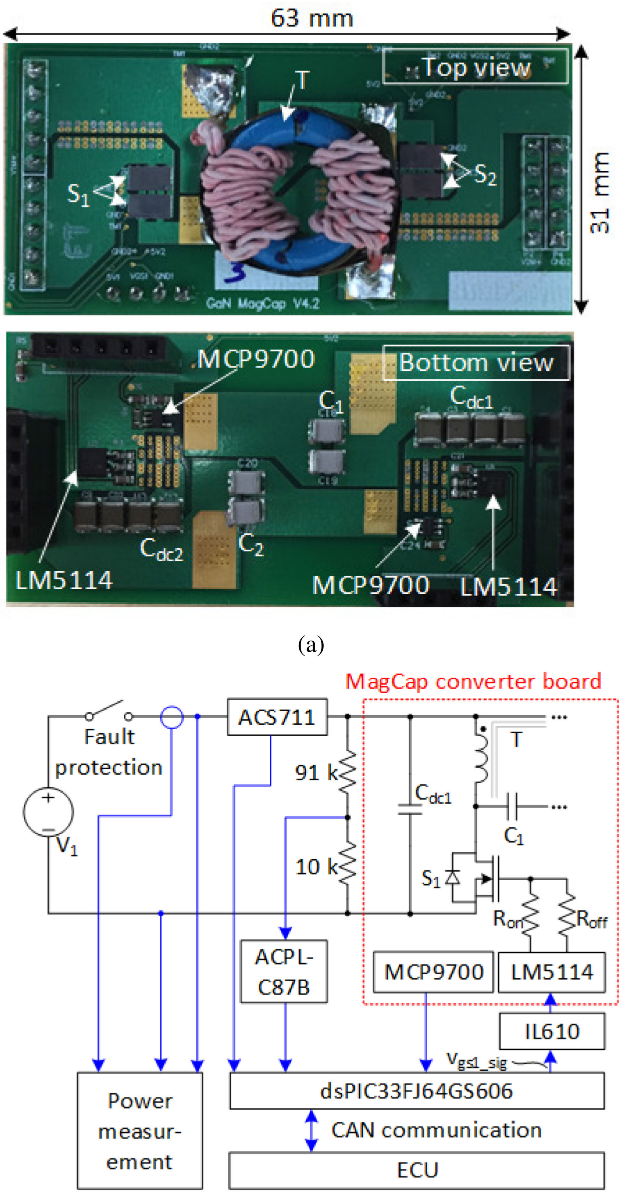


Fig. 12. Design flow for the MagCap converter.

The 1.3-$\mu$H $L_e$ can be realized by many factors, such as the magnetic core, air-gap length, and turns number of windings of the transformer $T$. Coupling coefficient of a toroidal core varies considerably by the relative distance between the windings and turns number and the leakage inductance can be set from wide



(a)

(b)

Fig. 13. (a) Photograph of prototype hardware (heat sinks are not shown). (b) Test setup including sensor ICs and power measurement for control. Dotted box indicates the part shown in (a).

range of values. In this paper, the magnetizing inductance was set around 5 $\mu$H by a toroidal core with 0.1-mm air gap and six-turn winding. Avoiding the airgaps to minimize the eddy current loss by fringing magnetic field, the positions of the primary and secondary windings were adjusted as shown in Fig. 13(a) to achieve 1.3-$\mu$H $L_e$ and 5.25-$\mu$H magnetizing inductance.

## V. Experimental Verification

### A. Operation With Monotonic On-Time Control

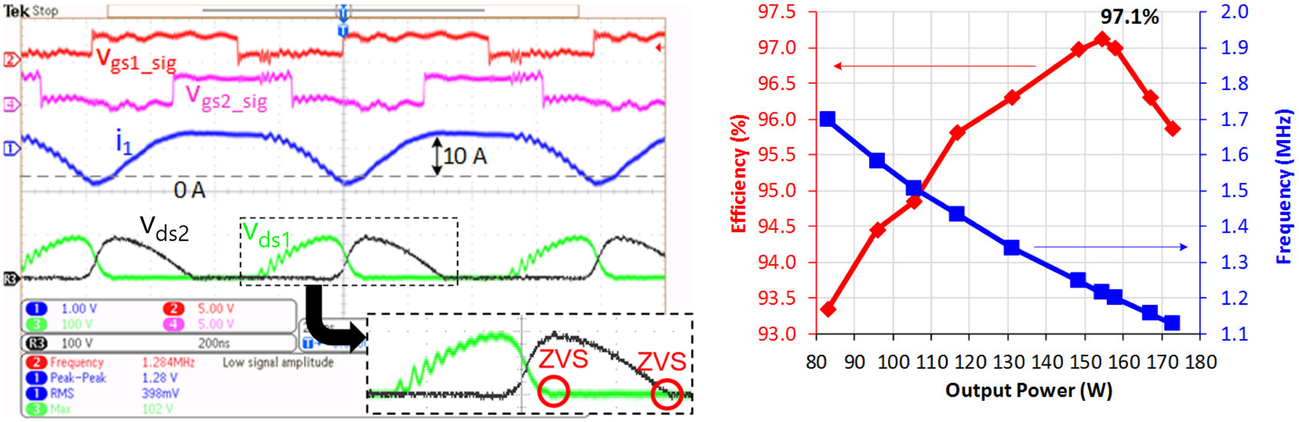
A prototype with 180-W rated power was implemented on a 63 mm × 31 mm printed circuit board (PCB) as shown in Fig. 13(a) and tested in the monotonic power range. Devices $\mathrm{S}_1, \mathrm{S}_2$, and $T$ were mounted on top of the PCB. Heat sinks were not shown to reveal $\mathrm{S}_1$ and $\mathrm{S}_2$. Gate drivers LM5114, temperature sensors MCP9700, and the capacitors were mounted beneath the PCB. Fig. 13(b) shows the signal flow using current sensor ACS711, voltage sensor ACPL-C87B, and signal isolator IL610. Only the primary side is drawn since the secondary side has the same configuration. A 16-bit digital signal controller dsPIC33FJ64GS606 controls the MagCap converter in constant power mode according to the command from the main electronic control unit. A simple algorithm of PI error amplification and antiwindup (roughly 10-s settling time) governed precharge process and power exchange operation between a battery emulator and a supercapacitor [15]. A heat sink was attached to the two parallel GaN FETs using a thermal interface material. Forced-air cooling was applied to these heat sinks by a 12-V dc fan. Components of the prototype converter are listed in Table II. $L_1, L_2, C_1$, and $C_2$ are as determined in Section IV.

TABLE II
Components of the MagCap Converter to Test Monotonic Power Range

| Component | Description | |
|---|---|---|
| $\mathrm{S}_1$, $\mathrm{S}_2$ | Efficient Power Conversion EPC2034 (Engineering sample, 200 V/48 A, two in parallel, no external capacitors added) | |
| $\mathrm{C}_{\mathrm{dc1}}$, $\mathrm{C}_{\mathrm{dc2}}$ | 40 µF (four 10 µF/50 V in parallel) | |
| $\mathrm{C}_1$, $\mathrm{C}_2$ | 44 nF (two 22 nF/1 kV in parallel) | |
| T | Core | TDK B64290L0632 N87 |
| | Turns number | 6:6 |
| | Air gap | 0.1 mm |
| | Magnetizing inductance | 5.25 µH |
| | $\mathrm{L}_1$, $\mathrm{L}_2$ | 660 nH |
| | Winding | Litz wire (65 AWG #36 wires), 3 strands braided |
| $\mathrm{R}_{\mathrm{on}}$, $\mathrm{R}_{\mathrm{off}}$ | 5 Ω | |
| Heat sink | Alphanova S1515-10W | |
| Thermal interface material | Bergquist GP5000S35-0.040-02-0816 | |
| Fan | Delta Electronics AFB0612EH (DC 12 V) | |

Voltage sources $V_1$ and $V_2$ were emulated by Kikusui PAS40-18 and PBZ40-10, respectively. A custom high-speed solid-state circuit breaker protects the system from overcurrent and short-circuit fault. Input and output powers of the MagCap converter were measured by Yokogawa DL850 by using its current probes 701933 and isolated voltage probes 700929. The data acquisition settings for all channels were set to 10 kHz without any data filtering or averaging.

Fig. 14(a) shows measured waveform of the prototype MagCap converter when $V_1 = V_2 = 24\,\mathrm{V}$, output power $= 134\,\mathrm{W}$, and switching frequency $= 1.28\,\mathrm{MHz}$ measured by Tektronix MDO3024. Traces $v_{gs1\_\mathrm{sig}}$ (red trace) and $v_{gs2\_\mathrm{sig}}$ (magenta) are the output of the digital signal controller as shown in Fig. 13(b). There is approximately 330-ns propagation delay between $v_{gs1}$ $(v_{gs2})$ and $v_{gs1\_sig}$ $(v_{gs2\_sig})$. The other traces are $i_1$ (blue), $v_{ds1}$ (green), and $v_{ds2}$ (black), respectively. All the wave shapes are as expected in Fig. 4. Switches $\mathrm{S}_1$ and $\mathrm{S}_2$ achieved



(a) (b)

Fig. 14. Experimental results when $V_1 = V_2 = 24$ V for monotonic power range. (a) Measured waveform when $P_o = 134$ W and $f_s = 1.28$ MHz. ($v_{gs1\_\mathrm{sig}}$ and $v_{gs2\_\mathrm{sig}}$: 5 V/div., $i_1$: measured by Rogowski coil, ac coupled, 10 A/div, $v_{ds1}$ and $v_{ds2}$ : 100 V/div., time scale: 200 ns/div.) (b) Measured efficiency and switching frequency versus output power.

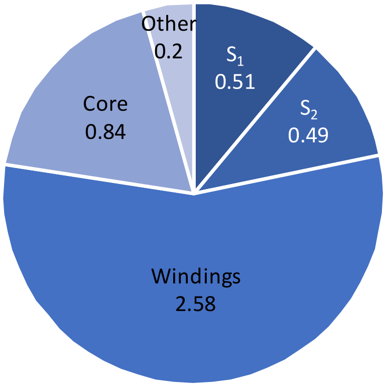


Fig. 15. Estimated loss breakdown of the total loss 4.6 W at 155-W output condition (unit: W).

soft switching as explained in Section II-B. The voltage stress of $\mathrm{S}_1$ and $\mathrm{S}_2$ was 102 V. This voltage is higher than 80 V designed by Fig. 11(b), because of the component tolerance and that the input voltage was not 20 but 24 V in the experiment. The current $i_1$ was measured by a Rogowski coil, power electronics measurements CWT03 of which sensitivity is 100 mV/A. Note that the 0-A reference level for $i_1$ is different from that of the oscilloscope channel because the Rogowski coil measures ac-coupled signal. The maximum $i_1$ was 10 A. Fig. 14(b) plots the efficiency and switching frequency versus output power when $V_1 = V_2 = 24$ V. Switching frequency ranged from 1.12 to 1.7 MHz, while the output power was from 83 to 173 W in the monotonic region. The maximum efficiency reached 97.1% at 155-W output power and 1.2-MHz switching. The temperature of GaN FETs measured by thermocouples did not exceed 45 °C (with an ambient temperature of 21 °C) in any operating conditions.

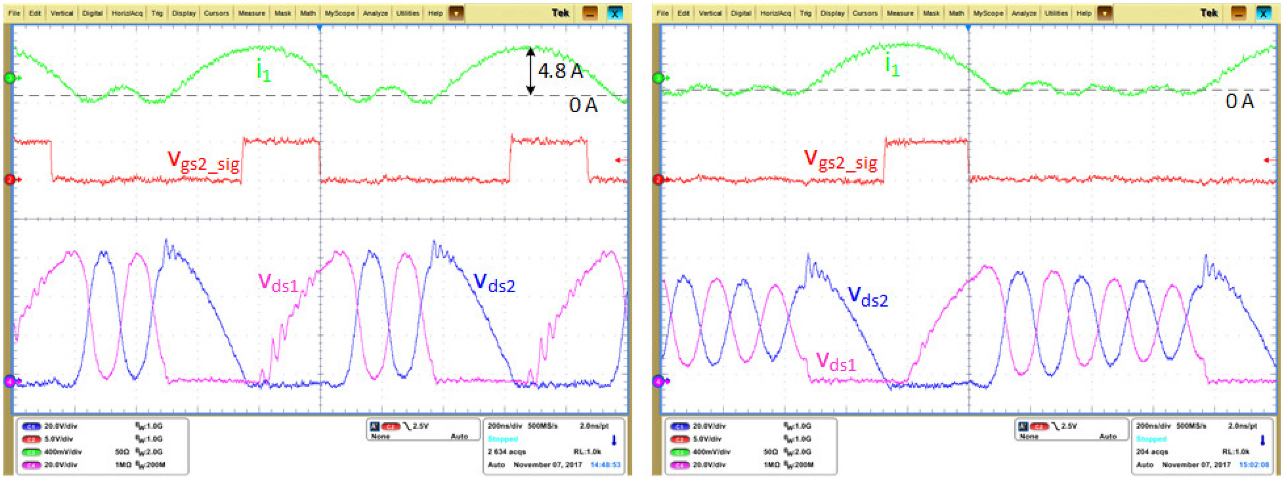
Total loss when $P_o = 155$ W with 97.1% efficiency is 4.6 W. Fig. 15 presents the estimated breakdown of the loss. The transformer contributes 3.42 W (74% of the total loss) by its windings and core. $\mathrm{S}_1$ and $\mathrm{S}_2$ provide 1 W only because their small ON-state resistance and soft switching save the loss. Losses from gate driving and contact/trace resistances are included in 0.2 W other losses.

### B. *Operation With QR Off-Time Control*

The QR operation described in Section III-B was also verified with different prototype hardware. To explore the converter operation with better resolution, $P_{\mathrm{cap}}$ of this prototype was increased to 126 W when $V_1 = V_2 = 24$ V by tuning $C_1$ and $C_2$ as 55 nF. Optimizing the efficiency at high current and high power was not considered in this prototype. Solid wires of AWG 22 were employed instead of Litz wires for cost-effectiveness. All the other components and measurements are the same as defined in Section V-A.

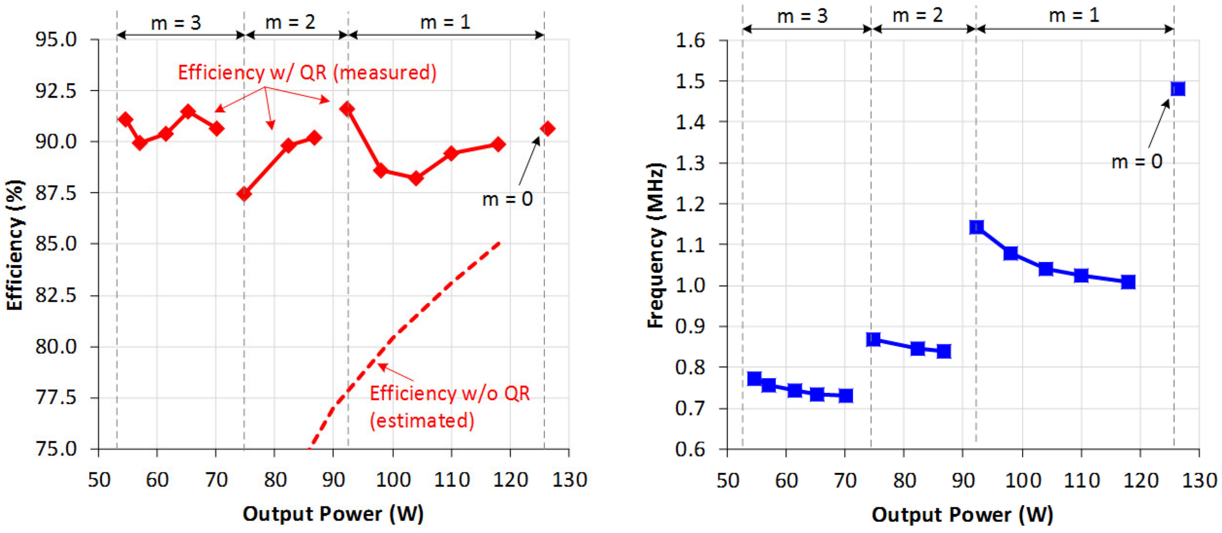
Fig. 16 shows the experimental waveform of the prototype measured using a Tektronix MDO3024. The four traces from the top are $i_1$ (green), $v_{gs2\_\mathrm{sig}}$ (red), $v_{ds1}$ (magenta), and $v_{ds2}$ (blue). In Fig. 16(a), $m = 1$ and $P_o = 92.4$ W, which corresponds to the waveform shown in Fig. 7(b). In Fig. 16(b), $m = 3$ for the smaller output power such as $P_o = 54.7$ W. Though $v_{ds1}$ was not perfectly zero at the turn-ON instant due to the resistive decay of the resonance, $\mathrm{S}_1$ still maintains soft switching with negligible loss.

Fig. 17 plots the efficiency and switching frequency versus output power. The right-most data points are when $P_o = P_{\mathrm{cap}} = 126$ W, and $m = P_{\mathrm{mag}} = 0$ as presented in Fig. 7(a). The efficiency, indicated by the diamond markers, stayed between 87.5% and 91.6%. The dashed line in Fig. 17(a) is the estimated efficiency if OFF-time modulation, as shown in Fig. 5(b), is applied instead of QR control. It is lower than the measured QR efficiency owing to the considerable switching loss caused by high-frequency hard switching and core loss. Switching frequency in Fig. 17(b) decreases as $m$ increases. This is logical since increased $m$ implies longer $t_{\mathrm{off}}$. Switching frequency decreases as $P_o$ increases when $m$ is fixed. This is a result of the modulation of $t_{\mathrm{on}}$ to control the output power as shown in Fig. 8(b).



(a) (b)

Fig. 16. (a) Measured waveform of a QR operation when $V_1 = V_2 = 24$ V ($v_{gs2\_sig}$ : 5 V/div., $i_1$: measured by Rogowski coil, ac coupled, 4 A/div, $v_{ds1}$ and $v_{ds2}$ : 20 V/div., time scale: 200 ns/div.). (a) $m = 1$, and $P_o = 92.4$ W. (b) $m = 3$, and $P_o = 54.7$ W.



(a) (b)

Fig. 17. (a) Measured efficiency and (b) switching frequency when the output power is controlled by the QR operation ($V_1 = V_2 = 24$ V).

## VI. CONCLUSION

A MagCap converter using GaN FETs is suitable to the power architecture of EV due to its simple structure, high efficiency, and bidirectional power transfer capability. The design guideline to determine the resonant components, such as leakage inductances and series-connected capacitors, are explained by considering the tradeoff between switching frequency, voltage stress across the switches, and conduction loss. For low-power operation, a QR control scheme was also introduced to maintain the soft switching and avoid excessive switching frequency. The prototype hardware optimized for 180-W rated power showed 97.1% peak efficiency with 155-W/24-V output and 1.2-MHz switching frequency. Another prototype for QR operation also verified that the MagCap converter can transfer low power while maintaining both soft switching and fair efficiency between 87.5% and 91.6%.

## APPENDIX

Average output current per switching period of the MagCap converter is $i_{S2\mathrm{avg}}$ as

$$i_{S2\mathrm{avg}} = \frac{P_O}{V_2}. \tag{a1}$$

Current $i_{S2\mathrm{avg}}$ is expanded by calculating the integral in (a2). Interval 4 is neglected

$$\begin{aligned} i_{S2\mathrm{avg}} &= \frac{1}{T_s}\int_{t_0}^{t_4} i_{S2}\,dt = \frac{1}{T_s}\left[\int_{t_1}^{t_2} i_{S2}\,dt + \int_{t_2}^{t_3} i_{S2}\,dt\right] \\ &\cong \frac{1}{T_s}\left[nI_k\left\{T_s - (n+1)\frac{\pi\sqrt{L_eC_e}}{2}\right\} + n\,(n+1)\,I_k\sqrt{L_eC_e}\right] \\ &= nI_k\left[1 - \frac{\pi\,(n+1)}{2T_s}\sqrt{L_eC_e}\left(1-\frac{2}{\pi}\right)\right]. \end{aligned} \tag{a2}$$

Substituting (2) into (a2) and rearranging yields

$$\begin{aligned} i_{\mathrm{S2avg}} &= \sqrt{\tfrac{C_e}{L_e}}\left(v_{C1}(t_0) - v_{C2}(t_0) + \tfrac{n+1}{n}V_1\right) \\ &\quad \times \left\{1 - \tfrac{\pi(n+1)}{2T_s}\sqrt{L_e C_e}\left(1 - \tfrac{2}{\pi}\right)\right\}. \end{aligned} \tag{a3}$$

The voltage $v_{C1}(t_0) - v_{C2}(t_0)$ is derived from (a3) and (a1)

$$\begin{aligned} &v_{C1}(t_0) - v_{C2}(t_0) \\ &= \frac{P_O}{V_2}\frac{1}{\sqrt{\frac{C_e}{L_e}} - \frac{\pi(n+1)C_e}{2T_s}\left(1 - \frac{2}{\pi}\right)} - \frac{n+1}{n}V_1. \end{aligned} \tag{a4}$$

At $t_0$, (a5) is true

$$v_{ds2}(t_0) = v_{ds2\,\max} = V_1 + V_2 + v_{C1}(t_0) - v_{C2}(t_0). \tag{a5}$$

Substituting (a4) into (a5), yields

$$\begin{aligned} v_{ds2\,\max} &= \left(V_2 - \frac{V_1}{n}\right) \\ &\quad + \frac{P_O}{V_2}\frac{1}{\sqrt{\frac{C_e}{L_e}} - \frac{\pi(n+1)C_e}{2T_s}\left(1 - \frac{2}{\pi}\right)}. \end{aligned} \tag{a6}$$

Equation (a7) is true when (29) is assumed, which is equal to (32)

$$\begin{aligned} &v_{ds2\,\max} = v_{ds1\,\max} \\ &\quad = v_{ds\,\max} = \frac{P_O}{V_2}\frac{1}{\sqrt{\frac{C_e}{L_e}} - \frac{\pi(n+1)C_e}{2T_s}\left(1 - \frac{2}{\pi}\right)}. \end{aligned} \tag{a7}$$

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