Investigation on Extending the DC Bus Utilization of a Single-Source Five-Level Inverter With Single Capacitor-Fed H-Bridge Per Phase

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***Abstract*—Enhancement of dc bus voltage utilization for a five-level inverter with single dc source and capacitor-fed H-bridge (CHB) units is investigated in this paper. A carrier-based modulation technique is used for boosting the dc bus utilization, which is established by providing detailed mathematical analysis. The five-level inverter used here is realized by cascading a CHB unit to each phase of a three-level neutral point clamped inverter. The increase in dc bus voltage utilization owes to the pole voltage redundancies offered by CHB units. The floating capacitors of H-bridge units are balanced within a quarter fundamental cycle using the switching state redundancies of pole voltage levels. The aforementioned modulation technique allows the inverter to enhance the dc bus utilization from 0.577 V_{dc} to 0.63 V_{dc} under unity power factor. This enhancement is obtained in the linear modulation range without increasing the dc bus voltage, and thus, the inverter can operate without the presence of low-order harmonics in its phase voltages. The strength of this paper lies in its detailed mathematical analysis for finding out the limiting modulation index and power factor condition in the light of floating capacitor voltage balancing issue. Simulation as well as experimental verification of the modulation scheme is carried out on an induction motor drive under various operating conditions. It is shown that this carrier-based modulation technique is suitable for any single source inverter topology with one CHB unit per phase.**

***Index Terms*—DC bus voltage utilization, floating capacitor (FC), linear modulation, multilevel inverter (MLI), single dc source.**

I. Introduction

THE advancement of multilevel inverters (MLIs) has diminished the role of two-level inverters in medium-voltage motor drive and power quality applications due to their numerous advantages like lower *dv/dt* output voltage, smaller common-mode voltage, less harmonic distortion, reduced filter size, and higher efficiency [1]–[3]. Diode-clamped, capacitor-clamped, and cascaded H-bridge are the three basic MLI topologies. Capacitor-clamped and cascaded H-bridge MLIs require large number of flying capacitors and isolated dc sources, respectively. Three-level diode-clamped, also known as neutral

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utilize two capacitor-fed H-bridge (CHB) units per phase for extending the dc bus utilization, hence requiring ten asymmetric switches per phase. Moreover, a proper mathematical analysis for establishing the improvement in utilization is absent in the paper.

This paper is an investigation on the possibility to increase dc bus voltage utilization of five-level three-phase MLIs having single CHB unit per phase. Though it is previously found in [24] that addition of CHB units can increase the dc bus utilization, this paper aims at improving the dc bus utilization using a single CHB unit per phase. The modulation technique proposed in this paper for increasing the dc bus utilization is applicable for all single-source three-phase five-level MLIs having single CHB unit per phase. Here, the principle of this modulation technique is demonstrated with the help of MLI topology proposed in [25] by Davis *et al.* The major contributions of this paper are summarized as follows.

1) To increase the dc bus voltage utilization of the inverter nearly to that of a six-step mode of operation using a single CHB unit per phase. The additional utilization is achieved in the linear modulation range by operating the inverter as a seven-level inverter (explained in Sections II and III). This operation in the linear modulation range eliminates low-order harmonics in the inverter phase voltages up to $0.63\,V_{dc}$ at u.p.f.
2) A detailed mathematical analysis is carried out in Sections II-D and II-E to establish the viability of the modulation scheme for improving the dc bus utilization. This gives more insight into the limiting conditions of modulation index and power factor during the steady-state seven-level operation.
3) The advantage mentioned in the first point is achieved by using minimum number of switching devices and floating capacitors (FCs). Less number of switching devices leads to lower switching losses and gate driver requirements. Moreover, optimal use of FCs reduces the requirement for voltage sensor circuits and complexity in capacitor voltage balancing technique.

The feasibility of the above-mentioned modulation scheme is verified by extensive simulation studies. A lab prototype of the inverter-fed induction motor (IM) drive is built for experimental validation of the modulation scheme.

II. Inverter Topology

A. Configuration

The five-level three-phase MLI used in this paper is shown in Fig. 1. A brief description of this MLI, which is previously proposed in [25], is provided here for the sake of convenience to the readers. The inverter has an NPC front end supplied by a single dc source V_{dc}. The primary unit of the inverter is a three-level structure that uses a bidirectional switch to clamp to the neutral point "O" between the two dc bus capacitors C_{d1} and C_{d2}. The presence of the NPC front end helps in the natural balancing of dc bus capacitors. An H-bridge unit with the FC is connected in series with each leg of the three-level unit to increase the number of voltage levels.

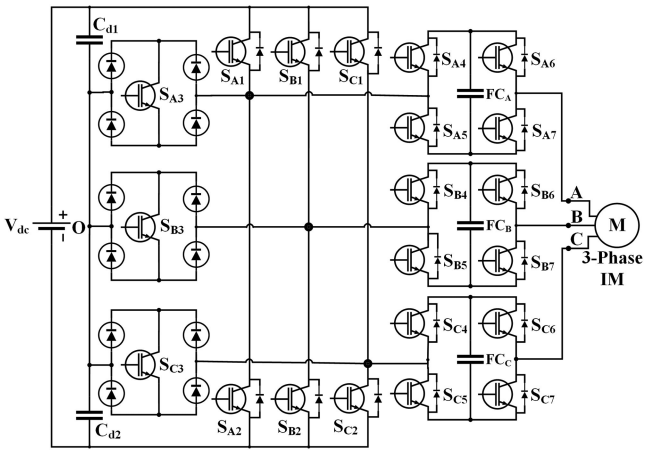

Fig. 1. Configuration of the three-phase five-level inverter.

TABLE I
Switching States of the Inverter

Pole Voltage V_{XO}	Switching States							State of FC_x	
	S_{X1}	S_{X2}	S_{X3}	S_{X4}	S_{X5}	S_{X6}	S_{X7}	$i_X > 0$	$i_X < 0$
$3V_{dc}/4$	1	0	0	0	1	1	0	↓	↑
$V_{dc}/2$	1	0	0	1	0	1	0	–	–
	1	0	0	0	1	0	1		
$V_{dc}/4$	1	0	0	1	0	0	1	↑	↓
	0	0	1	0	1	1	0	↓	↑
0	0	0	1	1	0	1	0	–	–
	0	0	1	0	1	0	1		
$-V_{dc}/4$	0	0	1	1	0	0	1	↑	↓
	0	1	0	0	1	1	0	↓	↑
$-V_{dc}/2$	0	1	0	1	0	1	0	–	–
	0	1	0	0	1	0	1		
$-3V_{dc}/4$	0	1	0	1	0	0	1	↑	↓

X denotes phase A,B, or C; '1'- switch is on; '0' - switch is off
'↓' - Discharging; '↑' - Charging; '—' - No Change

The voltage across floating capacitors FC_A, FC_B, and FC_C is maintained at one-fourth of the dc supply voltage. This enables the inverter to generate voltage levels at a step size of $V_{dc}/4$. Table I shows the possible switching states of the inverter. It can be seen from Table I that except for pole voltage levels $3\,V_{dc}/4$ and $-3\,V_{dc}/4$, there are redundant switching states for all other pole voltage levels. Due to the absence of redundant states, the pole voltage levels $3\,V_{dc}/4$ and $-3\,V_{dc}/4$ are not utilized for all operating conditions and the inverter is regarded as a five-level inverter.

B. Five-Level Operation

Level-shifted PWM is used to generate gating pulses for the inverter switches. For a five-level inverter, four level-shifted triangular carriers are required, which are compared with the sinusoidal reference voltage waveform to generate the required pulses. The pole voltage levels $V_{dc}/2$, 0, and $-V_{dc}/2$ have no effect on FC voltage. During the pole voltage levels $V_{dc}/4$ and $-V_{dc}/4$, the FC may be either charged or discharged depending on the load current direction, as shown in Table I. To obtain

a five-level pole voltage waveform, it is important to keep the FC voltages within a tolerance band around $\mathrm{V_{dc}}/4$. For this, the redundant states for the pole voltage levels $\mathrm{V_{dc}}/4$ and $-\mathrm{V_{dc}}/4$ need to be properly selected and executed by a modulation technique.

Voltage balancing of the FC using redundant states is discussed in [26] and [27]. This requires information about the load current polarity and status of FC voltage. Based on acceptable FC voltage ripple, the controller has to fix an upper and lower voltage limit for the FC voltage tolerance band. If the FC voltage falls below the lower limit, the redundant state for charging the capacitor is applied, taking into account the load current polarity. Similarly, if the FC voltage rises above the upper limit, redundant state for discharging the capacitor is applied. Therefore, it is possible to balance the FCs at pole voltage levels $\mathrm{V_{dc}}/4$ and $-\mathrm{V_{dc}}/4$ for different load conditions. Thus, the inverter is capable of working as a five-level inverter under all operating conditions during the entire range of linear modulation.

C. Seven-Level Operation

Seven-level operation of the inverter requires extreme pole voltage levels $3\,\mathrm{V_{dc}}/4$ and $-3\,\mathrm{V_{dc}}/4$ along with other pole voltage levels used for five-level operation. During pole voltage levels $3\,\mathrm{V_{dc}}/4$ and $-3\,\mathrm{V_{dc}}/4$, voltage balancing of the FC is not likely to achieve for all load conditions due to the absence of redundant switching states. However, seven-level operation of the inverter is possible with restrictions imposed either on modulation index or load power factor.

In the following sections, m_a^5 and m_a^7 represent the modulation index during five-level and seven-level operation, respectively. If reference pole voltage peak is denoted as $\hat{V}_{\mathrm{ref}}$, then $m_a^5 = \hat{V}_{\mathrm{ref}}/(\mathrm{V_{dc}}/2)$ during the five-level mode, and $m_a^7 = \hat{V}_{\mathrm{ref}}/(3\,\mathrm{V_{dc}}/4)$ during the seven-level mode.

D. Limiting Conditions for Seven-Level Operation

U.P.F. is the worst condition for FC voltage balancing during seven-level operation at modulation indices near to 1.15. As the modulation index reduces from 1.15, the influence of pole voltage levels $3\,\mathrm{V_{dc}}/4$ and $-3\,\mathrm{V_{dc}}/4$ on FC voltage balancing reduces. Therefore, seven-level operation is possible at u.p.f. below a particular value of modulation index. A detailed mathematical analysis is shown below to find out the limiting value of modulation index that determines the modulation range of a seven-level inverter for all load conditions. The analysis is carried out for a single-phase circuit of the five-level inverter during steady-state operation.

Fig. 2 shows the seven-level sinusoidal PWM (SPWM) waveform of pole voltage V_{XO} and load current i_{X} along with FC voltage V_{FC} corresponding to the limiting condition of modulation index at u.p.f.. θ_1 and θ_2 are the angles at which the fundamental reference pole voltage V_{ref} is equal to $\mathrm{V_{dc}}/4$ and $\mathrm{V_{dc}}/2$, respectively. V_{ref}, θ_1, and θ_2 are defined as follows, where m_a^7 and ω are the modulation index and angular frequency of the fundamental reference wave, respectively

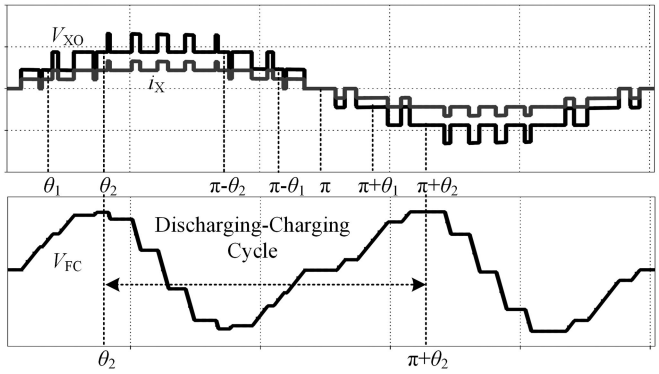

Fig. 2. PWM waveform of pole voltage V_{XO} and load current i_{X} with FC voltage V_{FC}.

$$V_{\mathrm{ref}} = m_a^7 \frac{3\mathrm{V_{dc}}}{4} \sin(\omega t) \tag{1}$$

$$\theta_1 = \sin^{-1}\left(1/3\,m_a^7\right) \tag{2}$$

$$\theta_2 = \sin^{-1}\left(2/3\,m_a^7\right). \tag{3}$$

For FC voltage balancing, only pole voltage levels $\mathrm{V_{dc}}/4$, $-\mathrm{V_{dc}}/4$, $3\mathrm{V_{dc}}/4$, and $-3\,\mathrm{V_{dc}}/4$ are relevant. The PWM duty ratios of these pole voltage levels are designated as d^1, d^{-1}, d^3, and d^{-3}, respectively, and they are expanded as follows:

$$d^1 = \begin{cases} 3\,m_a^7 \sin\omega t, & 0 \le V_{\mathrm{ref}} \le \mathrm{V_{dc}}/4 \\ 2 - 3\,m_a^7 \sin\omega t, & \mathrm{V_{dc}}/4 < V_{\mathrm{ref}} \le \mathrm{V_{dc}}/2 \end{cases} \tag{4}$$

$$d^{-1} = \begin{cases} -3\,m_a^7 \sin\omega t, & -\mathrm{V_{dc}}/4 \le V_{\mathrm{ref}} \le 0 \\ 2 + 3\,m_a^7 \sin\omega t, & -\mathrm{V_{dc}}/2 \le V_{\mathrm{ref}} < -\mathrm{V_{dc}}/4 \end{cases} \tag{5}$$

$$d^3 = -2 + 3\,m_a^7 \sin\omega t, \quad \mathrm{V_{dc}}/2 \le V_{\mathrm{ref}} \le 3\mathrm{V_{dc}}/4 \tag{6}$$

$$d^{-3} = -2 - 3\,m_a^7 \sin\omega t, \quad -3\mathrm{V_{dc}}/4 \le V_{\mathrm{ref}} \le -\mathrm{V_{dc}}/2. \tag{7}$$

At the u.p.f. limiting condition, FC is continuously charged during pole voltage levels $\mathrm{V_{dc}}/4$ and $-\mathrm{V_{dc}}/4$ (by using appropriate redundant switching states, as shown in Table I) to compensate for its discharge during pole voltage levels $3\,\mathrm{V_{dc}}/4$ and $-3\,\mathrm{V_{dc}}/4$, as shown in Fig. 2. This implies that the decrement in FC voltage ΔV_d must be equal to the increment in FC voltage ΔV_c. There are two discharging–charging cycles of FC present in a fundamental period of the reference pole voltage. The increment and decrement in FC voltage can be expressed using (8) and (9), respectively, where *C* represents the FC value. The load current magnitude is proportional to the corresponding pole voltage level at u.p.f, and it is taken as "I" at pole voltage level $\mathrm{V_{dc}}/4$. Here, the period from θ_2 to $\pi + \theta_2$ (one discharging–charging cycle) is considered for analysis in which θ_2 to $\pi - \theta_2$ is the discharging period and $\pi - \theta_2$ to $\pi + \theta_2$ is the charging period. On further simplification, (8) and (9) can be reduced to expressions given in (10) and (11), respectively,

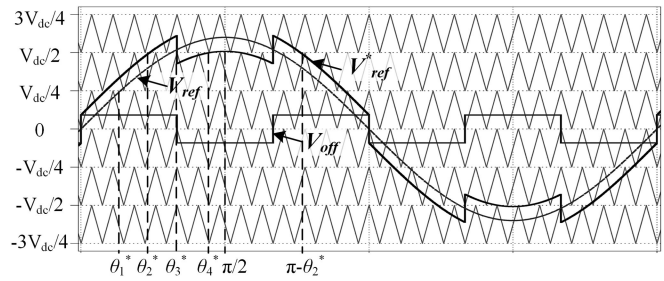

Fig. 3. Voltage references V_{ref} and V_{ref}^* along with square-wave offset V_{off} and triangular carriers.

as follows:

$$\Delta V_c = \frac{1}{C}\left[\int_{\frac{\pi-\theta_2}{\omega}}^{\frac{\pi}{\omega}} I \times d^1 dt + \int_{\frac{\pi}{\omega}}^{\frac{\pi+\theta_2}{\omega}} I \times d^{-1} dt\right] \tag{8}$$

$$\Delta V_d = \frac{1}{C}\int_{\frac{\theta_2}{\omega}}^{\frac{\pi-\theta_2}{\omega}} 3I \times d^3 dt \tag{9}$$

$$\Delta V_c = \frac{2I}{\omega C}\left[2(\theta_2-\theta_1) + 3\,m_a^7(\cos\theta_2 - 2\cos\theta_1 + 1)\right] \tag{10}$$

$$\Delta V_d = \frac{6I}{\omega C}\left[2\theta_2 - \pi + 3\,m_a^7\cos\theta_2\right]. \tag{11}$$

Since $\Delta V_c = \Delta V_d$, the expressions in (10) and (11) are equated to obtain (12), which corresponds to the limiting condition at u.p.f. It is observed from the following equation that the limiting condition is independent of the magnitude of load current, FC value, and frequency of the reference waveform

$$6m_a^7(\cos\theta_1 + \cos\theta_2) + 2(2\theta_2 + \theta_1) - 3(\pi + m_a^7) = 0. \tag{12}$$

After solving (2), (3). and (12), the limiting value of modulation index at u.p.f. is obtained as 0.8014. Therefore, the linear modulation range of seven-level operation is limited to 0.8014 for all load conditions using the SPWM technique.

The floating capacitance value *C* has to be suitably selected based on the maximum peak load current and allowable voltage ripple. The optimal value of *C* can be found out either from (10) or (11) with the maximum allowable FC voltage ripple as ΔV_c or ΔV_d.

E. Extension of the Linear Modulation Range During Seven-Level Operation

The linear modulation range of seven-level operation can be extended from $m_a^7 = 0.8014$ by adding a square-wave common-mode voltage V_{off} to the reference sine wave V_{ref}. In [24], the addition of square-wave offset is suggested for inverters having at least two CHB units per phase. Here, the possibility to extend the linear modulation range of inverters having single CHB unit per phase is analyzed.

Fig. 3 illustrates the resultant reference waveform V_{ref}^* obtained after square wave addition for $m_a^7 = 0.8014$. The new reference waveform V_{ref}^* allows intermittent charging and discharging of FC during the period θ_2^* to $\pi - \theta_2^*$ due to the switching of pole voltage levels $\text{V}_{\text{dc}}/4$ and $3\,\text{V}_{\text{dc}}/4$. This is unlike the case shown in Fig. 2 where a continuous discharge of FC happens during the period θ_2 to $\pi - \theta_2$. Therefore, the addition of square-wave offset helps in the balancing of FC with lower voltage ripple. This feature facilitates the extension of modulation index from 0.8014.

It is required to find the optimum magnitude of square-wave offset that can maximize the modulation range extension. High magnitude of square-wave may result in overmodulation, whereas low magnitude may not enhance the intermittent charging–discharging feature. A quarter fundamental cycle is considered here to determine the optimum value of square-wave offset and extended limiting value of modulation index. The calculations required for finding out the limiting value of m_a^7 is similar to that explained in Section II-D. The expressions for angles $\theta_1^*, \theta_2^*, \theta_4^*$ shown in Fig. 3 are given in (13)–(15), respectively, where θ_1^* corresponds to the angle at which $V_{\text{ref}}^* = \text{V}_{\text{dc}}/4$, and θ_2^*, θ_4^* correspond to the angles at which $V_{\text{ref}}^* = \text{V}_{\text{dc}}/2$. However, the angle θ_3^* shown in the figure is always equal to 60°.

$$\theta_1^* = \sin^{-1}((1 - \text{V}_{\text{off}})/3\,m_a^7) \tag{13}$$

$$\theta_2^* = \sin^{-1}((2 - \text{V}_{\text{off}})/3\,m_a^7) \tag{14}$$

$$\theta_4^* = \sin^{-1}((2 + \text{V}_{\text{off}})/3\,m_a^7). \tag{15}$$

d^{1*} and d^{3*} are the modified PWM duty ratios for pole voltage levels $\text{V}_{\text{dc}}/4$ and $3\,\text{V}_{\text{dc}}/4$, which are expanded, respectively, as follows:

$$d^{1*} = \begin{cases} 3\,m_a^7\sin\omega t + \text{V}_{\text{off}}, & 0 \le \theta \le \theta_1^* \\ -3\,m_a^7\sin\omega t - \text{V}_{\text{off}} + 2, & \theta_1^* < \theta \le \theta_2^* \\ -3\,m_a^7\sin\omega t + \text{V}_{\text{off}} + 2, & \theta_3^* \le \theta \le \theta_4^* \end{cases} \tag{16}$$

$$d^{3*} = \begin{cases} 3\,m_a^7\sin\omega t + \text{V}_{\text{off}} - 2 \text{ for } \theta_2^* \le \theta \le \theta_3^* \\ 3\,m_a^7\sin\omega t - \text{V}_{\text{off}} - 2 \text{ for } \theta_4^* \le \theta \le \pi/2. \end{cases} \tag{17}$$

The new increment (ΔV_c^*) and decrement (ΔV_d^*) in FC voltage is found by integration of load current during the respective pole voltage levels $\text{V}_{\text{dc}}/4$ and $3\,\text{V}_{\text{dc}}/4$. Since ΔV_c^* and ΔV_d^* shown in (18) and (19) need to be equal, they are equated to obtain the new limiting condition given in (20), as follows:

$$\begin{aligned}\Delta V_c^* = \frac{I}{\omega C}\big[&3\,m_a^7(0.5 - 2\cos\theta_1^* + \cos\theta_2^* + \cos\theta_4^*) \\ &+ \text{V}_{\text{off}}(2\theta_1^* - \theta_2^* + \theta_4^* - \pi/3) \\ &- 2(\theta_1^* - \theta_2^* - \theta_4^* + \pi/3)\big]\end{aligned} \tag{18}$$

$$\begin{aligned}\Delta V_d^* = \frac{3I}{\omega C}\big[&3\,m_a^7(-0.5 + \cos\theta_2^* + \cos\theta_4^*) \\ &- \text{V}_{\text{off}}(\theta_2^* - \theta_4^* + \pi/6) \\ &+ 2(\theta_2^* + \theta_4^* - 5\pi/6)\big]\end{aligned} \tag{19}$$

$$\begin{aligned}&6\,m_a^7(1 - \cos\theta_1^* - \cos\theta_2^* - \cos\theta_4^*) \\ &\quad + \text{V}_{\text{off}}(2\theta_1^* + 2\theta_2^* - 2\theta_4^* + \pi/6) \\ &\quad - 2(\theta_1^* + 2\theta_2^* + 2\theta_4^* - 13\pi/6) = 0.\end{aligned} \tag{20}$$

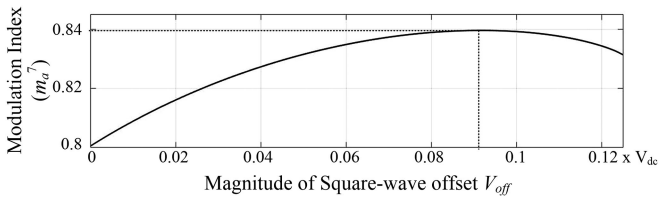

Fig. 4. Limiting value of modulation index m_a^7 for various magnitudes of square-wave offset $V_{\rm off}$.

Here, the limiting condition is represented by a single equation given by (20) with two unknown parameters m_a^7 and $V_{\rm off}$, which result in multiple solution sets. It is required to find that solution which maximizes the modulation index m_a^7. Since an explicit solution cannot be determined analytically, the equation is solved for various values of $V_{\rm off}$. The results are illustrated graphically in Fig. 4. As the offset magnitude is increased, the limiting modulation index increases until a critical value is reached, and thereafter it reduces. It is found that the maximum value of m_a^7 is obtained for $V_{\rm off} = 0.09175\,\mathrm{V_{dc}}$. Hence, the optimum value of square-wave magnitude to be added is $0.09175\,\mathrm{V_{dc}}$ and the corresponding value of m_a^7 is 0.8396. Thus, the linear modulation range of extended seven-level operation is up to 0.8396 using square-wave offset addition. Based on the above-mentioned analysis, the following section will show that the dc bus utilization of five-level inverters having single CHB unit per phase can be increased to a value closer to that of its six-step mode operation.

III. Increase in DC Bus Voltage Utilization

The maximum fundamental phase voltage peak of a single-source MLI operating in the linear modulation region is equal to $0.577\,\mathrm{V_{dc}}$, where $\mathrm{V_{dc}}$ is the dc bus voltage of the inverter. The inverter used in this paper can achieve $0.577\,\mathrm{V_{dc}}$ as phase voltage peak for all load conditions when operated in the five-level mode. In the case of the extended seven-level mode (as in Section II-E), the linear modulation range is limited to $m_a^7 = 0.8396$. Therefore, the maximum fundamental phase voltage peak of the inverter during seven-level operation is given by

$$V_{\mathrm{ph(peak)\,max}\,7L} = 0.8396\left(\frac{\mathrm{V_{dc}}}{2} + \frac{\mathrm{V_{dc}}}{4}\right) = 0.63\,\mathrm{V_{dc}}. \quad (21)$$

It is found from (21) that with the limited modulation range, seven-level operation of the inverter can achieve 9.18% higher phase voltage peak than five-level operation. This enhancement enables the inverter to operate near to the phase voltage peak of six-step mode operation of the five-level inverter (i.e., $0.637\,\mathrm{V_{dc}}$), but without adding low-order harmonics in the phase voltages. Alternatively, the dc bus voltage rating of the inverter can be reduced by 9.18%, keeping phase voltage peak equal to $0.577\,\mathrm{V_{dc}}$. For IM drive applications where u.p.f. is never the case, the improvement can be more than 9.18%, as shown in Section V. A space vector diagram depicting the linear modulation range of five-level and extended seven-level operation of the inverter is shown in Fig. 5. The linear operating range of the five-level mode is represented by the region inside the innermost circle in the figure, where $\mathrm{OA} = \mathrm{V_{dc}}$ and vector $V_1 = 0.866\,\mathrm{V_{dc}}$ represents the maximum reference voltage possible during the five-level mode. The inclusion of pole voltage levels $3\,\mathrm{V_{dc}}/4$ and $-3\,\mathrm{V_{dc}}/4$ during the seven-level mode increases the length of the OA-axis by $\mathrm{V_{dc}}/2$, which is represented as $\mathrm{OA}' = \mathrm{V_{dc}} + \mathrm{V_{dc}}/2$. For low power factor applications, it is possible for the inverter to operate in the entire region inside the outermost circle ($V_2 = 1.299\,\mathrm{V_{dc}}$). However, considering all load conditions including u.p.f., the linear operating range is restricted within the dotted circle ($V_3 = 0.948\,\mathrm{V_{dc}}$).

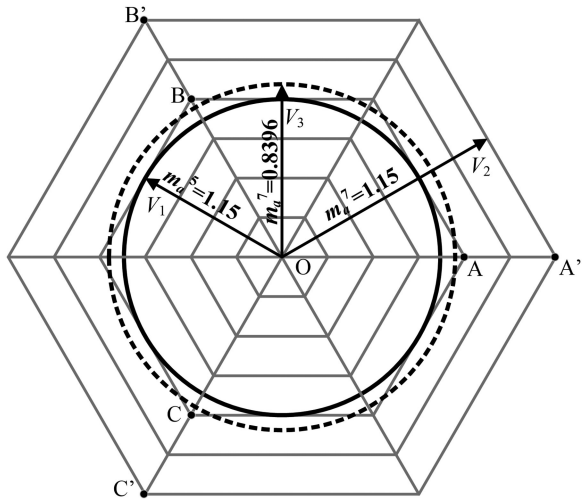

Fig. 5. Space-vector diagram of the inverter having single CHB unit per phase.

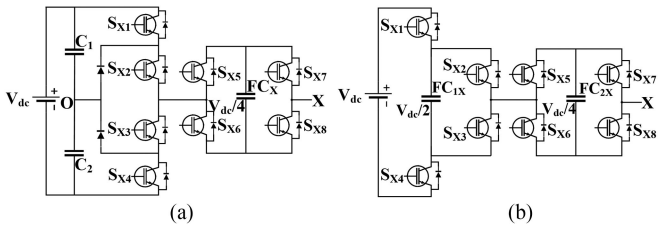

Fig. 6. Inverter topologies having single CHB unit per phase with primary unit as (a) NPC MLI [16] and (b) three-level FC MLI [17].

The modulation scheme described in Sections II-D and II-E is equally applicable for other inverter topologies fed with a single source and using single CHB unit per phase. The single-phase structure of two such inverter topologies is shown in Fig. 6(a) and (b), where a CHB unit is connected in series with an NPC inverter and three-level FC MLI, respectively [16], [17]. Table II illustrates comparison amongst different five-level topologies using the same dc bus voltage rating. It is observed from the table that topologies in [16] and [25] use optimal number of switches and capacitors when compared to the topologies in [17] and [24]. However, they use four and two clamping diodes per phase, respectively. It is also found that the topologies in [24] and [25] require two higher voltage rated switches per phase, whereas the capacitor voltage ratings are the same among all the listed topologies. The criteria for selection of the topol-

TABLE II
COMPARISON OF FIVE-LEVEL TOPOLOGIES

Topology	DC bus utilization	CHBs per phase	FCs per phase	DC bus Capacitors per phase	Total Capacitors	No. of Capacitors w.r.t rating		Total Switches per phase	Bidirectional Switches per phase	No. of Switches w.r.t rating				Clamping Diodes per phase	Rating of clamping diodes
						$V_{dc}/2$	$V_{dc}/4$			V_{dc}	$3V_{dc}/4$	$V_{dc}/2$	$V_{dc}/4$		
In [25]	Up to $0.63V_{dc}$	1	1	2	5	2	3	7	1	2	-	1	4	4	$V_{dc}/4$
In [16]	Up to $0.63V_{dc}$	1	1	2	5	2	3	8	0	-	-	4	4	2	$V_{dc}/2$
In [17]	Up to $0.63V_{dc}$	1	2	-	6	3	3	8	0	-	-	4	4	-	-
In [24]	Up to $0.633V_{dc}$	2	2	-	6	3	3	10	0	2	-	4	4	-	-
In [15]	Up to $0.577V_{dc}$	-	1	2	5	2	3	7	0	-	2	2	3	2	$V_{dc}/4$

TABLE III
SIMULATION PARAMETERS

Parameter	Specification
Input DC Voltage, V_{dc}	350 V
DC Bus Capacitors, C_{d1} and C_{d2}	2200 μF
Floating Capacitor, FC	2200 μF
Switching Frequency, f_s	1.35 kHz
FC Voltage, V_{FC}	87.5 V
FC Voltage Tolerance Band	3 V
Induction Motor, IM	4 kW, 400 V, 10 A

ogy depends on the power requirement and the device count. If power rating of the inverter is the major concern, topologies in [16] and [17] are more preferable as the voltage stress across the switches is comparatively lower than other topologies. If optimization of switching devices and capacitors is considered, then topology in [25] can be preferred. It is also observed from Table II that topology in [15] has lower device count and uses lower voltage rated switches than in [25], but the extension of dc bus utilization is not possible due to the absence of CHB units.

IV. SIMULATION RESULTS

The feasibility of the presented modulation scheme for inverters having single CHB unit per phase is verified using PLECS (version 4.1) simulation environment. Simulation studies are performed on the inverter topology proposed in [25], for an IM drive operating at different modulation indices and p.f. conditions. The parameters used for simulation are listed in Table III.

The steady-state waveforms of the inverter during five-level, seven-level (see Section II-D), and extended seven-level operation (see Section II-E) at high and low p.f. are shown in Fig. 7(a), (b), (c), and (d), respectively. During five-level operation, FC voltage is controlled and kept within the tolerance band, whereas in the case of seven-level and extended seven-level operation, controlled FC voltage may go outside the specified tolerance band depending on load current and power factor. However, the FC voltage ripple is within allowable limits, as shown in the zoomed view in Fig. 7(b) and (c). When the motor is lightly loaded (low p.f.), the inverter can operate up to a modulation index of 1.15, as shown in Fig. 7(d). The harmonic spectrum of line voltage for extended seven-level and six-step operation is shown in Fig. 8(a) and (b), respectively. It is evident that six-step operation results in fifth and seventh harmonics in the inverter output voltage, which are negligible in the case of extended seven-level operation.

The dynamic performance of the inverter during extended seven-level operation is shown in Fig. 9. In Fig. 9(a), the modulation index and frequency are linearly varied from 0.1 to 0.8396 (5.95–50 Hz) for a fixed load. It is seen from the figure that no precharging circuit is required for the FC during starting, as it automatically charges to the set voltage level. In Fig. 9(b), the transient operation of the inverter under sudden load variation is illustrated. Both the dc bus capacitor voltages and the FC voltage remain controlled during the entire transient period. The dc bus capacitor voltages remain balanced with the help of a neutral point potential (NPP) balancing algorithm proposed in [28].

V. EXPERIMENTAL RESULTS

A laboratory prototype of the inverter is built using SEMIKRON IGBT modules and SKYPER 32 PRO gate driver boards. The generation of switching signals and capacitor voltage balancing is implemented in TI DSP-TMS320F28335 based controller board. The dc bus capacitor voltages, FC voltages, and load currents are sensed and feedback to ADC channels of DSP for the balancing of capacitor voltages. The input dc voltage applied to the lab prototype is 200 V and the FC voltage is balanced at 50 V. Switching frequency used is 1.25 kHz. All other parameters are the same, as given in Table III. A 5-hp, 415 V, 7.5 A IM is connected as load and the performance of the inverter with open-loop *V/f* control is tested at the no-load condition for different values of modulation indices. Fig. 10 shows the test setup of the IM drive.

The steady-state waveforms of the inverter during five-level operation are shown in Fig. 11 for $m_a^5 = 1.15, 0.6$, and 0.2. The peak line voltage at $m_a^5 = 1.15$ is approximately 200 V.

Fig. 12 shows the steady-state waveforms of the inverter during seven-level operation for $m_a^7 = 1.15, 0.6$, and 0.2. Since the motor is running at the no-load condition (low p.f.), the linear

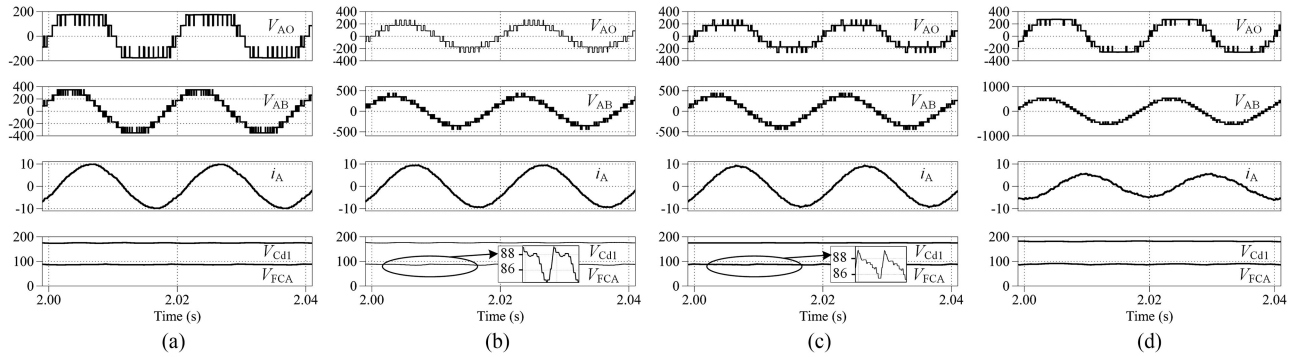

Fig. 7. Simulation results showing the steady-state waveforms of pole voltage V_{AO}, line voltage V_{AB}, line current i_A, dc bus capacitor voltage V_{Cd1}, and FC voltage V_{FCA} during (a) five-level operation at $m_a^5 = 1.15$, $f = 50$ Hz, (b) seven-level operation at $m_a^7 = 0.8$, $f = 50$ Hz, (c) extended seven-level operation at $m_a^7 = 0.8396$, $f = 50$ Hz, and (d) extended seven-level operation at $m_a^7 = 1.15$, $f = 50$ Hz.

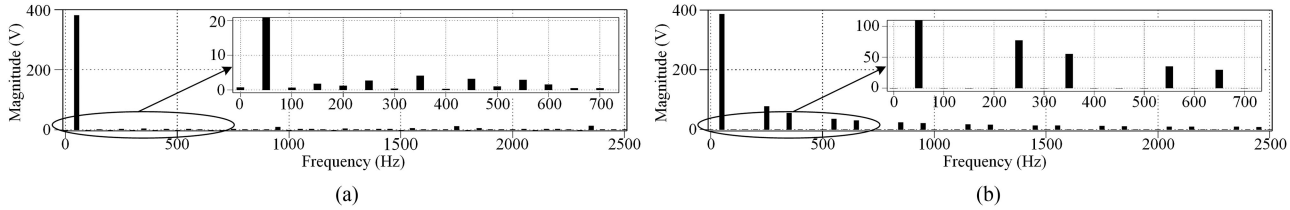

Fig. 8. Harmonic spectrum of line voltage at $f = 50$ Hz during (a) extended seven-level operation for $m_a^7 = 0.8396$ and (b) six-step operation of the five-level inverter.

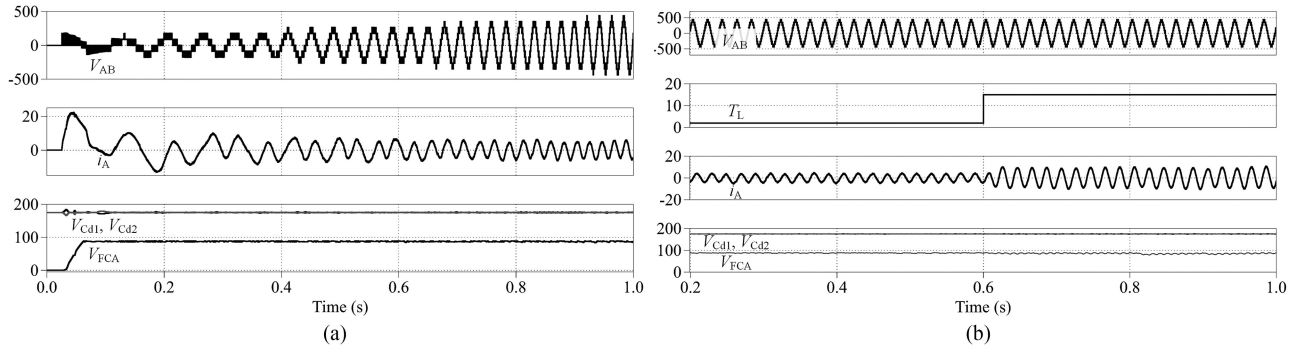

Fig. 9. Simulation results showing the transient waveforms of line voltage V_{AB}, line current i_A, dc bus capacitor voltages V_{Cd1} and V_{Cd2}, FC voltage V_{FCA}, and load torque T_L during extended seven-level operation of the inverter. (a) When m_a^7 and frequency is varied proportionally from 0.1 to 0.8396 and 5.95 to 50 Hz. (b) When T_L is changed from 2 to 15 Nm at $m_a^7 = 0.8396$.

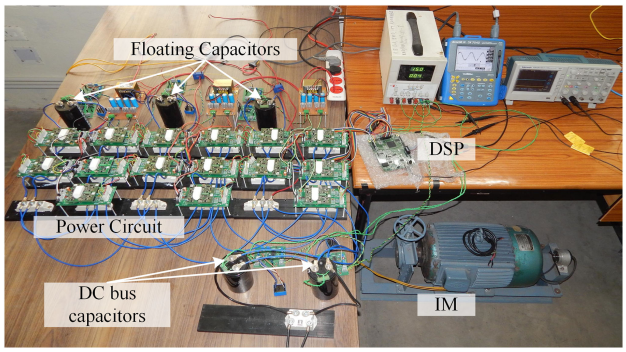

Fig. 10. Laboratory setup of the inverter-fed IM drive.

modulation range of the inverter can be extended up to 1.15. The peak line voltage at $m_a^7 = 1.15$ is approximately 298 V. This is 50% greater than that obtained during the five-level mode. Fig. 13 shows the harmonic spectrum of line voltage at $m_a^7 = 1.15$ having a percentage total harmonic distortion (THD) equal to 6.33%. The low-order harmonics shown in the zoomed view of the figure may be considered as trivial.

Fig. 14 illustrates *V/f* operation of the motor for $m_a^7 = 0.2$–1.15 (8.7–50 Hz) at the no-load condition. The use of the NPP balancing technique in [28] helps to keep the dc bus capacitor voltages balanced at 100 V. The NPP variation V_O is very small, as shown in Fig. 14, which proves the balancing of dc bus capacitor voltages. The voltages across the FCs also remain balanced at 50 V during the entire transient period.

From the analytical analysis discussed in Section II-E, it is found that the limiting value of modulation index for achieving the desired dc bus utilization of 0.63 V_{dc} at u.p.f. is 0.8396. This is experimentally verified by connecting the inverter to a resistive load and the modulation index is increased linearly from 0.75 to 0.85 and then reduced back to 0.75. This is illustrated

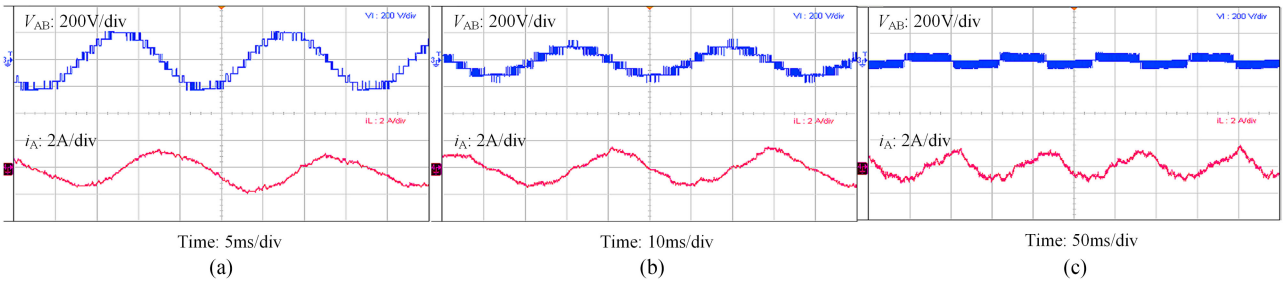

Fig. 11. Steady-state waveforms of line voltage V_{AB} and line current i_A during five-level operation at (a) $m_a^7 = 1.15$ (50 Hz), (b) $m_a^7 = 0.6$ (26 Hz), and (c) $m_a^7 = 0.2$ (8.7 Hz).

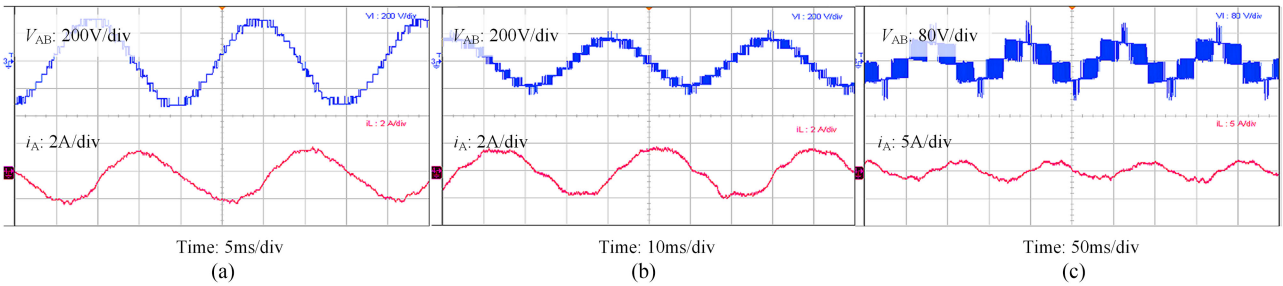

Fig. 12. Steady-state waveforms of line voltage V_{AB} and line current i_A during seven-level operation at (a) $m_a^7 = 1.15$ (50 Hz), (b) $m_a^7 = 0.6$ (26 Hz), and (c) $m_a^7 = 0.2$ (8.7 Hz).

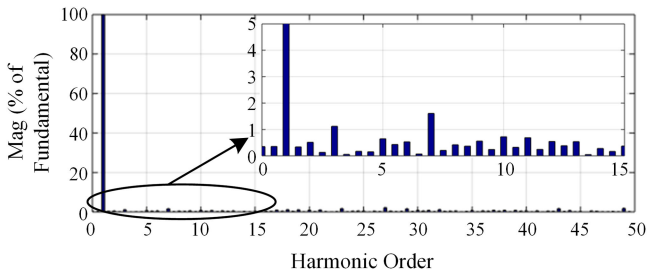

Fig. 13. Harmonic spectrum of line voltage at $m_a^7 = 1.15$ and $f = 50$ Hz during seven-level operation.

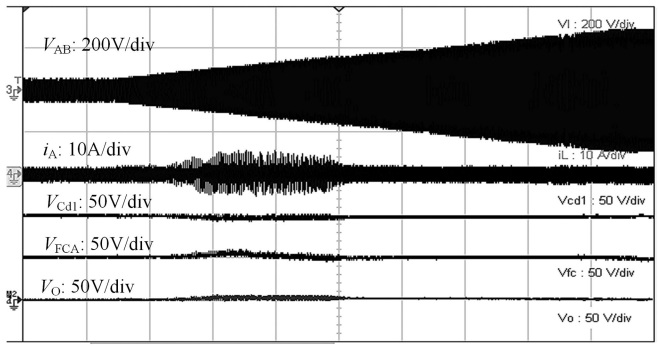

Fig. 14. Transient performance of the IM drive during seven-level operation when m_a^7 is varied from 0.2 to 1.15. Time: 6 s/div.

using Fig. 15(a) where the FC voltage remains balanced at 50 V below modulation index $m_a^7 = 0.83$, which is close to the theoretical limit. The steady-state waveforms during $m_a^7 = 0.83$ are shown in Fig. 15(b) where the FC voltage ripple is able to stay under controlled charge and discharge limits as shown in the zoomed view.

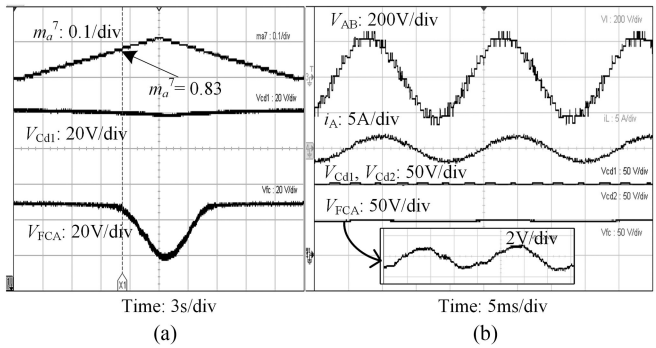

Fig. 15. (a) Modulation index and capacitor voltage waveforms during transient operation around the critical condition. (b) Steady-state waveforms at $m_a^7 = 0.83$.

VI. Conclusion

An investigation on increasing the dc bus utilization of inverters with single dc source and single CHB unit per phase is carried out in this paper. The linear modulation range of these inverters can be extended by using pole voltage redundancies offered by CHB units. From the mathematical analysis, the linear modulation range of the inverter during extended seven-level operation is found to be 0.8396 at unity p.f. without causing any FC voltage unbalance. This results in an improvement in the peak fundamental phase voltage from 0.577 V_{dc} to 0.63 V_{dc}. Although the work done in [24] shows improvement up to 0.633 V_{dc}, but this comes at the cost of extra switches and capacitors (see Table II). The presented modulation scheme can extend the dc bus utilization up to that of a five-level six-step mode of operation $(0.637\ V_{dc})$ for IM drive, where the p.f. is less than unity. It is also shown that at the lightly loaded condition of IM drive,

the inverter is capable of increasing the utilization by 50%. The linear PWM operation of the inverter eliminates low-order harmonics in the motor phase voltages and minimizes torque pulsations. Simulation and experimental results clearly validate the effectiveness of the presented modulation scheme for increasing the dc bus utilization of inverters with single CHB unit per phase.

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