Letters

Heterogeneous Integration of GaN and BCD Technologies and Its Applications to High Conversion-Ratio DC–DC Boost Converter IC

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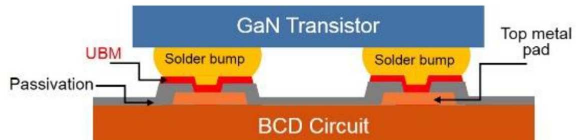
***Abstract*—This letter presents a novel technology for the integration of gallium nitride (GaN) power devices with silicon control circuits. It comprises stacked GaN power transistors and bipolar-CMOS-double-diffused metal-oxide-semiconductor (DMOS) (BCD) circuits. It leverages on both advantages of the high-voltage low-loss GaN devices and the high-integration BCD circuits. Using conventional manufacturing, packaging, and assembly techniques and equipment, the proposed technology is technology transferrable and applicable for commercial power electronic applications. To validate the concept, a 3.3–70 V dc–dc boost converter is designed, implemented, and verified experimentally. It features a conversion efficiency of 70.3%, output power of 1.68 W, and compact size of 0.32 × 0.18 cm^2.**

***Index Terms*—Boost converter, CMOS dc–dc converter complementarymetal-oxide-semiconductor (CMOS), gallium nitride (GaN), heterogeneous integration, high conversion ratio, integrated circuits (ICs).**



I. Introduction

DRIVEN by the advancement of semiconductor technologies and *Moore's Law*, the three-dimensional (3-D) integrated circuits (ICs), especially heterogeneous integration of III–V semiconductors and silicon process, become a hot research area in the past years. Among them, the integration of high-voltage gallium nitride (GaN) semiconductor and silicon (Si) complementary metal–oxide–semiconductor (CMOS) becomes a promising platform for the advanced microsystem developments [1]–[5].

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Fig. 2. Design flow of the GaN2BCD™ technology.

TABLE I
TYPICAL CHARACTERISTICS OF THE EPC2036 GaN FET

Parameter	Test Condition	Typical Value
$R_{DS(ON)}$ (Drain-source on resistance)	$V_{GS} = 5$ V, $I_D = 1$ A	50 mΩ
$V_{GS(TH)}$ (Gate threshold voltage)	$V_{DS} = V_{GS}$, $I_D =$ 0.6 mA	1.4 V
V_{DS_MAX} (Maximum drain-source voltage)	Continuous	100 V

the die-to-wafer transfer (D2W) assembly, followed by associated packaging and system-level testing. The integrated design environment and the entire fabrication process are provided within the GaN2BCD™ technology.

B. GaN Power Transistor

In this prototype, the enhancement mode (normally OFF) EPC2036 GaN FET [9] is selected as the power transistor to validate the proposed technology and design flow, practically. With the enhancement-mode nature, the associated driver circuit can be designed with nominal positive pulsewidth modulation (PWM) signals without additional negative-voltage-generation circuitry [1], [2].

Table I summarizes the typical device characteristics. The small drain-source on resistance $R_{DS(on)}$ of only 50 mΩ is the main advantage to reduce the conduction loss and hence improve the system efficiency. The gate threshold voltage $V_{GS(TH)}$ of 1.4 V provides the circuit design guide for the BCD driver. It is also noted that the device is capable to support converting operation up to 100 V.

Fig. 3 shows the die micrograph of the EPC2036 GaN FET with solder bumps. It has a size of 0.9×0.9 mm^2. It is noted that multiple dies can be connected in parallel for larger conduction current to meet the design requirements.

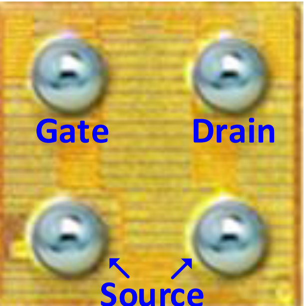

Fig. 3. Micrograph of EPC2036 eGaN FET in passivated die form with solder bumps [9]. (Die size: 0.9×0.9 mm^2.)

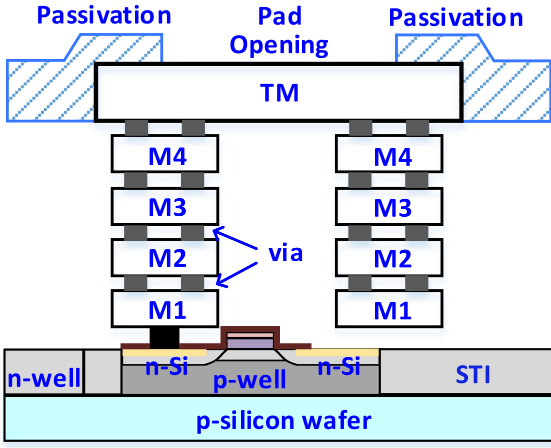

Fig. 4. Cross-sectional back-end-of-line metal stack of the GF's 0.18-μm BCDLite™ process. (STI)

C. BCD Process

The GLOBALFOUNDRIES 0.18-μm BCDLite™ process is used as the driver implementation platform. It features bipolar transistors, 1.8/5-V CMOS MOSFETs, and high-voltage (up to 65 V) laterally diffused metal oxide semiconductor. To cope with the EPC2036 control voltage (nominal $V_{GS} = 5$ V), the 5-V MOSFETs are utilized in implementing the PWM driver. On-chip metal–insulator–metal capacitors and electrostatic discharge circuits are designed and used in the driver implementation. As shown in the cross-sectional metal stack (Fig. 4), the TM is designed with two-pad opening types, i.e., the octagonal opening structure is used as the flip-chip pads soldered to the GaN devices and the square opening structure is used as the wire-bonding pads to the printed evaluation board. The shallow trench isolation (STI) layer mitigates the electric current leakage between the adjacent semiconductor device components, thus enhancing the circuit performance.

D. 3.3–70 V Boost Converter Prototype

To validate the GaN2BCD™ technology, an open-loop 3.3–70 V high conversion-ratio boost converter is designed, fabricated, and measured.

As shown in Fig. 5, the prototype comprises the sawtooth generator and comparator circuits in the BCD process, two EPC2036 GaN devices, and off-the-shelf inductors and

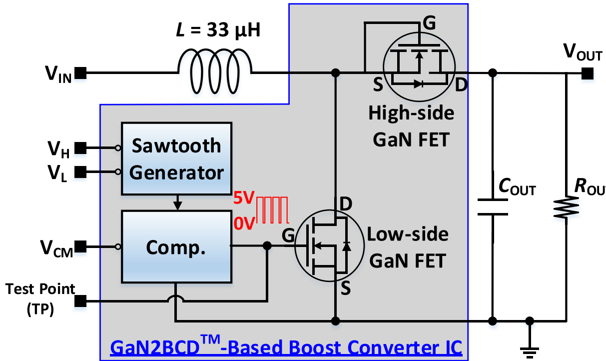

Fig. 5. Schematic of the 3.3–70 V boost converter prototype.

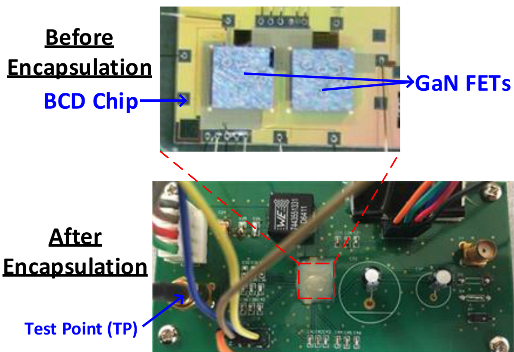

Fig. 6. Photographs of the boost converter prototype IC before encapsulation (top) and its evaluation board (bottom).

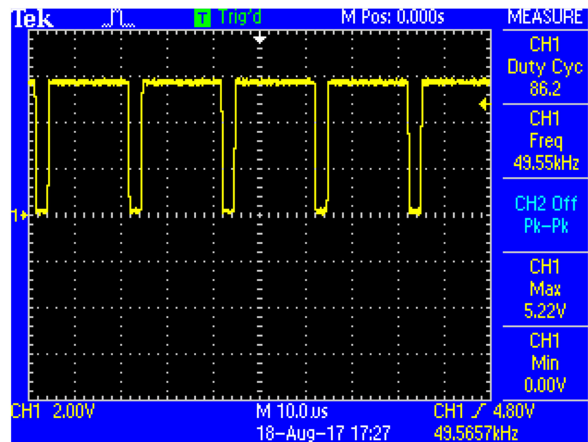

Fig. 7. Measured driving signal example at 86% duty-cycle and 49.5 kHz.

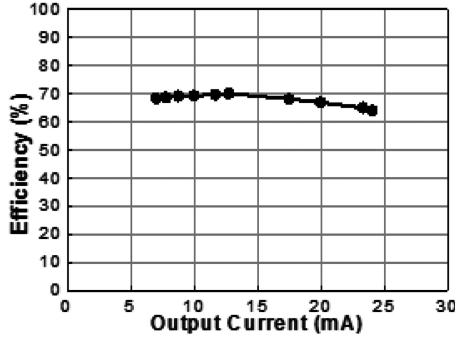

Fig. 8. Measured conversion efficiency versus output current.

capacitors. Following the design procedures in Fig. 2, the sawtooth generator and comparator are first designed to provide the square-wave gate driving signal. External pins V_H and V_L tune the frequency of the sawtooth waveform, which is 9.5–100 kHz in this design. The $V_{\rm CM}$ is the comparison reference of the sawtooth waveform and determines the duty cycle of the driving signal. Using 5-V MOSFET, the circuits provide a 0–5 V rail-to-rail duty-cycle-controllable driver for the power transistors. A testing pin (TP) is reserved to check the functionality of the BCD chips.

The low-side GaN FET is the power transistor, and the high-side one is configured as the boost diode with G–S connection for anode and D for cathode. Off-the-shelf components are used as boost inductor and filtering capacitors. Rheostat and resistor in series are used for testing the output voltages under various output current conditions. After the UBM and D2W assembly, the converter prototype IC is obtained as in Fig. 6. It occupies an area of $0.32 \times 0.18\ \mathrm{cm}^2$ including wire-bonding pads.

The measurement is performed with dc-power supplies and high-impedance oscilloscopes. At normal operation, the BCD driver circuits draw 2.1 mA current from a 5-V supply. Measured at the reserved TP in Figs. 5 and 6, Fig. 7 shows a driving signal example at 86% of the duty cycle and 49.5 kHz generated by the BCD driver. By varying the duty cycle and load resistance, the testing input/output currents are recorded under 3.3 V input and 70 V output voltages. Based on the raw data, the conversion efficiency is calculated and plotted in Fig. 8, which is 63.6%–70.3%. The maximum power delivery capability is 1.68 W.

TABLE II
COMPARISON WITH OTHER INTEGRATED DC–DC BOOST CONVERTERS

Ref	Tech.	Boost Diode	V_{IN}/V_{OUT} (V/V)	$P_{OUT,MAX}$ (W)	η_{MAX} (%)	Area (cm×cm)
[1]	GaN + CMOS + IPD	Int. #	12/18	4.16	47.3	0.94× 0.98
[6]	80 V BCD	OTS *	3.3/80	0.35	53	0.1× 0.1
[7]	80 V BCD	OTS *	3.3/70	0.3	52	not mentioned
This Work	GaN + BCD	Int. #	3.3/70	1.68	70.3	0.32× 0.18

#Integrated.
*Off-the-shelf.

III. COMPARISON AND DISCUSSION

Table II shows the performance comparison with other integrated dc–dc boost converters. This work demonstrates the advantages of high integration level, high conversion ratio, large output power, high efficiency, and compact size. In fact, one key advantage of this heterogeneous integration technology is that the gate driver is placed in very close proximity to the gate of the GaN HEMT, and thus the parasitic inductance between the driver and the gate of the HEMT is reduced by more than one

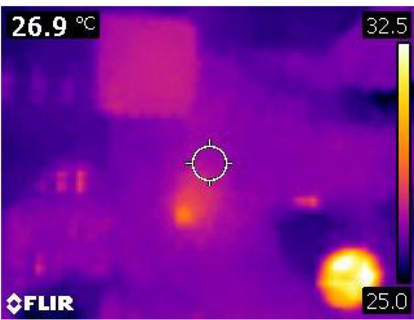

Fig. 9. *IR* image of the evaluation board top view after 30 min operation.

order of magnitude, achieving parasitic inductance values under 0.1 nH, compared to several nH for a typical printed circuit board integrated solution.

However, two concerns arise during our circuit design and implementation. First, the heat dissipation of both the BCD and GaN transistors must be handled by the BCD substrate/package. To fully consider the influences, we used the thermal management software *ANSYS Icepak* to simulate the temperature changes on the BCD chip surface due to GaN devices and incorporate the changes in the driver design process. In Fig. 9, the *IR* image shows a maximal surface temperature of 32.5 °C, which is acceptable in industrial applications.

The second concern is the total thickness of stacked GaN transistors and BCD may pose packaging limitations. In this prototype, the added thickness of the GaN transistor and the solder bump is 815 μm. Thinning of the BCD and/or GaN transistor substrates may be required depending on the final packaging solution.

IV. Conclusion

In this letter, a dc–dc boost converter was designed and fabricated using the GLOBALFOUNDRIES GaN2BCD™ technology. It features direct integration of a silicon BCD control circuit with two GaN power transistors, high conversion ratio (3.3–70 V), large output power, high conversion efficiency, and compact size. The GaN2BCD™ technology is a promising platform for power conversion applications.

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