Difference in Device Temperature Determination Using p-n-Junction Forward Voltage and Gate Threshold Voltage

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***Abstract*—Determination of chip temperature is a key element in the lifetime estimation of power devices. There are several temperature sensitive electrical parameters for this purpose, which allow accurate measuring of the chip temperature on fully packaged devices. Among all these parameters, the forward voltage of a p-n junction is probably the most widely used parameter for temperature determination of a power semiconductor device. In metal-oxide-semiconductor (MOS) gated power semiconductor devices, gate threshold voltage is an alternative parameter with high temperature resolution. In this paper, the p-n-junction forward voltage and the gate threshold voltage of MOS-gated power devices were investigated. The difference between temperature measurements via the two methods was analyzed.**

***Index Terms*—Insulated-gate bipolar transistors (IGBT), metal-oxide-semiconductor field-effect transistor (MOSFETs), p-n junctions, temperature measurement.**

I. Introduction

TO ALLOW reliable and sustainable performance of the power electronic system, a precise lifetime estimation of the power semiconductor devices at the design stage is of great importance. The major parts of the lifetime estimation procedure of the power semiconductor devices are shown in Fig. 1. Based on a given mission profile, which contains operation information such as mission time t_{mis}, phase current, battery voltage, switching frequency, etc., temperature profile of the power semiconductors $T_{\mathrm{j}}(t)$ can be calculated. Since power loss of the semiconductor device depends on its temperature, the calculation of the power loss and the temperature of semiconductor devices is normally performed in an iterative way, until the point of convergence is reached. By using cycle counting method, the corresponding temperature a profile can be reduced into a set of repeated single stress conditions with corresponding cycles *N*, which include lifetime-deciding information such as junction temperature swing ΔT_{j}, mean junction temperature T_{jm}, and load pulse duration t_{on}. For each single stress condition,

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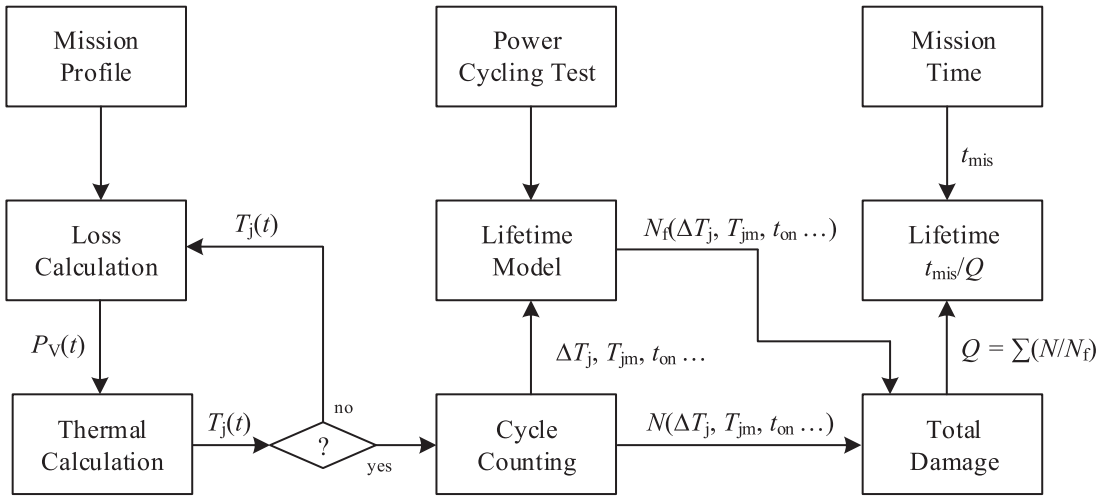

Fig. 1. Flow diagram for the lifetime estimation procedure.

measurement and simulation are discussed under power cycling test or thermal impedance measurement condition.

II. Measurement and Calculation Principle

A. p-n-Junction Forward Voltage

As a basic semiconductor structure, p-n-junction can be found in most semiconductor devices. Its forward voltage V_{pn} decreases strongly with the increasing temperature due to the enhancement of thermal generation of charge carriers. Therefore, V_{pn} is widely used as a temperature sensor for the qualification and testing of semiconductor devices. Typically, for the temperature measurement via the p-n-junction forward voltage, a very small measurement current will be used. It can be assumed that the voltage drop over other regions except the p-n junction, for example ohmic contacts, channel, or base region, can be neglected. The forward voltage of diode V_F (or voltage drop of MOSFET body diode V_{SD}) or the forward voltage drop of IGBT V_{CE} [see Fig. 3(a)] at a small current almost equals the forward voltage over the p-n-junction V_{pn}. For high-voltage devices with a thick base region, voltage drop over the base region may not able to be neglected any more. The *I–V* characteristic of an idealized p-n junction is given by the Shockley equation [8]

$$j = j_S \left(e^{qV_{pn}/kT} - 1 \right) \tag{1}$$

where j is the current density cross the device, q is the elementary charge, k is Boltzmann constant, V_{pn} is the voltage across the junction, T is the temperature, and j_S is the reverse bias saturation current density, which can be obtained as

$$j_S = qn_i^2 \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right) \tag{2}$$

where n_i is the intrinsic carrier concentration, D_n and D_p are the diffusion constants, L_n and L_p are the diffusion lengths of electrons and holes, respectively, and N_D and N_A are the donor density and acceptor density. A comparison of measured I_C versus V_{CE} characteristics of a 400-A 650-V IGBT from Infineon with analytical calculation based on (1) is shown in Fig. 2.

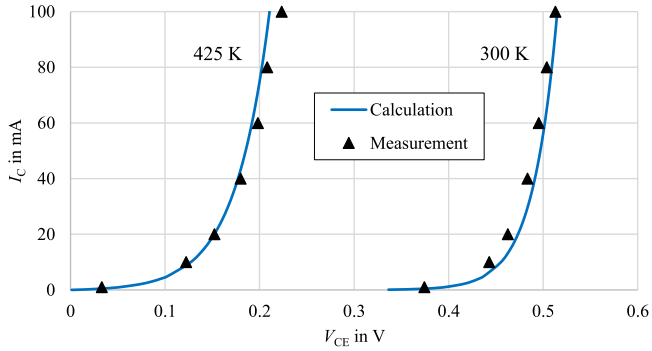

Fig. 2. Comparison of measured I_C versus V_{CE} characteristics of a 650-V 400-A IGBT with analytical calculation.

For using TSEP as a chip temperature sensor, the first step is temperature calibration. The measurement circuit for the temperature calibration by using p-n-junction forward voltage as TSEP is shown in Fig. 3(b). During the calibration procedure, DUT is kept in on-state and a small constant measurement current I_M will flow through the DUT. After the DUT being heated up externally, the forward voltage of the DUT and the corresponding temperature measured outside the device (typically with thermocouple) will be recorded during the slow cooling process, when the temperature of the whole system can be considered to be identical.

Calibration curves of the body diode of a 17-A 1200-V SiC MOSFET from Rohm at different measurement currents are shown in Fig. 4(b). Here, a negative gate voltage ($V_{GS} = -10$ V) is used to completely close the inversion channel of MOSFET. With sufficient negative gate voltage, the current is only flowing through the body diode. For using the forward voltage of the p-n junction as a temperature sensor, a small measurement current is preferred to limit the self-heating effect. Normally, 1/1000 of the device rated current is recommended as a measurement current [9]. However, measurement current should also not be

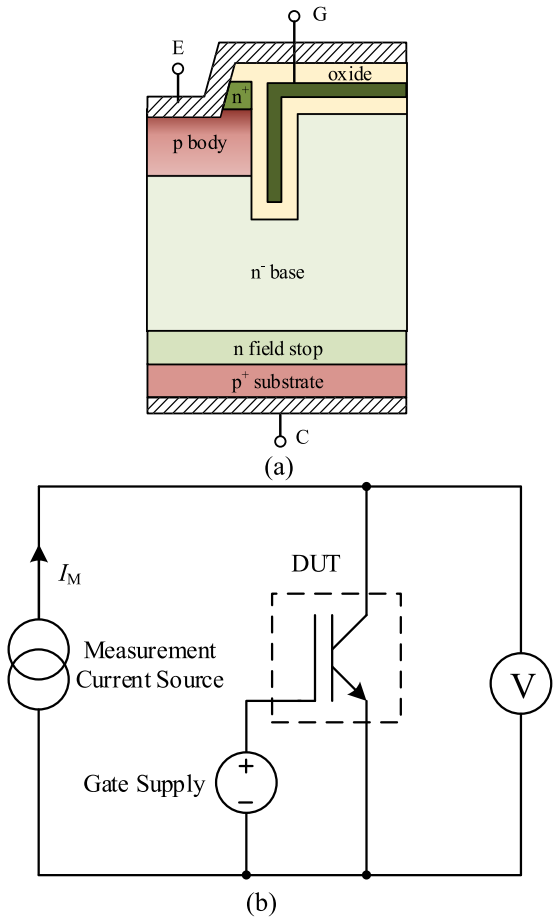

Fig. 3. (a) Structure of a 650-V IGBT with trench gate. (b) Calibration circuit for temperature measurement via p-n-junction forward voltage.

too small. For the IGBT, as shown in Fig. 4(a), the temperature resolution of V_{CE} at 100-µA measurement current close to 150 °C decreases dramatically. Therefore, the small measurement current will limit the suitable measurement range.

For both devices shown in Fig. 4, the temperature resolution of all calibration curves is around –2 mV/K. However, with increased measurement current, the temperature resolution is decreased slightly. It is because the forward voltage of IGBT V_{CE} or voltage drop of MOSFET body diode V_{SD} has a temperature compensation point (TCP). Below the TCP, their temperature dependency is dominated by the influence of thermal generation of charge carriers. Above the TCP, it is dominated by the influence of carrier mobility. Therefore, with a small measurement current below TCP, temperature resolution is decreasing with increasing measurement current.

B. Gate Threshold Voltage

Gate threshold voltage V_{th} is a very important characteristic of MOS-gated power semiconductors such as MOSFET and IGBT. Due to the fact that the exact value of V_{th} varies strongly with the thickness of the gate oxide and the doping of the substrate, it is widely used for the quality control in fabrication processes and function check in reliability tests. As an alternative TSEP

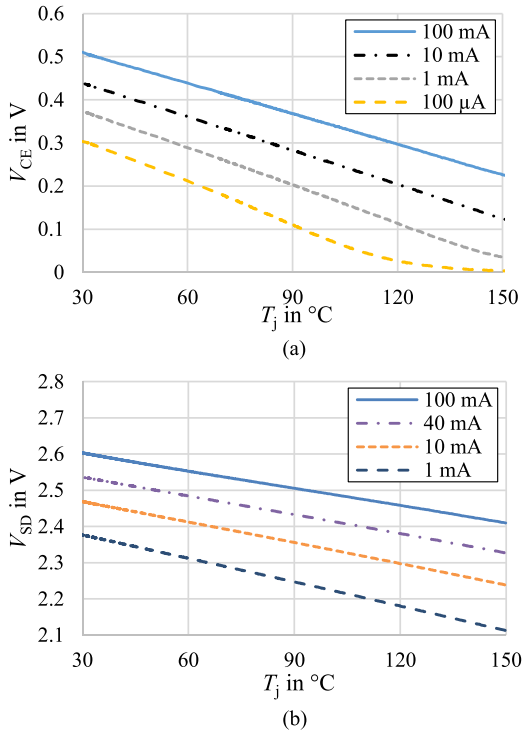

Fig. 4. Calibration curves of (a) 400-A 650-V Si IGBT ($V_{GE} = 15$ V) and (b) 17-A 1200-V SiC MOSFET body diode ($V_{GE} = -10$ V) at different measurement currents.

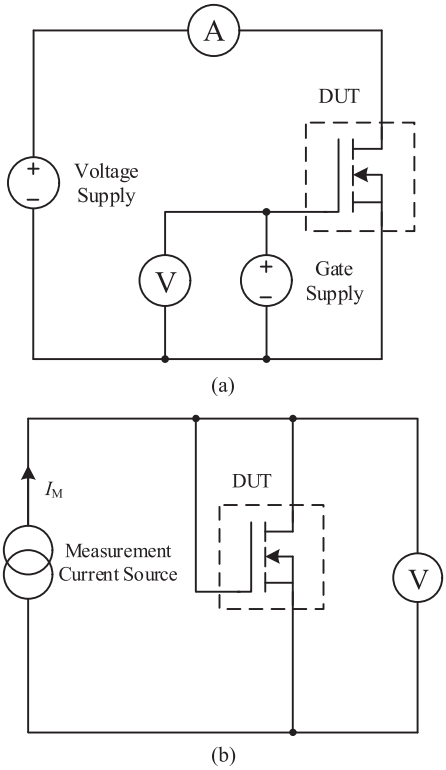

Fig. 5. Measurement circuit for gate threshold voltage. (a) With conventional methods. (b) With constant current method.

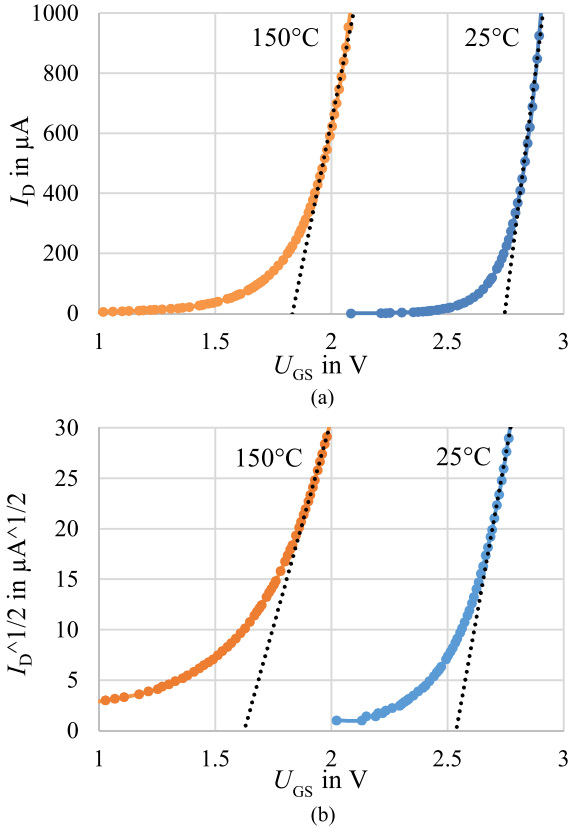

Fig. 6. I_D versus V_{GS} characteristics of a 50-A 150-V MOSFET. (a) In linear mode ($V_{DS} = 0.1$ V). (b) In saturation mode ($V_{DS} = 10$ V).

to the p-n-junction forward voltage, the gate threshold voltage has been already used for measuring the chip temperature of MOSFET and IGBT for a long time [10], [11]. The threshold voltage V_{th} of the MOS structure is given by [12]

$$V_{th} = \Phi_{MS} - \frac{Q_{SS}}{C_O} + 2\psi_B - \frac{Q_{SC}}{C_O} \tag{3}$$

where Φ_{MS} designates the metal semiconductor work function difference. In the power semiconductors, instead of metal, n^+-polysilicon gate is used extensively. Q_{SS} is the surface state charge density per unit area, C_O is the capacitance of the oxide per unit area, ψ_B is the Fermi potential of the substrate, and Q_{SC} is the space charge per unit area within the depletion region. For an n-channel device under the strong inversion condition, a tiny increase of the gate voltage (leads to a very small increase in band bending) results in a large increase of number of electrons in the inversion layer. In this case, the depletion region reaches its maximum width W_m and Q_{SC} can be given with [12]

$$Q_{SC} = -qN_A W_m = -\sqrt{4q\varepsilon_S N_A \psi_B} \tag{4}$$

where N_A is the impurity concentration of the substrate and ε_S is the permittivity of the semiconductor substrate.

The drain current of the MOSFET I_D in linear mode ($V_{DS} \leq V_{GS} - V_{GSth}$) and saturation mode ($V_{DS} > V_{GS} - V_{GSth}$) based on the ideal square law equation are given by the following equations [9]:

$$I_D = \mu_n C_O \frac{W_{ch}}{L_{ch}} \left(V_{GS} - V_{GSth} - \frac{V_{DS}}{2} \right) V_{DS} \tag{5}$$

$$I_D = \frac{1}{2} \mu_n C_O \frac{W_{ch}}{L_{ch}} (V_{GS} - V_{GSth})^2 \tag{6}$$

where μ_n is the electron mobility, C_O is the oxide capacitor, W_{ch} is the effective channel width, L_{ch} is the effective channel length, V_{GS} is the applied gate–source voltage, V_{GSth} is the gate threshold voltage, and V_{DS} is the drain–source voltage.

In the conventional method, which assumes the linear and square relationship between I_D and V_{GS} in linear mode and saturation, respectively, the I_D versus V_{GS} characteristics are measured under a given V_{DS}, as shown in Fig. 5(a). The measured characteristics of a 50-A 150-V Si MOSFET from Infineon in linear mode ($V_{DS} = 0.1$ V) and in saturation mode ($V_{DS} = 10$ V) are shown in Fig. 6(a) and (b), respectively. For each measured characteristic curve, a tangent line is drawn. The gate voltage value of the point of this tangent line crossing the horizontal axis indicates the point of $I_D = 0$ A. By taking this gate voltage value back into the (5) and (6) with $I_D = 0$ A, the gate threshold voltage of the device can be determined. It is to be noted that, even without a large lateral electric field, the electron mobility in the channel is reduced due to the influence of the semiconductor surface [9].

The linear or quadratic extrapolation method, normally referred as conventional method, was popular few decades ago, especially for the device simulation model determination. However, due to the fact that, the determination of the complete I_D versus V_{GS} characteristic is too time consuming, operational amplifier circuit is used to measure gate threshold voltage at which a certain constant current flows [13]. For device temperature determination, the exact value of the gate threshold voltage is not important. Only the temperature dependency of the gate threshold voltage needs to be used. Therefore, a simplified circuit with the gate and drain of the MOSFET being short, as shown in Fig. 5(b), is usually used. A small measurement current will flow though the device. The gate voltage (equals drain–source voltage) needed to drive this measurement current will then be taken as the gate threshold voltage V_{GSth}. The same method can also be used for IGBT.

The calibration curves of one 50-A 150-V Si MOSFET and one 400-A 650-V Si IGBT are shown in Fig. 7. The linearity of the calibration curves is not as good as the curves of the p-n-junction forward voltage. Therefore, for the calibration of the gate threshold voltage, measurement at only several temperature points is not enough. Compared with the p-n-junction forward voltage, the temperature resolution of the threshold voltage of both devices is higher. For the 400-A 650-V IGBT, its temperature resolution of the gate threshold voltage is between –10 and –15 mV/K, which is stronger than that of the 50-A 150-V MOSFET (between –6 and –11 mV/K). It is probably due to its thicker oxide layer or higher substrate impurity concentration in IGBT [12]. Similarly like the p-n-junction forward voltage, the transfer characteristic of IGBT and MOSFET also has a TCP. Therefore, with a small measurement current below

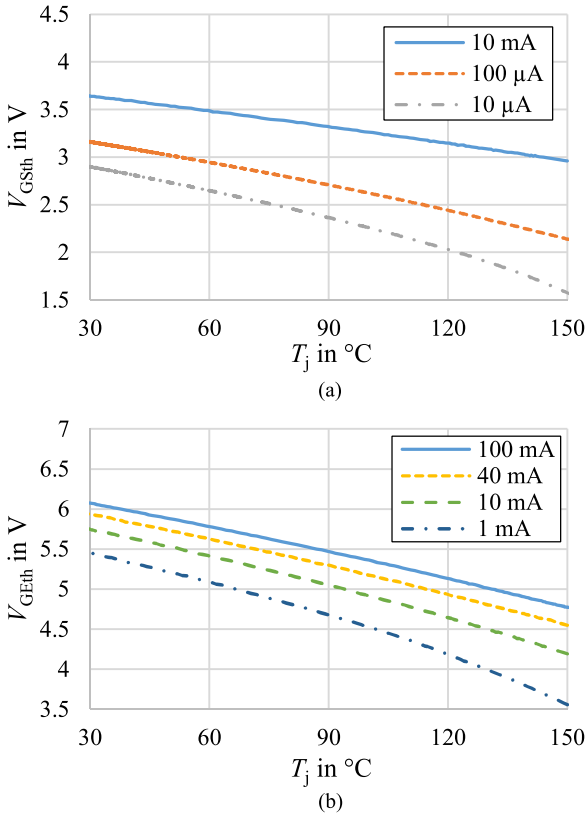

Fig. 7. Calibration curves of (a) 50-A 150-V Si MOSFET ($V_{DS} = V_{GS}$) and (b) 400-A 650-V Si IGBT ($V_{CE} = V_{GE}$) at different measurement currents.

TCP, temperature resolution is decreasing with increasing measurement current.

For the MOSFET, the measured temperature resolution with a constant measurement current method is between -6 and -10 mV/K. The calculated temperature resolution of this MOSFET based on (3) (assumed: $N_A = 2E17$ cm^{-3} and $d_O = 100$ nm) is about -7.1 mV/K. The calculated temperature resolution of V_{GSth} based on a linear or quadratic extrapolation shown in Fig. 6 is -7.3 mV/K. It needs to be noted, since the chosen measurement current for the constant current method is often specified by user, there is no physical connection between the chosen measurement current and the onset of strong inversion condition. The threshold voltage of the MOS structure, as calculated with (3), is under the strong inversion condition, when the channel surface electron concentration equals the original hole concentration in the substrate.

As mentioned earlier, for power cycling test, the TSEP characteristic should not change during the test. In an Si device, the shift of the gate threshold voltage is usually observed under a high gate voltage bias and a high temperature condition after a long time. In [14], an increase of the gate threshold voltage was observed after the thermal overstress tests of IGBTs. From eight samples, the sample with the most change in the gate threshold voltage showed an increase by 11%. It is to be noted that the maximum case temperature during the above-mentioned thermal overstress tests was 340°C, which is much higher than

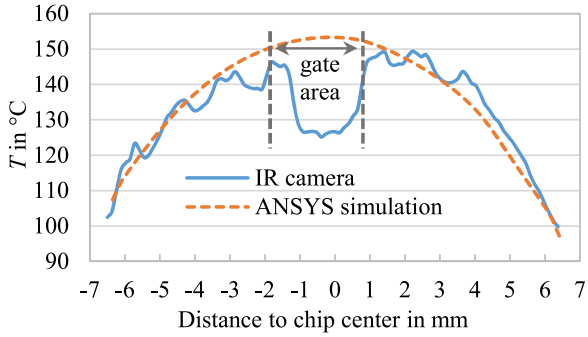

Fig. 8. Surface temperature distribution on an IGBT chip diagonal from IR camera and ANSYS simulation ($t_{on} = 20$ s, $P_V/A = 2.484$ W/mm²).

the operation temperature in standard power cycling tests. In power cycling test, IGBTs are normally stressed with the standard gate–voltage bias (+15 V) in a limited test time (usually a few weeks). After the power cycling tests, the gate threshold voltage of IGBTs normally shows an increase of 30–100 mV, which leads to a temperature measurement offset of about 3–10 K. In [15], similar results were reported for IGBTs in discrete package from three manufacturers after accelerated aging tests. During power cycling tests, gate oxide breakdown can also occur, which is usually a subsequent failure of bond wire liftoff. In this case, since the device has already reached its lifetime limit by a loss of the control ability, the impossibility to measure the device temperature is not critical. Therefore, for the Si device, the gate threshold voltage is in principle a possible TSEP for the power cycling test with high temperature resolution (low relative error). In SiC MOSFET, the transient trapping effect of channel electrons will lead to the shift of the gate threshold voltage depending on the gate–voltage bias [16], [17]. Therefore, the gate threshold voltage is not suitable for the temperature measurement of SiC MOSFET right now. Forward voltage of the body diode the p-n junction at a low measurement current with sufficient negative gate voltage was found to be the most reliable TSEP for SiC MOSFET under a power cycling test condition [18].

C. Current Related Average

Although using TSEP as a temperature sensor holds a lot of advantages, such as a low time constant and an applicability on package devices, it also has a major disadvantage that the temperature measured via TSEP cannot represent the whole chip temperature distribution. The temperature measured via TSEP lies usually between the maximum and the minimum temperature of the whole chip, which is only an "averaged" virtual chip temperature. For a large IGBT chip (total area: 99.54 mm²), temperature difference between the maximum and the minimum on chip under a typical operation condition ($t_{on} = 20$ s, $P_V/A = 2.484$ W/mm²) could be several 10 K, as shown in Fig. 8. In the center of the chip, there is a large difference between the ANSYS simulation results and measurement results with the IR camera. It is because of the gate bond wire contact region. Underneath this region, there is usually no active IGBT cells. Therefore, much less conduction losses will be generated in this region, which leads to a lower temperature compared to

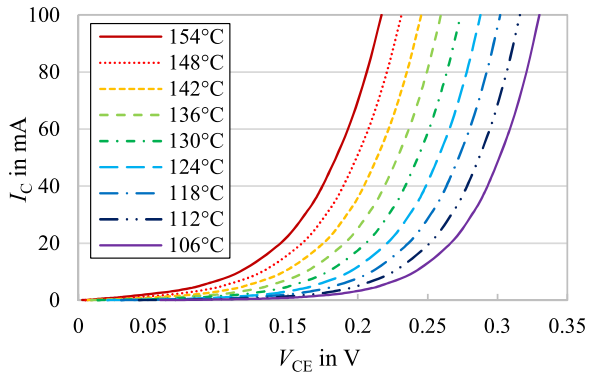

Fig. 9. I_C versus V_{CE} characteristics of a 400-A 650-V IGBT at different temperatures (measurement).

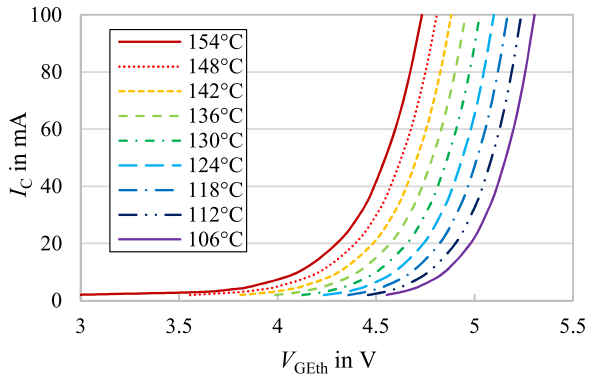

Fig. 10. I_C versus V_{GEth} characteristics of a 400-A 650-V IGBT at different temperatures (measurement).

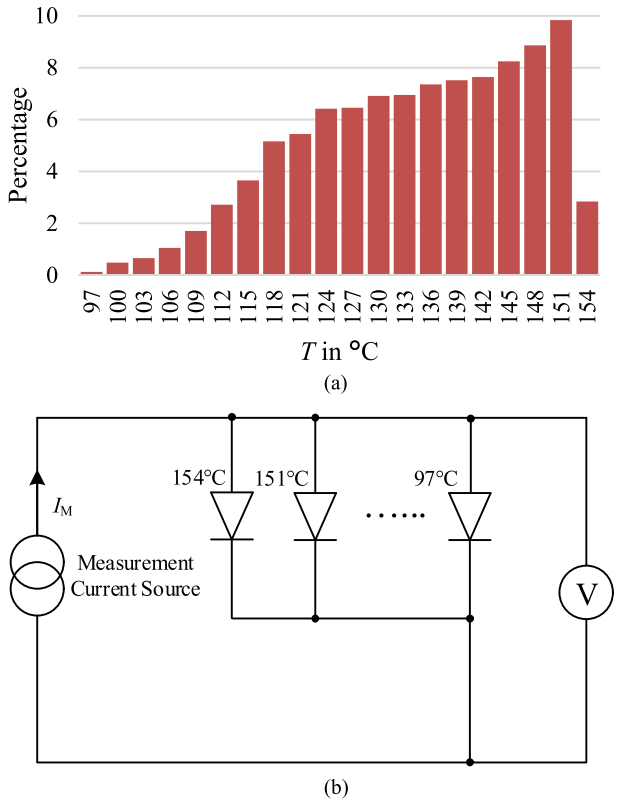

Fig. 11. (a) Histogram of chip surface temperature distribution from ANSYS simulation. (b) Simulation circuit for current related average method.

the active area round it. In the ANSYS simulation, this effect is not taken in consideration, since ANSYS is not made for the semiconductor simulation. Some devices from power semiconductor manufacturers use an extra build-in p-n junction as the chip temperature sensor, which is electrically isolated from the original chip [19], [20]. By using this method, a quick and accurate measuring of one part of the chip under most operation conditions is possible. However, the temperature map of the whole chip is still unknown.

As mentioned earlier, by using TSEP to measure the chip temperature, only an "averaged" chip temperature will be deduced. Depending on the used TSEP, deduced average temperature will also be different. Taking the IGBT forward voltage V_{CE} and the gate threshold voltage of V_{GEth} as an example, I_C versus V_{CE} and V_{GEth} characteristics of a 400-A 650-V IGBT at different temperatures are measured and shown in Figs. 9 and 10, respectively.

To simulate the current related average temperature based on semiconductor characteristics, one semiconductor chip is first divided into several thousand parts (depending on the mesh of an finite element method (FEM) simulation or the resolution of the IR camera). It is assumed that all the small parts of the chip are identical. A given chip surface temperature distribution, for example, the ANSYS simulation results, as shown in Fig. 8, will be sorted into several groups [see Fig. 11(a)]. Each group has a temperature range of 3 K (±1.5 K) and it will be modeled as a diode in the circuit simulation [see Fig. 11(b)]. Based on the percentage of the temperature groups, the diode characteristics in the circuit simulation will be adjusted. As shown in Fig. 11(a), about 3% of the chip active area is in the temperature group 154°C. In this case, 3% of the diodes in Fig. 11(b) will get the *I–V* characteristic of 154°C from the Figs. 9 or 10. After the diode characteristics of all temperature groups are set, a constant measurement current I_M will be given (for example 100 mA) and the voltage drop can be then converted to the current related average temperature by using the calibration curve of the corresponding measurement current.

A comparison of virtual chip temperature determined by different methods is shown in Fig. 12. The blue line shows the mean surface temperature of the chip T_{avg}, which is covered by the yellow line. The green line shows the temperature calculated by using 1/3-method $T_{1/3}$, as shown in (7), where T_{max} and T_{min} are the maximal and minimal chip surface temperature

$$T_{1/3} = \frac{2T_{\max} + T_{\min}}{3}. \tag{7}$$

The current related average temperature T_{VCE} calculated by using the p-n-junction forward voltage is around 134.1 °C (yellow line). It is to be seen that the virtual chip temperature calculated by using the mean surface temperature, 1/3-method or the p-n-junction forward voltage characteristics is close to each other with a negligible difference. This conclusion has also been verified by other research groups in measurement of IGBT and diodes, when comparing TSEP results with the IR camera

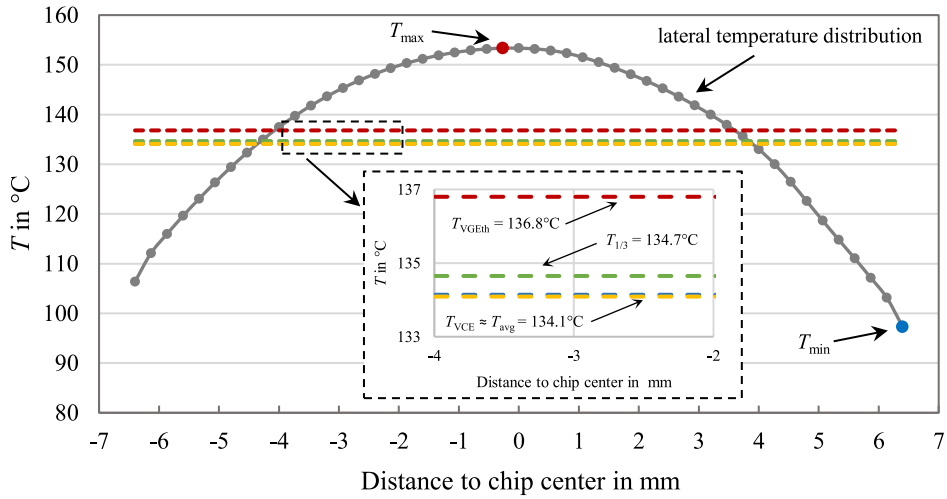

Fig. 12. Comparison of chip lateral temperature distribution with virtual chip temperature determined by different methods (simulation).

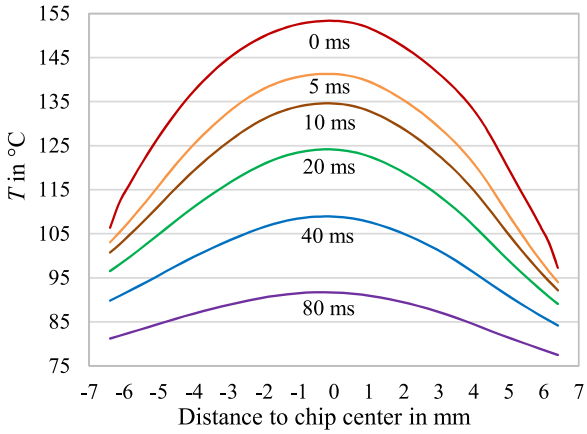

Fig. 13. Chip top surface lateral temperature distribution in the first 80 ms after turning off the load current (ANSYS simulation).

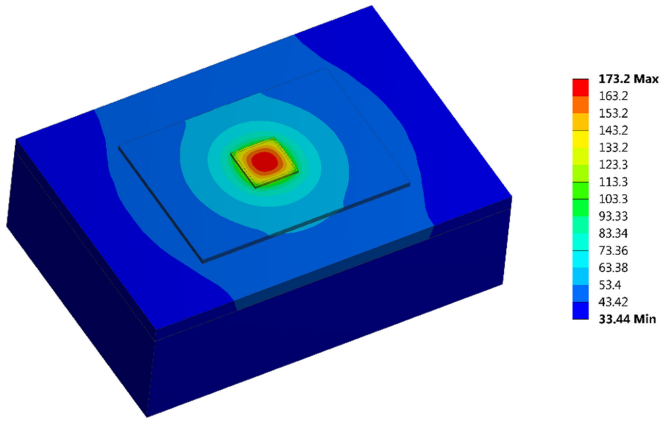

Fig. 14. Single chip benchmark system in ANSYS simulation.

TABLE I
COMPARISON OF CHIP TEMPERATURE DETERMINATION BY DIFFERENT METHODS DURING COOLING PHASE (SIMULATION)

t_{off} in ms	0	5	10	20	40	80
T_{avg} in °C	134.1	123.4	118.3	110.1	99.0	86.6
T_{VCE} in °C	134.1	123.4	118.3	110.2	99.0	86.5
T_{VGEth} in °C	136.8	125.3	119.8	111.1	99.7	87.1
ΔT_1 in K	2.7	1.9	1.5	0.9	0.7	0.6

[21]–[23]. However, the virtual chip temperature calculated by using the gate threshold voltage characteristics T_{VGEth} (red line) under the same condition is about 3 K higher than the other values, although the given lateral temperature distribution is identical.

As the ANSYS simulation result in Fig. 13 shows, the device cools down fast in the first 80 ms after turning OFF the load current. For all chip top surface lateral temperature distributions, a virtual chip temperature is determined by using the p-n-junction forward voltage (T_{VCE}) and the gate threshold voltage (T_{VGEth}). The difference between these two methods ΔT_1 is calculated and summarized in Table I. As can be seen from the simulation results, the gate threshold voltage always indicates a higher current related average temperature than the p-n-junction forward voltage, when a lateral temperature distribution is exiting. ΔT_1 is decreasing during the cooling phase, because the lateral temperature gradient is getting smaller concurrently.

D. Position Caused Difference

Besides the characteristic caused difference, which is indicated by the current related average value, the vertical position caused difference will also play a part, if the power loss density P_V/A is high and the chip thickness d is large enough. Since the power loss of the IGBT chip is mostly produced in the base region and in the p-n-junction layer, the heat will be produced inside the whole chip. Due to the fact that the cooling from the bottom side is dominating, not only a lateral but also a vertical temperature gradient is present inside the high-voltage IGBT chip. For MOSFET, position caused difference is negligible, since the p-n junction of its body diode lies on the source side, which is also closed to the chip top surface (near gate structure).

TABLE II
DIMENSION OF THE SINGLE CHIP BENCHMARK SYSTEM (SIMULATION)

Layer	Material	Length in mm	Width in mm	Thickness in µm
Chip	Si	8 (10)	8 (10)	70/470
Chip solder	$Sn_{96.5}Ag_{3.5}$	10	10	50
Substrate	Cu	42	30	300
	Al_2O_3	42	30	380
	Cu	42	30	300
System solder	$Sn_{96.5}Ag_{3.5}$	42	30	100
Baseplate	Cu	72	50	3000
TIM	Compound	72	50	50
Heatsink	Al	72	50	20000

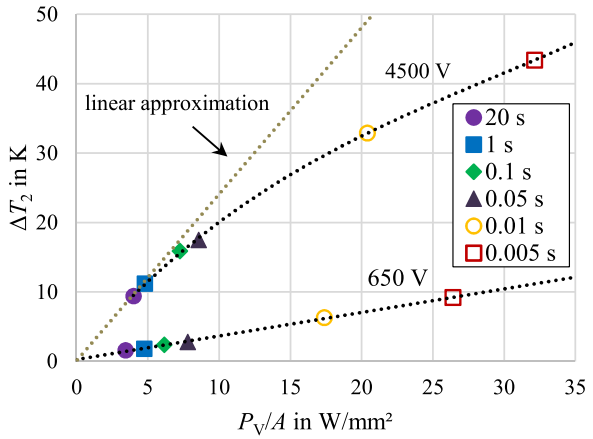

Fig. 15. Mean temperature difference between top and bottom surface plotted over power loss density, power loss density varied with heating time to achieve an identical mean surface temperature $T_{avg} = 150\,^{\circ}C$ (ANSYS simulation).

To visualize the position caused difference, a single chip benchmark system, as shown in Fig. 14, was built in ANSYS. The assumed dimension and structure information of this benchmark system are summarized in Table II. The IGBT chip size is set to be 100 mm² with an active area of 64 mm². Only the chip thickness is varied according to the voltage class. In the ANSYS simulation, a homogenous heat generation is defined in the chip volume of the active area to represent the conduction losses. In the reality, the power loss generated in the chip is not homogeneous, which is not considered in this simulation. At the bottom surface of the aluminum heat sink block, the water cooling was modeled by a convection layer with a defined coolant temperature and a convection coefficient. For the same structure, two different IGBT chips (650 and 4500 V) were simulated under different conditions. For all the simulations, the power loss density is varied to realize an identical mean surface temperature $T_{avg} = 150^{\circ}C$ in different given heating times.

Mean temperature difference between the top and bottom surface of the chip ΔT_2 with different heating time is plotted over power loss density in Fig. 15. The thermal time constant of one layer τ_{th} is given with thickness d, specific heat c, density ρ, and thermal conductivity λ, as shown in (8). If the thickness of this layer is increased seven times, the thermal time constant will increase for about 50 times

$$\tau_{th} = R_{th}C_{th} = \frac{c\rho d^2}{\lambda}. \tag{8}$$

For the 650-V IGBT chip, which has a thickness $d = 70\,\mu m$, 5-ms heating time is already enough to fully charge the thermal capacitance C_{th} of the chip layer. Therefore, the temperature difference between the top and bottom surface of the chip is almost linear to the power loss density applied. For the 4500-V IGBT chip, since the chip is much thicker ($d = 470\,\mu m$), 100 ms is still not enough to fully charge the thermal capacitance of the chip. Therefore, only simulation results of 1 and 20 s are lying on the linear approximation. It is, however, still clear to be seen that at the same power loss density, ΔT_2 of the thick chip (4500 V) is much larger than the ΔT_2 of the thin chip (650 V).

For measurements with extremely high power density, for example under surge current measurement condition, the position caused difference between temperatures measured via the two methods could be very large. In [24], chip temperature of a 650-V IGBT and a 4500-V IGBT during a 10-ms surge current pulse were measured via the p-n-junction forward voltage and the gate threshold voltage (temperature measured short after cutting off surge current pulse). For 4500-V IGBT, the temperature difference between two methods at maximal chip temperature is around 30 K, while for 650-V IGBT it is around 10 K, which is similar with the ANSYS simulation results at about 26 W/mm².

E. Verification by Technology Computer Aided Design (TCAD) Simulation

To verify the current related average method and the position caused difference by using semiconductor simulator, TCAD model was made for the 650-V and 4500-V IGBT chip with the whole packaging layers and cooling. Due to the complex gate structure of IGBT, a simplified equivalent diode model was created to make the large-size chip simulation in TCAD possible. In this equivalent diode, active area ($1.44\,cm^2$), thickness of the chip, p^+ region, n buffer region, and the doping in n^- region are completely identical as in the IGBT [see Fig. 16(a)]. The forward voltage drop and carriers lifetime of the equivalent diode are also same as in the IGBT. The thickness of n^- region and n region on "emitter" side (top surface) in diode model is selected to match the electric field inside the IGBT chip during isothermal forward bias simulation. The black dashed line and the red solid line in Fig. 16(a) are the doping profile of the original IGBT and the equivalent diode, respectively. In this equivalent diode model, material as well as thickness of all layers are conformed to the real IGBT module. From top to the bottom of the TCAD model, as shown in Fig. 16(b), the layers are surface metallization, chip, chip solder, substrate, system solder, base plate, thermal grease, and heatsink respectively. The junction termination (2 mm) is shown at the edge of the chip.

During the simulation, the device is first heated up by a 10-s load current pulse. After turning OFF the load current, a small measurement current is given. The voltage drop (collector–

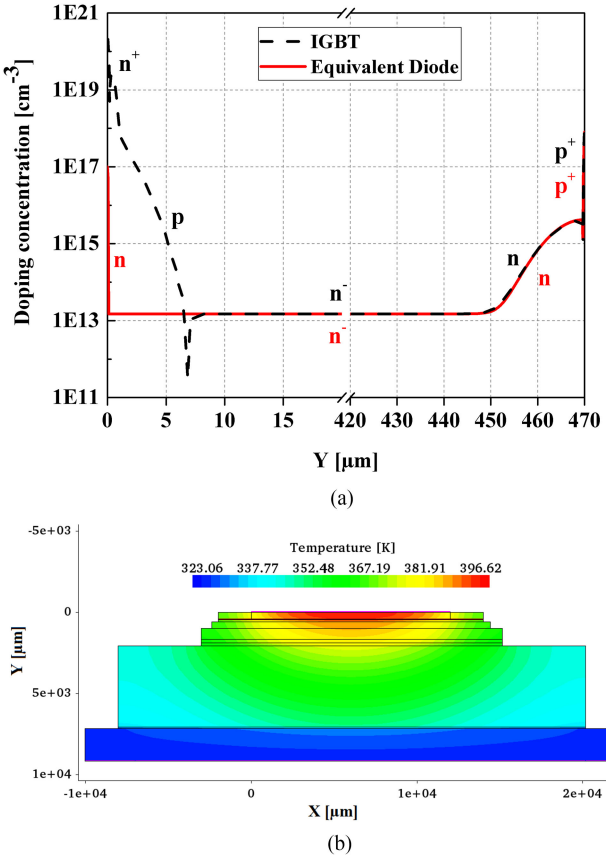

Fig. 16. (a) Doping profile of the 4500-V IGBT and of a simplified equivalent diode. (b) Temperature distribution in 4500-V IGBT model (TCAD simulation results).

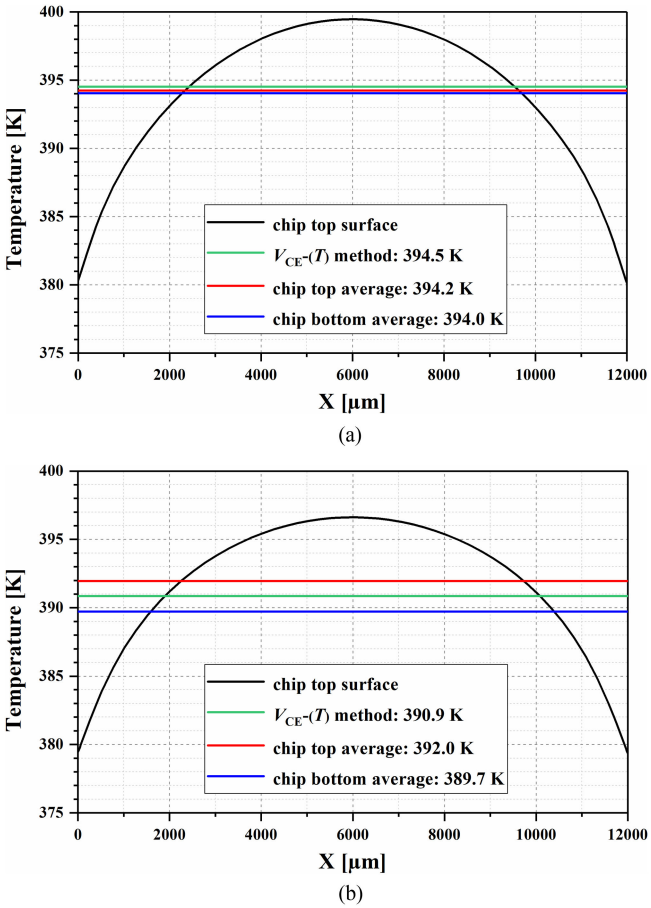

Fig. 17. Comparison of temperature of the equivalent diode chip (TCAD simulation). (a) 650-V IGBT. (b) 4500-V IGBT.

TABLE III
COMPARISON BETWEEN MEASUREMENT AND SIMULATION (650 V)

t_{on} in s	P_v/A in W/mm^2	Experiment	Simulation	
		ΔT_1 in K	ΔT_2 in K	ΔT_3 in K
20	2.827	4.1	0.1	3.4
1	3.584	5.4	0.2	5.3
0.1	6.116	8.3	0.3	7.4

TABLE IV
COMPARISON BETWEEN MEASUREMENT AND SIMULATION (4500 V)

t_{on} in s	P_v/A in W/mm^2	Experiment	Simulation	
		ΔT_1 in K	ΔT_2 in K	ΔT_3 in K
20	1.271	7.2	3.6	7.6
1	2.021	8.9	5.6	10.9
0.1	4.666	10.8	11.7	18.5

emitter voltage V_{CE}) of the chip is read at the time point 800 µs after the load current pulse was switched OFF. At this moment, the temperature distribution is shown in Fig. 16(b). In the next step, the virtual junction temperature T_{vj} at this moment can be read from the in TCAD simulated calibration line (V_{CE} versus T_{vj}), which is then compared with the temperature distribution through the chip top surface as well as the top and bottom average temperature of the chip.

The black line in Fig. 17 indicates the lateral temperature distribution on the top surface of the chip. The red and the blue line are average temperature of the top and bottom surface of the chip, respectively. The temperature calculated by using $V_{CE} - (T)$ method (p-n-junction forward voltage) is shown with green line. For the 650-V chip shown in Fig. 17(a), chip thickness is 70 µm. Therefore, the temperature difference between the top and bottom surface of the chip is very small (0.2 K under this condition). In this case, virtual chip temperature calculated by using $V_{CE} - (T)$ method is almost equal to the chip average temperature, which has confirmed the current related average method (see Fig. 12).

For the 4500-V chip, even with a low power loss density (1.198 W/mm^2), there is still about 2-K difference between the top and bottom surface temperature of the chip. For this chip with a thickness of 470 µm, "current related average" temperature indicated by the forward voltage of IGBT ($V_{CE} - (T)$ method) lies between the average temperature of the top and the bottom surface of the chip. It is due to the reason that the base region of this 4500-V chip is relative thick and the voltage drop over base region is not negligible. Therefore, for-

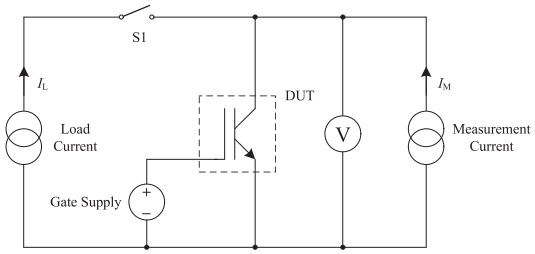

Fig. 18. Circuit to determine chip temperature using p-n-junction forward voltage under power cycling test or Z_{th} measurement conditions.

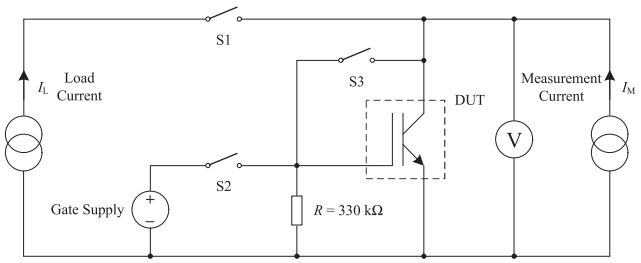

Fig. 19. Circuit to determine chip temperature using gate threshold voltage under power cycling test or Z_{th} measurement conditions.

ward voltage of IGBT V_{CE} at a small measurement current represents not only the temperature of the p-n-junction layer, but also the temperature of the base region. This simulation matches the measurement results for 4500 V IGBT shown later (see Table IV) for verifying position caused difference.

III. Experiments

In this paper, a temperature measurement via the p-n-junction forward voltage and the gate threshold voltage was investigated under power cycling test and transient thermal impedance Z_{th} measurement conditions. For these two experiment conditions, the measurement setup is identical.

A. Measurement Setup

For using the p-n-junction forward voltage as chip temperature sensor, the measurement circuit is shown in Fig. 18. The DUT is kept in on-state during the measurement while the load current is turned ON and OFF by the switch S1. During the conducting, the conductivity of the base region in bipolar devices (IGBT, diode or MOSFET body diode) is modulated by carrier injection. After turning OFF the device, it takes some time for the carrier to be removed. An accurate and correct measurement of the maximal chip temperature by using the p-n-junction forward voltage is only possible after a certain measurement delay t_{md} [25]. In this paper, a measurement delay of 800 µs is used for both measurement methods to enable a better comparison.

In the Fig. 19, the measurement circuit for using the gate threshold voltage under power cycling test or Z_{th} measurement conditions is shown. The pulse pattern of auxiliary switches for temperature measurement by using gate threshold voltage is shown in Fig. 20. Short before turn-ON, switch S3 to short gate and collector is opened. To avoid conflict and damage of control

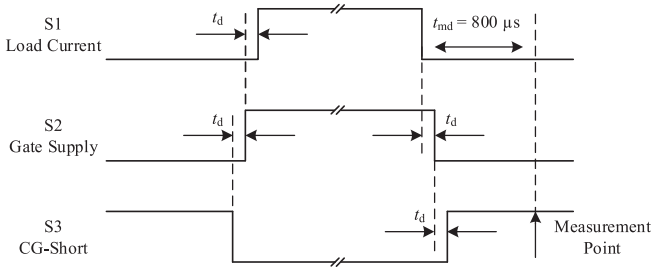

Fig. 20. Pulse pattern for the temperature measurement by using gate threshold voltage.

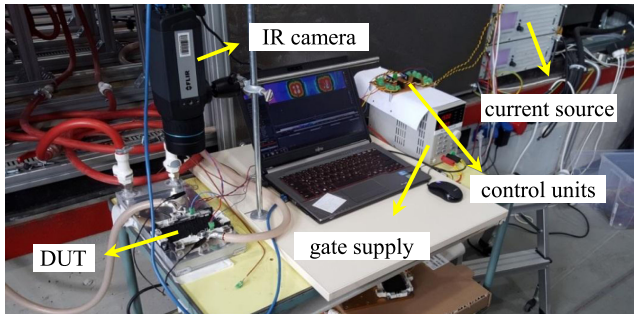

Fig. 21. Measurement setup for temperature measurement under power cycling test or Z_{th} measurement conditions.

systems, gate voltage supply will be turn-ON though switch S2 after a small delay time t_d. The delay time t_d is adjustable from the control program (typically 50–200 µs). Again, after a small delay time, the load current will be turned on via the switch S1. During the load current is flowing, the device is heated up by its conduction losses. When the desired heating time is achieved, the load current will be turned OFF by switch S1. After delay time t_d, the gate voltage supply will also be turned OFF. At last, the gate and collector of the IGBT will be shorted again by switch S3 and the device is operating again in the gate threshold voltage measurement mode. After 800-µs measurement delay t_{md}, the temperature of the device during the cooling can be recorded by using the calibration curve.

The realized measurement setup is shown in Fig. 21. Device for measurement is mounted on a water heatsink, whose coolant inlet temperature and flow rate are kept constant. The load current switch S1 is realized with two parallel connected 2400-A IGBT modules and the gate control switches S2 and S3 are realized with solid state relays. The control of the test and the measurement data acquisition is based on a real-time field programmable gate array (FPGA) system from National Instruments, whose operation interface is built in LabVIEW program.

For measurement with the IR camera, the DUT needs to be opened and be coated with a suitable paint to control the surface emissivity. Since the emissivity of the paint also depends on temperature, the emissivity of the region of interest on device should also be calibrated before the measurement. The maximal image frequency of the in this work used IR camera from FLIR is only 200 Hz. Therefore it is only suitable for the temperature measurement at a steady state. It needs to be noted that the

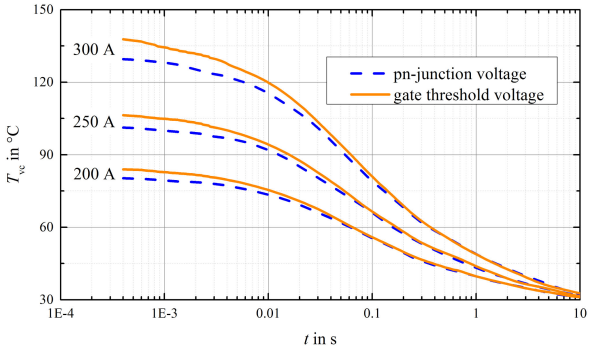

Fig. 22. Comparison of temperature course measured via two methods during the cooling from steady state (650-V IGBT).

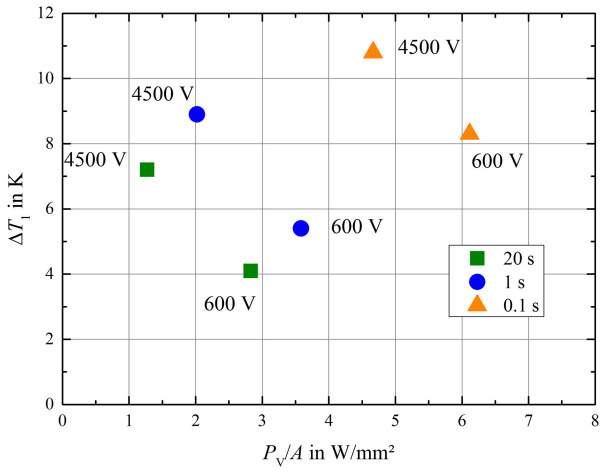

Fig. 23. Temperature difference between two TSEP methods plotted over power loss density (measurement).

virtual chip temperature measured with the p-n-junction forward voltage at small current is always after a certain measurement delay (typically some hundred microseconds). During this time, the device can already cool down for several Kelvins.

B. Experiment Results

As the current related average method indicates, the temperature measured via gate threshold voltage is always higher than the value measured via the p-n-junction forward voltage. The steeper is the lateral temperature gradient, the larger is the difference between the temperatures measured via the two methods. To confirm this statement, measurements were first performed on the 400-A 650-V IGBT with both TSEP methods under three different load conditions (see Fig. 22). In this case, since the 650-V IGBT chip is relatively thin ($d = 70\,\mu\text{m}$), the position caused difference could be neglected. For all the measurements, the device was first heated up to the steady state with the given load current. During the cooling phase, virtual chip temperature T_{vc} was measured via the two TSEP methods. As can be seen from the Fig. 22, the higher is the load current (power loss), the larger is the temperature difference at the beginning, and the longer it takes till the difference between the two methods is no more visible. After about 10 s, when the device is almost completely cooled down and the lateral temperature gradient of the chip is no more existing, temperatures measured by the two methods are almost identical.

To verify the two aforementioned factors (characteristic and position), which are responsible for the difference between results from the two TSEP methods, experiments and simulations were undertaken on 400-A 650-V IGBT module ($d = 70\,\mu\text{m}$) and 1200-A 4500-V IGBT module ($d = 470\,\mu\text{m}$). For different load pulse duration t_{on}, power loss density of the DUTs P_{V}/A was adjusted to reach the same virtual chip temperature measured via gate threshold voltage ($T_{\text{VGEth}} = 150\,^{\circ}\text{C}$). With the same P_{V}/A and t_{on}, the maximal virtual chip temperature was measured again via the p-n-junction forward voltage. For both measurement methods, maximal virtual chip temperature was measured around 800 µs after turning off the load current. The difference between temperatures measured via both methods ΔT_1 is then plotted over power loss density in Fig. 23.

As can be seen from the Fig. 23, the difference measured via the two TSEP methods is higher for device with thick chip (4500 V) than device with thin chip (650 V). It is mainly caused by the position caused difference, because the thick chip has a steeper vertical temperature gradient than the thin chip under the same power loss condition. For the same chip, difference between temperatures measured via the two TSEP methods is also increasing with increasing power loss density due to the impact of the lateral temperature gradient. For higher power loss density, the lateral temperature gradient will be steeper, which will increase the characteristic caused difference as already discussed before.

For both DUTs in this paper, reference thermal simulation was undertaken in ANSYS to verify the measurement results. The simulation results of the 650-V and the 4500-V IGBT under the same load conditions are summarized in Tables III and IV, respectively. As can be seen from the simulation results of the 650–V IGBT, the difference between the mean top and bottom surface temperature ΔT_2 at the corresponding measurement time point (800 µs after turn OFF) is very small (<0.4 K). That is to say, in the case of 650-V IGBT, the position caused difference is negligible under the given conditions. The difference between the measured temperatures via the two methods is mainly caused by the characteristic. In order to verify this point, the chip top surface temperature driven from ANSYS simulation was taken for the calculation of current related average temperature by using the characteristic of gate threshold voltage (see Fig. 10), because the gate channel region is near the chip top surface. Similarly, the chip bottom surface temperature from the ANSYS simulation was taken for the calculation of current related average temperature by using the characteristic of the p-n-junction forward voltage (see Fig. 9). The difference between the current related average temperatures with consideration of position difference is taken as ΔT_3. The simulation results of the 650-V IGBT fit in general well with the measurement results.

The same simulation and evaluation procedure were also performed on the 4500-V IGBT and the results are summarized in Table IV. As the difference between the mean top and bottom surface temperature ΔT_2 shows, the position caused difference will play a role in the measurement of the 4500-V IGBT under

TABLE V
CASE STUDY: ERROR IN LIFETIME PREDICTION (650 V)

t_{on} in s	P_V/A in W/mm^2	ΔT_1 in K	ΔT_j in K	Error in %	
				α = -4.4	α = -5
20	2.827	4.1	115.9	17	19
1	3.584	5.4	114.6	23	26
0.1	6.116	8.3	111.7	37	43

TABLE VI
CASE STUDY: ERROR IN LIFETIME PREDICTION (4500 V)

t_{on} in s	P_V/A in W/mm^2	ΔT_1 in K	ΔT_j in K	Error in %	
				α = -4.4	α = -5
20	1.271	7.2	112.8	31	36
1	2.021	8.9	111.1	40	47
0.1	4.666	10.8	109.2	51	60

the given conditions, even if the used power loss density is lower than in the measurements of 650-V IGBT. The difference between the current related average temperatures ΔT_3, which also considers the position caused difference, does not fit with the measurement results of the 4500-V IGBT well. As previously discussed, the main reason for this deviation is that the voltage drop across the base region is also one nonnegligible part of the forward voltage of the 4500-V IGBT, since its base region is relative thick. The forward voltage of IGBT represents thus not only the temperature of the p-n-junction layer, but also the temperature of the base region. In the calculation of difference between the current related average temperatures ΔT_3, the bottom surface temperature is used for the calculation of the current related average temperature by using the p-n-junction forward voltage. Therefore, difference expected by ΔT_3 is too large for the 4500-V IGBT.

C. Case Study: Error in Lifetime Prediction

For IGBT modules, power cycling lifetime N_f depends strongly on the junction temperature swing ΔT_j. The low cycle fatigue is usually characterized by the Coffin–Manson law, as shown in (9). For power module package, the Coffin–Manson exponent α is typically in the range of -4.4 to –5 (see [1]–[3])

$$N_f \ \Delta T_j^{\alpha}. \tag{9}$$

In order to visualize the influence of using two different TSEPs on the power cycling lifetime, the measurements results shown in Section III-B are reanalyzed and shown in Tables V and VI, respectively. In the measurements, power loss density of the device P_V/A was adjusted to reach the same virtual chip temperature measured via gate threshold voltage ($T_{VGEth} = 150\ ^\circ$C). The difference between temperatures measured via both methods is given as ΔT_1, which is in this case the measurement error made by using two different methods. The temperature swing measured via the p-n-junction voltage is given with ΔT_j. If the chip temperature was measured via the p-n-junction voltage in the thermal characterization procedure, but it is measured via the gate threshold voltage in the power cycling test, the power cycling lifetime is then overestimated. For example, for the measurement of 4500-V IGBT with $t_{on} = 0.1$ s shown in Table VI, the measurement error of temperature swing is about 10.8 K. This will result in a relative error of about 60% in the power cycling lifetime, if the Coffin–Manson exponent $\alpha = -5$. Even for a smaller Coffin–Manson exponent $(\alpha = -4.4)$, the relative error of power cycling lifetime is more than 50%.

IV. CONCLUSION

In this paper, a p-n-junction forward voltage and a gate threshold voltage as chip temperature sensor in MOS-gated power devices were investigated.

The virtual chip temperature measured via the p-n-junction forward voltage represents the mean top surface temperature of the power semiconductor chips in the most cases (MOSFET and diode), independent of the lateral temperature distribution form. For IGBTs, the p-n junction is closed to the bottom surface of the chip. If a high power loss density is used and the chip is thick enough, which leads to a nonnegligible temperature difference between the top and bottom surface, the temperature measured via the p-n-junction forward voltage corresponds to the mean area temperature of a certain layer in base region near the p-n junction (depending on doping profile and chip thickness). Since power cycling tests are executed usually with the p-n-junction forward voltage for temperature determination, the temperature swing at the chip surface, which triggers the bond wire liftoff and aluminum metallization reconstruction, is underestimated for high-voltage IGBTs, especially if short load pulse duration and high power loss density are used.

The difference of temperature measurement results via the p-n-junction forward voltage and the gate threshold voltage could be caused by two main factors: first, characteristic; and second, position. Due to the difference in characteristics, the gate threshold voltage always represents a higher current related average temperature than the p-n-junction forward voltage, when lateral temperature gradient is presenting. The steeper the lateral temperature gradient, the larger is the difference measured by the two TSEP methods. The gate threshold voltage has a higher temperature resolution than the p-n-junction forward voltage, which will reduce the relative measurement error. Depending on the measurement condition, difference between the measurement results via the two methods could be very large.

For power cycling test, only the parameter, which will not change with the aging, can be used. Most transient thermal impedance measurement and power cycling tests of the power semiconductor devices up to know were undertaken by using the p-n-junction forward voltage at small current as temperature sensor. It is shown in the case study that violating the consistency during lifetime estimation procedure by using different TSEPs in different parts will lead to a certain error in the final lifetime expectation. Since the two TSEP methods will deliver different temperature results under the same load and cooling condition, exact information about the TSEP method used in power cycling test and the thermal characterization procedure should be noticed for better understanding and comparison of results from different groups. To ensure a correct and precise

lifetime estimation, TSEP used for thermal characterization and reliability tests should be identical.

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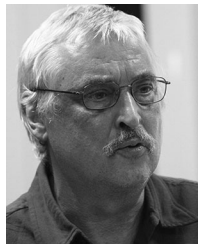

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