Constant ΔT_j Power Cycling Strategy in DC Mode for Top-Metal and Bond-Wire Contacts Degradation Investigations

Son-Ha Tran, Zoubir Khatir, Richard Lallemand, Ali Ibrahim, Jean-Pierre Ousten, Jeffrey Ewanchuk, *Member, IEEE*, and Stefan V. Mollov

***Abstract*—The study of the impact of junction temperature swings (ΔT_j) on degradation mechanisms during power cycling tests (PCTs) requires both a control of the applied thermal stress and a separation of degradation modes. The first requirement can be obtained by using a "constant ΔT_j" power cycling strategy that allows to minimize the cross interactions between the influencing factors. The second one is made by using a dedicated power module well suited for targeting only the chips top-side degradations (metallization and bond-wire contacts). In this paper, a constant ΔT_j strategy by gate voltage regulation is performed for PCTs in the dc mode. The tested modules are ideally designed for top-metal and bond-wire contacts degradation investigations. From aging indicator on the collector–emitter voltage (V_{CE}), the results clearly show that three regimes of degradation occur systematically at the insulated gate bipolar transistor (IGBT) chips top side, whatever the stress conditions. Moreover, comparative results in "constant ΔT_j" and conventional "constant ΔI" PCT strategies have shown that the feedback between stresses and damages encountered in the second strategy is more important for low ΔT_j values than for high ΔTj values. In addition, results show that in case of high stresses, the "constant ΔT_j" strategy with V_{GE} regulation gives values close to a "constant ΔI" strategy but that the extrapolation toward low values of ΔT_j can be questionable for the "constant ΔT_j" strategy.**

***Index Terms*—Accelerated aging, degradation, IGBT, junction temperature swing, lifetime model, power cycling, test strategy, wire bond.**

I. Introduction

DURING the operation, power modules are subjected to thermal and mechanical stresses arising from power loss dissipated in semiconductor devices. Temperature swings, combined with the thermal expansion coefficients mismatch, pro-

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sintering for the connections to DBC layer [12]. In the second step, the interaction between failure mechanisms should be taken into account through a combination of "separated models" and a failure mechanism interaction model.

Concerning the second point, it is related to the choice of a power cycling test (PCT) strategy. Different strategies have been presented in [13] and [14] based mainly on constant load current (I_L), constant junction temperature swing (ΔT_j), and constant power (*P*). As described by these later publications, these different strategies lead to different lifetime results. However, because of their opposite philosophy, only the two first methods are discussed hereafter as the constant power strategy can be considered as an intermediary strategy between them.

The constant load current strategy is the most popular choice for the PCT. It is also the most severe because degradations in the power module immediately result in an increase of ΔT_j with no compensation in the control strategy. Hence, the positive feedback relationship between the interconnection degradations and ΔT_j leads to the lowest lifetimes. However, it is interesting to evaluate the effect of this interaction between the stresses and degradations in the power module lifetime and its dependence on the level of stress (ΔT_j). The results highlighted in this paper, thus, compare the two strategies to give a first indication as to the level of this effect. In addition, concerning the constant load current strategy, the initial ΔT_j is used for positioning the aging test point in the N_f–ΔT_j graph, even if there is a continuous change in ΔT_j during the tests until the failure.

The constant ΔT_j strategy can be obtained by varying $t_{\mathrm{ON}}/t_{\mathrm{OFF}}$ [13], [14] or gate voltage regulation. This strategy leads to avoid the positive feedback between degradations and thermal stresses. Contrary to the constant load strategy, this strategy compensates degradation effects in the module and therefore leads to highest lifetimes. The constant ΔT_j method has been implemented by varying the $t_{\mathrm{ON}}/t_{\mathrm{OFF}}$ parameters [13]–[15] but very few papers report a gate voltage regulation implementation [16], [17]. However, since the t_{ON} parameter also has a strong influence on lifetime results, this way to maintain constant ΔT_j presents an important drawback and leads to difficulty in the interpretation of the results.

In order to overcome this issue, we implemented the other way for achieving a constant ΔT_j strategy, i.e., by regulating the gate voltage (V_{GE}).

From an academic point of view, this PCT strategy by V_{GE} regulation allows

1) a rigorous positioning of the test point in the N_f–ΔT_j graph to avoid inaccuracies in the extrapolation at low ΔT_j. With the other strategies, the shift in ΔT_j during aging makes unclear this positioning in the graph;
2) the investigation of cumulative damage mechanisms under constant thermal stress conditions.

Concerning this last point, one should keep in mind that the stress profiles in real applications consist of different ΔT_j levels in arbitrary sequence. Hence, the linearity of cumulated damage, or Miner rules, needs to be verified. Thus, the constant ΔT_{j} strategy allows to simplify further investigation on the effect of sequence and interaction of various ΔT_j. Therefore, the presented method to perform constant ΔT_j tests, in combination with a control of $T_{J\mathrm{MIN}}$, makes it possible to clearly show the effect of each test parameter.

The main objective of this paper is to describe the results obtained using a dc-mode power cycling with a constant ΔT_j strategy by gate voltage regulation. The PCT tests have been done on SKIM63 modules from Semikron in order to compare the results obtained by the proposed test strategy with those done with a constant load current strategy in [4]. This comparison is intended to enhance the knowledge on the effect of the thermal parameters and the quality of lifetime models. Moreover, as the test vehicles are without baseplates, assembled in pressure contact technology with silver sintering die-attaches, the top-metallization and wire-bond contact degradation mechanisms can be specifically targeted during such power cycles.

II. Constant ΔT_{j} Power Cycling Strategy

A special feature of the proposed power cycling strategy consists of controlling the temperature swing ΔT_j. For this purpose, gate voltage regulation cards (V_{GE} cards) have been designed. Their operation is based on the modification of the gate voltage V_{GE} based on a proportional–integral controller. When ΔT_j is higher or lower than the set-point value, the controller reacts on the gate voltage V_{GE} to increase or decrease ΔT_j. The quantity of the incremental or decremental voltage is calculated from the difference between the measured ΔT_j and the set-point value. The variation of the gate voltage V_{GE} causes a change in the collector–emitter voltage (V_{CE}), and thus in the dissipated power in the insulated gate bipolar transistors (IGBTs) and adjusts the temperature swing ΔT_j. The gate voltage regulation is only activated during the heating phase of each cycle. During the cooling phases of the power cycling, the load current is switched-OFF by the auxiliary devices and the gate voltages of the tested modules are forced to 15 V. This is done in order to monitor the maximum junction temperature ($T_{J\mathrm{MAX}}$) by V_{CE} measurement [thermosensitive parameter/thermosensitive electrical parameter (TSEP)] at $V_{\mathrm{GE}} = 15$ V, at the early beginning of the cooling phase at each cycle.

A result of the temperature swing regulation at the low side of a module is illustrated in Fig. 1 for the test conditions $\Delta T_j = 110$ °C, $t_{\mathrm{ON}} = 3$ s, and $T_{\mathrm{REF}} = 35$ °C. From a low value of temperature swing ΔT_j around 102 °C, the V_{GE} controller progressively reduces the gate voltage during the heating phases, i.e., during t_{ON}, and thus increases the power losses until ΔT_j reaches the desired value (110 °C), see Fig. 1(a). The obtained ΔT_j fluctuates with a margin of ± 0.5 °C around the set-point values. The minimum junction temperature ($T_{J\mathrm{MIN}}$) reaches the cooling temperature, referred to as reference temperature, with little evolution of this temperature observed throughout the testing. A detailed view of the gate voltage waveform during some cycles is shown in Fig. 1(b), where it can be observed that for that case conditions, V_{GE} is regulated around 11.5 V during the heating phases (t_{ON}) of power cycles and, as explained above, set to 15 V during the cooling phases (t_{OFF}) for TSEP measurements. As a result, the temperature profile during PCT is completely regulated.

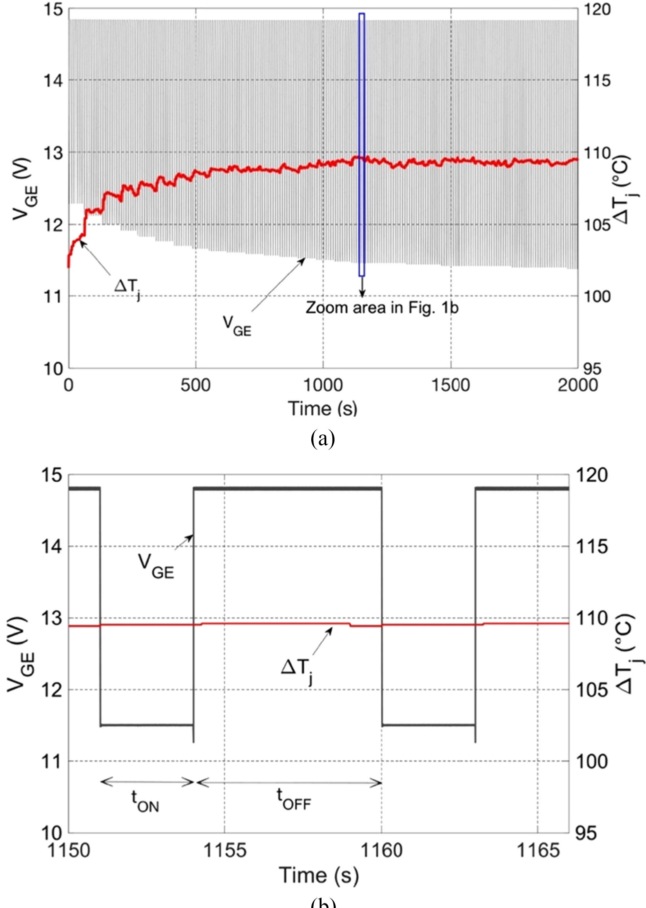

Fig. 1. Example of temperature regulation ($\Delta T_j = 110$ °C, $t_{ON} = 3$ s, and $T_{REF} = 35$ °C). (a) Gate voltage regulation during a long period. (b) Detail of the gate voltage waveform during some cycles.

Finally, as indicated above, a thermal calibration is needed for the TSEP measurements. This calibration allows to establish a relation between the direct drop voltage (V_{CE}) and the junction temperature (T_j). This is done by using a calibrated low collector current ($I_{SENSE} = 50$ mA), in order to avoid any self-heating, and controlled temperature environment for the devices under test (DUTs). The obtained thermal sensitivity of the DUTs is –2.5 mV/K.

III. Experimental Set Up

A. Description of the Test Modules and Their Environment

The tested modules are commercially available SKIM63 (1200 V–300 A), produced by Semikron. These devices are six-pack modules with three individual phase legs on separated DBC substrates.

The power cycling is carried out only on the central leg of tested modules, which constitutes two DUTs high-side and low-side switches as shown in Fig. 2. Each DUT includes four IGBTs and two freewheel diodes on the DBC with silver-sintered die-attaches. Additionally, the DBC is directly mounted on the heatsink by pressure contacts and pre-applied thermal grease without lead frame. This allows to target the degradation only at the top side connection, made by traditional aluminum wire bonds, and to minimize degradation at other layers of the module. All controls and measurements are realized with a spring contact system, in order to ensure secure and even pressure. A specially designed printed circuit board (PCB) interface card is mounted on each module to access the measurement of the drop voltage V_{CE} and the control of the gate voltage V_{GE}.

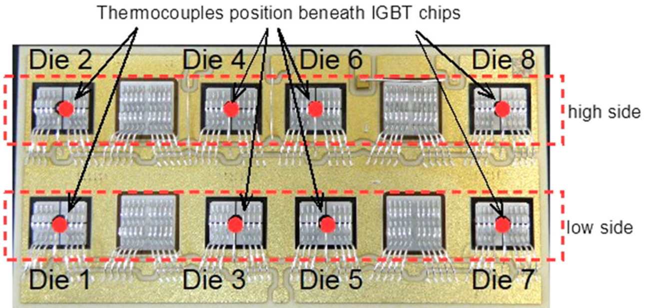

Fig. 2. Central leg of module SKIM63.

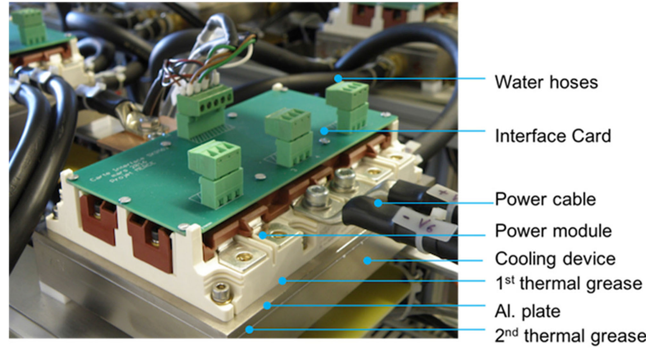

Fig. 3. Mounting detail of the SKIM63 module on the heatsink.

In order to reach high-temperature swing levels (110 °C), a 5-mm-thick aluminum plate is inserted between the module and the cooling device (cf., Fig. 3). A thermal grease layer is deposited between the module and the aluminum plate. The test modules are also mounted on the coolers, which are designed to respect the homogeneity of water flow rates.

B. Description of the DC Power Cycling Test Bench

The developed dc test bench is capable of performing tests on two groups of three power modules under two independent conditions. This is done in order to parallelize the tests because of the large number of tests to be performed (see Table I). For this purpose, the test bench includes two power supplies AMREL 16 V–600 A (SPS16-600-K0E3). Each one supplies the dc current for each group of modules. The schematic power circuit for each group of the test bench is shown in Fig. 4. The switching system is managed by a Micro830 programmable controller so that only one module, for each group, conducts at any time. The current setting is also controlled by the Micro830. The load current is measured by current sensors. All electrical and

TABLE I
PCT TEST CONDITIONS

(S) : Short cycles (3s) **(L)** : Long cycles (20s)		**ΔTj**		
		70°C	**90°C**	**110°C**
Tjmin	**55°C**	Group A(S) Group A(L)	Group B(S) Group B(L)	Group C(S) Group C(L)
	35°C	Group D(S) Group D(L)	Group E(S) Group E(L)	Group F(S) Group F(L)

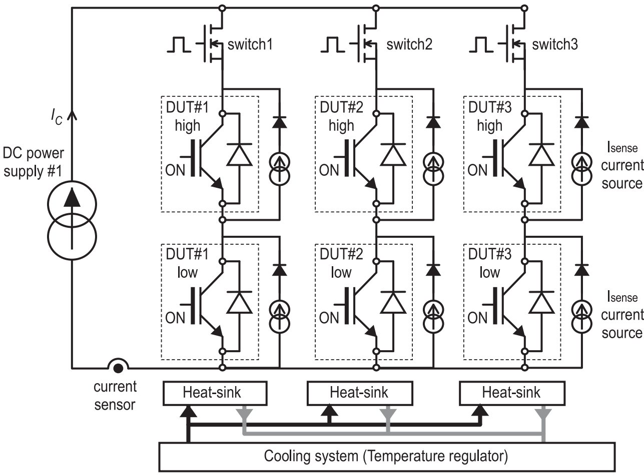

Fig. 4. Schematic power circuit for one group.

TABLE II
COMPARATIVE PCT TEST CONDITIONS

Test conditions	This paper	Ref. [4]
PCT strategy	Constant ΔT_J	Constant ΔI
ΔT_J (K)	110, 90, 70	130, 110, 90, 70
T_{JMIN} (°C)	35	40
t_{ON} (s) / t_{OFF} (s)	3 / 6	2 / 2

thermal measurements are monitored and recorded with a data acquisition system (Dewetron). The switching sequence is controlled by an electrical circuit using auxilliary power MOSFETs. A permanent low current ($I_{\rm SENSE} = 50$ mA) is flowing through the DUTs in order to get the junction temperature (T_j) by the TSEP, i.e., the collector–emitter voltage ($V_{\rm CE}$ @ $V_{\rm GE} = 15$ V).

The case temperature, below each IGBT chip of the central leg, and inlet water temperature are measured by close thermocouples for evaluating junction-to-case ($R_{\rm THJC}$) and junction-to-water ($R_{\rm THJW}$) thermal resistances. In order to highlight the effect of thermal stress factors on the power module lifetime, a total of 12 tests are performed, based on a fractional experimental design considering three factors: junction temperature swing (ΔT_j), minimum junction temperature ($T_{J\rm MIN}$), and power-ON time ($t_{\rm ON}$), see Table II. The test conditions are defined taking into consideration the maximum operating temperature of the SKIM63 module (175 °C). Furthermore, the minimum junction temperature is kept above the dew point temperature (15 °C) to avoid problems due to moisture and humidity.

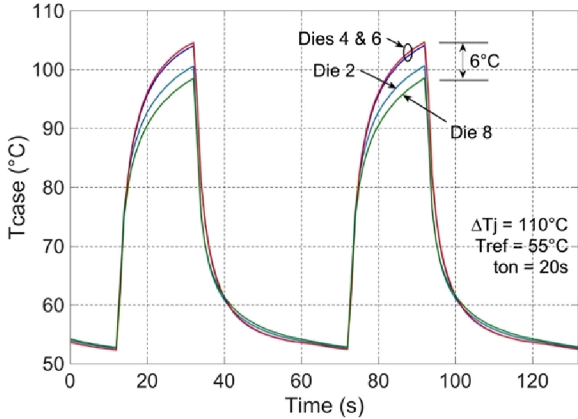

Fig. 5. Case temperature evolution under the chips of a high-side switch (see Fig. 2) during power cycles ($\Delta T_j = 110$ °C, $t_{\rm ON} = 20$ s).

Two different power-ON duration tests were performed in order to investigate the effect of this parameter on the lifetime and on the degradation process: short cycles ($t_{\rm ON} = 3$ s, $t_{\rm OFF} = 6$ s) and long cycles ($t_{\rm ON} = 20$ s, $t_{\rm OFF} = 40$ s). It has been verified that both the long and short cycles have led to the same damage and failure mode, i.e., at the top-side interconnection, and no degradation has been produced at the die attach. The power-OFF duration ($t_{\rm OFF}$) is twice as long as the power-ON duration ($t_{\rm ON}$) in order to reach the reference temperature of the cooling system at the end of each power cycle. The load current I_L and water temperature T_W are defined as setting parameters. For the best temperature swing regulation, initial gate voltage is set around 11 V. For security reason, stop conditions (warnings) were implemented on the test bench. These alarms are managed by the data recorder (Dewetron) and Micro830 programmable controller. Conditions and criteria for these alarms are given as follows.

1) Abnormal drop voltage ($V_{\rm CE} > 3.1$ V).
2) Loss of ΔT_j control ($V_{\rm GE} < 10.4$ V).
3) Excessive case temperature (depending on test conditions).
4) Excessive junction temperature ($T_{J\rm MAX} > 170$ °C).

A possible problem, due to a reduction in gate voltage with paralleled IGBT dies, could lead to a small decrease in the positive temperature coefficient and to a less homogeneous current and temperature distributions among the dies. As shown in Fig. 2, the substrates used here have four IGBT chips per switch. The junction temperature ($T_{\rm j}$) being measured by the TSEP, which gives an average value over the set of four chips, it is impossible to have the distribution on each of them. Fortunately, case temperatures are measured under each chip by thermocouples, very close to the chips as there is no base plate. As illustrated, Fig. 5 shows that the maximum case temperatures ($T_{C\text{-max}}$) of the two central chips are 6 °C hotter than the lateral ones during PCTs for the worst-case test conditions ($\Delta T_j = 110$ °C, $t_{\rm ON} = 20$ s, $T_{\rm ref} = 55$ °C). This is, of course, a consequence of a temperature difference in chips, which is mainly due to thermal coupling between the central chips. In addition, if a significant current imbalance is reached between

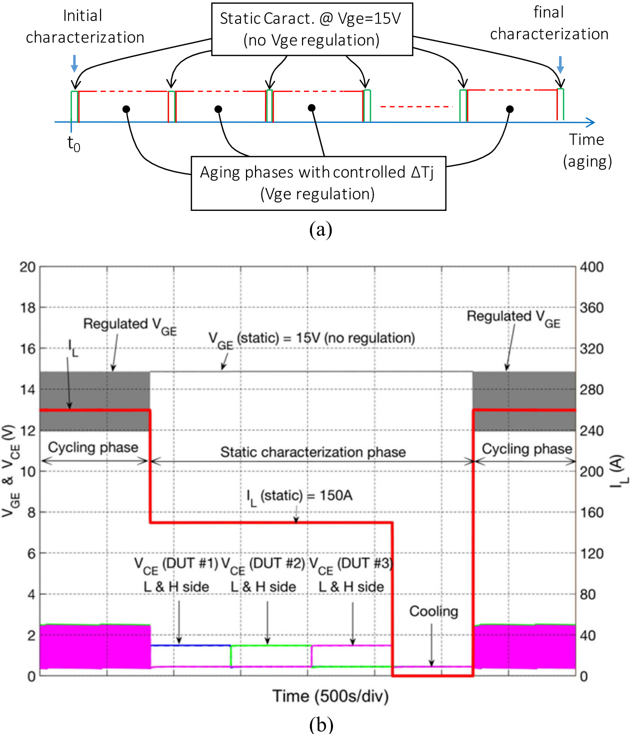

Fig. 6. Aging/characterizations phases' procedure. (a) Schematic diagram of aging/characterization phases. (b) Load current (I_L), forward drop voltage (V_{CE}), and gate voltage (V_{GE}) measurement during a characterization phase between two cycling phases.

the chips, it would lead to more severely damaging the chips that have the highest stress (central ones) and therefore increasing their collector–emitter voltage (V_{CE}). This would result in rebalancing the current to the lateral chips. In conclusion, the results obtained show that the possible imbalance of current directly due to the reduction of V_{GE} (between 15 and 11 V) is not significant.

The chosen aging indicators are collector–emitter voltage drop (V_{CE}) and junction-to-water thermal resistance (R_{THJW}). These parameters are always measured under the same conditions before, during, and after the aging in a static characterization phase. During the power cycling, the aging is automatically and regularly interrupted and the characterizations of aging indicators are performed, as shown in Fig. 6(a). During this "characterization phase," the control of ΔT_j is interrupted, the gate voltage V_{GE} is set to 15 V and the load current I_L is set to 150 A, as shown in Fig. 6(b). This current is injected alternatively in each module during 10 min and then switched-OFF for a cooling phase.

A characterization current I_{SENSE} of 50 mA, permanently injected into each DUT, allows to monitor the junction temperature T_j by the TSEP (V_{CE}) measurement. This is done in order to determine the maximum junction temperature $T_{J\mathrm{MAX}}$ at the end of each heating phase just after the current is switched-OFF when thermal equilibrium is reached.

It should be noted that the measured voltage V_{CE} may possibly include a contribution ($\Delta V_{\mathrm{CE_therm}}$) due to an increase in thermal resistance from possible delamination of the die attach or other layers below. This contribution needs to be removed from the measured V_{CE} in order to detect only the contribution due to top-die interconnection degradations. Any delamination is detected by thermal resistance measurements. Thus, a correction on the measured V_{CE} is done ($V_{\mathrm{CE_cor}}$) that represents only the degradations related to top metal and bonding wires contacts.

For the estimation of $\Delta V_{\mathrm{CE_therm}}$, a thermal calibration is carried out at the beginning of PCT at the same conditions as the aging indicators characterizations ($I_L = 150$ A and $V_{\mathrm{GE}} = 15$ V). The drop voltage V_{CE} is recorded and plotted in a temperature range from 75 °C to 90 °C after reaching thermal equilibrium. This variation in temperature is obtained by modifying the inlet water flow to change the cooling performance. The obtained dependence between the junction temperature (T_j) and the drop voltage (V_{CE}) is linear and offers an average corrective coefficient of V_{CE} about 1.19 mV/K. This enables a corrective $\Delta V_{\mathrm{CE_therm}}$ to account for the possible difference between T_{j0} and T_j, respectively, the measured junction temperatures at initial and actual characterizations. As expected, all tests have led to insignificant R_{th} increase, so that $\Delta V_{\mathrm{CE_therm}} \approx 0$ and so $V_{\mathrm{CE_cor}} \approx V_{\mathrm{CE}}$.

A test on a module is stopped as soon as one of the aging criteria is met by one of the two DUTs in series in the same module.

1) The corrected drop voltage $V_{\mathrm{CE_cor}}$ reaches 5% increase.
2) The junction-to-water thermal resistance R_{THJW} reaches 20% increase.

IV. Power Cycling Test Results

As expected, no delamination occurred during aging, especially at the sintering layer used for the die attach. This result is confirmed by scanning acoustic microscopy (SAM) analyses performed after the aging for both long [see Fig. 7(a)] and short cycling [see Fig. 7(b)]. Hence, the degradation of wire bonds is the only failure mode.

All cycling tests were stopped due to the failure condition on the corrected drop voltage $V_{\mathrm{CE_cor}}$, corresponding to an increase of more than 5%. Within the test modules, the device failed arbitrarily in either low side or high side or both. The equivalent probability of the defective side proves that thermal coupling is homogeneous between the high and low side of the DUTs.

After the aging tests, the wire bonds degradations are investigated by digital microscopy. An example of the failure analysis results, performed on a module of the campaign B(S) (see Table I), is summarized in Fig. 8(a). Wire bond lift-off is the only failure mechanism detected and no heel cracks were observed. Furthermore, the lifted bond wires have been found mainly at the center IGBT dies of the failed side in all cases, as indicated by red rectangles of dies 4 and 6. The number of defective bond pads of each side seems to be coherent with the corrected V_{CE} rates. Fig. 8(b) shows a local view of four lifted-off bond wires of die 6. This can be explained by the mutual thermal effects between the two center chips, which lead to higher thermal stress. This observation has been verified by case temperature under the four central dies of the low and high side. As already mentioned,

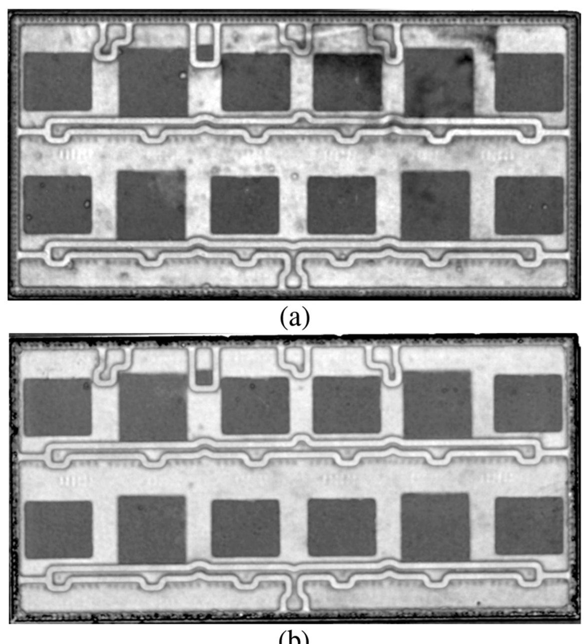

Fig. 7. SAM image of a SKIM63 module under long cycling. (a) Test conditions: $T_{J\,\mathrm{MIN}} = 35\ ^\circ\mathrm{C}$, $\Delta T_j = 110\ ^\circ\mathrm{C}$, $t_{\mathrm{ON}}/t_{\mathrm{OFF}} = 20$ s/40 s, and under short cycling. (b) Test conditions: $T_{J\,\mathrm{MIN}} = 55\ ^\circ\mathrm{C}$, $\Delta T_j = 90\ ^\circ\mathrm{C}$, and $t_{\mathrm{ON}}/t_{\mathrm{OFF}} = 3$ s/6 s.

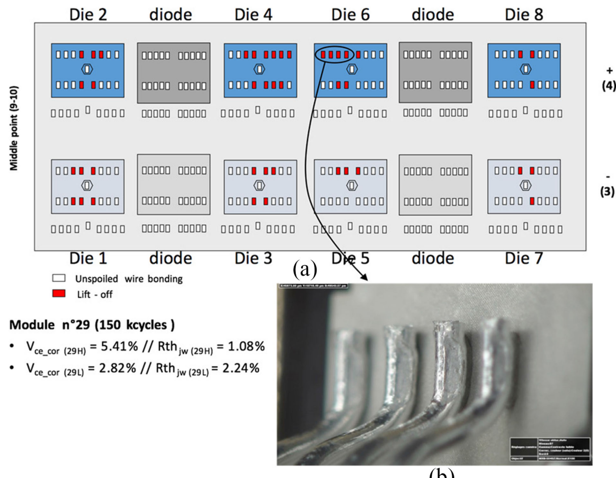

Fig. 8. Failure analysis of a module of campaign B(S), characterized by $T_{J\,\mathrm{MIN}} = 55\ ^\circ\mathrm{C}$, $\Delta T_j = 90\ ^\circ\mathrm{C}$, $t_{\mathrm{ON}} = 3$ s, $t_{\mathrm{OFF}} = 6$ s, $I_C = 240$ A, and $T_W = 43\ ^\circ\mathrm{C}$.

during the PCT, case temperature measured by thermocouples is about 5–6 °C higher at center dies than in corner ones for highest stress conditions.

As results illustrative of the aging process, Figs. 9, 10, and 11 show the increase of the relative variation of V_{CE} between the initial and the current values ($\Delta V_{\mathrm{CE}}/V_{\mathrm{CE}}$) during tests for the three swing temperatures $\Delta T_j = 110\ ^\circ\mathrm{C}$, $90\ ^\circ\mathrm{C}$, and $70\ ^\circ\mathrm{C}$, respectively, with all of other conditions remaining constants ($t_{\mathrm{ON}} = 3\ \mathrm{s}/t_{\mathrm{OFF}} = 6$ s, $T_{J\,\mathrm{MIN}} = 55\ ^\circ\mathrm{C}$). All results concerning

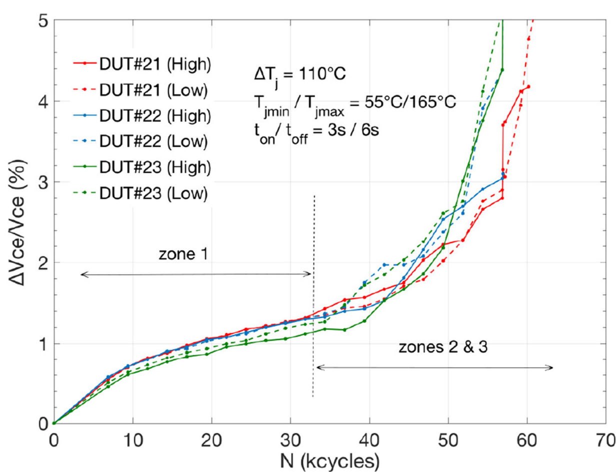

Fig. 9. Evolution of corrected collector–emitter voltage of the three modules of test C(S), $T_{J\,\mathrm{MIN}} = 55\ ^\circ\mathrm{C}$, $\Delta T_j = 110\ ^\circ\mathrm{C}$, $t_{\mathrm{ON}} = 3$ s, $t_{\mathrm{OFF}} = 6$ s, $I_L = 260$ A, and $T_W = 40\ ^\circ\mathrm{C}$.

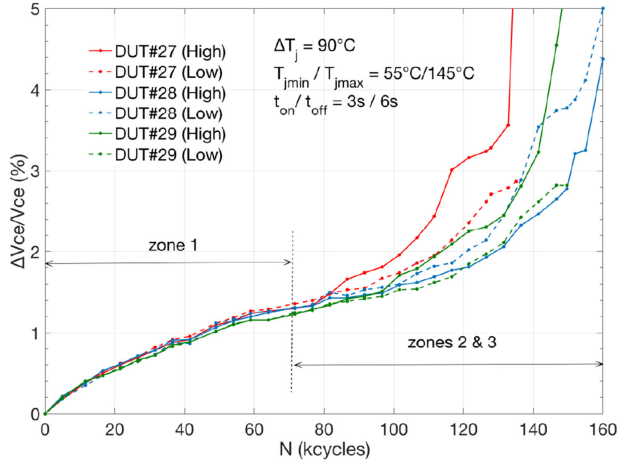

Fig. 10. Evolution of corrected collector–emitter voltage of the three modules of test B(S), $T_{J\,\mathrm{MIN}} = 55\ ^\circ\mathrm{C}$, $\Delta T_j = 90\ ^\circ\mathrm{C}$, $t_{\mathrm{ON}} = 3$ s, $t_{\mathrm{OFF}} = 6$ s, $I_L = 240$ A, and $T_W = 43\ ^\circ\mathrm{C}$.

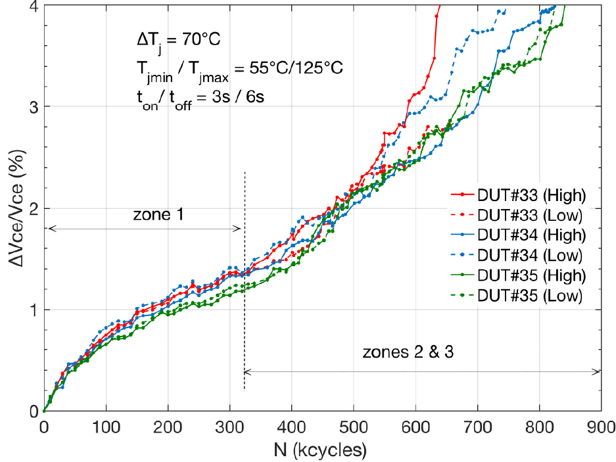

Fig. 11. Evolution of corrected collector–emitter voltage of the three modules of test A(S), $T_{J\,\mathrm{MIN}} = 55\ ^\circ\mathrm{C}$, $\Delta T_j = 70\ ^\circ\mathrm{C}$, $t_{\mathrm{ON}} = 3$ s, $t_{\mathrm{OFF}} = 6$ s, $I_L = 210$ A, and $T_W = 46\ ^\circ\mathrm{C}$.

the three DUT modules are shown, both on the high sides (solid lines) and low sides (dotted lines) of each leg.

These figures highlight the following findings.

1) The increase in V_{CE} begins at the very beginning of the aging process. This indicates that a degradation process starts from the first cycle whatever the stress condition.
2) Three different regimes can clearly be observed from all curves.
   a) The first one (zone 1) shows a $\Delta V_{CE}/V_{CE}$ increase with a saturation-like shape until a value around 1.3%.
   b) The second regime (zone 2) exhibits rather an exponential increase of $\Delta V_{CE}/V_{CE}$ until approximately 3%.
   c) The third regime has been already reported by many authors and shows a sharp and stepped V_{CE} increase, which appears when bond-wire lift-off occurs at the final stage of the aging [3], [8], [15].

In these figures, zone 1 is remarkably reproducible for all DUTs under the same test conditions. It starts from the beginning and ends at approximately the same increase of the relative variation value in V_{CE} (around 1.3%). More dispersions of the increase in V_{CE} are visible in zone 2 (see Fig. 10). This is why zones 2 and 3 are not clearly distinguished, as this is only possible for individual curves.

These observations suggest that from the very beginning, three different degradation processes take place and can be clearly detected. In the following, some hypotheses and interpretations are proposed but they still have to be confirmed by specific experimental characterizations. At the very beginning, the first regime could be the expression of the degradation of the top metal (reconstruction), which could lead to an increase of $\Delta V_{CE}/V_{CE}$ with a saturation effect on this parameter through an increase of the top-metal resistance. Then, a second degradation mechanism is superimposed, which could be due to the crack initiation and propagation of the wire-bond contact with the top metallization. The observed exponential-like increase of $\Delta V_{CE}/V_{CE}$ is coherent with a regular increase of the electrical contact resistance due to the crack propagation at the bond contact. At the end, the final step is the bond-wire lift-off as traditionally observed and clearly expressed by sharp and stepped V_{CE} increase.

As an additional finding, if the previous curves (from Figs. 9–11) are plotted in the same graph with a normalized *x*-axis to number of cycle to failure (N_f), the obtained figure highlights the following remarkable finding: globally, the shape of the V_{CE} increase does not depend on ΔT_j. This is visible in Fig. 12 but for the sake of clarity, only one of the six curves for each ΔT_j condition is represented.

This suggests that for the constant ΔT_j power cycling strategy not only are the same damage mechanisms taking place at the same N/N_f ratio of the aging process, but also that a linear cumulative damage law could be a reasonable assumption.

The results of ten test campaigns allow to generate the evolution laws $N_f(\Delta T_j)$ for different combinations $T_{JMIN} - t_{ON}$ (see Fig. 13). As a result, it can be observed that the slopes are systematically increased in the range $\Delta T_j = [70 - 90\ °C]$ comparatively to those in the range [90–110 °C] whatever T_{JMIN} and t_{ON}. This can be possibly explained by the missing positive feedback between stresses and damages, as shown in Section V. Specific numerical studies, including the damages effects on the electro-thermo-mechanical behavior of the devices, have to be performed in order to understand how this feedback acts for a given stress level. It should also provide information on how this feedback acts for low ΔT_j conditions, i.e., under field operating conditions, and also on the possible interactions between stresses, if any.

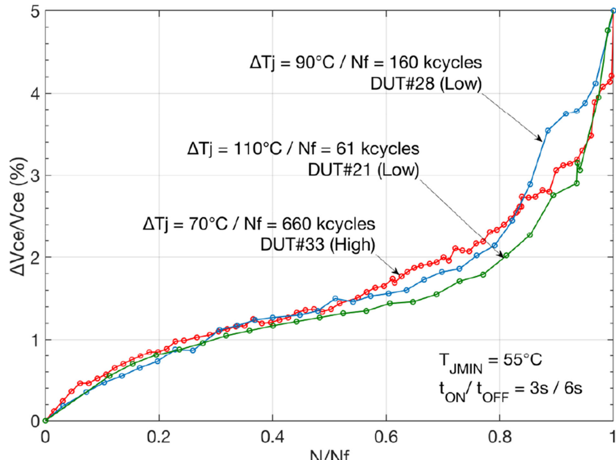

Fig. 12. Evolution of corrected collector–emitter voltage cycle to failure graph ($T_{JMIN} = 55\ °C$, $\Delta T_j = 70\ °C$, 90 °C, and 110 °C).

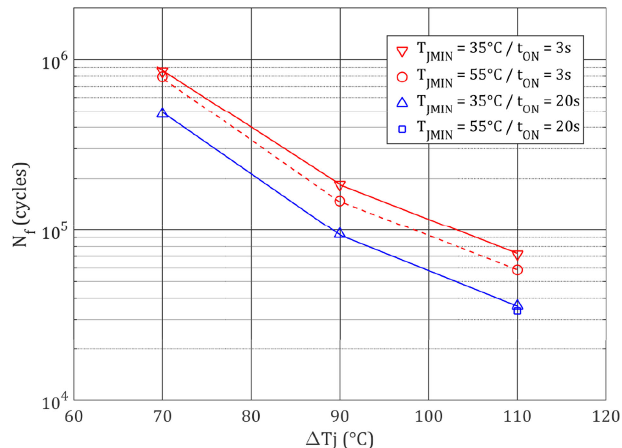

Fig. 13. Dependence of N_f on setting parameters ΔT_j, T_{JMIN}, and t_{ON}.

Finally, in spite of the slope change, a constant factor between 1.8 and 2 is found between cycles to failure (N_f) given by short PCTs ($t_{ON} = 3$ s) and long PCTs ($t_{ON} = 20$ s) under the same conditions of ΔT_j at $T_{JMIN} = 35\ °C$. This factor is coherent with the results published in [7] and [10].

V. Discussion

The obtained results, in Fig. 13, are performed at test conditions relatively close to those presented in [4], which have been obtained using the "constant ΔI" strategy, as shown in Table II.

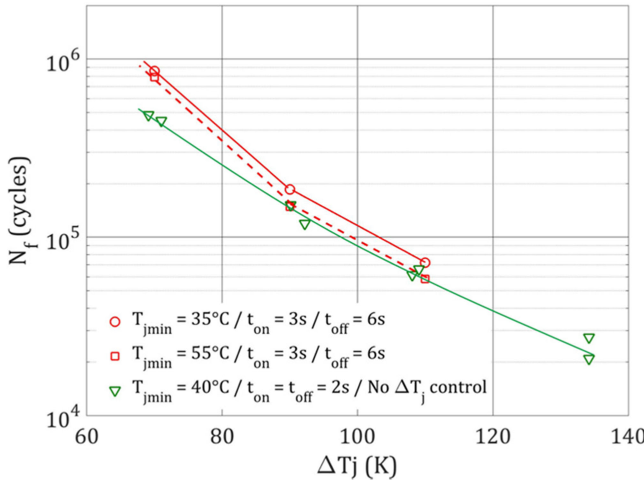

Fig. 14. Comparison between our PCT results (in red) and published results in [4] (in green).

The parameter $t_{\rm OFF}$ does not have any direct influence on number of cycles to failure ($N_{\rm f}$), and therefore, it is interesting to compare obtained results and to analyze the influence of the tests strategies.

The comparison between these results (in red markers) and those in [4] (in green markers) is plotted in Fig. 14.

First of all, if one considers the results from this paper with $T_{J\rm MIN}$ 35 °C (solid red line) and those in [4] for $T_{J\rm MIN}$ 40 °C (solid green line), it can be noted that the latter results are relatively close in the range $\Delta T_j = [90 - 110\ ^{\circ}\text{C}]$ but slightly lower for $\Delta T_j = 70\ ^{\circ}\text{C}$.

For a relevant comparison of these results, since the other parameters are almost the same, two factors have to be considered: $t_{\rm ON}$ and test strategy. On the one hand, the smaller the $t_{\rm ON}$, the higher the lifetime should be, on the other hand, "constant ΔI" should lead to lower lifetimes. If we consider the test strategy, the N_f values obtained in this paper should be greater than those in [4], but it is the contrary if we consider $t_{\rm ON}$. In view of the comparative results in Fig. 14, the test strategy seems to have more influence than $t_{\rm ON}$ in the lifetime.

However, there is one factor that can potentially hinder this comparison. As ΔT_j is not constant in [4], this parameter will rise during PCT, and probably $T_{J\rm MIN}$ as well considering the insufficient cooling time. In other words, the lower lifetimes observed in [4] are caused mainly by the test strategy that leads to gradual increase of ΔT_j during aging, and also because of the probable increase of $T_{J\rm MIN}$ caused by the small value of $t_{\rm OFF}$.

In addition, not only the values but also the slopes in the range $\Delta T_j = [\ 90\text{–}110^{\circ}\text{C}]$ are quite identical for both tests before divergence for lower ΔT_j. This suggests that the feedback impacts between stresses and damages encountered in the "constant ΔI" strategy are more important for low ΔT_j (i.e., high $N_{\rm f}$) and almost negligible for high ΔT_j (i.e., low $N_{\rm f}$). A possible interpretation is that for tests with high stresses, the interaction with the damage does not have the time to take place and to produce these effects. While for lower values on ΔT_j, these interactions and their effects take place largely, leading to higher discrepancies in lifetime between the two tests strategies.

These results suggest that in the case of high stresses, the "constant ΔT_j" strategy with $V_{\rm GE}$ regulation gives values close to a "constant ΔI" strategy but that the extrapolation toward low values of ΔT_j remains questionable for the first strategy. It should be noted that these conclusions could only be possible by performing constant ΔT_j tests by $V_{\rm GE}$ regulation that is the best way to compare correctly the results with a "constant ΔI" strategy. So far, this type of comparison has been done with a "constant ΔT_j" strategy by $t_{\rm ON}$ regulation that would produce different results to those obtained in this paper. Of course, this discussion does not take into account the possible inaccuracies in results on PCT tests both in [4] and in this paper.

Beyond these comparisons of PCTs in the dc mode, it would be interesting to know how advanced PCTs, in the pulsewidth modulation mode [18]–[20], would position themselves in relation to these dc tests.

VI. Conclusion

In this paper, power cycling with the "constant ΔT_j" strategy has been performed by using gate voltage ($V_{\rm GE}$) regulation in order to correctly compare results with other PCT strategies. The tests have been done specifically on SKIM63 modules that are well-suited to investigate the effects of thermal stresses (ΔT_j) on top-metal and bond-wire contacts degradations. These tests have also been used in order to compare results on the same modules in a "constant ΔI" strategy with quite similar stress conditions.

As expected, the results have led to bond-wires lift-off failures only. From aging indicator on the collector–emitter voltage ($V_{\rm CE}$), the results clearly show three regimes of degradation whatever the applied stress conditions. As an additional finding, the results suggest a reasonable assumption of linear cumulative damage law for a constant ΔT_j power cycling strategy. However, this has to be confirmed with further tests.

Comparative results in "constant ΔT_j" and "constant ΔI" PCTs have shown that the feedback impacts between stresses and damages encountered in the second strategy are more important for low ΔT_j than for high ΔT_j. Furthermore, the results show that in case of high stresses, the "constant ΔT_j" strategy with $V_{\rm GE}$ regulation gives values close to a "constant ΔI" strategy but that the extrapolation toward low values of ΔT_j remains questionable for the first strategy.

These results and assumptions need to be completed by further numerical analyses by taking into account such stress-degradation interactions.

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