Letters

A Single Gate Driver Based Solid-State Circuit Breaker Using Series Connected SiC MOSFETs

Yu Ren, *Student Member, IEEE*, Xu Yang, *Member, IEEE*, Fan Zhang, *Student Member, IEEE*, Fred Wang, *Fellow, IEEE*, Leon M. Tolbert, *Fellow, IEEE*, and Yunqing Pei, *Member, IEEE*

***Abstract*—Semiconductor devices based solid-state circuit breakers (SSCBs) are promising in the dc power distribution system as protective equipment for their ultrashort action time. This letter proposes a topology of SSCB using series connected silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs), which only requires a single isolated gate driver. The SSCB has very low cost and high reliability because it only has 13 components including passive components and diodes apart from two SiC MOSFETs to achieve both balanced voltage distribution during short-circuit interruption duration and reliable positive gate voltage during ON-state. The SSCB prototype is built and experimentally verified to interrupt 75 A short-circuit current under the dc-bus voltage of 1200 V within 1.5 μs.**

***Index Terms*—Series-connection, silicon carbide (SiC) metal oxide semiconductor field effect transistor (MOSFET), solid-state circuit breaker (SSCB), voltage balancing, wide-band-gap device.**

I. Introduction

CIRCUIT breakers protect both alternating current (ac) and direct current (dc) power distribution systems from damage caused by overload or short circuit [1], [2]. Compared with a traditional mechanical circuit breaker, semiconductor devices based solid-sate circuit breakers show more promise for dc power distribution which has no natural zero-crossing in

Manuscript received June 1, 2018; revised July 5, 2018; accepted July 22, 2018. Date of publication July 31, 2018; date of current version February 5, 2019. This work was supported in part by the National Key Basic Research Program of China (973 Program) under projects 2015CB251001 and 2015CB251004. The work of Y. Ren during the visit to the University of Tennessee, Knoxville, TN, USA, was supported by China Scholarship Council (CSC). *(Corresponding author: Xu Yang.)*

Y. Ren is with the State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Xi'an 710049, China, and also with the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN 37996-2250 USA (e-mail:

II. Structure of the Proposed SSCB

The topology of the proposed SSCB is illustrated in Fig. 1. It is designed based on the novel gate control circuit for two series connected SiC MOSFETs, which has been proposed in our previous paper [17]. Several changes have been made to make the circuit operate as SSCB. Two varistors V_{ar1} and V_{ar2}, two RC snubbers, and a high voltage diode D_1 have been added to the circuit. Besides, additional gate resistor R_{g3} has been added to the gate loop of SiC device M_2. To reduce the cost, only one Zener diode is applied to guarantee the gate reliability of M_2 rather than two reverse series connected Zener diodes in our previous paper. The function of these components contained in the SSCB will be described in detail in the following part. The SSCB is connected to the grid with power terminals P and N and can be directly controlled with control terminals A and B.

To clarify the function of these passive components and diodes, component parts with the same function have been marked in the same background color. Varistors V_{ar1} and V_{ar2} absorb the interruption energy stored in the current limiting inductor which will be shown in Fig. 3(a) to suppress the overvoltage across M_1 and M_2. R_1 and R_2 assure the balanced voltage distribution across M_1 and M_2 during OFF-state. RC snubbers benefit the transient voltage balancing during switching processes. C_1 provides the required gate charge for M_2. C_2 is added to the circuit to compensate the influence of C_1 on the transient unbalanced voltage distribution. During the ON-state, D_1 provides the current path for the gate circuit of M_2 to guarantee the reliable positive gate voltage. Zener diodes Z_{d1}–Z_{d3} prevent the gate voltage from exceeding the safe range. R_{g1}–R_{g3} provide the damping for gate voltage oscillation.

The proposed series connected SiC MOSFETs based SSCB is cost effective and relatively robust compared with conventional voltage balancing methods based SSCB and this is beneficial to large-scale use of SiC MOSFET SSCB. As shown in Fig. 2, the two series connected SiC MOSFETs based SSCB with conventional voltage balancing methods requires two gate control sets for two devices. Each gate control set contains isolated power supply, gate signal isolation, and a driver integrated circuit (IC). The voltage unbalance issue resulted by different device parameters and unsynchronized gate signal need to be handled very well. There are several methods such as active gate control, active clamping circuits, and passive snubber circuits can be used to minimize voltage unbalance across individual devices in series strings of SiC MOSFETs [18], [19]. Comparatively, only 13 components including passive components and diodes can achieve the reliable gate control and voltage balance which will make the proposed SSCB have lower cost and higher robustness.

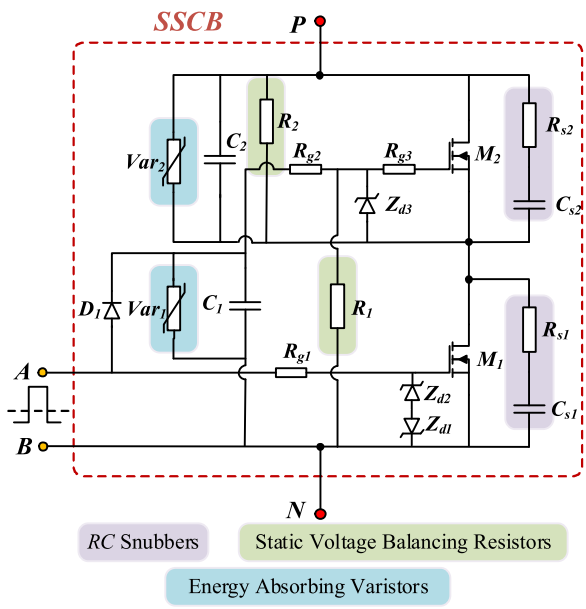

Fig. 1. Topology of proposed series connected SiC MOSFETs based SSCB.

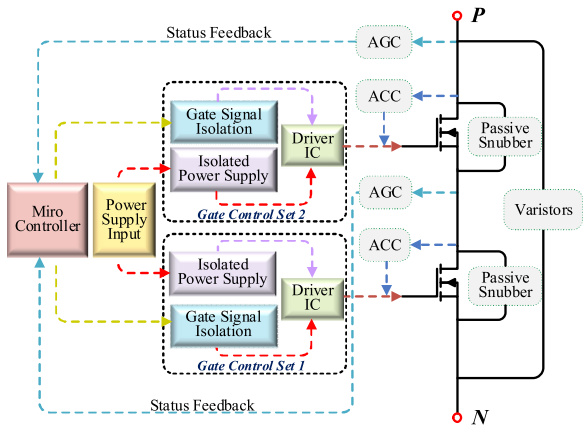

Fig. 2. Simplified architecture of two series connected SiC MOSFETs based SSCB with conventional voltage balancing methods.

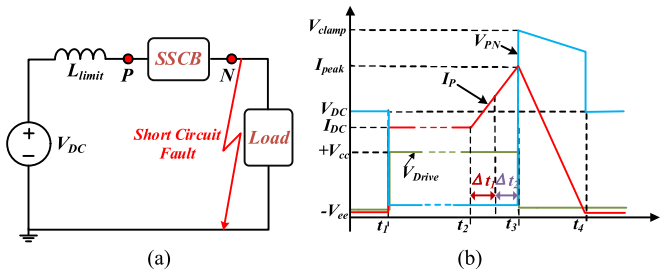

Fig. 3. (a) Simplified SSCB application circuit. (b) Typical operation waveforms of SSCB.

III. Operation Principles

The basic operation principles have been elaborated in published paper by authors [17]. This letter only focuses on the changes which have been made and the operation principles under specific working condition as SSCB.

The simplified application circuit of SSCB is shown in Fig. 3(a). Typical waveforms are given conceptually in Fig. 3(b). At the time of t_1, the SSCB is turned-ON. Then the load current I_{DC} flows through the SSCB from dc power supply to the load. Suddenly, the short circuit fault occurs inside the circuit at t_2. Consequently, the current through the SSCB rise rapidly. After the detection time and some control delay, the SSCB starts to interrupt the fault current at t_3. The time interval between t_2 and t_3 includes the response time of the protection Δt_1, and the action

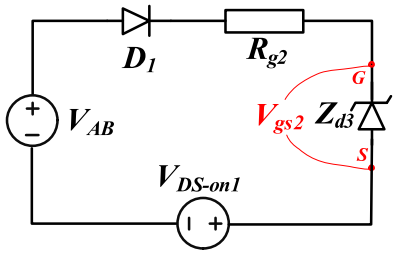

Fig. 4. Equivalent circuit of driver loop for M_2 during ON-state.

time of SSCB Δt_2. At t_3, the current through SSCB reaches the maximum value I_{peak} and this value should be lower than maximum current breaking capability of SSCB. The voltage across the SSCB is then clamped by varistors to the maximum value V_{clamp}. The short circuit energy will be absorbed by the varistors during the period before the interruption process finishes at t_4. From t_4, the SSCB withstand the dc-bus voltage V_{DC}. Overall, the largest two challenges for proposed SSCB are that device M_2 should have reliable positive gate voltage during ON-state and two SiC MOSFETs devices should have symmetric voltage distribution during fault current interruption process.

A. ON-state

To assure M_2 has reliable positive gate voltage, the high voltage diode D_1 has been added to the circuit. It provides the gate current for M_2 from the standard gate driver. The equivalent driver circuit of M_2 is shown in Fig. 4. $V_{\text{DS}-\text{on1}}$ represents the conduction voltage drop of M_1. The positive gate voltage provided by the outside gate driver is represented by V_{AB}. Then, the gate voltage of M_2 equals to the Zener voltage of Z_{d3} when the following relationship is established:

$$I_{Z(\min)} \leq \frac{V_{AB} - V_{\text{DS}-\text{on1}} - V_D}{R_{g2}} \tag{1}$$

where V_D is the forward voltage drop of D_1 and $I_{z(\min)}$ represents the minimum Zener current. Otherwise, the gate voltage of M_2 can be defined by

$$V_{gs-M2} = V_{AB} - V_{\text{DS}-\text{on1}} - V_D - i_{\text{loop}} \cdot R_{g2} \tag{2}$$

where I_{loop} is the current flow inside the circuit. Therefore, the reliable gate voltage can be guaranteed in both cases.

B. Fault Current Interruption Process

To illustrate the fault current interruption process more clearly, some typical current paths have been shown in Fig. 5. As shown in Fig. 3(b), the SSCB begins to handle the short-circuit fault after the response time of the protection Δt_1 at $t_2 + \Delta t_1$, the gate voltage of M_1 starts to decrease. Therefore, M_1 starts the process of turning-OFF. Then, C_1 will be charged with i_1 shown in Fig. 5. Consequently, the gate capacitor of M_2 will be discharged which means that M_2 starts the process of turning-OFF the same as M_1. As shown in Fig. 3(b), the inductive current limiter stores a lot of energy during the time interval between t_2 and t_3. At t_3, two series connected devices are all turned OFF. The energy stored in the inductive limiter will transfer to the

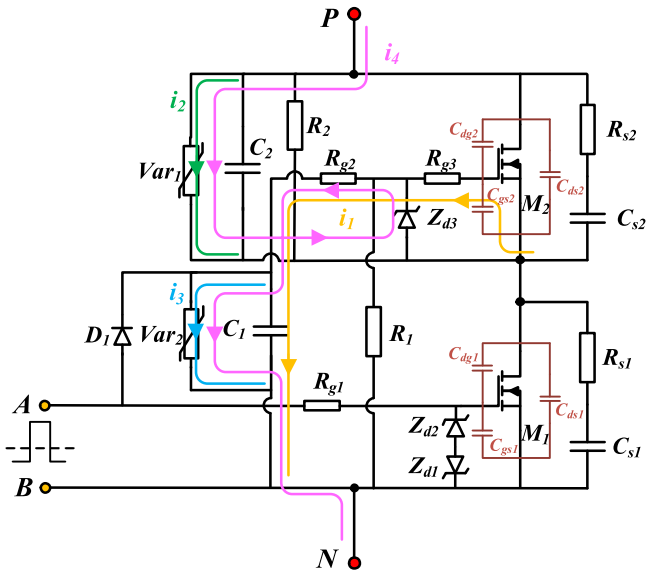

Fig. 5. Typical current paths during fault current interruption process.

capacitors C_{ds} and C_{gd} of M_1 and M_2, which will lead to the rapid voltage rise. At the same time, the voltage across both varistors V_{ar1} and V_{ar2} and capacitors C_1 and C_2 all rise rapidly and synchronously. When the voltage across both varistors V_{ar1} and V_{ar2} reaches the clamping limit voltage V_{limit} defined by their inherent electrical characteristics, their equivalent resistance will become very small. As a result, the energy stored in the components inside the SSCB will be dissipated in two varistors by current i_2 and i_3 separately. Residual energy stored in the inductor will transfer to varistors with current path i_4. The interruption process ends at t_4 when all short-circuit energy has been consumed by varistors thoroughly.

IV. Experimental Results

As mentioned previously, the proposed SSCB should verify both that there is reliable positive gate voltage for M_2 and it is feasible for short-circuit interruption. To experimentally demonstrate the effectiveness of this proposed SSCB, two tests have been conducted, and corresponding experiment circuits are shown in Fig. 6. The resistive load test circuit shown in Fig. 6(a) will be used to obtain the ON-state gate voltage. The positive time of gate control voltage T_{on1} should be up to several hours. The inductive load test circuit shown in Fig. 6(b) helps to verify the current interruption process. The gate control signal is one pulse signal and the positive time of gate control voltage T_{on2} is determined by

$$T_{\text{on2}} = \frac{I_{\text{peak}} \cdot L_{\text{limit}}}{V_{\text{DC}}}. \tag{3}$$

The SSCB prototype and experiment setup with inductive load are shown in Fig. 7(a) and (b), respectively. It should be noted that, the single standard gate driver board also has been embedded on the SSCB board to minimize the driver loop for M_1. The detailed parameters and descriptions of components

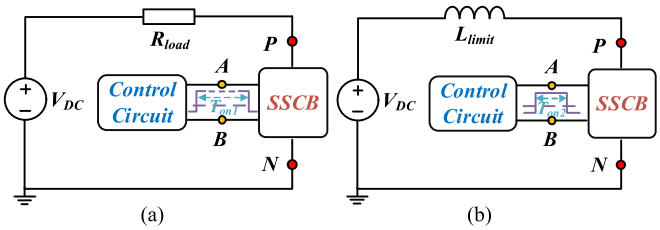

Fig. 6. Experiment circuits of the proposed SSCB. (a) With resistive load. (b) With inductive load.

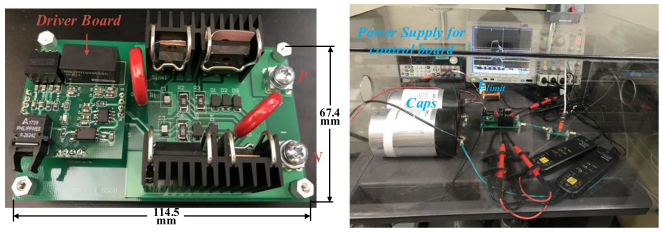

Fig. 7. (a) Photograph of SSCB prototype. (b) Photograph of experimental setup with inductive load.

TABLE I
PARAMETERS IN THE TEST

Symbol	Value	Descriptions
V_{DC}	800 V/1.2 kV	DC-bus voltage
L_{limit}	20 μH	current limiting inductor
M_1, M_2	1.7 kV, 72 A	C2M0045170D from Wolfspeed
R_{g1}	10 Ω	gate resistor of M_1
R_{g2}	2.2 Ω	gate resistor of M_2
R_{g3}	4.7 Ω	gate resistor of M_2
C_1	330 pF	driving capacitor of M_2
C_2	330 pF	voltage balancing capacitor of M_2
C_{s1}, C_{s2}	2.2 nF	capacitors of RC snubber
R_{s1}, R_{s2}	200 Ω	resistors of RC snubber
R_1, R_2	100 kΩ	static voltage balancing resistor
Z_{d1}	6.2 V	gate protection Zener diode
Z_{d2}, Z_{d3}	20 V	gate protection Zener diode
V_{ar1}, V_{ar2}	889.5 V, 6.5 kA	energy absorbing Varistors
D_1	2.2 kV, 30 A	providing gate current for M_2

contained in the SSCB topology are shown in Table I. Specifically, the SiC MOSFET chosen in the prototype is the most high-power rating discrete device available in the commercial market.

Fig. 8(a) shows the gate voltage waveforms of both devices with resistive load. Due to the limit of the dc power supply, they are tested under 1 A load current and waveforms captured after running for several hours with differential probes. Nevertheless, the reliable gate voltage for both devices can be verified.

The inductive load test results under the two cases are shown in Fig. 8(b) and (c). The current through the inductive load can be defined by ON-time T_{on} and dc-bus voltage. In the case shown in Fig. 8(b), the dc-bus voltage is 800 V and the maximum current is 50 A. In the case shown in Fig. 8(c), the dc-bus voltage is 1200 V and the maximum current is 75 A.

All voltage waveforms are recorded by differential-voltage probes, and the load current is measured by a current shunt. It

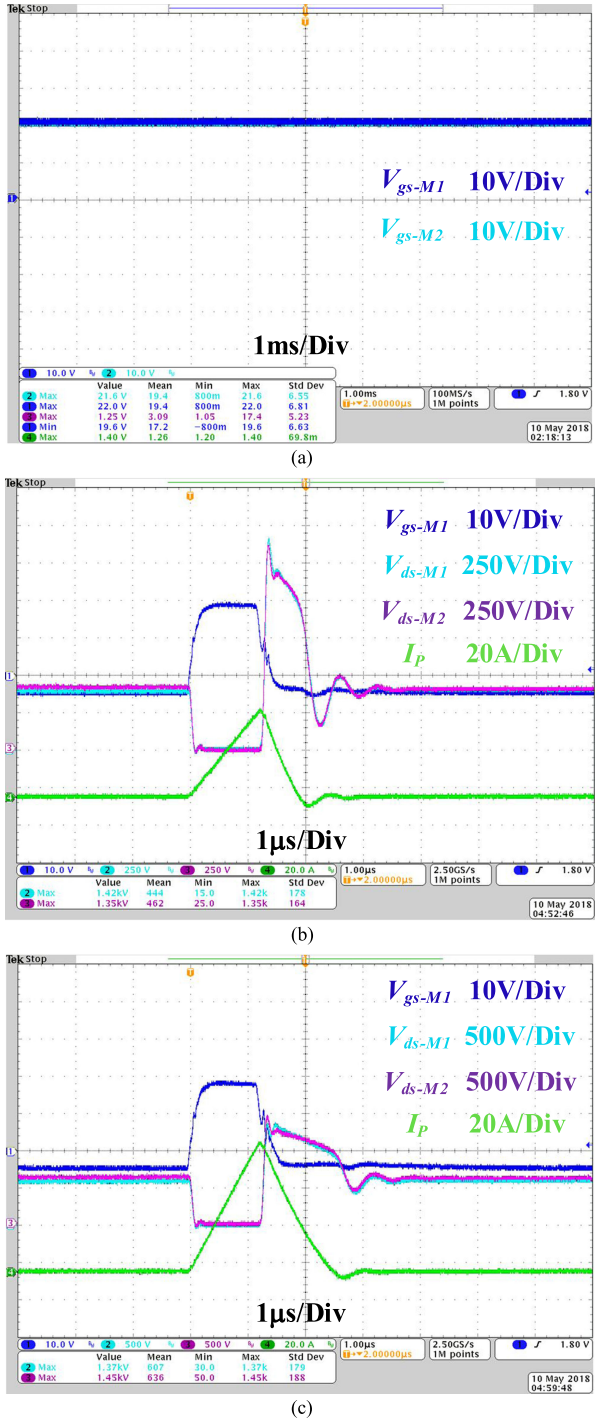

Fig. 8. (a) Experimental results of gate voltage during ON-steady-state with resistive load. (b) Experimental waveforms of the SSCB with inductive load under 800 V dc-bus voltage. (c) Experimental waveforms of the SSCB with inductive load under 1200 V dc-bus voltage.

should be noted that the drain-source voltage scale shown in Fig. 8(b) is 250 V/div and the value is 500 V/div, as shown in Fig. 8(c). The results reveal that the SSCB can successfully interrupt the current within 1 μs and 1.5 μs separately under the two cases. They are ultrasmall values compared with reported SSCBs in [15]. The highest V_{ds} voltage of both devices is much lower than the maximum blocking voltage which is 1.7 kV.

Importantly, the voltage across the SSCB is evenly distributed among the two devices during the phase of current drop and oscillation. Two series-connected SiC MOSFETs show high drain-source voltage consistency even with only one gate driver.

V. Conclusion

This letter proposes a SiC MOSFETs based SSCB. With several passive components and diodes, it can operate reliably both during ON-steady-state and fault current interruption process. Specifically, the robustness and compactness have been increased with the smaller cost since it only requires a single gate driver to control the behavior of two series connected devices. The prototype has been built and its feasibility has been verified experimentally. Ultrashort interruption process is also achieved. 75 A short-circuit current under the dc-bus voltage of 1200 V can be interrupted within 1.5 μs. The proposed SSCB provides an effective design and can be applied to future much more high power rating SiC MOSFETs to gain higher power rating SSCB.

Acknowledgment

The support provided by China Scholarship Council (CSC) during the visit of Yu Ren to The University of Tennessee, Knoxville is acknowledged.

References

[1] D. Salomonsson, L. Soder, and A. Sannino, "Protection of low-voltage DC microgrids," *IEEE Trans. Power Del.*, vol. 24, no. 3, pp. 1045–1053, Jul. 2009.

[2] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.

[3] C. Meyer, S. Schroder, and R. W. D. Doncker, "Solid-state circuit breakers and current limiters for medium-voltage systems having distributed power systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1333–1340, Sep. 2004.

[4] A. Abramovitz and K. M. Smedley, "Survey of solid-state fault current limiters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2770–2782, Jun. 2012.

[5] E. L. Wellner and A. R. Bendre, "IGCTs vs. IGBTs for circuit breakers in advanced ship electrical systems," in *Proc. IEEE Elect. Ship Technol. Symp.*, 2009, pp. 400–405.

[6] F. Lei, G. Ruifeng, Z. Fang, Y. Xiaoping, and Z. Fan, "Development of a 10kV solid-state DC circuit breaker based on press-pack IGBT for VSC-HVDC system," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, 2016, pp. 2371–2377.

[7] Z. Chen *et al.*, "Analysis and experiments for IGBT, IEGT, and IGCT in hybrid DC circuit breaker," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 2883–2892, Apr. 2018.

[8] Y. Ren *et al.*, "Voltage suppression in wire-bond-based multichip phase-leg SiC MOSFET module using adjacent decoupling concept," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8235–8246, Oct. 2017.

[9] Q. Zhang, R. Callanan, M. K. Das, S. H. Ryu, A. K. Agarwal, and J. W. Palmour, "SiC power devices for microgrids," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 2889–2896, Dec. 2010.

[10] Y. Sato, Y. Tanaka, A. Fukui, M. Yamasaki, and H. Ohashi, "SiC-SIT circuit breakers with controllable interruption voltage for 400-V DC distribution systems," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2597–2605, May 2014.

[11] Z. Miao, G. Sabui, A. M. Roshandeh, and Z. J. Shen, "Design and analysis of DC solid-state circuit breakers using SiC JFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 863–873, Sep. 2016.

[12] Z. J. Shen, G. Sabui, Z. Miao, and Z. Shuai, "Wide-bandgap solid-state circuit breakers for DC power systems: Device and circuit considerations," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 294–300, Feb. 2015.

[13] D. P. Urciuoli, D. Ibitayo, G. Koebke, G. Ovrebo, and R. Green, "A compact 100-A, 850-V, silicon carbide solid-state DC circuit breaker," in *Proc. IEEE Energy Conversion Congr. Expo.*, 2016, pp. 1–5.

[14] X. Song, C. Peng, and A. Q. Huang, "A medium-voltage hybrid DC circuit breaker, part I: Solid-state main breaker based on 15 kV SiC emitter turn-OFF thyristor," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 278–288, Mar. 2017.

[15] L. L. Qi, A. Antoniazzi, L. Raciti, and D. Leoni, "Design of solid-state circuit breaker-based protection for DC shipboard power systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 260–268, Mar. 2017.

[16] S. Ji, S. Zheng, F. Wang, and L. M. Tolbert, "Temperature-dependent characterization, modeling, and switching speed-limitation analysis of third-generation 10-kV SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4317–4327, May 2018.

[17] Y. Ren *et al.*, "A compact gate control and voltage-balancing circuit for series-connected SiC MOSFETs and its application in a DC breaker," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8299–8309, Oct. 2017.

[18] F. Zhang, X. Yang, Y. Ren, L. Feng, W. Chen, and Y. Pei, "A hybrid active gate drive for switching loss reduction and voltage balancing of series-connected IGBTs," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7469–7481, Oct. 2017.

[19] R. Withanage and N. Shammas, "Series connection of insulated gate bipolar transistors (IGBTs)," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2204–2212, Apr. 2012.