A Reduced Switch Hybrid Multilevel Unidirectional Rectifier

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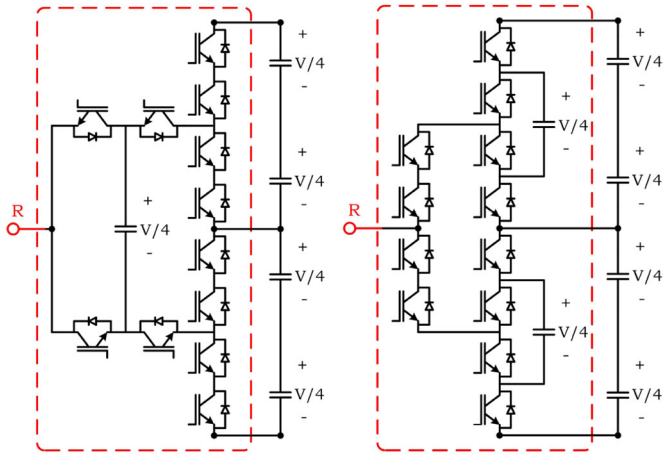
***Abstract*—Nonregenerative pulsewidth-modulated (PWM) rectifiers are increasingly being considered for applications, where the power flow is unidirectional, such as power supplies for telecommunications, X-ray, the machine-side converter for wind energy conversion systems, etc. They use fewer active switches, which increase their power density and reduce cost. This paper proposes a novel reduced switch topology for a multilevel (five-level or higher) nonregenerative PWM rectifier. It uses only four controlled switches and eight diodes per phase for a five-level rectifier. Half of the diodes are naturally commutated (zero current switching) at the line frequency, which reduces switching losses. This topology has several other advantages compared to similar topologies reported in the literature, such as minimum voltage stress across the devices, elimination of transient voltage-balancing snubbers, no extra hardware for balancing the flying capacitors, the dc-link mid-point voltage, etc. In this paper, switching cycle average modeling and the carrier-based modulation strategy for this rectifier are also presented to maintain a balanced dc link and to regulate flying capacitor voltages, while achieving unity displacement factor at the rectifier input terminals. The overall performance of the rectifier is verified by experimental results.**

***Index Terms*—AC–DC converter, flying capacitor (FC), multilevel converter, neutral point clamped (NPC), three-phase rectifier, unity power factor (upf) rectifier.**

I. Introduction

MULTILEVEL converters have several advantages over their two-level counterparts, such as reduced voltage stress on the semiconductor devices, lower switching frequency (or reduction in filter size), lower common-mode voltage, lower dv/dt, and, hence, lower electromagnetic interference [1]–[3]. For medium-voltage (MV) applications, where a common dc link is a requirement, the most established and commercialized topologies are diode-clamped (neutral point clamped, NPC [4]) and capacitor-clamped (flying capacitor, FC) converters [2]. The three-level NPC converter has been very popular because of its simpler structure, with less number of semiconductor devices and capacitors [5]. For higher number of levels, in the NPC structure, several clamping diodes are to be connected in series, which increases the conduction and switching losses [5] and



(a) 5L-FC-ANPC (b) 5L-DFC-ANPC

Manuscript received November 17, 2017; revised March 28, 2018; accepted May 11, 2018. Date of publication May 14, 2018; date of current version February 5, 2019. Recommended for publication by Associate Editor G. Konstantinou. *(Corresponding author: Debranjan Mukherjee.)*

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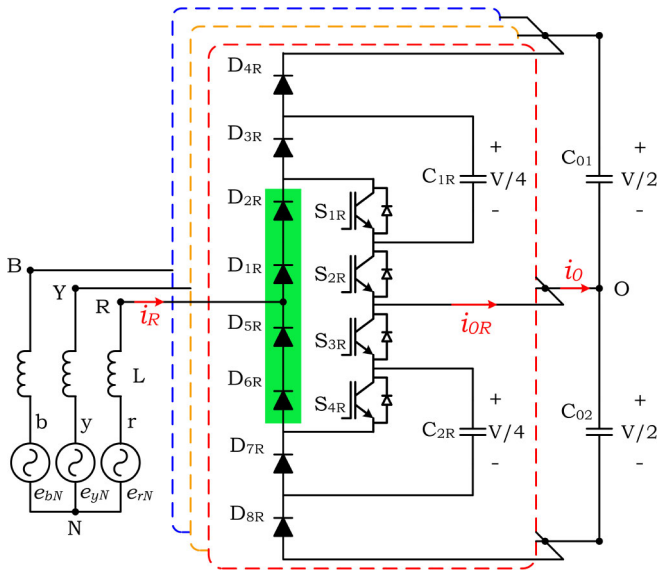

Fig. 2. Proposed five-level unidirectional dual FC-NPC-based rectifier topology.

For applications, where power flow is unidirectional, such as power supplies for telecommunications, aircraft, naval propulsion systems, X-ray, pumps and blowers requiring no regenerative braking, the machine-side converter for wind energy conversion systems, etc., nonregenerative pulsewidth-modulated (PWM) rectifiers are being preferred [15]–[19]. A forced-commutated three-level boost-type unidirectional rectifier was proposed in [16]. The circuit structure is the same as that of a 3L-NPC converter. However, some of the active switches in the 3L-NPC are replaced by diodes in [16]. The circuit in [16] was later modified in [17] to arrive at the three-phase three-switch three-level VIENNA rectifier. The derivation of some of the unidirectional topologies from the conventional bidirectional converters, such as the NPC, FC-based, and cascaded H-bridge converters, has been discussed in [18]. Several multilevel unidirectional topologies have been proposed in the literature [19]–[23]. The main problems of these topologies are the following.

1) The voltage rating of the semiconductors is not reduced, so several such devices in series are required for MV applications, which increase switching and conduction losses and require transient voltage-balancing snubber circuits [20]–[23].
2) Distribution of losses among the devices is not equal, which limits the nominal power rating of the converter [19]–[23].
3) Extra hardware circuitry is required to balance the dc-link capacitor voltages, which increases the cost, volume, and weight and reduces reliability [19]–[23].

In this paper, a unidirectional multilevel converter topology is derived from a hybrid multilevel converter topology presented in [6], [13], and [14]. The proposed dual FC-NPC-based unidirectional rectifier, as shown in Fig. 2, has the following features:

1) active switch and gate driver requirement is less (only four per phase);
2) low and equal voltage stress across the semiconductor devices;
3) no transient voltage-balancing snubber is required;
4) regulated dc-link voltage, dc-link mid-point voltage, and FC voltage;
5) no extra hardware is required for dc-link mid-point and FC voltage balancing;
6) no shoot-through problem in the topology;
7) half of the diodes are soft switched, which reduces switching loss;
8) the topology can be extended for a higher number of levels.

Several control strategies have been proposed for the three-phase unity power factor (upf) rectifiers [24]–[28], which can also be used to control the proposed rectifier. The control strategies described in [24]–[26] do not require input voltage sensors, which reduce the cost and increase reliability [26]. The control strategies proposed in [24] and [25] are of scalar control type. The main disadvantage of these strategies is the lower utilization of the converter switching frequency due to mutual interaction of the phase current controllers. In [24], no strategy has been proposed for closed-loop regulation of the dc-link mid-point voltage, and bulky capacitors are used in the dc link to limit unbalance. However, the resistance emulation technique is used in [24] and [25], which makes the terminal power factor unity and thus increases the modulation range [25]. Due to structural characteristics, the unidirectional rectifiers have the limitation on the input displacement factor. As described in [27] and [28], the dc-link voltage is fully utilized when the terminal displacement factor is unity. In these papers, source displacement factor is actively controlled; however, no technique has been proposed to actively control the terminal displacement factor under all operating conditions (transient and steady state). In this paper, a control strategy is proposed for these types of converters with the following features:

1) unity terminal displacement factor under all operating conditions (transient and steady state);
2) input voltage sensors are not required;
3) follows space vector approach unlike [24], [25].

The rest of this paper is organized as follows. In Section II, the topology and its operating modes are investigated. Modeling, control, and modulation strategies are discussed in Section III. The feasibility of the proposed topology and the effectiveness of various controllers are verified by experimental results in Section IV. Finally, conclusions are drawn in Section V.

II. Proposed Topology and Its Operating Modes

The dual-FC-NPC-based unidirectional rectifier, as shown in Fig. 2, is derived from its bidirectional counterpart [see Fig. 1(b)] by replacing two-third of the active switches by diodes. At upf operation in the rectification mode, control of the replaced switches is redundant. Replacing active switches by diodes reduces the number of isolated gate drivers, in turn, reducing volume, weight, and cost. Moreover, diodes are more reliable than active switches and shoot-through is no more a problem.

The proposed topology, as shown in Fig. 2, can be viewed as two unidirectional three-level-FC-based converters connected

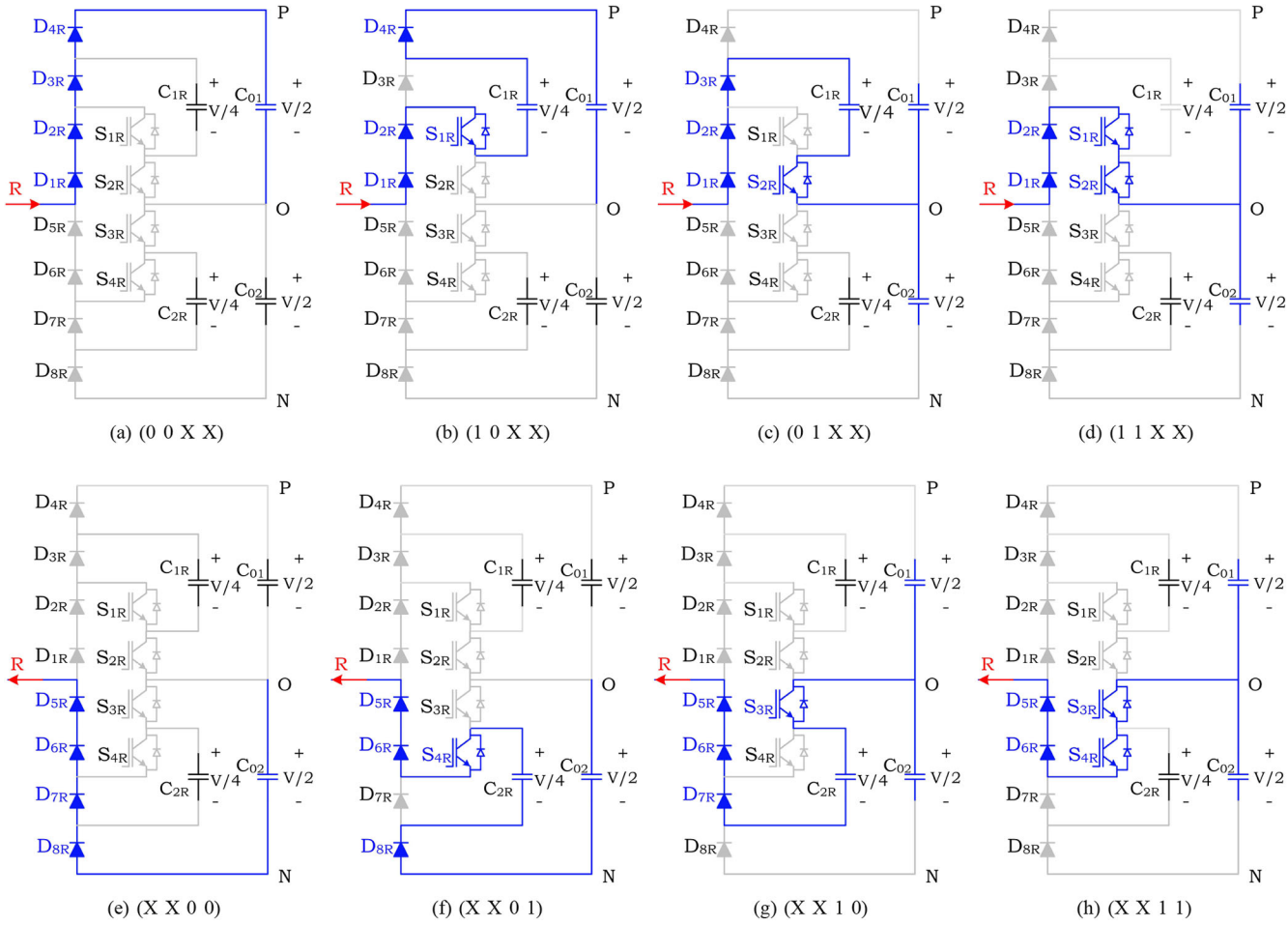

Fig. 3. Different current flowing paths of the proposed rectifier for different switching states. (a)–(d) For positive current. (e)–(h) For negative current. (a) (0 0 X X). (b) (1 0 X X). (c) (0 1 X X). (d) (1 1 X X). (e) (X X 0 0). (f) (X X 0 1). (g) (X X 1 0). (h) (X X 1 1).

to the ac input phase ("R"-phase) by the line frequency diodes (D_{1R}, D_{2R}, D_{5R}, and D_{6R}). During the positive half cycle, the top FC unit consisting of high-frequency devices (S_{1R}, S_{2R}, D_{3R}, and D_{4R}) and capacitor C_{1R} generates the PWM waveforms. The bottom FC unit with the high-frequency devices (S_{3R}, S_{4R}, D_{7R}, and D_{8R}) and capacitor C_{2R} does the same during the negative half cycle. The PWM waveforms generated by the top and bottom FC units are applied to the ac input by diodes D_{1R} and D_{2R} and diodes D_{5R} and D_{6R}, respectively. During the positive half cycle of the line current, only the top half of the circuit is active, while the bottom half is idle and vice versa. Therefore, the average switching frequency of the devices becomes half of the carrier frequency. When i_R is positive (see Fig. 2), there are four possible current paths dictated by the switching conditions of S_{1R} and S_{2R}, as shown in Fig. 3(a)–(d). During this interval, S_{3R} and S_{4R} have no control over the circuit operation. Similarly, for negative i_R, four possible current paths exist [see Fig. 3(e)–(h)]. Now, S_{1R} and S_{2R} have no control over the circuit operation.

Under normal operating conditions, FC voltages are $V/4$ and the dc link is balanced, i.e., positive link is at $+V/2$ and the negative link is at $-V/2$. Table I shows the circuit conditions under different operating modes. There are two states to generate $v_{R0} = +V/4$ for positive i_R: one of them charges the top FC and the other discharges it. These two redundant switching states are used to control the voltage of the top FC. Similarly, two redundant switching states are there to control the bottom FC voltage. As the FCs carry current only for half the cycle, the root-mean-square current flowing through the capacitor is $\sqrt{2}$ times smaller than that of a 5L-FC-ANPC [see Fig. 1(a)]. So, a longer lifetime can be expected from these FCs.

TABLE I
OPERATING MODES OF THE PROPOSED RECTIFIER

i_R	Switching signals (S_{1R} S_{2R} S_{3R} S_{4R})	State S_R	v_{RO}	C_{1R}	C_{2R}	i_{0R}
+Ve	(0 0 X X)	+2	+V/2	N.A	N.A	0
	(1 0 X X)	+1D	+V/4	D	N.A	0
	(0 1 X X)	+1C	+V/4	C	N.A	+Ve
	(1 1 X X)	0	0	N.A	N.A	+Ve
-Ve	(X X 0 0)	-2	-V/2	N.A	N.A	0
	(X X 0 1)	-1D	-V/4	N.A	D	0
	(X X 1 0)	-1C	-V/4	N.A	C	-Ve
	(X X 1 1)	0	0	N.A	N.A	-Ve

X: Don't care condition
C: Charging, D: Discharging, N.A: Not affected

TABLE II
COMPARISON OF THE FIVE-LEVEL CONVERTER TOPOLOGIES

Topology	Switch	Diode	Flying Capacitor
Bidirectional Topologies			
5L-NPC	24	36*	0
5L-FC	24	0	18
5L-FC-ANPC [9]	36*	0	3
5L-DFC-ANPC [13]	36	0	6
Unidirectional Topologies			
Topology in [20]*1	12	24*	9
Topology in [22]*1	12	36*	0
Topology in [23]*1	24*	24*	0
Proposed Topology	12	24	6

*: Series connection of high frequency switching devices
*1: Required extra hardware circuit for voltage balancing

Under normal operating conditions, the blocking voltages of the high-frequency diodes (i.e., D_{3R}, D_{4R}, D_{7R}, and D_{8R}) and the switches are $V/4$. However, voltage stress across the series-connected line frequency diodes is $V/2$. To make the voltage stresses of all the semiconductor devices same, a series connection of two line frequency diodes is used considering that the blocking voltage will be shared equally between the two diodes by static voltage-balancing snubber circuits.

It can be seen from Fig. 3 that diodes D_{1R} and D_{2R} are continuously ON for positive i_R and D_{5R} and D_{6R} are ON for negative i_R. The commutation of these diodes happens only when the line current changes its direction. So, during the commutation interval, zero or very small current flows through the diodes, making the transition less lossy. Besides, this smooth changeover eliminates the requirement of transient voltage-balancing snubber circuits for the series-connected diodes. However, static voltage-balancing resistors are to be connected to ensure equal sharing of blocking voltage. The proposed topology is compared with other existing five-level topologies in terms of the switch, diode, and FC count in Table II. All the devices in this table are assumed to block the same dc voltage $V/4$.

The proposed rectifier topology can be extended for a higher number of levels. A general N-level circuit topology is shown in Fig. 4. As the topology is symmetric about the dc-link midpoint, the number of levels should be odd and equal to or more than five. Each of the top and bottom units is $\frac{(N+1)}{2}$-level unidirectional FC converter. These are connected to the ac phase through the strings of diodes, which operate at the line frequency. No transient snubber circuit is required for these strings. Each FC unit voltage can be controlled by the redundant switching states. However, dedicated voltage-balancing mechanism is required for the series-connected capacitors. The voltage stresses of all diodes, switches, and capacitors are equal to $\frac{V}{(N-1)}$. The modulation and control strategies discussed in Section III can be generalized and applied to control this N-level unidirectional rectifier.

III. MODELING AND CONTROL

It is well known that for a given dc-link voltage (hence device voltage rating) and current rating of the devices, a unidirectional rectifier (such as the proposed rectifier) handles the maximum active power when operated at upf at its input terminals [27], [28]. In order to ensure upf operation of the proposed rectifier under both during transient and steady-state conditions, an input current reference-frame-oriented modeling and control strategy of the rectifier is proposed in this section. As will be pointed out, this control strategy is considerably simpler to implement compared to the conventional input-voltage-oriented reference-frame-oriented control strategy.

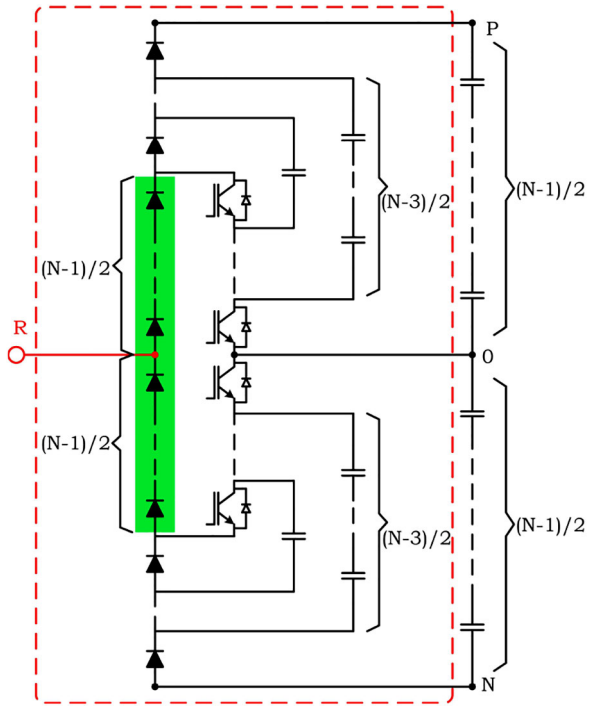

Fig. 4. N-level generalized topology of the proposed converter.

A. Modeling the Proposed Grid-Connected Rectifier in the Input-Current-Oriented Reference Frame

The dynamics of the proposed grid-connected rectifier can be described in the space vector notation as

$$\vec{e} = \vec{v} + R\vec{i} + L\frac{d\vec{i}}{dt} \tag{1}$$

where $\vec{e}$, $\vec{v}$, and $\vec{i}$ are the grid voltage, rectifier pole voltage, and line current vectors, respectively. L and R are the equivalent series inductance and resistance of the source, respectively. If the system is modeled in the input voltage vector ($\vec{e}$) reference frame [see Fig. 5(a)], then

$$\begin{cases} e_q = |e| = v_q + Ri_q + L\frac{di_q}{dt} + \omega_e L i_d \\ e_d = 0 = v_d + Ri_d + L\frac{di_d}{dt} - \omega_e L i_q = 0 \end{cases} \tag{2}$$

where ω_e is the angular speed of the input voltage vector and the q-axis of the reference frame is aligned along $\vec{e}$. To implement the control system in this reference frame, two current controllers (one for i_q and another for i_d) are required. Also, the input voltage vector needs to be either sensed or estimated. Even then, it is not possible to ensure upf operation at the rectifier input terminals (for maximum utilization of the rectifier VA

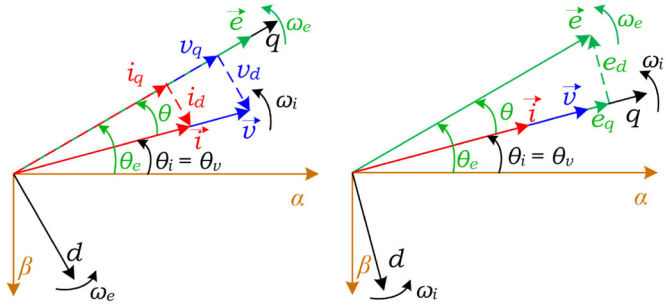

Fig. 5. Space vectors of the rectifier in the (a) input-voltage- and (b) input-current-oriented reference frame.

rating as pointed out earlier) since the line reactance (including source impedance) will, in general, be variable. Moreover, as discussed in [29], in this reference frame, the limiting values of v_q and v_d imposed by voltage, current, and power factor limitations of the upf rectifier vary with the position of the reference frame with respect to the stationary $\alpha\beta$ frame and are interdependent, which makes them difficult to be computed online. To avoid all these problems, the system is modeled in the input current vector reference frame [see Fig. 5(b)], where the q-axis is aligned along the current vector $\vec{i}$. For upf operation at the rectifier input terminals, the modulator ensures the alignment of $\vec{v}$ along $\vec{i}$ at all time. Under these conditions, we have

$$\begin{cases} i_d = 0,\ v_d = 0\,; \ \text{hence}, i_q = i,\ v_q = v \\ \theta_v = \theta_i\,; \ \omega_i = \text{the angular speed of } \vec{i}. \end{cases} \tag{3}$$

The combination of (1) and (3) yields

$$\begin{cases} e_q = |e|\ \cos\theta = v + Ri + L\dfrac{di}{dt} \\ e_d = -|e|\ \sin\theta = -\omega_i L i \\ \omega_i = \dfrac{d\theta_i}{dt} = \omega_e - \dfrac{d\theta}{dt}. \end{cases} \tag{4}$$

The inductor (L), used for filtering out the switching frequency components of the line current, is usually very small, which makes $e_d \ll e_q$ and $e_q \approx |e|$.

Fig. 6 shows the model of the system in the input-current-oriented reference frame based on (4). Only one proportional–integral (PI) controller is required, which controls the magnitude of the current space vector, i. Sensing or estimation of the instantaneous input voltages is not required to implement the controller. However, it does require the value of $|e|$ in the feed-forward term, which is a constant for normal grid-connected operation. The angular speed of the input current vector "ω_i" is found by a phase-locked-loop block, as shown in Fig. 6. The small-signal model of the system given by (4) can be shown to be very highly damped under all operating conditions. Therefore, for all practical purposes even under transient conditions, ω_i may be chosen to be equal to the angular frequency of the grid voltage ω_e, which is a constant under normal operating conditions. Moreover, as $\vec{v}$ is always along $\vec{i}$, from the space vectors of an unidirectional rectifier (VIENNA rectifier [26]), the maximum value of average v that can be generated at any instant is

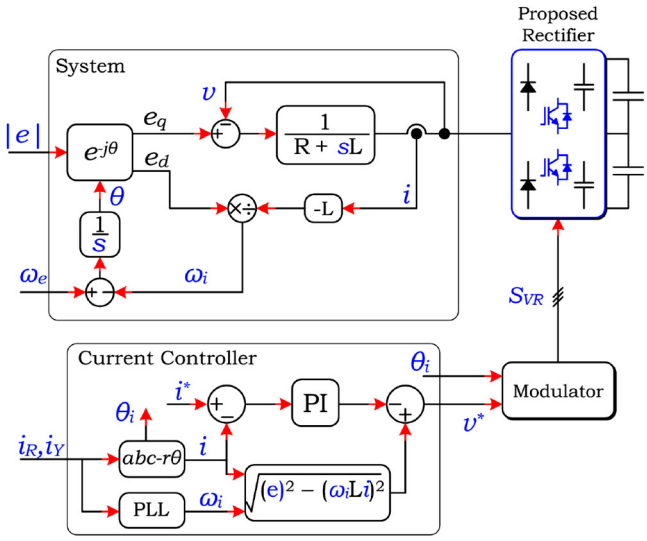

Fig. 6. System model in the current-oriented reference frame and its current controller.

given by

$$v|_{\max} = \frac{\sqrt{3}}{2}V \tag{5}$$

which is proportional to the dc-link voltage V only and does not depend on the position of the reference frame unlike in an input-voltage reference-frame-oriented controller.

B. Switching Cycle Average Model of the Proposed Converter

At any instant, the pole voltages of the proposed rectifier with respect to the dc-link mid-point (V_{XO} ; $X = \{R, Y, B\}$) are determined by the switching signals and the phase current as

$$\begin{cases} V_{XO} &= +\frac{V}{4}(2 - S_{1X} - S_{2X}), \quad \text{if } i_X \text{ is } +\text{ve} \\ V_{XO} &= -\frac{V}{4}(2 - S_{3X} - S_{4X}), \quad \text{if } i_X \text{ is } -\text{ve} \end{cases} \tag{6}$$

where S_{iX} ($i = \{1, 2, 3, 4\}$) are the switching states that take the value 1 when the corresponding switch is "ON" and 0 otherwise. As can be seen in Fig. 3 and Table I, the role of S_{1R} in charging or discharging the FC C_{1R} is the same as that of S_{4R} for C_{2R}. Also, it can be noted that when S_{1R} is active, S_{4R} has no control over the circuit operation and vice versa. So, for simplicity, switching states S_{1R} and S_{4R} can be made the same. With the same logic, switching states S_{2R} and S_{3R} can also be made the same. Hence, the pole voltages of the proposed rectifier can be rewritten as

$$V_{XO} = \text{sgn}(i_X)\left[\frac{V}{4}(2 - S_{1X} - S_{2X})\right] \tag{7}$$

where $\text{sgn}(i_X)$ is the polarity (sign) of the corresponding phase current. In the continuous conduction mode, neglecting the ripples in the dc link and FC voltages, the average rectifier pole voltages in a switching period are

$$v_{XO} = \text{sgn}(i_X)\left[\frac{V}{4}(2 - d_{1X} - d_{2X})\right] \tag{8}$$

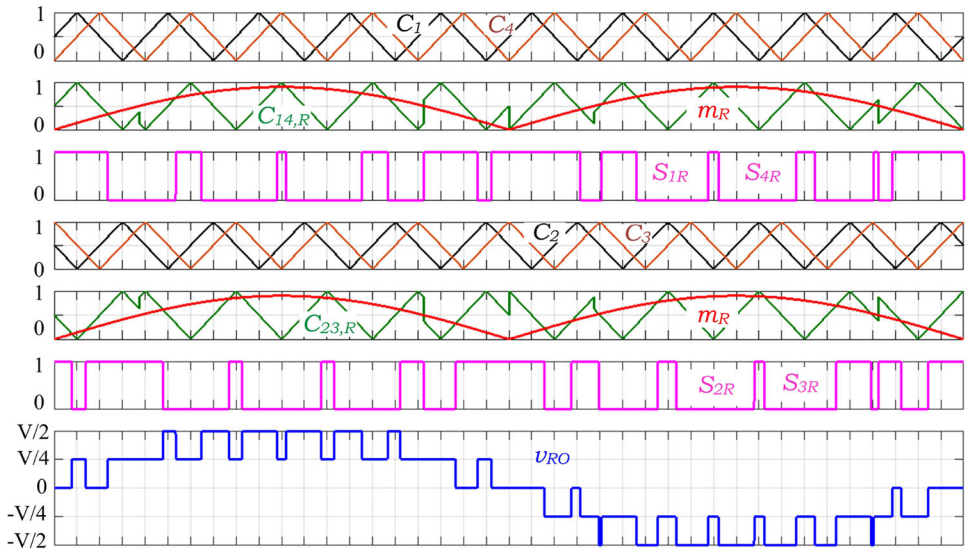

Fig. 7. Carrier-based modulation strategy.

where d_{1X} and d_{2X} are the duty ratios of the switches (S_{1X} or S_{4X}) and (S_{2X} or S_{3X}), respectively. Applying Kirchhoff's voltage law to the three phases of the grid, we obtain

$$e_{xN} = L\frac{di_X}{dt} + v_{XO} + v_{ON} \tag{9}$$

where e_{xN} ($x = \{r, y, b\}$) are the grid phase voltages with respect to the grid neutral, as shown in Fig. 2. For a balanced three-phase three-wire system, we have

$$i_R + i_Y + i_B = 0 \tag{10}$$

$$e_{rN} + e_{yN} + e_{bN} = 0. \tag{11}$$

The average rectifier pole voltages (V_{XO}) and the terminal voltages of the rectifier with respect to the supply neutral point (V_{XN}) are related as

$$v_{XO} = v_{XN} + K(t) \tag{12}$$

where $K(t)$ is an arbitrary time-varying signal (zero-sequence component).

If the rectifier is controlled to have a sinusoidally varying input current at unity terminal power factor, then

$$\begin{cases} v_{RN} = v^* \cos(\theta_i(t)) \\ v_{YN} = v^* \cos(\theta_i(t) - \frac{2\pi}{3}) \\ v_{BN} = v^* \cos(\theta_i(t) + \frac{2\pi}{3}) \end{cases} \tag{13}$$

where $\theta_i(t)$ is the instantaneous position of the current vector $\vec{i}$ with respect to the stationary reference frame and v^* is the desired magnitude of the rectifier input voltage, which is generated by the input current controller (see Fig. 6). The combination of (8), (12), and (13) gives

$$\begin{cases} 2\,m_R := (2 - d_{1R} - d_{2R}) = & \frac{4\,v^*}{V}|\cos(\theta_i(t))| \\ & + \frac{4\,K(t)}{V}\,\mathrm{sgn}(i_R) \\ 2\,m_Y := (2 - d_{1Y} - d_{2Y}) = & \frac{4\,v^*}{V}|\cos(\theta_i(t) - \frac{2\pi}{3})| \\ & + \frac{4\,K(t)}{V}\,\mathrm{sgn}(i_Y) \\ 2\,m_B := (2 - d_{1B} - d_{2B}) = & \frac{4\,v^*}{V}|\cos(\theta_i(t) + \frac{2\pi}{3})| \\ & + \frac{4\,K(t)}{V}\,\mathrm{sgn}(i_B). \end{cases} \tag{14}$$

Equation (14) is the key equation to implement the modulator to generate the switching pulses, as discussed in the next subsection.

C. Carrier-Based Modulation Strategy

Various modulation strategies, such as carrier-based technique [30] or space vector modulation strategy [31], can be adopted to generate the PWM signals for the proposed rectifier. Apart from generating the required average line-to-line voltage, the modulation strategies for this topology should also ensure that the dc-link mid-point voltage is balanced and the FC voltages are controlled to their nominal values. Such a carrier-based modulation strategy, following (14), is presented in this subsection for this rectifier.

Equation (14) can be written as

$$\begin{cases} (1 - d_{1R}) + (1 - d_{2R}) & = 2\,m_R \\ (1 - d_{1Y}) + (1 - d_{2Y}) & = 2\,m_Y \\ (1 - d_{1B}) + (1 - d_{2B}) & = 2\,m_B. \end{cases} \tag{15}$$

Under normal operating conditions, to keep the FC voltages unchanged in a switching period, d_{1X} and d_{2X} must be equal,

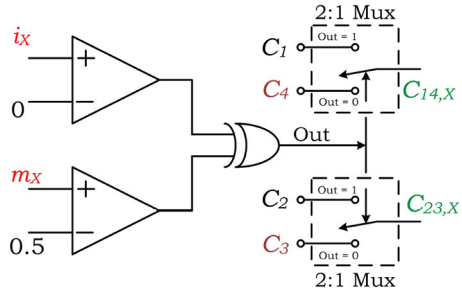

Fig. 8. Carrier signal generation strategy.

which gives

$$\begin{cases} (1-d_{1R}) = (1-d_{2R}) & = m_R \\ (1-d_{1Y}) = (1-d_{2Y}) & = m_Y \\ (1-d_{1B}) = (1-d_{2B}) & = m_B. \end{cases} \tag{16}$$

Equation (16) can be implemented by a modulator by comparing the modulating signals m_X ($X = \{R, Y, B\}$) with the phase-shifted triangular carriers (PSC). Fig. 7 shows the PWM generated by this modulation strategy using PSC with sinusoidal modulating signals for the "R" phase. The carrier signals $C_{14,X}$ and $C_{23,X}$ are used to generate the pulses for (S_{1X}, S_{4X}) and (S_{2X}, S_{3X}), respectively. Depending upon the current direction and the magnitude of the modulation signal, $C_{14,X}$ is generated from C_1 and C_4, and $C_{23,X}$ is generated from C_2 and C_3 as per Fig. 8.

It can be seen in Fig. 7 that the switching transitions are evenly distributed among the top and bottom switches. Also, the total number of switchings of the high-frequency diodes is the same as that of the active switches. So, the switching loss is evenly distributed among the eight high-frequency devices. Since the topology is symmetric for positive and negative half cycles, a better distribution of conduction losses can be achieved compared to that of a 5L FC-ANPC structure [9], [10] [see Fig. 1(a)].

1) FC Voltage Control: Under normal operation, the duty ratios (d_{1X} and d_{2X}) are equal to maintain FC voltages unchanged over a switching period. However, active controllers need to be implemented for regulating the FC voltages, modifying the duty ratios (d_{1X} and d_{2X}) from their nominal values ($d_{1X} = d_{2X}$) while keeping ($d_{1X} + d_{2X}$) same as in (14). The duty ratios (d_{1X} and d_{2X}) are modified by the FC voltage regulators as

$$\begin{cases} (1-d_{1X}) = m_X + \Delta m_X = m_{X1} \\ (1-d_{2X}) = m_X - \Delta m_X = m_{X2}. \end{cases} \tag{17}$$

Fig. 9 shows the effect of addition/subtraction of a positive constant (Δm_R, output of the FC voltage regulator) to the modulating signal (m_R) on the rectifier input voltage and switching signals. It can be seen in Fig. 9(a) that when $\Delta m_R = 0$, both switches S_{1R} and S_{2R} conduct for the same duration. In Fig. 9(b), Δm_R is added to the modulating signal to generate the gate signal of S_{1R}, and the same is subtracted for switch S_{2R}. Now, the conduction time for S_{1R} decreases, whereas, for S_{2R}, it increases, which makes the switching cycle average value of the rectifier input voltage to remain the same. However,

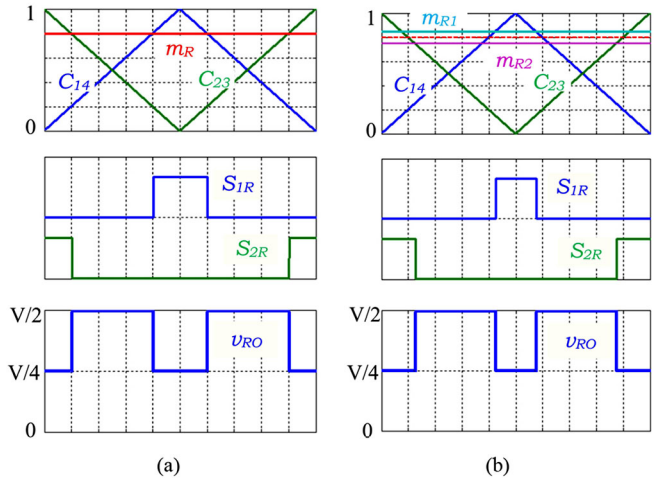

Fig. 9. Effects of addition/subtraction of a constant to the modulating signal on the rectifier input voltage and switching signals (a) before modification and (b) after modification.

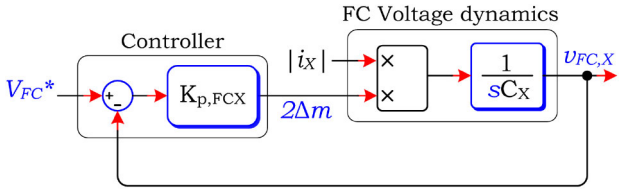

Fig. 10. Model of the FC voltage dynamics and its controller.

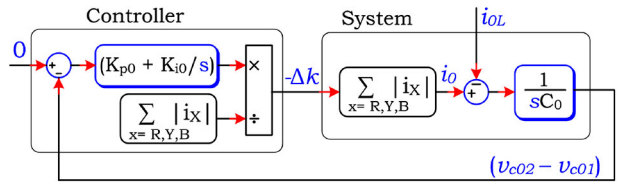

Fig. 11. Model of the dc-link mid-point voltage dynamics and its controller.

as S_{2R} conducts longer than S_{1R}, a positive average current flows through the FC C_{1R}, which increases its voltage. Reverse will happen when Δm_R is negative. So, by controlling Δm_R, the voltage of the active FC can be controlled. The effect of Δm_R on the FC voltage can be expressed as

$$v_{\text{FC}} = 2 \int \left[\frac{|i_X|}{C_X} \Delta m_X \right] dt \tag{18}$$

where C_X is the capacitance value of the FC under consideration. Fig. 10 shows the FC voltage dynamics along with a proportional controller to regulate the FC voltage, where V_{FC}^* is the reference value for the FC voltage controller. It is to be noted that only one FC voltage can be regulated in each half cycle. However, as no current flows through the other FC, its voltage remains constant.

2) DC-Link Mid-Point Voltage Control: For dc-link voltage balancing, a common-mode voltage [K_t in (14)] is to be injected to the phase voltage waveforms [17]. If $K(t) \neq 0$ in (14), then

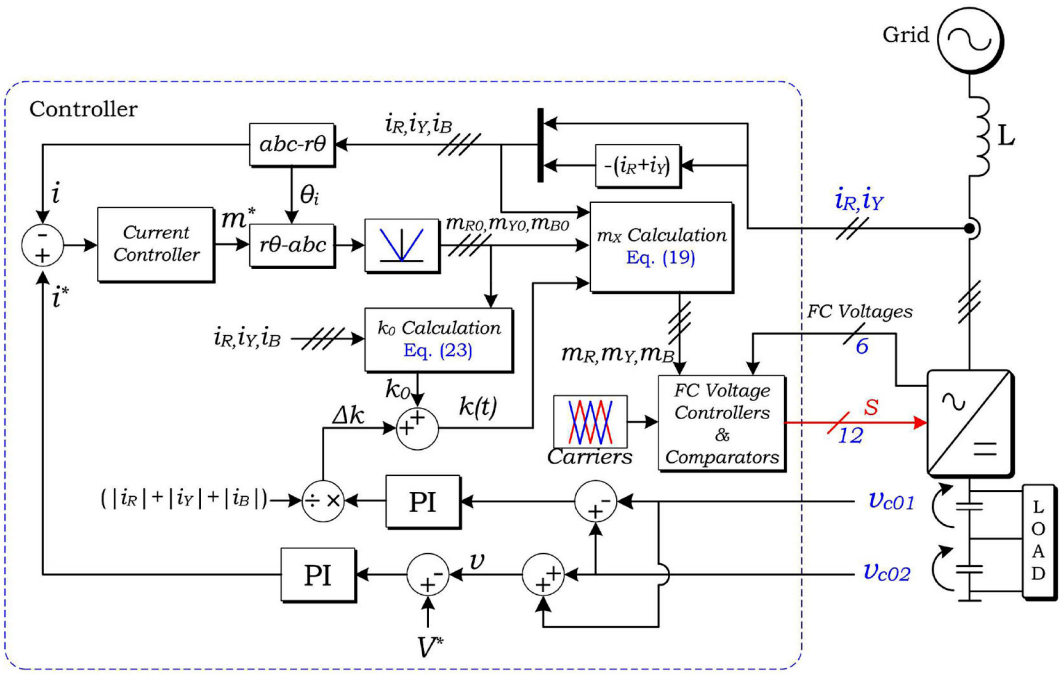

Fig. 12. Block diagram of the complete control system.

the modulation signals are

$$\begin{cases} m_R = & m^*\,|\cos(\theta_i(t))| + k(t)\,\mathrm{sgn}(i_R) \\ m_Y = & m^*\,|\cos(\theta_i(t) - \frac{2\pi}{3})| + k(t)\,\mathrm{sgn}(i_Y) \\ m_B = & m^*\,|\cos(\theta_i(t) + \frac{2\pi}{3})| + k(t)\,\mathrm{sgn}(i_B) \end{cases} \tag{19}$$

where $m^* = \dfrac{2\,v^*}{V}$ and $k(t) = \dfrac{2\,K(t)}{V}$.

Under normal operating conditions, when $d_{1X} = d_{2X}$, from (16), we have

$$d_{2X} = 1 - m_X\,. \tag{20}$$

Switching cycle average of current i_0 flowing into the mid-point of the dc link can be calculated as

$$i_0 = (d_{2R}\,i_R) + (d_{2Y}\,i_Y) + (d_{2B}\,i_B). \tag{21}$$

Using (20) and (19) in (21), we obtain

$$\begin{aligned} i_0 = & -\{(m_R\,i_R) + (m_Y\,i_Y) + (m_B\,i_B)\} \\ = & -\{(m_{R0}\,i_R) + (m_{Y0}\,i_Y) + (m_{B0}\,i_B)\} \\ & - k(t)\big[|i_R| + |i_Y| + |i_B|\big] \end{aligned} \tag{22}$$

where m_{R0}, m_{Y0}, and m_{B0} are, respectively, the modulation signals m_R, m_Y, and m_B given by (19) with $k(t) = 0$. In (22), the switching cycle average value of i_0 can be made zero for $k(t) = k_0(t)$, where

$$k_0(t) = \frac{-\{(m_{R0}\,i_R) + (m_{Y0}\,i_Y) + (m_{B0}\,i_B)\}}{\{|i_R| + |i_Y| + |i_B|\}}. \tag{23}$$

The addition of $k_0(t)$ to the modulation signals as per (19) has no control over the line current; however, it ensures zero average current flowing into the dc-link mid-point from the rectifier side. A feedback controller is required to compensate the effects of the nonidealities in the system and/or unbalanced dc loading. For designing the controller, first, the dc-link mid-point voltage dynamics is modeled as follows:

$$C_0\frac{d(v_{c02} - v_{c01})}{dt} = i_0 - i_{0L} \tag{24}$$

where i_{0L} is the dc-link mid-point load current. The dc-link capacitors are considered to have the same value, C_0. DC-link mid-point current, i_0 is given by (22), in which $k(t)$ has two components: a feed-forward term $k_0(t)$ and a feedback term Δk. If $k_0(t)$ is generated as per (23), (22) becomes

$$i_0 = -\Delta k\big[|i_R| + |i_Y| + |i_B|\big]. \tag{25}$$

Combining (24) and (25), we obtain

$$C_0\frac{d(v_{c02} - v_{c01})}{dt} = -\Delta k\big[|i_R| + |i_Y| + |i_B|\big] - i_{0L}. \tag{26}$$

Equation (26) describes the dynamic behavior of the dc-link mid-point voltage. A PI controller, as shown in Fig. 11, is designed to generate Δk and make the closed-loop system to follow a second-order equation

$$-(v_{c02} - v_{c01})\Big(K_{p0} + \frac{K_{i0}}{s}\Big) = C_0 s(v_{c02} - v_{c01}) + i_{0L} \tag{27}$$

where K_{p0} is the proportional gain and K_{i0} is the integral gain of the controller. K_{p0} and K_{i0} are chosen to give suitable control bandwidth and damping ratio. K_{i0} is designed from

$$K_{i0} = \omega_n^2 C_0 \tag{28}$$

where ω_n is the desired control bandwidth. K_{p0} is designed from

$$K_{p0} = 2\xi\omega_n C_0 \tag{29}$$

where ξ is the desired damping ratio.

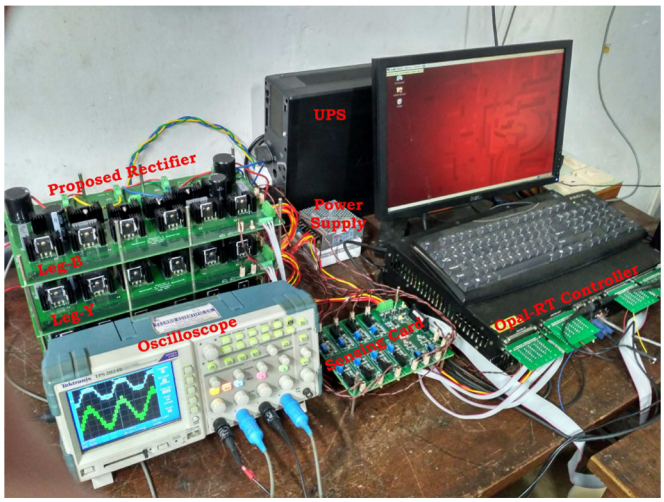

Fig. 13. Laboratory prototype of the proposed five-level rectifier.

TABLE III
RATINGS AND PARAMETERS OF THE EXPERIMENTAL SETUP

System Ratings and Parameters	
Rated Input Voltage	125 V
Frequency	50 Hz.
DC-link Voltage	220 V
Rated Input Current	16 A
Filter Inductance (excluding auto-transformer)	2.5 mH
DC-link Capacitor	3000 μF each
Flying Capacitors	1000 μF each
Controller Parameters	
Carrier Frequency	1 kHz.
Line current controller's bandwidth	250 Hz.
DC-link voltage controller's bandwidth	50 Hz.
DC-link mid-point voltage controller's bandwidth	50 Hz.
FC voltage controller's proportional gain	0.005 per Volt

The overall block diagram of the control strategy for the proposed grid-connected rectifier is shown in Fig. 12. There are several control loops, such as the outer dc-link voltage and inner current control loops, and dc-link mid-point and FC voltage control loops. The control strategy requires sensing of two input currents, two dc-link voltages, and six FC voltages. Grid voltage sensors are not required for the implementation.

IV. EXPERIMENTAL RESULTS

To verify the proposed topology and the effectiveness of the control and modulation strategies, experiments were conducted on a laboratory prototype (see Fig. 13) of the proposed five-level rectifier. Ratings and parameters of the experimental setup are given in Table III. The rectifier is designed with discrete MOSFETs (IRFP260NPBF) and diodes (VS-60CPU02-F) and is connected to a 230-V 50-Hz three-phase grid through an auto-transformer and filter inductors. For experimentation, the auto-transformer output is set to 125 V. The dc output of the rectifier is connected to a 220-V 5-kW load box with a load resolution of 0.5 kW. The controller for the rectifier is implemented in an OPAL-RT (OP4500) controller, which takes ten input signals (two line currents, two dc-link voltages, and six FC voltages). Considering the usefulness of the proposed converter for MV applications, the carrier frequency is maintained at 1 kHz. (Average switching frequency of the devices is 500 Hz, as they conduct only for half the fundamental cycle.) Parameters of the various controllers are listed in Table III. The PWM signals generated by the controller are applied to the inputs of the gate drivers of the rectifier.

Fig. 14 shows the experimental waveforms of the rectifier in the steady state at an input voltage of 125 V, a frequency of 50 Hz, an output dc-link voltage of 220 V, and a load power of 2.5 kW. Fig. 14(a) shows all the line currents (i_R, i_Y, and i_B) along with the PWM line–line voltage (v_{RY}). The line currents are balanced, and the line–line voltage v_{RY} is seen to have nine levels, which is the characteristic feature of a five-level converter. In Fig. 14(b), the line current i_R is shown to be in phase with the "R"-phase voltage with respect to the grid neutral (v^*_{RN}), which is generated as per (13) inside the controller. The average "R"-phase voltage with respect to the dc-link mid-point (v^*_{RO}) along with its PWM waveform (v_{RO}) is also shown in Fig. 14(b). It is to be noted that v^*_{RO} differs from v^*_{RN} by a common-mode voltage, as calculated by using (23). Fig. 14(c) shows the effectiveness of the dc-link mid-point voltage controller and the FC voltage controllers by the waveforms of the individual dc-link voltages (v_{c01} and v_{c02}) and the FC voltages of the "R"-phase (v_{c1R} and v_{c2R}). Even though each FC voltage is regulated in alternate half cycles of the line current, overall, they are maintained to be equal by the proposed controller. Fig. 14(d) shows the blocking voltages of the series-connected diodes of the "R"-phase ($v_{D1,R}$, $v_{D2,R}$) along with the line current (i_R). Both the diodes are ON for positive i_R and are sharing the blocking voltage equally when the current is negative. The equal sharing of blocking voltage is ensured by the equal value resistors (100 kΩ) connected across the individual series-connected diodes. Fig. 14(e) shows the line current (i_R) along with the supply voltages after and before the autotransformer (e_{ry} and $e_{ry,\text{grid}}$, respectively). In the input-voltage-sensor-based control strategy, the line voltage after the transformer (e_{ry}) has to be used, since the actual grid may be far off and $e_{ry,\text{grid}}$ may not be available for measurement. The harmonic spectrum of the line voltage (e_{ry}, total harmonic distortion (THD) $= 2.44\%$) and the line current (i_R, THD $= 2.49\%$) are shown side by side in Fig. 14(f). It shows that the line voltage contains some lower order harmonics (i.e., fifth, seventh, 11th, and 13th). As the current controller bandwidth had to be restricted to only 250 Hz (due to the limited carrier frequency of 1 kHz), the controller could not eliminate the effects of these harmonics (250, 350, 550, and 650 Hz) present in the line voltage. Therefore, prominent harmonic contents at those frequencies are observed in the line current spectrum in Fig. 14(f). However, for MV applications, the grid voltage is expected to be much cleaner, which may improve the current quality further.

The THD of the line current is reduced as the load is increased, as shown in Fig. 15(a). The power factor of the topology at the rectifier terminals is always maintained at unity. However, at the source terminals, the power factor deviates more from unity,

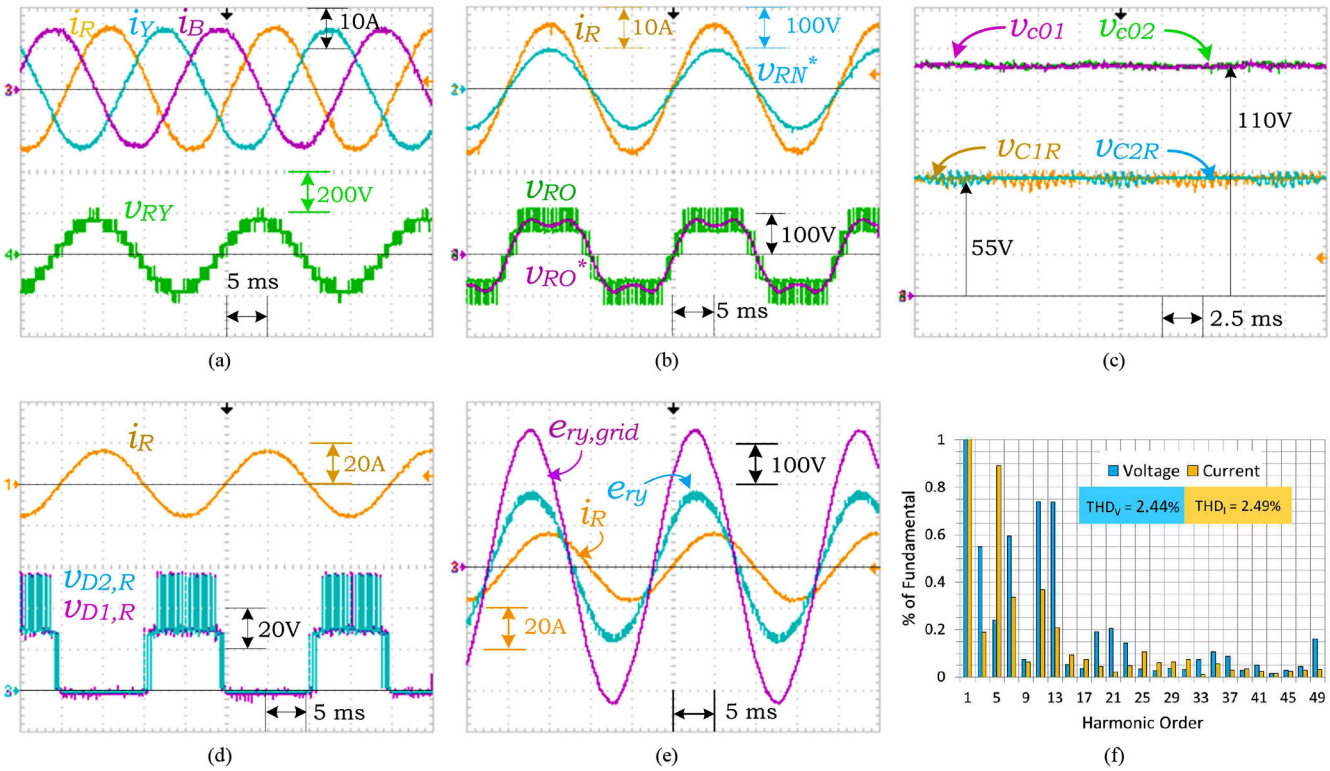

Fig. 14. Experimental results showing various steady-state waveforms of the proposed rectifier (input voltage: 125 V, 50 Hz, output dc-link voltage: 220 V, load: 2.5 kW).

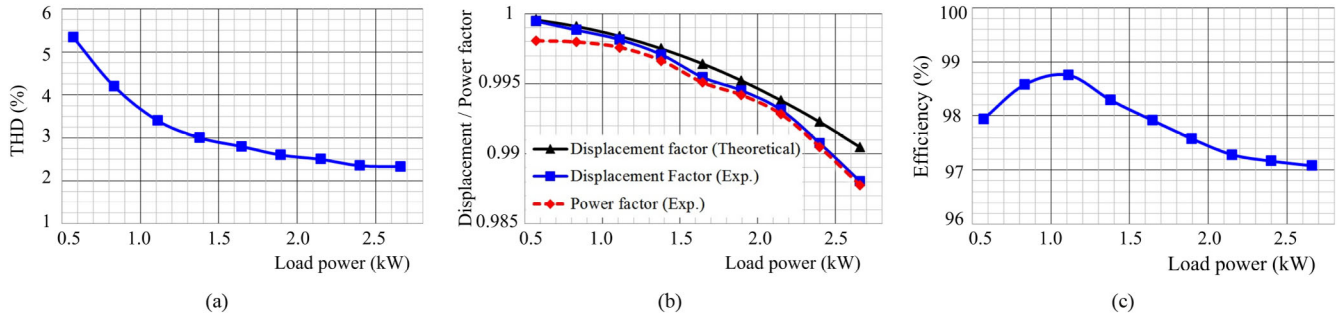

Fig. 15. Quantitative plots. (a) THD. (b) Source displacement factor and power factor. (c) Efficiency as a function of load power.

as the load increases because of the voltage drop across the filter inductors, as can be seen in Fig. 15(b). The figure shows the variation of the displacement factor (experimental) and the power factor (experimental) at the source terminals with load power. Variation of the displacement factor is also theoretically calculated from the source voltage, line current, and the line impedance values and plotted in Fig. 15(b) [displacement factor (theoretical)]. As the current quality improves with load, the difference between the displacement factor and the power factor reduces, as can be seen in the figure. The power factor at the source is always maintained above 0.988 over the entire load range. The converter efficiency for different loading conditions is plotted in Fig. 15(c). It is found that the efficiency of the converter is always more than 97%, and the maximum efficiency is 98.75% at 1.11 kW. For all the experimental results shown in Fig. 15, the input voltage, the frequency, and the output voltage were maintained constant at 125 V, 50 Hz, and 220 V, respectively.

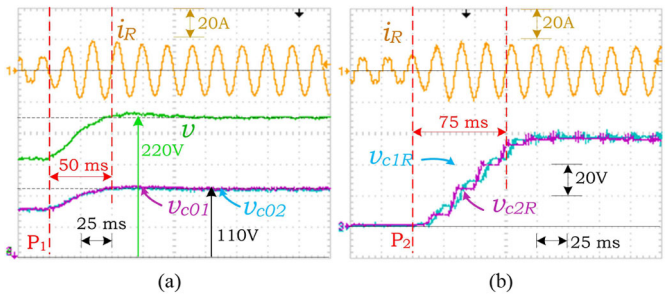

Fig. 16. Experimental results showing various starting responses of the proposed rectifier with the control strategy.

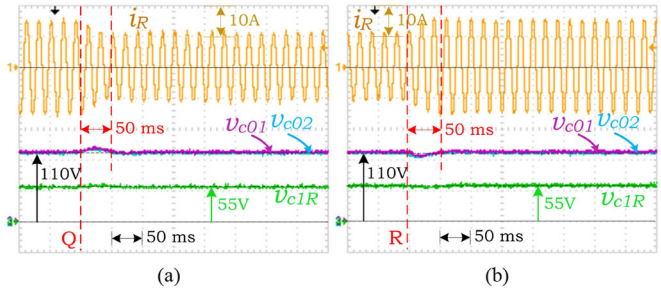

Fig. 17. Experimental results showing various transient responses of the proposed rectifier with the control strategy. (a) Load is decreased from 2.5 to 2 kW at Q. (b) Load is increased from 2 to 2.5 kW at R.

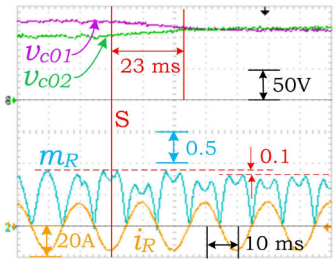

Fig. 18. Experimental results showing the performance of the dc-link mid-point voltage controller; a voltage-balancing controller is turned ON at S.

Fig. 16 shows the starting responses of the line current i_R, individual dc-link voltages v_{C01} and v_{C02}, the total dc-link voltage v, and the FC voltages of the "R"-phase (v_{c1R}, v_{c2R}) of the proposed rectifier. In Fig. 16(a), the controller is turned ON at P_1. Before P_1, the converter was working as a three-phase diode bridge rectifier, and after P_1, it takes around 50 ms to reach the steady state. In Fig. 16(b), when controller was OFF, none of the FCs was charged. At P_2, when the controller is turned ON, the FC voltages start being regulated and reach their reference of 55 V after a transient time of around 75 ms. It is to be noted that, in practice, FCs have to be precharged to the target value to avoid overvoltage across the semiconductor devices during starting. A startup procedure with a series-connected resistor for the FC rectifier has been proposed in [32], which can also be used for the proposed topology.

Fig. 17 shows transient responses of the line current i_R, individual dc-link voltages v_{C01} and v_{C02}, and one of the FC voltages of the "R"-phase (v_{c1R}) of the proposed rectifier during the load change. In Fig. 17(a), the load on the dc side is decreased from 2.1 to 1.6 kW at the instant Q. The dc load is increased from 1.6 to 2.1 kW at the instant R in Fig. 17(b). It is seen in these figures that due to these load changes, the dc-link voltages deviate from their nominal values by a maximum of 8 V for about 50 ms. However, the FC voltage is seen to be unaffected by the load change.

To show the effectiveness of the dc-link mid-point voltage controller, an experiment was conducted with unbalanced loading on the dc link. Unbalanced loading was obtained by connecting a 20-Ω (2.5-kW, 220-V) resistor across the full dc link and another 150-Ω resistor across the lower capacitor (v_{c2}). The dc-link mid-point voltage controller is turned ON at S. Fig. 18 shows that the dc link was not balanced and the modulation signal (m_R) was of rectified sinusoidal type before the instant S. After the instant S, the dc-link mid-point voltage is brought to the balanced condition within 23 ms. Also, the addition of a feedforward term [see (23)] to the modulation signal reduces its peak by about 0.1, which increases the linear modulation range. The figure also shows the in-phase relationship of the line current and the modulation signal, which confirms the controllability of the dc-link mid-point voltage during the whole interval of the fundamental period.

V. Conclusion

In this paper, a reduced switch multilevel rectifier based on the dual FC and NPC topology is proposed, which can be extended to any odd (more than five) number of levels. It uses only four controlled switches and eight diodes per phase for a five-level rectifier. This hybrid topology combines the advantages of NPC- and FC-based converters. The rectifier topology is useful for unidirectional power flow applications. As it can handle higher voltages with a higher number of levels, it is suitable for MV applications.

The switching cycle average model of the proposed rectifier and the carrier-based modulation strategy are presented in this paper. It is shown that input voltage sensors are not required for implementation when the rectifier is controlled at unity terminal power factor in the input-current-oriented reference fame. No extra hardware circuit is required for dc-link mid-point voltage balancing and FC voltage control. Experimental results verify that the converter maintains the efficiency to more than 97% for the full-load range and a maximum efficiency of 98.75%. The THD of the line current is found to be within the limit. However, due to the distortion in the supply voltage, lower order harmonics are found to be present in the line current, which can be eliminated if the switching frequency is increased in low-voltage applications. In MV applications (where the switching frequency cannot be increased), the supply voltage distortion is expected to be much lower, which will also improve the input current quality further. It is also experimentally established that even though the rectifier is controlled to maintain upf at the rectifier terminals, the source power factor also remains higher than 0.988 over the entire range.

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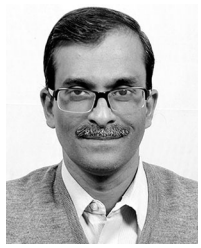

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