A New Single DC Source Six-Level Flying Capacitor Based Converter With Wide Operating Range

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***Abstract*—This paper presents a new six-level flying capacitor based (FC-based) multilevel converter with one dc source and the capability of operating in all power factors and modulation indexes. Multilevel converters with one dc voltage source are attractive in many applications as they do not need rather expensive and bulky multiwinding input transformer connection at the dc side. On the other hand, not all classic multilevel converters with one dc source can produce any desirable number of output voltage levels at all power factors and/or modulation indexes. In this paper, a hybrid structure is proposed in which six voltage levels can be realized at the ac terminals. The modulation technique and the control strategy for the FC voltage balancing are presented. To show the advantages of the proposed converter, different performance criteria, such as switch count and rating, the size of capacitors, switching frequency, and power losses, are compared with other existing six-level topologies. The results indicate that the proposed structure is superior to other six-level converters from different standpoints. Simulation results are used to further evaluate the performance of the proposed converter. A laboratory-type experimental setup is used to validate the theoretical results.**

***Index Terms*—Capacitor voltage balancing, flying capacitor multicell (FCM) converter, hybrid topology, level-shifted carrier pulsewidth modulation (PWM), multilevel converter.**

I. Introduction

MULTILEVEL converters are the main solution in response to the industrial demand to high power converters. Different multilevel converters are employed in a wide variety of high power applications including motor drives, static compensators, and renewable energy conversion systems [1]–[4]. These improvements owe to the mature technology of medium-voltage and -current devices.

Multilevel technologies provide attractive features, such as better voltage quality in terms of harmonic distortion, lower switching frequency, extended power range, and lower electromagnetic interference [5], [6]. In this regard, there are many challenges associated with the classic topologies, such as limited range of power factor (PF) and/or modulation index, high switch and capacitor count, and the need of multiple dc sources.

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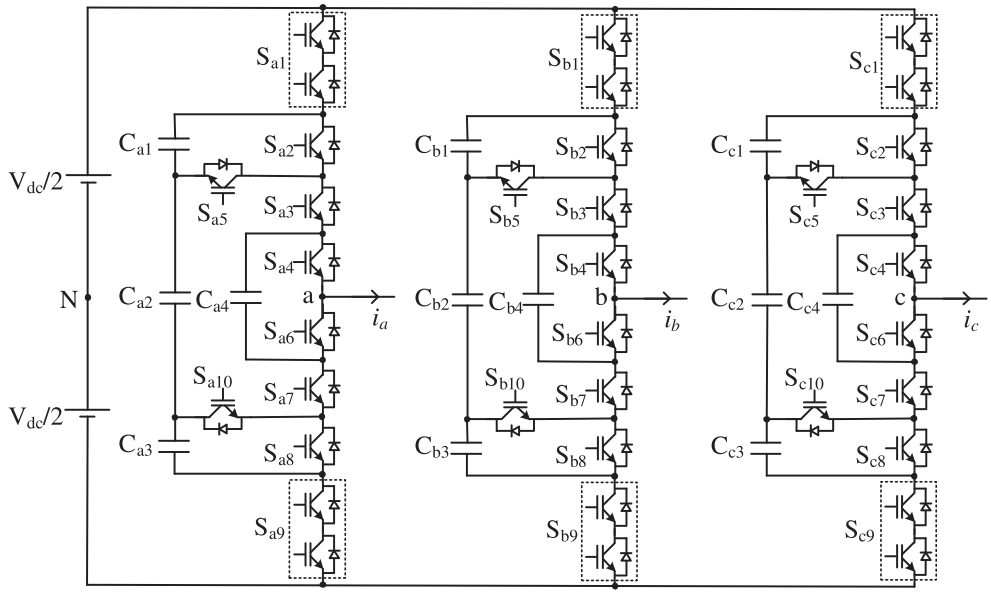

Fig. 1. Proposed six-level three-phase converter topology.

usually more complex than those in classic topologies [24], [25]. For example, one of the main challenges in hybrid topologies is to balance the voltage of flying or split dc-link capacitors without increasing the switching frequency. Due to such complexities, the number of proposed hybrid topologies with high voltage levels is limited in industry and literature.

A new five-level topology, called nested neutral point clamped (NNPC), has been proposed in [26]. This topology is based on the combination of the FCM and NPC topologies. By considering the advantages of other commercialized hybrid topologies including the five-level H-bridge NPC (HNPC) [27] and the 5L-ANPC, the five-level NNPC converter has some advantages such as transformerless operation and reduction of the number of components.

Recently, a six-level hybrid inverter (6L-HI) topology has been proposed [28]. In this topology, similar to the DCM topologies, the dc link is divided into multiple sections by employing series-connected capacitors. In order to balance the dc-link capacitor voltages, an auxiliary balancing circuit is used. The balancing circuit increases component count, cost, size, and losses of the converter. However, it is shown that the cost and losses of this topology is lower in comparison with the classic 6L-FCM and DCM topologies.

In this paper, a new six-level flying capacitor based topology (6L-FCB) is proposed. The proposed topology uses a single dc source and, thus, is attractive for many medium- and high-power applications. Unlike DCM-based topologies, the dc link of the proposed topology is not split into multiple sections, and thus, there is no need of auxiliary balancing circuits or high-frequency modulation techniques. While realizing different output voltage levels, the proposed topology only employs converter switching states to balance FC voltages. This is accomplished by a special voltage balancing algorithm. It will be shown in this paper that the proposed topology has lower component count as compared to other existing 6L topologies. Another important feature of the proposed converter is that it can operate under all PFs and modulation indexes without compromising other converter characteristics.

Compared to the NNPC topology [26], the proposed topology requires lower voltampere of FCs. Furthermore, the proposed topology is based on the single dc link and does not require isolated dc sources similar to the HNPC and packed U-cell [29] topologies. Unlike 5L-ANPC, 7L-ANPC, and T-type topologies [30], the dc link of the proposed topology is not subdivided into two parts, and thus, there is no need to regulate the dc-link capacitor voltages. This, in turn, reduces the control complexity.

This paper is organized as follows. Section II presents the basic converter topology. The modulation technique and the capacitor voltage balancing strategy are explained in Sections III and IV, respectively. Section V provides a comprehensive comparison among the proposed converter and other existing converters in the same family. This helps the reader understand and compare different performance criteria of multilevel converters from different standpoints. Simulation results are illustrated in Section VI to verify the proposed converter operation. The experimental verification is presented in Section VII using a scaled-down setup. Section VIII concludes this paper.

II. Proposed Topology

The proposed 6L-FCB converter topology is shown in Fig. 1. The output voltage levels are synthesized by adding or subtracting FC voltages from the dc-link voltage. To ensure equally spaced steps in the output voltages, the FCs are charged to $V_{\rm dc}/5$. A total of 6 output levels can be achieved from 16 distinct switching combinations. The blocking voltage of switches $S_{\rm x1}$ and $S_{\rm x9}$ is equal to $2V_{\rm dc}/5$, while that of other switches is $V_{\rm dc}/5$. The output-phase voltage levels are equal to $0.5V_{\rm dc}$, $0.3V_{\rm dc}$, $0.1V_{\rm dc}$, $-0.1V_{\rm dc}$, $-0.3V_{\rm dc}$, and $-0.5V_{\rm dc}$ with respect to the midpoint dc-link voltage.

The switching states corresponding to the proposed converter are shown in Table I. Similar to other FC-based converters, the

TABLE I
SWITCHING STATES OF THE PROPOSED 6L CONVERTER AND THE FC CHARGING/DISCHARGING STATUS

State	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	S_{x9}	S_{x10}	V_{Cx1}	V_{Cx2}	V_{Cx3}	V_{Cx4}	V_{xN}	Level
F	1	1	1	1	0	0	0	0	0	1	N	N	N	N	$0.5V_{dc}$	5
E3	1	1	1	0	0	1	0	0	0	1	N	N	N	C (i_x>0) D (i_x<0)		
E2	1	0	1	1	1	0	0	1	0	0	C (i_x>0) D (i_x<0)	N	N	N	$0.3V_{dc}$	4
E1	1	1	0	1	0	0	1	0	0	1	C (i_x>0) D (i_x<0)	C (i_x>0) D (i_x<0)	N	D (i_x>0) C (i_x<0)		
D4	1	0	1	0	1	1	0	1	0	0	C (i_x>0) D (i_x<0)	N	N	C (i_x>0) D (i_x<0)		
D3	1	1	0	0	0	1	1	0	0	1	C (i_x>0) D (i_x<0)	C (i_x>0) D (i_x<0)	N	N	$0.1V_{dc}$	3
D2	1	0	0	1	1	0	1	1	0	0	C (i_x>0) D (i_x<0)	C (i_x>0) D (i_x<0)	C (i_x>0) D (i_x<0)	D (i_x>0) C (i_x<0)		
D1	0	1	1	1	0	0	0	0	1	1	D (i_x>0) C (i_x<0)	D (i_x>0) C (i_x<0)	D (i_x>0) C (i_x<0)	N		
C4	0	1	0	1	0	0	1	0	1	1	N	N	D (i_x>0) C (i_x<0)	D (i_x>0) C (i_x<0)		
C3	0	0	1	1	1	0	0	1	1	0	N	D (i_x>0) C (i_x<0)	D (i_x>0) C (i_x<0)	N	$-0.1V_{dc}$	2
C2	0	1	1	0	0	1	0	0	1	1	D (i_x>0) C (i_x<0)	D (i_x>0) C (i_x<0)	D (i_x>0) C (i_x<0)	C (i_x>0) D (i_x<0)		
C1	1	0	0	0	1	1	1	1	0	0	C (i_x>0) D (i_x<0)	C (i_x>0) D (i_x<0)	C (i_x>0) D (i_x<0)	N		
B3	0	0	0	1	1	0	1	1	1	0	N	N	N	D (i_x>0) C (i_x<0)		
B2	0	1	0	0	0	1	1	0	1	1	N	N	D (i_x>0) C (i_x<0)	N	$-0.3V_{dc}$	1
B1	0	0	1	0	1	1	0	1	1	0	N	D (i_x>0) C (i_x<0)	D (i_x>0) C (i_x<0)	C (i_x>0) D (i_x<0)		
A	0	0	0	0	1	1	1	1	1	0	N	N	N	N	$-0.5V_{dc}$	0

C: Charging D: Discharging N: No Change

proposed converter has redundant switching states to generate output voltage levels. For example, there are four redundant switching states to generate the voltage levels of $0.1V_{dc}$ and $-0.1V_{dc}$, and three redundant switching states to generate the voltage levels of $0.3V_{dc}$ and $-0.3V_{dc}$. Each redundant switching state provides a different charging and discharging current path for FCs. This feature is used to achieve voltage balancing of the FCs.

III. MODULATION TECHNIQUE

There are two basic carrier-based modulation techniques to realize the desired staircase output voltage in multilevel converters, namely phase-shifted carrier pulsewidth modulation (PSC-PWM) and level-shifted carrier PWM (LSC-PWM) [31], [33]. The LSC-PWM scheme is a well-known method used in both commercially available FCM and CHB converters [33]. An attractive feature of the LSC-PWM is the relatively low harmonic contents of the output voltage [34]. In this paper, the in-phase LSC-PWM along with an appropriate capacitor voltage balancing method is employed. The details of switching signal generation using LSC-PWM scheme have been presented in textbooks and literature and, thus, is not presented here. It must be noted that other modulation techniques, such as space-vector PWM (SV-PWM), are also applicable to the proposed converter.

To implement the LSC-PWM in the proposed converter, first, the desired staircase output voltage is synthesized by the proper comparison of the reference (or modulating) and carrier signals. Once the output voltage pattern and its levels are synthesized, the switching states corresponding to these voltage levels are obtained and applied to the power switches. Table I shows different voltage levels along with their corresponding switching states. It can be seen that there are redundant switching states associated with some voltage levels, which are the result of the converter topology. Each redundant switching state can charge or discharge the FCs in different manner, which is also shown in Table I. By selecting the appropriate switching state at different instants, the FC voltages are regulated at the desired level. Such an algorithm is usually known as capacitor voltage balancing method in the literature and is discussed in detail in Section IV.

IV. CAPACITOR VOLTAGE BALANCING METHOD

Capacitor voltage balancing is an important task in FC-based topologies and is accomplished by the help of redundant switching states. Table I shows different switching states for the proposed converter for phase x ($x = a, b, c$). For each switching state, the capacitor's charging/discharging status is determined based on the phase current direction, as shown in Table I. It is worth noting that similar to other FC-based topologies, the voltage of FCs in each phase is only dependent on the same phase

current. Therefore, the algorithm of switching state selection for capacitor voltage balancing can be independently derived for each phase.

The deviation of the FC voltages from their nominal values can be expressed as

$$\begin{aligned}\Delta V_{Cx1} &= V_{Cx1} - 0.2V_{\rm dc}\\ \Delta V_{Cx2} &= V_{Cx2} - 0.2V_{\rm dc}\\ \Delta V_{Cx3} &= V_{Cx3} - 0.2V_{\rm dc}\\ \Delta V_{Cx4} &= V_{Cx4} - 0.2V_{\rm dc}, \quad x = a, b, c\end{aligned} \tag{1}$$

where V_{Cx1}, V_{Cx2}, V_{Cx3}, and V_{Cx4} are the FC voltages of phase *x*. To achieve capacitor voltage balancing, these voltage deviations should be adjusted as close to zero as possible. In this regard, a cost function can be defined as [30]

$$J_x = \frac{1}{2}\sum_{k=1}^{4} C\left(\Delta V_{Cxk}\right)^2, \quad x = a, b, c \tag{2}$$

where J_x is the cost function associated with phase *x* and reaches its minimum value at zero when the voltage deviations are equal to zero. To minimize this cost function, the following condition should be satisfied:

$$\frac{dJ_x}{dt} = \sum_{k=1}^{4} C\,\Delta V_{Cxk}\frac{dV_{Cxk}}{dt} = \sum_{k=1}^{4}\Delta V_{Cxk}\cdot i_{Cxk} \le 0 \tag{3}$$

where i_{Cxk} is the current of the flying capacitor *k* of phase *x*. It is worth noting that the capacitor currents can be derived by knowing the phase current i_X and the switching state.

The switching state selection scheme is as follows. The employed modulation technique determines each phase voltage level. Upon any phase voltage level change, the capacitor voltages V_{Cx1}, V_{Cx2}, V_{Cx3}, and V_{Cx4} and the phase current i_X are measured. Furthermore, all possible redundant switching states that result in the given voltage level are obtained from Table I. Consequently, (3) is calculated for all switching states and the switching state that results in the lowest dJ_x/dt is selected to ensure the fastest convergence of J_x to its minimum value. For example, let us assume that the modulation technique assigns voltage level 3 to phase *a*. The four redundant switching states D_1, D_2, D_3, and D_4 (corresponding to level 3 in Table I) are the candidates to produce this voltage level. Each of these states produces its own charging/discharging current for the capacitors in phase *a*. Thus, i_{Cak} can be determined based on each switching state and the phase current i_X. Finally, knowing the value of ΔV_{Cak} by measurement, (3) is calculated for each switching state, and the one which results in the lowest dJ_x/dt is selected. The flowchart corresponding to this switching state selection technique is presented in Fig. 2.

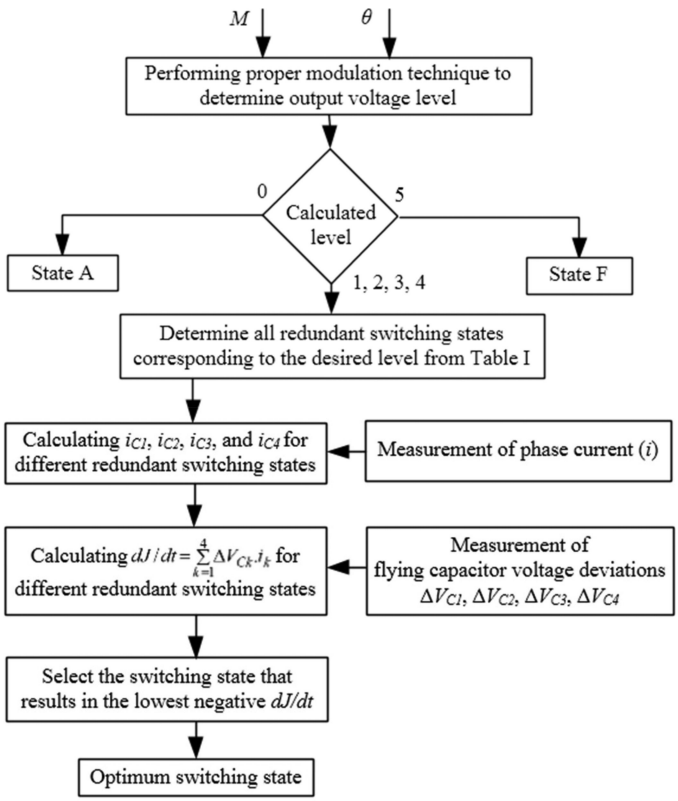

Fig. 2. Capacitor voltage balancing algorithm.

V. Comparison

Many parameters are involved in selecting a multilevel converter for a given application. These include the number of active switches and diodes, the number of capacitors, the quality of output voltage (the number of levels and total harmonic distortion, the operating range of inverter in terms of output PF and modulation index, losses, and the required number of dc source.

To make a realistic and fair comparison, in this section, the proposed converter is compared with other existing six-level converters with single dc source. This is because the topologies with multiple isolated dc sources (such as CHB) may not be economically feasible in some applications. On the other hand, as stated in Section I, the number of proposed six-level converters with single dc supply is limited in the literature.

Based on the above explanation, a 6L-DCM, a 6L-FCM, and the 6L-HI, presented in [28], are selected for the comparison. The first two converters belong to two classic families of multilevel converters by which any number of voltage levels can be theoretically realized. In reality, however, the capacitor voltage balancing in 6L-DCM requires special techniques that lead to increased switching frequency [16].

In the following section, different parameters that have direct influence on the size, cost, and performance of the converters under study are compared. For a meaningful comparison, the dc-link voltage ($V_{\rm dc}$), the effective switching frequency, and the voltampere rating of the compared converters are assumed to be the same.

A. Semiconductor Count and Rating

The number of semiconductor switches is an important parameter in a power electronic converter as it directly affects the size, cost, complexity, and losses of the converter.

TABLE II
COMPARISON OF SEMICONDUCTOR CHARACTERISTICS AMONG DIFFERENT 6L CONVERTERS AND THE PROPOSED CONVERTER

Topology	No. of Switches	Blocking Voltage of Switches (per unit)	Total Blocking Voltage of Switches (per unit)	No. of Diodes
DCM	30	1	30	70
FCM	30	1	30	0
6L-HI	26	1 and 2	38	5
Proposed 6L-FCB	30	1 and 2	36	0

TABLE III
SYSTEM PARAMETERS FOR THE TOPOLOGIES UNDER COMPARISON

Parameter	Value
DC Source Voltage (V_{dc})	5 kV
Carrier Frequency (f_c)	2 kHz
Capacitance of Flying Capacitors	2.2 mF
Blocking Voltage of Actual Switches	1 kV
Modulation Index	0.95
Load Current	360 A
Load Power Factor	0.8

The actual switch count in a converter depends not only on its topology, but also on the current and voltage rating of switches. In other words, the current and voltage rating of a switch determine the actual number of semiconductor switches needed to realize that switch. The specifications of the switches used in the topologies under comparison are listed in Table II. In the table, it is assumed that the current rating of all switches is more or less the same, and thus, the actual number of switches is determined based only on the converter topology and the voltage rating of switches. Therefore, the total blocking voltage of switches, calculated in column four, is used as an index to show the actual number of active switches employed in the converter structure. In calculating this index, it must be noted that in DCM and FCM topologies, all the switches have the same voltage rating, whereas in 6L-HI and the proposed 6L topologies, some switches have voltage rating twice as much as others. Based on the total blocking voltage index, it can be seen from Table II that the 6L-FCM topology has the lowest number of switches among other topologies. However, this topology suffers from the high number of capacitors, as explained in Section I [5], and, thus is not attractive for industrial applications. The 6L-DCM has similar total blocking voltage, but needs 60 diodes that makes it unattractive. Furthermore, the dc-link capacitor voltage balancing requires special techniques for a 6L-DCM converter [14]–[16]. It can be seen that the proposed 6L-FCB converter has lower total blocking voltage than the 6L-HI converter besides not needing any extra diode.

Based on Table II, and as it is already elaborated in [28], the 6L-HI topology outperforms both classic 6L-DCM and 6L-FCM topologies. For example, due to the decrease in the component count in the 6L-HI, it is shown that the total cost of the 6L-HI is about 60% and 81% compared to the DCM and FCM converters, respectively [28]. Therefore, in the rest of this section, the proposed 6L-FCB topology is compared only with 6L-HI topology from the standpoint of other comparison criteria.

TABLE IV
CAPACITORS VOLTAMPERE CALCULATION FOR THE 6L-HI TOPOLOGY

Measured Parameters		Required Capacitors: DC link split capacitors	Required Capacitors: Flying capacitors (each leg)	Required Capacitors: Total
Voltages (kV)		1, 3, 1	2	11
PF=0	Currents (A)	225, 240, 225	243	
	∑VI (kVA)	1170	486	**2628**
PF=0.2	Currents (A)	279, 285, 279	240	
	∑VI (kVA)	1413	480	**2853**
PF=0.4	Currents (A)	324, 348, 324	225	
	∑VI (kVA)	1692	450	**3042**
PF=0.6	Currents (A)	375, 414, 375	198	
	∑VI (kVA)	1992	396	**3180**
PF=0.8	Currents (A)	456, 498, 456	156	
	∑VI (kVA)	2406	312	**3342**
PF=1	Currents (A)	498, 504, 498	123	
	∑VI (kVA)	2490	246	**3228**

TABLE V
CAPACITORS VOLTAMPERE CALCULATION FOR THE PROPOSED 6L-FCB TOPOLOGY

Measured Parameters		Required Capacitors: Flying capacitors (each leg)	Required Capacitors: Total
Voltages (kV)		1, 1, 1, 1	12
PF=0	Currents (A)	246, 252, 246, 270	
	∑VI (kVA)	1014	**3042**
PF=0.2	Currents (A)	246, 246, 246, 264	
	∑VI (kVA)	1002	**3006**
PF=0.4	Currents (A)	246, 252, 246, 252	
	∑VI (kVA)	996	**2988**
PF=0.6	Currents (A)	225, 225, 225, 225	
	∑VI (kVA)	900	**2700**
PF=0.8	Currents (A)	186, 192, 192, 204	
	∑VI (kVA)	774	**2322**
PF=1	Currents (A)	162, 165, 165, 192	
	∑VI (kVA)	684	**2052**

B. Capacitors

Capacitors are widely used in power electronic converters to absorb the current ripple and provide smooth dc voltage. In high-power applications, these capacitors usually consist of several smaller capacitor units connected in a serial/parallel configuration to attain both the desired capacitance and voltage/current rating. As a result, the actual number of capacitor units used in a converter is determined by the number of capacitors shown in the topology and their voltage/current rating. Therefore, similar to the total blocking voltage index used for semiconductor switches, the total capacitors voltampere in each topology can

TABLE VI
COMPARISON OF SWITCHING FREQUENCIES BETWEEN THE 6L-HI AND THE PROPOSED 6L-FCB CONVERTERS

Topology	6L-HI					Proposed 6L-FCB				
Switch	S_1	S_2	S_3	S_4	S_{aux}	S_1	S_2	S_3	S_4	S_5
Average Switching Frequency (Hz)	2000	2000	450	500	1400	650	750	550	750	500

be used as an index to get an estimate of the size of capacitors used in a converter.

The rms current of capacitors in different load PFs is obtained using simulations on PSIM software for two topologies. The parameters associated with the converters used in these simulations are listed in Table III. Tables IV and V show the characteristics of required capacitors in 6L-HI and the proposed 6L-FCB converters, respectively. The total capacitors voltampere are shown in the right column of Tables IV and V for different load PFs. Taking the worst case into consideration, the total voltampere of capacitors in the proposed 6L-FCB topology is about 10% lower than the 6L-HI topology.

C. DC-Link Capacitor Voltage Balancing

It has been explained in Section I that capacitor voltage balancing problem in DCM converters can be overcome by using auxiliary circuits [14]. This approach has been used in the 6L-HI converter. However, as mentioned in [28], the total cost of the 6L-HI topology is increased by about 40% due to the auxiliary balancing circuit. On the other hand, the proposed 6L-FCB converter is based on a single dc link (without split capacitors), which eliminates the need for complex additional balancing circuit.

D. Switching Frequency

The average switching frequency ($f_{sw,avg}$) of different switches for two converters is listed in Table VI when LSC-PWM with the carrier frequency of 2 kHz is employed. As can be seen, $f_{sw,avg}$ is about one-fourth to one-third of the carrier frequency in the proposed 6L-FCB converter, which is common when employing LSC-PWM schemes. However, $f_{sw,avg}$ is equal to the carrier frequency, i.e., 2 kHz, for outer switches S_{x1} and S_{x2} ($x = a, b, c$) in the 6L-HI. This is due to the fact that these switches have to be active for each voltage-level transition. Therefore, $f_{sw,avg}$ of these switches is equal to the number of voltage-level transitions, which is equal to the carrier frequency in LSC-PWM schemes. Such a high switching frequency could limit the application of this converter in medium- and high-power applications, especially when noting that the blocking voltage of these switches is twice as much as other switches in this structure. In Section V-E, it can be seen that the high switching frequency of these switches leads to higher switching losses.

One must note that when using the same type of carrier-based modulation technique for two converters with different topology, the resultant output voltage pattern would be the same. Having said that, the harmonic spectra of output voltages are the same for both the proposed 6L-FCB and the 6L-HI topologies in this comparison.

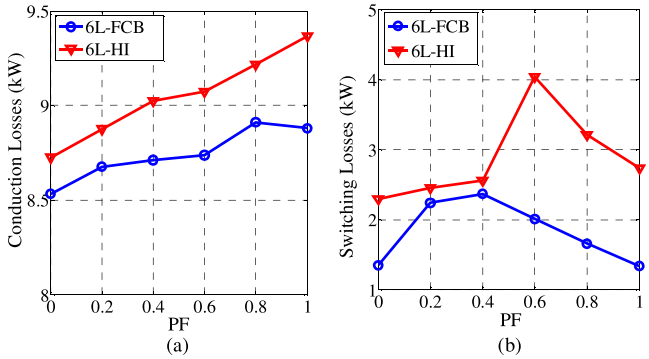

Fig. 3. Power losses versus load PF in the proposed 6L-FCB and the 6L-HI topologies. (a) Conduction losses. (b) Switching losses.

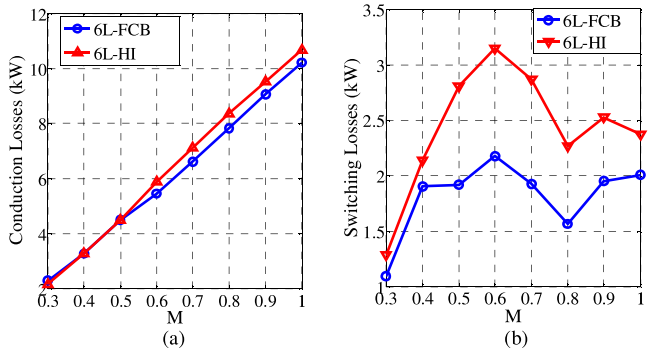

Fig. 4. Power losses versus modulation index in the proposed 6L-FCB and the 6L-HI topologies. (a) Conduction losses. (b) Switching losses.

E. Power Losses

The power loss calculation is carried out using the loss simulation package of PSIM software. For this purpose, CM1000HA-24H switch rated at 1000 A at 1200 V made by POWEREX was used. One and two series connections of this device are used for the switches with the blocking voltages of $V_{dc}/5$ and $2V_{dc}/5$, respectively. The parameters associated with the power loss simulation are listed in Table III. With this implementation, both the proposed 6L-FCB and 6L-HI topologies utilize 12 insulated gate bipolar transistor (IGBTs) in each converter phase.

The conduction and switching losses for two converters under different load PFs and modulation indexes are shown in Figs. 3 and 4, respectively. As can be seen, the losses of the proposed topology are lower than 6L-HI topology in the entire operating range.

The higher switching loss of 6L-HI converter can be contributed to the higher switching frequency of the main switches, as explained in Section V-D. The conduction loss of 6L-HI converter is slightly higher than that of the proposed topology. This is due to the additional switches and diodes in the input voltage balancing stage. As a matter of fact, a major portion of converter

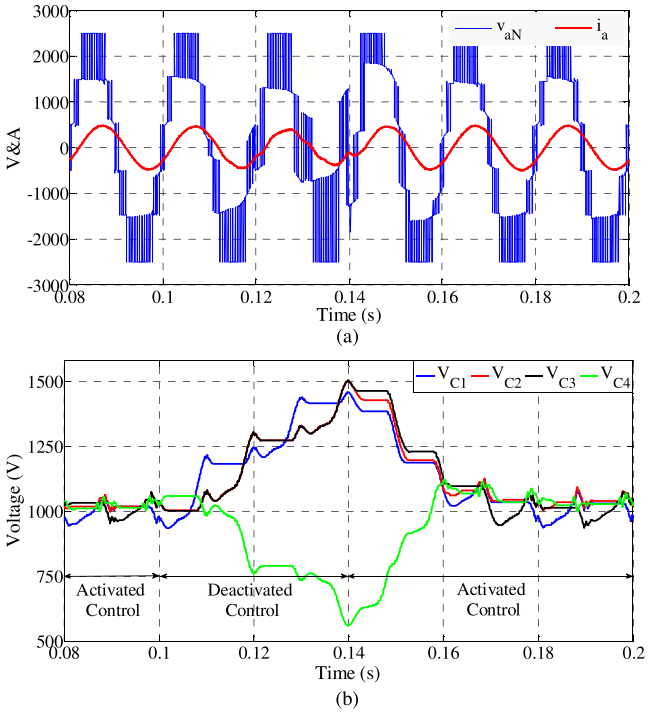

Fig. 5. Simulation results in the steady-state condition when the capacitor voltage balancing control is deactivated at $t = 0.1$ s and activated again at $t = 0.14$ s. (a) Output voltage and current. (b) FC voltages.

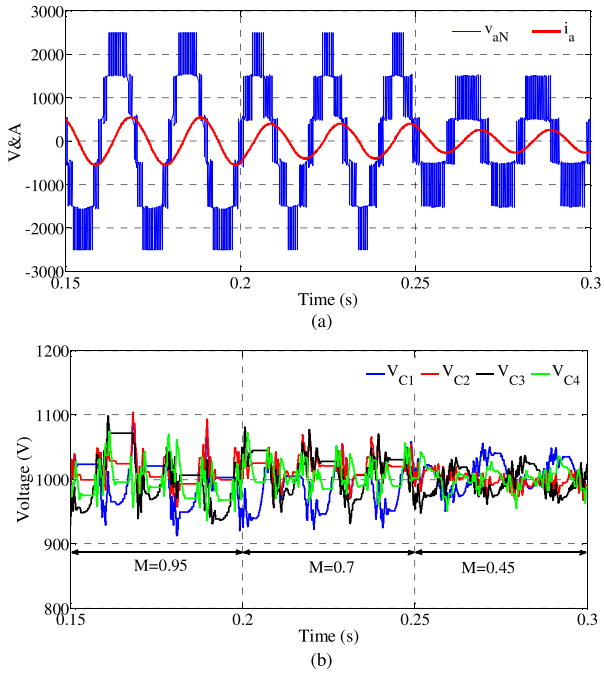

Fig. 6. Simulation results corresponding to the modulation index change. (a) Output voltage and current. (b) FC voltages.

voltampere is handled by the voltage balancing stage, which is basically a high-power dc–dc converter.

F. Loss Balancing

An important practical issue in selecting a multilevel converter is that how balanced the semiconductor losses for different switches are [5]. In this regard, the FC-based topologies inherently have better loss balancing characteristics as the average capacitors' currents must be zero, which results in the same rms current in all switches and, thus, the same conduction losses. The switching frequency in these topologies is also more or less the same. Therefore, a good loss balancing can also be expected in the proposed 6L-FCB converter due to its symmetry and the fact that it is derived from an FC-based topology.

On the other hand, as shown in Sections V-D and V-E, the switching frequency is not the same in all switches in 6L-HI converter, and thus, imbalance in the loss of different switches can be expected. This issue is not elaborated in this paper.

VI. Simulation Results

In this section, the proposed 6L-FCB topology is simulated as the first step to evaluate the performance of the converter along with the proposed voltage balancing algorithm. All simulations are carried out with PSIM software for a converter with the parameters given in Table III. All switches are assumed to be ideal at this stage as the scope of simulation is to evaluate the modulation technique and voltage balancing algorithm.

Fig. 5 illustrates the simulation results when the LSC-PWM scheme has been employed [28]. In the beginning, the capacitor

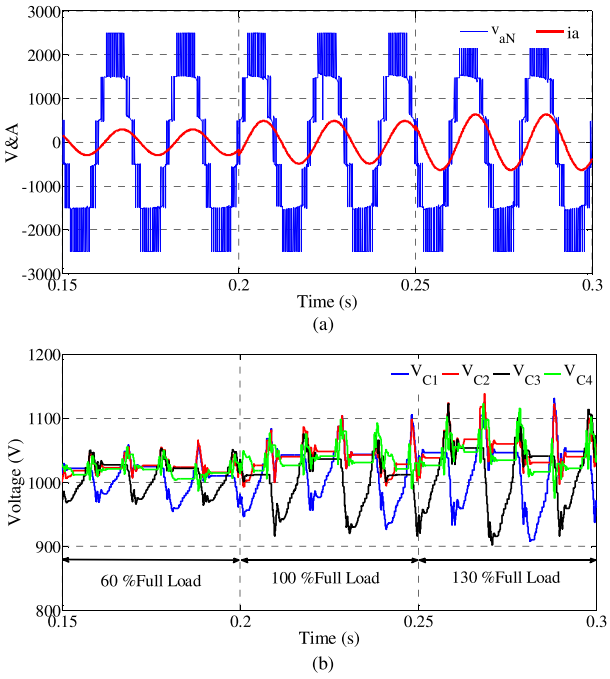

Fig. 7. Simulation results corresponding to load change from 60% to 100% at $t = 0.2$ s and to 130% at $t = 0.25$ s. (a) Output voltage and current. (b) FC voltages.

voltage balancing algorithm is operational, and thus, the FC voltages are regulated at desired values, i.e., $V_{dc}/5$. At $t = 0.1$ s, the balancing control is deactivated and each output voltage level is generated with a fixed switching state. As expected, the FC voltages are deviated from their nominal values. At $t = 0.14$ s,

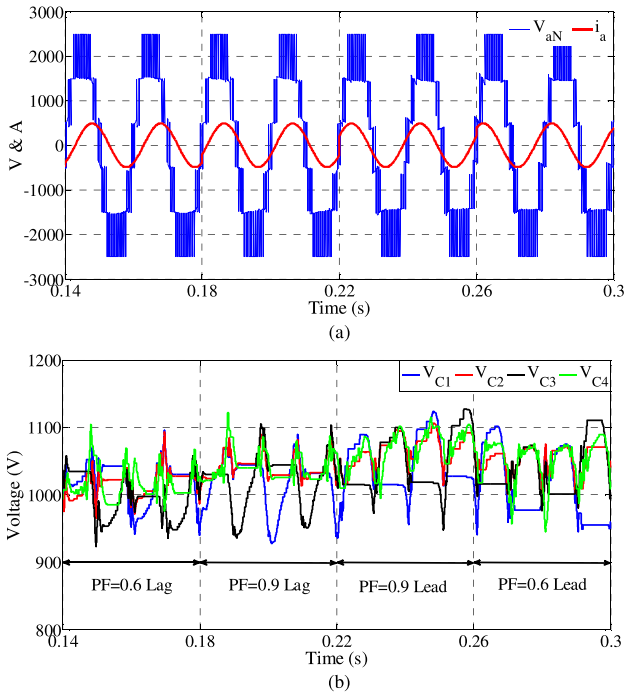

Fig. 8. Simulation results corresponding to the PF change. (a) Output voltage and current. (b) FC voltages.

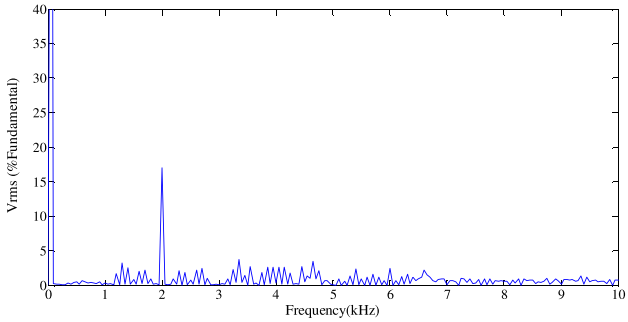

Fig. 9. Output voltage frequency spectra in steady state.

TABLE VII
EXPERIMENTAL SYSTEM PARAMETERS

System Parameter	Value
IGBTs	BUP400D
Current and voltage ratings of IGBTs	22A, 600 V
DC sources voltage (V_{dc})	125 V
Capacitance of flying capacitors	2.2 mF
PWM carrier frequency (f_c)	2 kHz
Reference voltage frequency (f_o)	50 Hz
Modulation index (M)	0.95
Load-Resistive, Inductive (R_L, L_L)	30 Ω, 70 mH

the balancing algorithm is activated again and FC voltages are regulated to their nominal values.

In order to show the transient performance of the proposed voltage balancing scheme, two step changes from $M = 0.95$ to $M = 0.7$ at $t = 0.2$ s and to $M = 0.45$ at $t = 0.25$ s are applied. The output voltage, phase current, and FC voltages are shown

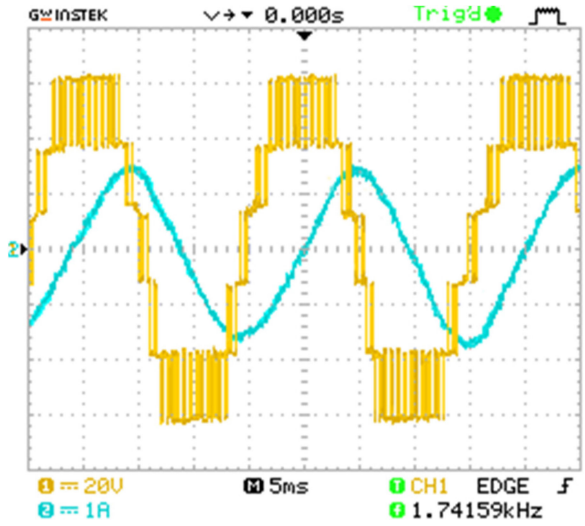

Fig. 10. Experimental results showing output voltage and load current.

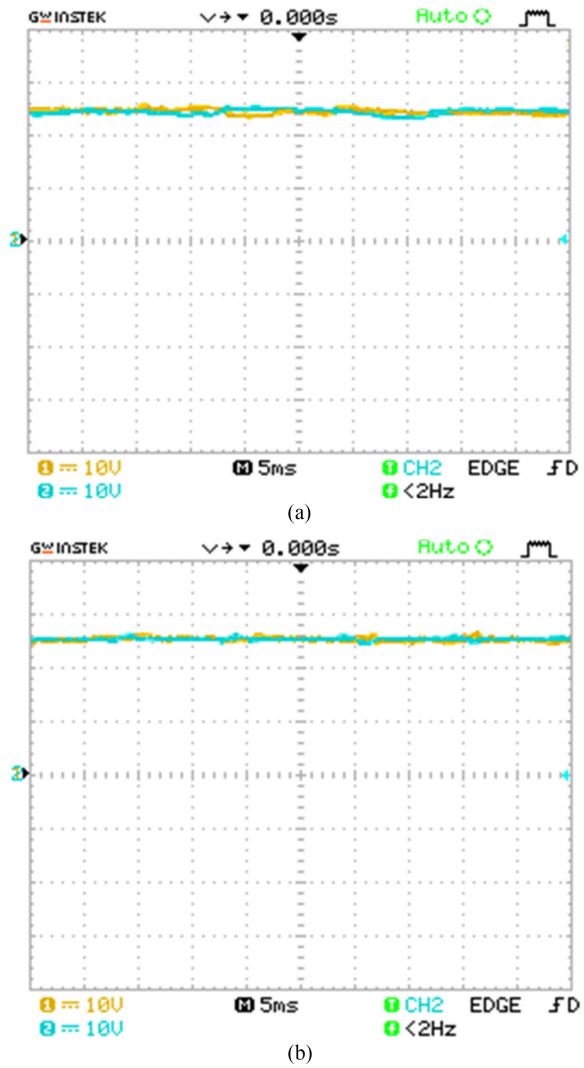

Fig. 11. Experimental results showing FC voltages. (a) V_{C1} and V_{C3}. (b) V_{C2} and V_{C4}.

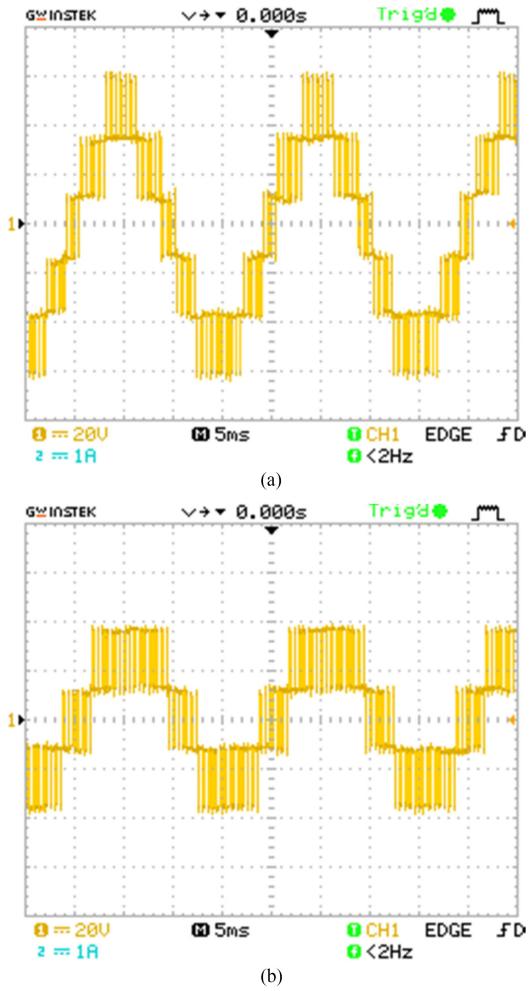

Fig. 12. Experimental results of output voltage at different modulation indexes. (a) $M = 0.7$. (b) $M = 0.45$.

in Fig. 6. As can be observed, the FC voltages remain regulated at the desired values with modulation index variations.

Fig. 7 shows system's performance under load change from 60% full load to 100% full load at $t = 0.2$ s and to 130% full load at $t = 0.25$ s. It can be seen that the FC voltages are well regulated at the desired values during load change. As expected, the amplitude of the capacitor voltage ripples is higher at higher loads.

Fig. 8 shows the simulation results with different load PFs. The proposed 6L-FCB converter properly generates a six-level output-phase voltage and the FC voltages are regulated under all operating conditions. It can be seen that the ripple voltage of FCs has been reduced under lower load PFs.

The frequency spectra of the output voltage are shown in Fig. 9. The first dominant harmonics of the output voltage are centered on the carrier frequency f_c.

VII. Experimental Results

In order to verify the practicability of the proposed topology, a scaled-down version of the proposed 6L-FCB converter was implemented in the laboratory. The parameters of this experimental setup are listed in Table VII.

Fig. 10 shows the experimental waveforms associated with the proposed 6L-FCB converter. The voltages of the FCs are also shown in Fig. 11. As can be seen, the FC voltages are well regulated around $V_{dc}/5$, i.e., 25 V. In order to show the performance of the proposed topology in different operating points, the modulation index is set to the different values of $M = 0.7$ and 0.45. The measured voltages are shown in Fig. 12.

VIII. Conclusion

In this paper, a new six-level multilevel converter topology with a single dc source was proposed. The proposed converter demonstrates many advantages over existing six-level converters in the same family in terms of component count and rating, switching losses, and range of operation. These parameters are crucial in selecting a suitable topology for a multilevel converter. While six-level voltage pattern results in a high-quality ac voltage, using single dc source in the converter structure makes it attractive in applications where the converter is to be supplied by a bulk dc supply, thus avoiding rather expensive and bulky multi-dc-source topologies. The proposed modulation strategy in this paper makes it possible to control and regulate all capacitor voltages without the need of auxiliary circuits or increasing switching frequency. Simulation and experimental results illustrate the converter operation under different operating conditions.

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