A Hybrid Nine-Level, 1-ϕ Grid Connected Multilevel Inverter With Low Switch Count and Innovative Voltage Regulation Techniques Across Auxiliary Capacitor

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***Abstract*—A 1-ϕ hybrid nine-level inverter (H9LI) topology has been proposed in this paper. The proposed H9LI topology uses a simple phase disposition pulsewidth modulation strategy to generate nine-voltage levels in the output. The main advantage of this topology is that it has a low switch count (ten switches) compared to the existing nine-level inverter topologies. To regulate the voltage across auxiliary capacitor, two innovative control techniques are proposed, which are integrated with the inverter modulation technique itself. Hence, it does not require any extra voltage balancing circuits to maintain the voltage across the auxiliary capacitor and input dc capacitors. A major advantage of these control techniques is that they eliminate the sensing of the coupled inductor current. Another significant advantage of H9LI is that loss distribution among all the power switches is more uniform compared to existing nine-level inverters. Due to low part count and absence of extra voltage balancing circuits, the H9LI achieves higher efficiency ($\eta \approx 94.5\%$) and lower cost. Furthermore, the requirement of filter size reduces due to the presence of coupled inductor in H9LI. The proposed 1-ϕ grid connected H9LI is verified through MATLAB/Simulink simulations and validated through experiments on a laboratory prototype of 400-VA rating.**

***Index Terms*—Auxiliary capacitor, hybrid nine-level inverter (H9LI), multilevel inverter (MLI), phase disposition pulsewidth modulation (PDPWM).**

I. Introduction

IN RECENT years, the multilevel inverter (MLI) technology has become very popular. Generally, the MLIs are preferred for medium voltage and high-power applications [1]. The major applications of MLIs are electric drives, traction, HVdc, utility interface for renewable energy systems, and STATCOM [2], [3]. Even though the MLIs comprise several devices and components

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components in this MLI makes hardware implementation a bit difficult. To reduce the power component count, Babaei [7] proposed a nine-level MLI. It consists of 14 power switches and four input dc sources. Among the power switches, some are bidirectional. To reduce the number of power components further, Ebrahimi *et al.* [8] also proposed a nine-level MLI topology, which uses fewer power switches. This nine-level MLI topology requires 12 power switches and four input dc sources. Peng [9] has come up with a generalized MLI topology with single input dc source, but this topology uses several auxiliary capacitors and the voltage regulation of all these capacitors is a cumbersome task.

Some other researchers have also proposed MLI topologies that accommodate auxiliary capacitors to generate multilevel output voltage [10]–[18]. These include nested neutral point clamped (NNPC) MLI [10], [11], FC-based active neutral point clamped (FC-ANPC) MLI [12], [13], and FC-based hybrid active neutral point clamped (FC-HANPC) MLIs [14]–[17]. The FC-ANPC MLI consists of many switches and auxiliary capacitors, due to which complex control is required to regulate the voltage across auxiliary capacitors. The NNPC and FC-HANPC MLIs also use many auxiliary capacitors similar to FC-ANPC MLI, which increases the complexity of hardware implementation. Some authors have worked on modular multilevel converters (MMC) for medium voltage and high-power applications, but they also require many auxiliary capacitors [18]–[21]. In fact, MMCs also need complex algorithms to regulate the voltage across auxiliary capacitors. Some researchers have proposed coupled inductor based MLI configurations [22]–[24], which require fewer power switches, but these configurations require extra voltage balancing circuits to balance the voltages across the input dc capacitors.

To overcome the disadvantages, such as high count of power switches, auxiliary capacitors and dc sources in the existing MLI topologies, this paper proposes a new hybrid nine-level inverter (H9LI) topology. The main objective of H9LI is to produce ac output voltage of minimum or negligible distortion with low component count. The nine-level output voltage is generated with fewer power switches leading to simple control, low maintenance, and most importantly, enhanced reliability. The proposed topology combines the advantages of diode-clamped MLI, capacitor clamped MLI, and coupled inductor based MLIs. The major advantages of the H9LI are summarized as follows.

1) It uses fewer power switches (only ten switches per phase leg).
2) It requires only one auxiliary dc capacitor and two input dc capacitors.
3) It uses a coupled inductor for reducing the requirement of dc capacitors. The dc capacitors are known to have a low lifespan.
4) The topology is capable of inherent regulation of the auxiliary capacitor voltage. No extra current sensors are required.
5) The loss distribution (especially conduction losses) among all the high-frequency power switches and low-frequency switches are uniform.
6) Lower common mode voltage.

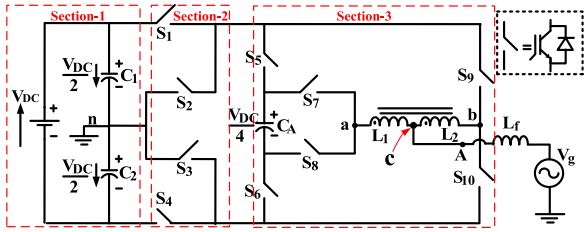


Fig. 1. Proposed 1-ϕ H9LI topology.

TABLE I
INPUT AND OUTPUT VOLTAGES OF COUPLED INDUCTOR

V_{an}	V_{bn}	V_{An}
$+4V_{DC}/8$	$+4V_{DC}/8$	$+4V_{DC}/8$
$+2V_{DC}/8$		$+3V_{DC}/8$
0		$+2V_{DC}/8$
$+4V_{DC}/8$	0	$+2V_{DC}/8$
$+2V_{DC}/8$		$+V_{DC}/8$
0		0
$-4V_{DC}/8$	$-4V_{DC}/8$	$-4V_{DC}/8$
$-2V_{DC}/8$		$-3V_{DC}/8$
0		$-2V_{DC}/8$
$-4V_{DC}/8$	0	$-2V_{DC}/8$
$-2V_{DC}/8$		$-V_{DC}/8$

7) It can provide reactive power support to the grid, which makes it (low voltage ride through) LVRT capable.

The reduction in the number of switches and auxiliary capacitors is achieved by incorporating a coupled inductor. Though a coupled inductor is not always preferable in all types of applications, it is advantageous from the reliability point of view. The capacitors are considered as the weak link of an electrical circuit and the switches are the most sensitive part of the circuit. Every single switch needs a separate control circuit along with the protection circuit which again increases the maintenance as well as the overall cost of the circuit. Reduction in the number of controlled devices helps the topology to be robust and cost effective.

II. DESCRIPTION AND THE WORKING PRINCIPLE OF H9LI

Fig. 1 shows the proposed H9LI topology. It generates a nine-voltage levels in the output with only ten power switches, one auxiliary capacitor (C_A), and two input dc capacitors (C_1, C_2). It has joint features of diode clamped, FC, and coupled inductor based MLIs. The H9LI has a single dc source at the input, which is divided into two halves with the support of C_1 and C_2. The three-level NPC voltages are divided into five voltage levels by using an auxiliary capacitor, C_A, which is regulated at a voltage of $V_{DC}/4$. A coupled inductor is incorporated in the H9LI, whose two ends experience five voltage levels ($\pm 4V_{DC}/8, \pm 2V_{DC}/8$ and 0) and three voltage levels ($\pm 4V_{DC}/8$ and 0), respectively, due to which the H9LI generates nine different voltage levels at the midpoint "c" of the coupled inductor, as listed in Table I. The nine voltage levels produced by H9LI are $\pm 4V_{DC}/8, \pm 3V_{DC}/8, \pm 2V_{DC}/8, \pm V_{DC}/8$ and 0, as shown in Fig. 2. Each switch used in H9LI is a

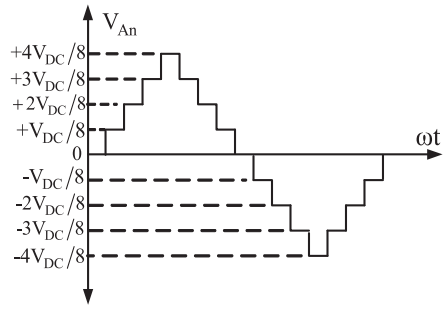


Fig. 2. Synthesized output voltage waveform of the H9LI.

TABLE II
ALL 16 SWITCHING STATES OF THE H9LI

SWITCHES CONDITION (1=ON, 0=OFF)										V_{An}	Switches states	switches conducting
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}			
1	0	1	0	1	0	1	0	1	0	$+4V_{DC}/8$	1	5
1	0	1	0	1	0	0	1	1	0	$+3V_{DC}/8$	2	5
1	0	1	0	0	1	1	0	1	0	$+3V_{DC}/8$	3	5
1	0	1	0	0	1	0	1	1	0	$+2V_{DC}/8$	4	5
1	0	1	0	1	0	1	0	0	1	$+2V_{DC}/8$	5	5
1	0	1	0	1	0	0	1	0	1	$+V_{DC}/8$	6	5
1	0	1	0	0	1	1	0	0	1	$+V_{DC}/8$	7	5
1	0	1	0	0	1	0	1	0	1	0	8	5
0	1	0	1	1	0	1	0	1	0	0	9	5
0	1	0	1	1	0	0	1	1	0	$-V_{DC}/8$	10	5
0	1	0	1	0	1	1	0	1	0	$-V_{DC}/8$	11	5
0	1	0	1	0	1	0	1	1	0	$-2V_{DC}/8$	12	5
0	1	0	1	1	0	1	0	0	1	$-2V_{DC}/8$	13	5
0	1	0	1	1	0	0	1	0	1	$-3V_{DC}/8$	14	5
0	1	0	1	0	1	1	0	0	1	$-3V_{DC}/8$	15	5
0	1	0	1	0	1	0	1	0	1	$-4V_{DC}/8$	16	5

combination of a fully controlled switch and an antiparallel diode, which allows the current to freewheel through the switches.

Section I of Fig. 1 represents the supply block where the single input dc supply is divided into two equal parts by using two input dc capacitors $(\mathrm{C}_1, \mathrm{C}_2)$ to provide the advantage of an NPC inverter. Section II comprises four switches. These four switches help in altering the voltage across Section III in positive and negative half cycles by changing the capacitors from one configuration to another. The polarity alternating feature could have been provided by a bridge circuit without splitting the dc source. But altering the polarity with single supply can only be used for the single-phase inverter. Therefore, the splitting technique makes the converter suitable for three-phase application. All possible 16 switching states of H9LI corresponding to nine-different levels of the output voltage are given in Table II. The current through the inductor and voltage across $\mathrm{C_A}$ are regulated by using the complementary switching states which gives better loss distribution among the various power switches. The role of complementary switching states is regulation of voltage across $\mathrm{C_A}$, control of current through inductor $(\mathrm{I_{L1}})$, and improvement of loss distribution among the various power switches. Switches S_1 to S_4 and $\mathrm{S}_9, \mathrm{S}_{10}$ have to withstand half of the dc link voltage, whereas switches S_5 to S_8 have to withstand one-fourth of the dc link voltage. Either, switches of different rating can be chosen as per the requirement in the circuit or more than one switch can be used in series to use switches of the same rating. The proposed H9LI can be used for the 3-ϕ application as well by adding two more legs consisting of Sections II and III and by keeping Section I common for all the three phases.

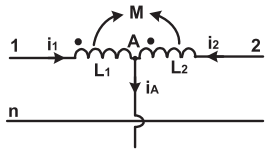


Fig. 3. Basic coupled inductor.

A. Role of the Coupled Inductor

The proposed H9LI can generate nine levels by using the coupled inductor [23], [24]. The basic operation of the coupled inductor [see Fig. 3] is explained with the help of the following equations:

$$M = K\sqrt{\mathrm{L}_1 \times \mathrm{L}_2} \tag{1}$$

$$\mathrm{V_{1n}} - \mathrm{V_{An}} = \mathrm{L}_1 \frac{di_1}{dt} - M\frac{di_2}{dt} = (\mathrm{L}_1 + M)\frac{di_1}{dt} - M\frac{di_A}{dt} \tag{2}$$

$$\mathrm{V_{2n}} - \mathrm{V_{An}} = \mathrm{L}_2 \frac{di_2}{dt} - M\frac{di_1}{dt} = (\mathrm{L}_2 + M)\frac{di_2}{dt} - M\frac{di_A}{dt} \tag{3}$$

where n denotes the neutral point.

Assume that self-inductances $(\mathrm{L}_1, \mathrm{L}_2)$ of the coupled inductors are equal and the coupling coefficient $K = 1$. Then, the mutual inductance (M) of the coupled inductor is equal to L_1 (or L_2). By applying the KCL at node "A" [see Fig. 3] the node current, i_a is given as follows:

$$i_1 + i_2 = i_A. \tag{4}$$

Adding (2) and (3) yields the following:

$$\mathrm{V_{An}} = \frac{\mathrm{V_{1n}} + \mathrm{V_{2n}}}{2}. \tag{5}$$

Using (5), the output voltage V_0 of the proposed H9LI topology is given as follows:

$$\mathrm{V}_0 = \mathrm{V_{An}}. \tag{6}$$

It can be observed that the coupled inductor adds the two input voltages $\mathrm{V_{1n}}$ and $\mathrm{V_{2n}}$. Without coupled inductor, the proposed H9LI can only generate five levels. But due to coupled inductor, the proposed H9LI can give nine voltage levels in the output voltage $(\mathrm{V_{An}})$ by varying the voltages applied across the coupled inductor (i.e., $\mathrm{V_{1n}}$, $\mathrm{V_{2n}}$).

B. Possible Switching States of H9LI

Table II gives the possible 16 switching states of H9LI, which generates nine different voltage levels at the output terminal. The gate pulses of switches S_1 and S_2 are complementary to each other. Similarly, S_3, S_4 also have complementary gate pulses. The switches $\mathrm{S}_1, \mathrm{S}_3$ are ON for switching states from1 to 8 (i.e., in positive half-cycle) and the power switches $\mathrm{S}_2, \mathrm{S}_4$ are ON for switching states from 9 to 16 (i.e., in negative half-cycle), which reduces the switching losses in the switches S_1 to S_4. The other complementary switching pairs are (S_5, S_6), (S_7, S_8), and (S_9, S_{10}).

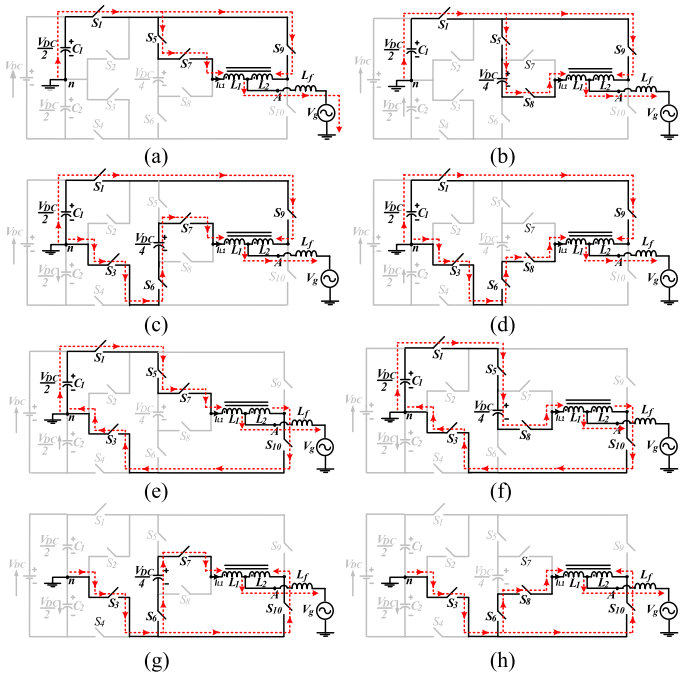


Fig. 4. All switching states (SS) of the 1-ϕ H9LI. (a) SS-1 (b) SS-2. (c) SS-3. (d) SS-4. (e) SS-5. (f) SS-6. (g) SS-7. (h) SS-8.

1) Switching States for the Positive Half-Cycle: In the positive half-cycle of the output voltage, the switches S_1 and S_3 are always kept ON in all the switching states. Similarly, in the negative half-cycle of the output voltage, the switches S_2 and S_4 are always kept ON in all the switching states. The switching states corresponding to the positive half-cycle are explained as follows.

Switching state 1: This state begins with turning ON of the switches S_1, S_3, S_5, S_7, and S_9. According to (6) the $+4V_{DC}/8$ output voltage level is generated by using this switching state-1. The current conduction path during switching state-1 is depicted in Fig. 4(a).

Switching state 2: This state begins with turning ON of switch S_3, S_8 and turning OFF switch S_7. According to (6), the $+3V_{DC}/8$ output voltage level is generated by using this switching state-2. The states of other switches remain unchanged or same as the previous switching state (i.e., switching state-1). The working of switching state-2 is shown in Fig. 4(b).

Switching state 3: This state begins with turning ON of switches S_3, S_6, S_7 and turning OFF switches S_5, S_8. According to (6), the $+3V_{DC}/8$ output voltage level is achieved by using this switching state-3. The states of the other switches remain the same as previous switching state (i.e., switching state-2). The current path during switching state-3 is shown in Fig. 4(c). The switching states 2 and 3 are complementary to each other and are used to charge or discharge "C_A" depending upon the direction of the current through it.

Switching state 4: This state begins with turning ON of switches S_3, S_8 and turning OFF of the switch S_7 while the states of other switches remain the same as the previous switching state (i.e., switching state 3). According to (6), the $+2V_{DC}/8$ output voltage level is generated by using the switching state 4. The working of switching state 4 is shown in Fig. 4(d).

Switching state 5: This state begins when the switches S_3, S_5, S_7, S_9 are turned ON and switches S_6, S_8, S_9 are turned OFF. All other switches continue to remain in their previous state (i.e., switching state 4). According to (6), the $+2V_{DC}/8$ output voltage level is generated by using this switching state 5. The working of switching state 5 is explained through Fig. 4(e), which shows the conduction path. Switching states 4 and 5 are complementary to each other, which are used to balance the voltage across the coupled inductor.

Switching state 6: This state begins with turning ON of switch S_3, S_8 and turning OFF of switch S_7. The states of the other switches are left unchanged or same as the previous switching state (i.e., switching state 5). According to (6), the $+V_{DC}/8$ output voltage level is achieved using this switching state 6. The working of switching state 6 is shown in Fig. 4(f).

Switching state 7: The beginning of this state is marked by the turning ON of switches S_3, S_6, S_7 and turning OFF of switches S_5, S_8. The other switches continue in the same state as the previous one (i.e., switching state 6). According to (6), the $+V_{DC}/8$ output voltage level is realized by utilizing switching state 7. The current conduction path during switching state 7 is shown in Fig. 4(g). Here, the switching states 6 and 7 are complementary to each other and are used to charge or discharge C_A depending on the direction of current through it.

Switching state 8: This state begins with turning ON of switch S_3, S_8 and turning OFF of switch S_7 by keeping the states of other switches unchanged (i.e., same as the switching state 7). According to (6), the "0" output voltage level is generated by using the switching state 8. The working of switching state 8 is shown in Fig. 4(h).

From Table II, it can be observed that for any output voltage level there are always five switches, which are conducting. Moreover, if all the 16 switching states are considered, it can be observed that any switch in the given topology conducts for eight switching states in a complete cycle. This helps in achieving a better loss distribution among all the switches.

C. Application of the Complementary Switching States

The switches of H9LI can be operated in 16 different combinations to produce nine distinct voltage levels. There are a total of seven pairs of switching combinations, which generate the same output voltage. These pairs are called as complementary switching combinations or switching states. To control the output voltage of H9LI, the voltage across auxiliary capacitor and current through coupled inductor are sensed. Depending on the direction of current through coupled inductor (I_{L1}), the voltage across the auxiliary capacitor is regulated. For a specific direction of current through the coupled inductor, the complementary switching states can change the current direction through the auxiliary capacitor without changing the terminal voltages of the coupled inductor. From Fig. 4(b) and (c), it can be observed that for a specific direction of current (I_{L1}) through inductor L_1, the direction of current through C_A is exactly opposite during switching states 2 and 3. If I_{L1} is positive, the current enters

TABLE III
EFFECT ON C_A DUE TO COMPLEMENTARY SWITCHING STATES

I_{L1}	Switching states	V_{An}	Effect on C_A
>0 or <0	2	$3V_{DC}/8$	+/-
	3		-/+
	6	$V_{DC}/8$	+/-
	7		-/+
>0 or <0	10	$-V_{DC}/8$	+/-
	11		-/+
	14	$-3V_{DC}/8$	+/-
	15		-/+

'+' Charging, '-' Discharging

TABLE IV
SELECTION OF THE COMPLEMENTARY SWITCHING STATES

Auxiliary capacitor voltage, V_{CA}	Current through Inductor, I_{L1}	Switching state
$>V_{Cmax}$	>0	3
$>V_{Cmax}$	<0	2
$<V_{Cmin}$	>0	2
$<V_{Cmin}$	<0	3

TABLE V
EFFECT OF COMPLEMENTARY SWITCHING STATES ON COUPLED INDUCTOR

Switching state	Output voltage (V_{An})	Voltage across coupled inductor
4	$+2V_{DC}/8$	$-4V_{DC}/8$
5	$+2V_{DC}/8$	$+4V_{DC}/8$
12	$-2V_{DC}/8$	$-4V_{DC}/8$
13	$-2V_{DC}/8$	$+4V_{DC}/8$

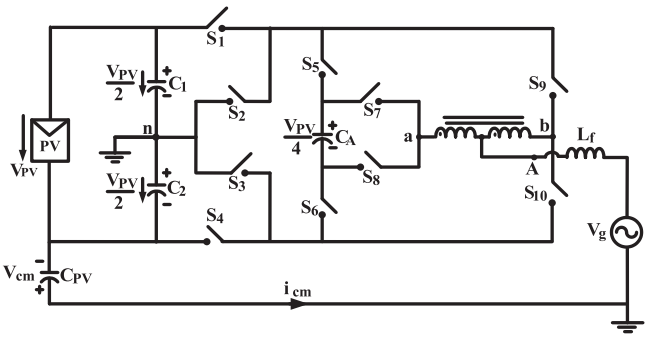


Fig. 5. Common mode model of the proposed H9LI configuration.

into C_A through the positive terminal which results in charging of C_A in switching state 2. In the switching state 3, current goes out of the positive terminal which results in discharging of C_A. During switching state 2, voltage at the positive terminal (V_{An}) of the coupled inductor is $+2V_{DC}/8$ (i.e., input capacitor voltage—auxiliary capacitor voltage). Similar to the switching state 2, in switching state 3 the voltage at the positive terminal (V_{An}) of the coupled inductor is $+2V_{DC}/8$ (auxiliary capacitor voltage). Both the switching states 2 and 3 produce an output voltage $= +3V_{DC}/8$, but result in charging or discharging of C_A depending upon the direction of I_{L1}, as per Table III.

In this way, the voltage across C_A can be regulated by using the complementary switching states 2 and 3 for the same output voltage. Likewise, for an output voltage of $+V_{DC}/8$ the switching states 6 and 7 are used. In the negative half-cycle, for output voltages of $-V_{DC}/8$ and $-3V_{DC}/8$, switching states 10, 11 and 14, 15 can be used, respectively. The effect of complementary switching states on C_A for negative I_{L1} is exactly opposite to the positive "I_{L1}," as given in Table III. So, depending on the direction of I_{L1} and the instantaneous voltage across C_A, the complementary switching states are chosen appropriately as per Table IV.

The voltage across coupled inductor needs to be controlled by using complementary switching states. These complementary switching states apply exactly the same but opposite polarity voltage across the coupled inductor keeping the total terminal voltage fixed. The switching states 4 and 5 apply voltages $-4V_{DC}/8$ and $+4V_{DC}/8$ across the coupled inductor (output voltage is same for both the switching states). So, the switching state 4 or 5 can be used to decrease or increase I_{L1} by introducing negative or positive voltage across the coupled inductor. Therefore, to control I_{L1}, the switching states 4 and 5 are used, which generate the same output voltage of $+2V_{DC}/8$. Similarly, during the negative half-cycle, switching states 12 and 13 are used. During these complementary switching states, the voltages appeared across the coupled inductor as per Table V. But the voltage across input capacitors C_1, C_2 are automatically regulated at half the input dc source voltage (i.e., $V_{DC}/2$) because C_1, C_2 supply power to the load equally in the positive and negative half-cycles, respectively.

D. Evaluation of the Common-Mode Voltage

In recent years, the grid-connected transformerless inverters have become very popular due to their several advantages, e.g., high power density, higher efficiency, and lower cost. But they suffer from safety issues due to the galvanic connection between the photo voltaic (PV) source and the grid. In transformerless inverters, if the common mode voltage varies, the common mode leakage current flows through the parasitic capacitance between the PV source and the ground [25].

In case of single-phase H9LI, the situation is different. The common mode model of the H9LI is shown in Fig. 5. Here, C_{PV} is the parasitic capacitor between the PV source and ground, v_{cm} is the common mode voltage, and i_{cm} is the common mode leakage current. The expression of the common mode current is given as follows:

$$i_{cm} = C_{pv} \cdot \frac{dv_{cm}}{dt}. \tag{7}$$

From Fig. 5, it can be observed that the voltage across the parasitic capacitor is given by

$$v_{cm} = v_{C_2} \tag{8}$$

where v_{C_2} is the voltage across the capacitor C_2. From the modes of operation [see Fig. 4(a)–(h)] of H9LI, it can be observed that the voltage across C_2 is maintained constant (ripple voltage is ignored). Hence, in the ideal condition, the common mode leakage current i_{cm} is equal to zero similar to a half-bridge inverter. The simulated leakage current waveform of H9LI is shown in Fig. 6. The peak and RMS value of leakage current

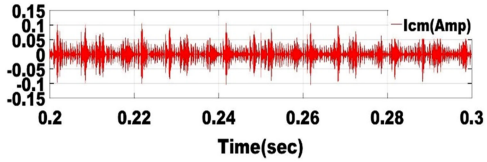


Fig. 6. Simulated leakage current waveform of the H9LI.

is observed to be 100 and 29 mA, respectively, which are well within the standard limits.

E. Design of the Coupled Inductor

To design the coupled inductor, it is very important to obtain relationship between the coupled inductor currents i_1, i_2 and output current i_A. The currents in the coupled inductor can be written as

$$i_1 = \frac{1}{2}(-i_A + i_{\text{ripple}}) \tag{9}$$

$$i_2 = \frac{1}{2}(-i_A + i_{\text{ripple}}). \tag{10}$$

The ripple current in the coupled inductor can be determined as

$$i_{\text{ripple}} = \frac{1}{2M}\int \mathrm{V}_{12}dt. \tag{11}$$

The coupled inductor can be designed by considering the worst case of ripple current, which is limited to ΔI. The output voltage is always equal to $\mathrm{V_{dc}}/2$ within one period. The largest ripple current in the coupled inductor can be calculated and the mutual inductance can be determined. The maximum ripple current in the coupled inductors can be written as [23]

$$i_{\text{ripple(max)}} = \Delta I = \frac{1}{2M}\int_0^{T_S} \frac{\mathrm{V_{DC}}}{2}dt = \frac{T_S \mathrm{V_{DC}}}{4M}. \tag{12}$$

According to (12), the inductances L_1 and L_2 must satisfy the following equation:

$$M \geq \frac{T_S \mathrm{V_{DC}}}{4i_{\text{ripple(max)}}}. \tag{13}$$

III. Pulsewidth Modulation (PWM) and Control Techniques of H9LI

The driver or the brain of the inverter is the control scheme. An intelligent control technique can make the inverter more reliable from protection and performance point of view. After the measurement of the actual current, the controller generates a reference voltage and provides gate pulses to the switches depending on the capacitor voltage and inductor current. The control strategy for producing a reference signal, PWM techniques and generating gate pulses for the proposed H9LI are explained as follows.

A. PWM Technique of H9LI

The PWM signals for all the switches of the proposed H9LI topology can be generated by comparing one modulation waveform $m(t)$ (reference signal: sine wave) and eight carrier waveforms $\mathrm{V}_i(t)$; where 'i' is a variable quantity, which varies from 1 to 8. These eight high-frequency carrier waves are level shifted waveforms. The modulation strategy of the H9LI is shown in Fig. 7. The peak value of the modulation waveform is $|m(t)|_{\max}$ and the modulation index m_a is defined as

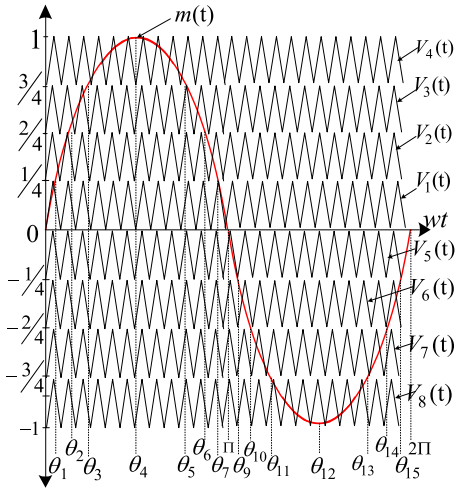


Fig. 7. PDPWM strategy of the proposed H9LI.

$$m_a = \frac{|m(t)|_{\max}}{4|\mathrm{V}_i(t)|_{\max}}. \tag{14}$$

The high-frequency PWM signals are generated for the switches S_1 to S_{10} depending on the location of $m(t)$. The generation of switching pulses for the switches S_1 to S_{10} is shown in Table VI.

The parameter values of angles are defined as follows:

$$\theta_0 = 0; \theta_4 = \pi/2; \theta_8 = \pi; \theta_{12} = 3\pi/2; \theta_{16} = 2\pi. \tag{15}$$

Some of the angles are calculated as

$$\theta_1 = \sin^{-1}\left(\frac{\mathrm{V}_i(t)_{\max}}{m(t)_{\max}}\right); \theta_2 = \sin^{-1}\left(\frac{2\mathrm{V}_i(t)_{\max}}{m(t)_{\max}}\right);$$
$$\theta_3 = \sin^{-1}\left(\frac{3\mathrm{V}_i(t)_{\max}}{m(t)_{\max}}\right) \tag{16}$$

$$\theta_5 = \pi - \theta_3; \quad \theta_6 = \pi - \theta_2; \quad \theta_7 = \pi - \theta_1; \quad \theta_9 = \pi + \theta_1;$$
$$\theta_{10} = \pi + \theta_2; \quad \theta_{11} = \pi + \theta_3; \quad \theta_{13} = 2\pi - \theta_3$$
$$\theta_{14} = 2\pi - \theta_2; \quad \theta_{15} = 2\pi - \theta_1 \tag{17}$$

The gate signals can be obtained according to Table II for the required output voltage level. For example, the complementary switching states 2 and 3 can be chosen to realize an output voltage of $+3\mathrm{V_{DC}}/8$ depending upon the direction of $\mathrm{I_{L1}}$ to control the voltage across $\mathrm{C_A}$. Similarly, complementary switching states 6 or 7, switching states 10 or 11, and switching states 14 or 15 are used to regulate the voltage across the $\mathrm{C_A}$.

TABLE VI
OUTPUT VOLTAGE ACCORDING TO SWITCHES STATES

	Item	Condition	Switching states	Output voltage V_{An}
Positive Half cycle	$0 < m(t) \le \theta_1$	$m(t) > V_1(t)$	6, 7	$0 \leftrightarrow \frac{V_{dc}}{8}$
		$m(t) < V_1(t)$	8	
	$\theta_1 < m(t) \le \theta_2$	$m(t) > V_2(t)$	4, 5	$\frac{V_{dc}}{8} \leftrightarrow \frac{2V_{dc}}{8}$
		$m(t) < V_2(t)$	6, 7	
	$\theta_2 < m(t) \le \theta_3$	$m(t) > V_3(t)$	2, 3	$\frac{2V_{dc}}{8} \leftrightarrow \frac{3V_{dc}}{8}$
		$m(t) < V_3(t)$	4, 5	
	$\theta_3 < m(t) \le \theta_4$	$m(t) > V_4(t)$	1	$\frac{3V_{dc}}{8} \leftrightarrow \frac{4V_{dc}}{8}$
	$\theta_4 < m(t) \le \theta_5$	$m(t) < V_4(t)$	2, 3	
	$\theta_5 < m(t) \le \theta_6$	$m(t) > V_3(t)$	2, 3	$\frac{2V_{dc}}{8} \leftrightarrow \frac{3V_{dc}}{8}$
		$m(t) < V_3(t)$	4, 5	
	$\theta_6 < m(t) \le \theta_7$	$m(t) > V_2(t)$	4, 5	$\frac{V_{dc}}{8} \leftrightarrow \frac{2V_{dc}}{8}$
		$m(t) < V_2(t)$	6, 7	
	$\theta_7 < m(t) \le \pi$	$m(t) > V_1(t)$	6, 7	$0 \leftrightarrow \frac{V_{dc}}{8}$
		$m(t) < V_1(t)$	8	
Negative Half cycle	$\pi < m(t) \le \theta_9$	$m(t) > V_5(t)$	10, 11	$0 \leftrightarrow -\frac{V_{dc}}{8}$
		$m(t) < V_5(t)$	9	
	$\theta_9 < m(t) \le \theta_{10}$	$m(t) > V_6(t)$	12, 13	$-\frac{V_{dc}}{8} \leftrightarrow -\frac{2V_{dc}}{8}$
		$m(t) < V_6(t)$	10, 11	
	$\theta_{10} < m(t) \le \theta_{11}$	$m(t) > V_7(t)$	14, 15	$-\frac{2V_{dc}}{8} \leftrightarrow -\frac{3V_{dc}}{8}$
		$m(t) < V_7(t)$	12, 13	
	$\theta_{11} < m(t) \le \theta_{12}$	$m(t) > V_8(t)$	16	$-\frac{3V_{dc}}{8} \leftrightarrow -\frac{4V_{dc}}{8}$
	$\theta_{12} < m(t) \le \theta_{13}$	$m(t) < V_8(t)$	14, 15	
	$\theta_{13} < m(t) \le \theta_{14}$	$m(t) > V_7(t)$	14, 15	$-\frac{2V_{dc}}{8} \leftrightarrow -\frac{3V_{dc}}{8}$
		$m(t) < V_7(t)$	12, 13	
	$\theta_{14} < m(t) \le \theta_{15}$	$m(t) > V_6(t)$	12, 13	$-\frac{V_{dc}}{8} \leftrightarrow -\frac{2V_{dc}}{8}$
		$m(t) < V_6(t)$	10, 11	
	$\theta_{15} < m(t) \le \theta_{16}$	$m(t) > V_5(t)$	10, 11	$0 \leftrightarrow -\frac{V_{dc}}{8}$
		$m(t) < V_5(t)$	9	

TABLE VII
COMPARISON OF THE PROPOSED H9LI WITH THE EXISTING NINE-LEVEL MLIS

Item	FC	NPC	CHB	MMC	FC-ANPC	H9LI
Input DC sources	1	1	4	1	1	1
Input DC Capacitors	8	8	4	0	2	2
Auxiliary Capacitors	7	0	0	16	3	1
Auxiliary Diodes	0	14	0	0	0	0
Power Switches	16	16	16	32	12	10
Coupled Inductor	0	0	0	0	0	1
Loss Distribution	Very good	Poor	Good	Good	Fair	Good
Power Switches Stress	$V_{DC}/8$	$V_{DC}/8$	$V_{DC}/4$	$V_{DC}/8$	$V_{DC}/2$	$V_{DC}/2$
Number of voltage sensors	8	8	4	16	3	1
Number of current sensors	0	0	0	0	0	0

B. Comparison of the Number of Power Switches of Proposed H9LI With the Existing MLIs

The proposed H9LI topology has a lower power switch count in comparison with the other existing nine-level MLIs, as given in Table VII. In the proposed topology, only ten power switches are used to control the output voltage. The H9LI comprises one auxiliary capacitor (rmC_{A}) and two input d capacitors ($\mathrm{C}_1, \mathrm{C}_2$). The use of fewer power devices increases the efficiency and reliability of the system. The extra component present in the H9LI is the coupled inductor. The presence of coupled inductor in the H9LI may increase the system size but the increment in system size is compensated by the reduction in the power switch count. The presence of magnetic component in the inverter will increase the reliability of the system compared to any other power device. Due to the flexibility of the switching states, H9LI provides good loss distribution among all power switches.

TABLE VIII
VOLTAGE STRESS ACROSS ALL POWER SWITCHES OF H9LI

Item	Voltage stress table										Total blocking voltage
Switch	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	$4V_{DC}$
Voltage stress	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{4}$	$\frac{V_{DC}}{4}$	$\frac{V_{DC}}{4}$	$\frac{V_{DC}}{4}$	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$	

TABLE IX
LOSS CALCULATIONS FOR ALL POWER SWITCHES OF H9LI FOR 10-KW AND 400-W SYSTEMS

	Item	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	
10kW system	Switching Losses	0	0	0	0	15W	15W	15W	15W	17W	17W	$\eta \approx 96.5$
	Conduction Losses	30W	30W	30W	30W	25W	25W	25W	25W	25W	25W	
400W system	Switching Losses	0	0	0	0	0.5W	0.5W	0.5W	0.5W	0.5W	0.5W	$\eta \approx 94.5$
	Conduction Losses	2W	2W	2W	2W	2W	2W	2W	2W	2W	2W	

From Table II, it can be observed that all high-frequency power switches (S_5 to S_{10}) have equal conduction periods in a full cycle (i.e., 50-Hz cycle). For example, the switch S_5 conducts during the voltage levels of $+\mathrm{V_{DC}}/8$ to $+3\mathrm{V_{DC}}/8$, $+2\mathrm{V_{DC}}/8$ to $+\mathrm{V_{DC}}/8, 0$ to $-\mathrm{V_{DC}}/8$ and $-2\mathrm{V_{DC}}/8$ to $-3\mathrm{V_{DC}}/8$. Effectively switch S_5 conducts for one half-cycle of grid frequency (i.e., 50-Hz cycle). Similarly, other high-frequency switches (S_6 to S_{10}) also conduct for one half-cycle of grid frequency. Thus, all high-frequency switches have equal conduction losses (switching losses are different). Similarly, the low-frequency power switches (S_1 to S_4) also have equal conduction losses (i.e., switching losses are neglected for low-frequency switches) among them. The theoretical calculations of loss distribution for the H9LI are given in Table IX for 10-kW and 400-W systems.

Furthermore, the proposed H9LI has been compared with one of the well-known topologies [13] (i.e., nine-level NPC) for the same kVA rating (with same input dc source ($\mathrm{V_{DC}}$) and load). It can be observed that the H9LI topology consists of ten power switches, two input dc capacitors, and one auxiliary capacitor, whereas an NPC has 16 power switches, four diodes, and eight input dc capacitors. The voltage stress across all power switches of H9LI is given in Table VIII. It can be observed from Table VIII that the total blocking voltage of switches is $4\mathrm{V_{DC}}$, whereas in the nine-level NPC, the total blocking voltage of devices is $10\mathrm{V_{DC}}$.

C. Current Control Strategy of H9LI

The main aim of the current control strategy is to feed power into the grid through the proposed H9LI. Fig. 8 shows the current control strategy of the proposed H9LI. The current control strategy works in two steps as follows.

1) *Generation of the modulating signal:* Actual current fed to the grid is measured and compared with a reference current to check the error. The obtained error is fed into

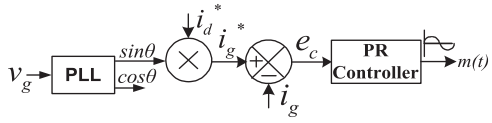


Fig. 8. Current control strategy for the H9LI [25].

a proportional resonant (PR) controller to produce the reference (modulation waveform) signal.

2) *Generation of the switching pulses:* Modulating signal ($m(t)$) is compared with the carrier waves to generate gate pulses for the switches (see Fig. 7). Complementary switches are switched with a specified dead band to avoid short circuit through the switches. In the case of complementary switching states, which are capable of performing voltage/current balancing activity, these complementary switching states are selected to balance the voltage across coupled inductor and regulate voltage across the auxiliary capacitor.

Some complementary switching states produce the same output voltage. One of the complementary switching states charges the auxiliary capacitor, whereas the other discharges with a unidirectional current. These switching states are selected on the basis of the voltage across the auxiliary capacitor and the current direction. Therefore, for selection of the switching states, the control techniques should have the information about the voltage level and current direction. In this paper, two new voltage balancing methods have been introduced along with the conventional direct current measurement method. All of these three methods measure auxiliary capacitor voltage directly from the circuit and the current direction is measured only in the conventional method. Unlike conventional voltage balancing techniques, these new methods do not measure the current directly. In the direct current measurement method, for a unidirectional current, which is measured directly from the circuit, is channelized through the auxiliary capacitor either from the positive terminal to negative terminal or from negative to positive terminal to charge or discharge the capacitor depending on the capacitor voltage.

1) First Method: In the first method, the current direction is assumed to be either of the two (positive or negative inductor current) and then the switching state is selected. If the change in the auxiliary capacitor voltage helps in maintaining the voltage within its specified band, then the current direction is kept same as earlier or else it is changed. As the technique depends on the change in capacitor voltage of the previous step, it might give wrong input to the controller in every transition of capacitor voltage and inductor current. The uncontrolled change in the capacitor voltage due to the wrong information can be controlled by adjusting the sampling rate. Feeding wrong information can also be prevented by adding some checkpoints in the control strategy.

2) Second Method: In the second method, the current direction is decided on the basis of the previous switching state and the change in the capacitor voltage. Let us say, switching state 2 was in ON condition during the last sampling period. During this period, capacitor voltage can be increased with positive directional current and it can be decreased with the negative directional current. So, by calculating the change in voltage, the current direction can be decided during the switching state without physically measuring the current from the circuit. This strategy may feed garbage information in every transition of the inductor current. As the frequency of the coupled inductor current is very less compared to that of the sampling frequency, the deviation in the capacitor voltage due to the wrong information during every transition will not hamper the performance of the inverter. The reference current $(i_g{}^*)$ is used to generate modulating signal in the next steps. In the next step, the reference current $(i_g{}^*)$ is calculated by multiplying $i_d{}^*$ with the phase-locked loop (PLL) output, where $i_d{}^*$ is the peak of the reference current corresponding to the power fed in to the grid. The comparison of reference current $(i_g{}^*)$ and actual grid current (i_g) gives error signal (e_c). The modulating signal $(m(t))$ is generated by passing (e_c) through a PR controller. The obtained modulating signal and the carrier waves are then used in the controller for using them in PWM technique. Depending on the auxiliary capacitor voltage and the I_{L1}, the switching states are chosen and the gate pulses are given to the switches as per the PWM output. The grid current is controlled through the PR controller [25]. PR controller is designed to achieve 0.1% maximum steady-state error at 50-Hz frequency. The designed PR controller $(T_{PR}(s))$ is given by

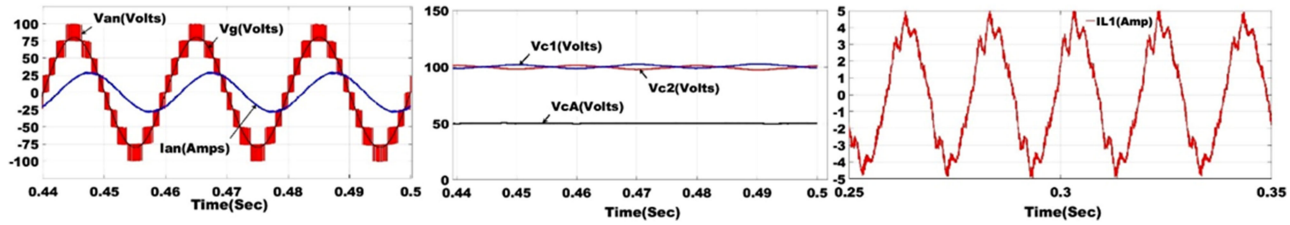
$$T_{PR}(s) = \frac{s^2 + 314.1s + 98596}{s^2 + 0.314s + 98596}. \tag{18}$$

IV. Simulation and Experimental Results

The proposed H9LI is validated through MATLAB simulation and experimental results. This section depicts the simulation steps, simulation results, implementation steps of the topology, and experimental results.

A. Simulation Results of H9LI

The simulations are carried out in MATLAB/Simulink environment for a 400-VA grid connected system. The simulation results are comparable with the theoretical expectations. The simulation generates a proper nine-level voltage at the output terminal of the inverter. The output voltage is fed into the grid through a filter to further reduce the harmonic content. Fig. 9(a) shows the waveforms of the nine-level output voltage at the inverter terminals, grid voltage, and current with closed-loop operation. Fig. 9(b) shows the waveforms of the voltages across input capacitors and auxiliary capacitor. It can be observed that the voltage across input capacitors and auxiliary capacitors are maintained at their desired values by using Method 3 (i.e., determination of the inductor current status from previous switching steps [see Fig. 11)]. Fig. 9(c) shows the waveform of the current through the coupled inductor (I_{L1}). The THD in grid current is observed to be 1.6%. The parameters used for system studies are listed in Table X.



(a) (b) (c)

Fig. 9. (a) H9LI output voltage (V_{an}), grid voltage (V_g), and current (I_{an} is scaled up by 2.5 times) waveforms. (b) Waveforms of voltages across input capacitors (V_{C1}, V_{C2}) and C_A. (c) Waveform of current through coupled inductor (I_{L1}).

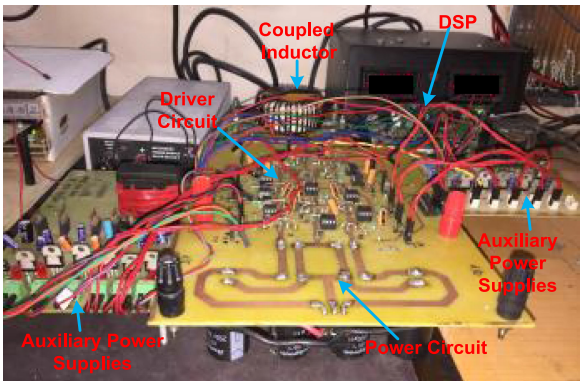


Fig. 10. Hardware setup for H9LI.

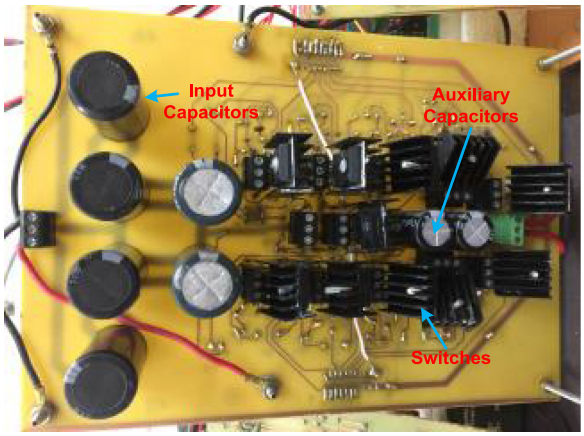


Fig. 11. Power circuit of the H9LI.

B. Experimental Results of H9LI

The laboratory prototype of the proposed H9LI has been built for the 400-VA system, as given in Table XI. The input voltage of the MLI is considered to be 200 V. The hardware setup is made on a printed circuit board (PCB), as shown in Figs. 10 and 11. A dc source is used for supplying the inverter and the output of the inverter is connected to an *R–L* load. There are total ten switches and the gate pulses are given from ten different driver circuits. All the drivers are provided with isolated auxiliary supplies and the corresponding gate pulses are generated by the DSP controller (TMS320F28069). Three 1000-μF capacitors are used in parallel to get a 3000-μF capacitor for input as well as an auxiliary capacitor. One coupled inductor of 4-mH mutual inductance is used in the circuit.

TABLE X
PARAMETERS USED IN THE SYSTEM STUDIES

1	Input DC supply:V_{DC}	200V
2	System power rating	400VA
3	Output inductor:L_f	2mH
4	%THD in current	1.6
5	Input DC capacitors: C_1,C_2	3300μF
6	Auxiliary capacitor: C_A	3300μF
7	Frequency of carrier waveform	3kHz
8	Mutual inductance (M)	4mH
9	Peak of grid voltage	80V

TABLE XI
DETAILS OF THE EXPERIMENTAL SETUP

1	Input DC supply:V_{DC}	200V
2	System power rating	400VA
3	Output inductor:L_f	2mH
4	%THD in current	1.9
5	Input DC capacitors: C_1,C_2	3300μF
6	Auxiliary capacitor: C_A	3300μF
7	Frequency of carrier waveform	3kHz
8	Mutual inductance (M)	4mH
9	Peak of grid voltage	80V

C. Implementation of the Grid Current Control Strategy

The working principle of the current control strategy is described in the following steps.

1) Amplitude and Phase Detection of Modulating Wave: A dc current is calculated to represent the real power to be fed. This dc current is converted into ac reference current. This ac reference current is compared with the actual current to generate error signal. Then, the modulating signal is generated by passing the error value into the PR controller. This obtained modulating signal is used as the reference signal for the controller.

2) Generation of the Switching Pulses: The reference modulating wave is compared with the carriers to decide the output voltage level of the inverter. Depending on the requirement of the inverter output, voltage gate pulses are given to the switches. There are complementary switching states which are used to charge or discharge the auxiliary capacitor for generating the same output voltage. These complementary switching states are chosen for balancing the voltage across the auxiliary capacitor.

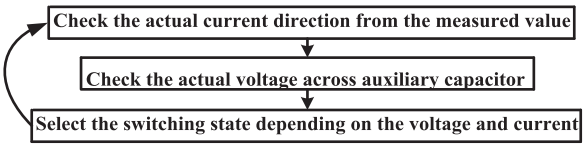


Fig. 12. Auxiliary capacitor voltage balancing through direct current measurement.

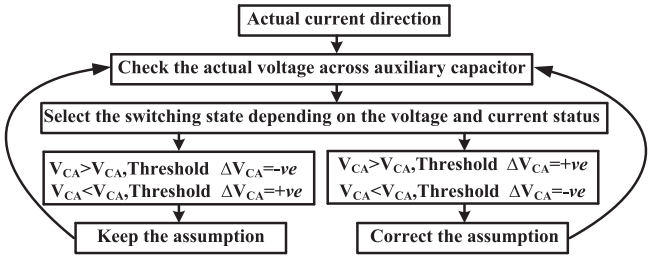


Fig. 13. Auxiliary capacitor voltage balancing through current assumption technique (ΔV_{C_A} = change in the voltage across C_A).

3) Methods to Regulate the Voltage Across Auxiliary Capacitor: It is mandatory to maintain the voltage across the auxiliary capacitor to produce a balanced output voltage in positive and negative half-cycles and also to produce uniform steps in the output voltage. The complementary switching states charge or discharge the auxiliary capacitor depending on the direction of the current through the capacitor. For the selection of the switching states, the current direction and voltage across the capacitor should be known. In the hardware setup, the voltage across the auxiliary capacitor is directly measured and given to the DSP. For finding the current direction, the following three different methods are used.

1) *Direct measurement of the current:* In the direct measurement technique, the current is directly measured at the input terminal of the coupled inductor to check the direction of the current. Depending on the direction of I_{L1} and voltage across C_A, switching states are selected to charge the auxiliary capacitor when the voltage is less than the threshold voltage and discharge the capacitor when the capacitor voltage is more than the threshold voltage. The switching state selection procedure is described in the flowchart. Fig. 12 shows the flowchart of the direct measurement technique.
2) *Current assumption technique:* In this technique (see Fig. 13), the current is not measured directly from the circuit. At first, the current direction is assumed and then it follows the same steps as in the case of direct measurement technique. During the next sampling, the capacitor voltage and the change in capacitor voltage are checked. If the change in the voltage is in the desired direction (decrease in the auxiliary capacitor voltage when the voltage is higher than the threshold value or increase in the voltage when the capacitor voltage is lesser than the threshold voltage), the current direction is kept as it was in earlier sampling. If the change in the capacitor voltage is against the desired direction (increase in the auxiliary capacitor voltage even when the voltage is higher than the threshold value or decrease in the voltage even when the capacitor voltage is lesser than the threshold voltage), the current direction is changed from the earlier one. The technique is described in Fig. 13 with the help of a flowchart.
3) *Determination of the inductor current status from previous switching steps:* Similar to the previous technique, the current is not measured directly in this technique too. In this technique, the current status is decided on the basis of previous switching state and the change in capacitor voltage, as given in Fig. 14. Similar to the previous technique, the current is assumed in any of the direction. The switching state is selected as per the actual capacitor voltage and the assumed current direction. In the next sampling period, change in the capacitor voltage and the earlier switching state is checked. Depending on this information, the current direction in the earlier switching state is calculated, as shown in Table XII, and same current direction is used for the next switching state selection.

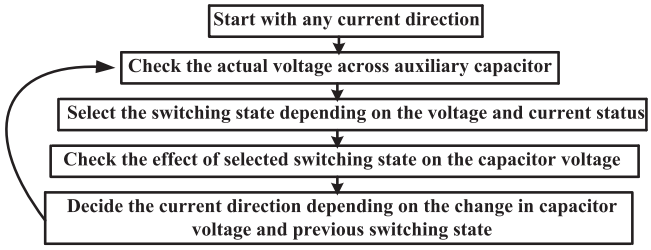


Fig. 14. Balancing of the voltage across C_A through current information from previous switching steps.

TABLE XII
CURRENT DIRECTION DEPENDING ON THE SWITCHING STATE AND CHANGE IN VOLTAGE

Switching state	Change in Auxiliary capacitor voltage, ΔV_{CA}	Inductor current, I_{L1}
2	*+ve*	>0
2	*-ve*	<0
3	*+ve*	<0
3	*-ve*	>0

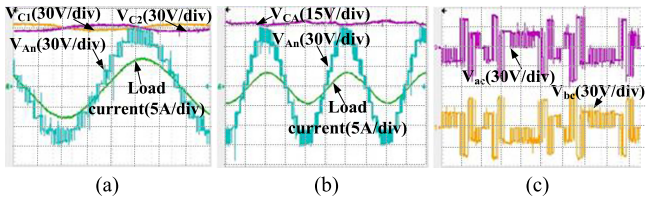


Fig. 15. Experimental waveforms of H9LI for an *R–L* load. (a) Output voltage, voltage across input capacitors (V_{C1}, V_{C2}), and the output current. (b) Voltage across the auxiliary capacitor (V_{CA}). (c) Voltage across the coupled inductor (V_{ac}, V_{bc}).

Fig. 15(a) depicts the waveforms of the nine-level output voltage and current of the inverter for an *R–L* load. There is no requirement of balancing the voltage across input dc capacitors by any external means or through any external controller. The voltage across the input capacitors is varied according to the direction of the current through the capacitor. The voltage across

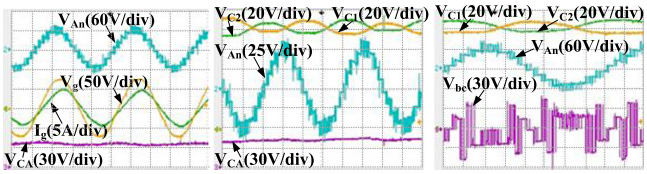


Fig. 16. (a) Experimental waveforms of the inverter output voltage (V_{An}), voltage across the auxiliary capacitor (V_{CA}), grid voltage (V_g), and the currents (I_g). (b) Waveforms of the voltage across the input capacitors (V_{C1}, V_{C2}). (c) Waveform of the voltage across the coupled inductor (V_{bc}).

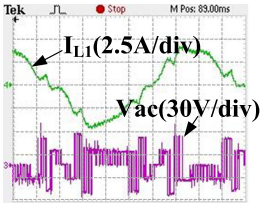


Fig. 17. Experimental waveform of the current through coupled inductor.

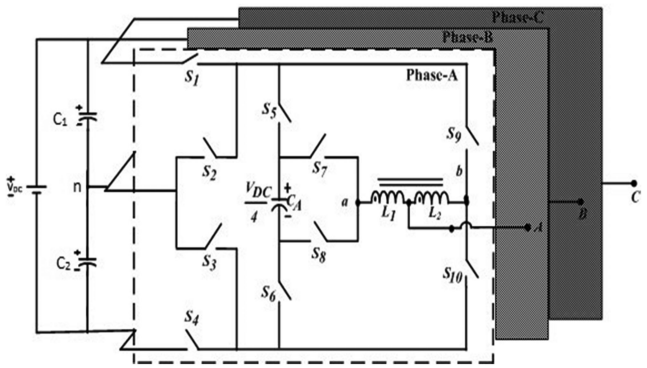


Fig. 18. 3-ϕ version of the proposed H9LI.

input capacitors have 100-Hz, ripple as shown in Fig. 15(a). The voltage across the auxiliary capacitor is maintained within the specified band as defined in the DSP controller. The variation in the voltage across C_A is shown in Fig. 15(b). The voltages (V_{ac}, V_{bc}) across the coupled inductor are shown in Fig. 15(c).

The H9LI topology is connected to the single-phase grid for the power rating of 400 VA for nonunity power factor ($\phi = 18^0$). Fig. 16(a) shows the waveforms of the nine-level output voltage (V_{An}) of H9LI, grid voltage, and current waveforms. The THD in the grid current is observed to be 1.9% which is well matching with the simulation results. The waveforms of the voltage across input capacitors are shown in Fig. 16(b). The waveform of the voltage across the coupled inductor (V_{bc}) is shown in Fig. 16(c). The waveform of the current through the coupled inductor is shown in Fig. 17.

V. Conclusion

This paper has presented a new H9LI topology for 1-ϕ grid-connected applications. A coupled inductor has been used in the H9LI to increase the number of levels in the output voltage. This also improves the lifespan of the system by obviating the need for low lifespan power components, such as the dc capacitors. It can feed high-quality power into the grid with a current THD of only 1.9%. The H9LI has a lower part count in comparison to the other nine-level inverters, due to which it has low cost, higher reliability, and higher efficiency($\eta \approx 94.5\%$). The H9LI has a good loss distribution amongst its various switches due to the availability of redundant switching states. The topology facilitates self-balancing of the auxiliary capacitor voltage. The presence of magnetic component (which reduces the number of switches and capacitors) in the inverter increases the reliability of the system.

Besides the new topology, an attractive control scheme was introduced and tested. The scheme is implemented in two steps. The first step is to generate the reference voltage waveform for the inverter. Second step, i.e., selection of switching states uses two new control techniques other than the conventional one (i.e., direct measurement of current method). Switching selection is part of the control scheme where self-balancing of the auxiliary capacitor voltage takes place. For regulating the auxiliary capacitor voltage, conventional inverters use direct current measurement sensing methods. This paper has introduced two different voltage balancing techniques that do not use direct current measurements. These techniques reduce the dependability of the sensing mechanism and improve the reliability of the control scheme. Also, the reduced number of hardware parts decreases the cost of the control circuit and its maintenance requirements. The proposed control techniques can be adopted for any topology where auxiliary capacitor voltage control (maintaining at the specified value) is required.

Furthermore, there is a possibility to extend the proposed 1-ϕ H9LI to the 3-ϕ application, as shown in Fig. 18. The main advantage of 3-ϕ H9LI is that the three legs share a common input dc source (V_{DC}). Each leg produces nine levels in the output voltage (V_{An}) and the line to line voltages (V_{AB}, V_{BC}, and V_{CA}) produce 17 voltage levels. The results corresponding to the 3-ϕ version of H9LI will be presented in a future paper.

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