A Generalized Associated Discrete Circuit Model of Power Converters in Real-Time Simulation

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***Abstract*—Power converters in the system-level real-time simulation are usually emulated by L/C-based associated discrete circuit (L/C-ADC). However, the L/C-ADC approaches may suffer from two issues: How to mitigate the unacceptable virtual power loss especially in high-frequency applications, and how to tune LC parameters setting which is affected by the external circuit. This paper proposes a novel generalized associated discrete circuit (G-ADC) model with parameterized history current sources. By utilizing the stability region of the feasible parameter space, the optimized G-ADC models with the best damping characteristic are developed for both two-level and three-level converters. The analytical results also guarantee that the parameters of the optimized G-ADC model are independent of the external circuit for most power grid applications. Furthermore, an field programmable gate array (FPGA)-based real-time simulation platform is built to verify the feasibility of the proposed scheme. Extensive simulation and hardware-in-loop experiment results demonstrate the effectiveness and superiority of best-damped models as well as the modeling flexibility corresponding to insensitivity to operating conditions and external system parameters.**

***Index Terms*—Associated discrete circuit (ADC), FPGA, power converter model, real-time simulation.**

I. Introduction

In THE past decades, there is a dramatic increase in installation of renewable energy plants, distributed generators, VSC-HVDC, and FACTS devices in the power grid [1]. Most researches on these power electronic devices rely on the accurate and efficient modeling and simulation [2]. Especially in hardware-in-the-loop (HIL) applications, real-time simulations are required, which are used for designing, testing, and analyzing power system devices [3], including electrical machines, power transformers, and power electronic devices [4]–[7]. However, the discrete characteristic and high-frequency characteris-

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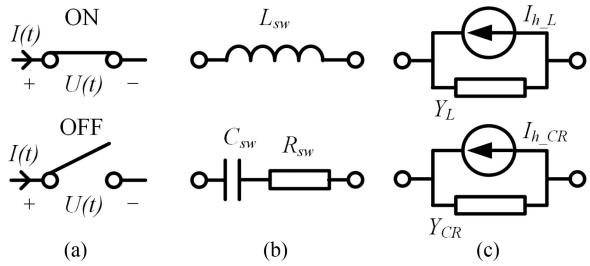

Fig. 1. Basic idea of the L/C-ADC model.

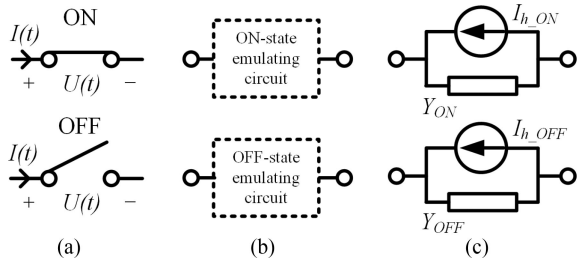

Fig. 2. Basic idea of the G-ADC model.

dimensional parameter space than L/C-ADC model. We show that the "best-damping" characteristic of the optimized G-ADC model cannot be achieved by only tuning the circuit parameters of L/C-ADC model.

2) The effective analysis method and parameter setting approach of G-ADC model are developed to overcome the "parameter tuning" obstacle of the L/C-ADC model. The feasible parameter space of G-ADC model is only related to the particular converter topology under several reasonable assumptions. In other words, the G-ADC model can be decoupled from external circuits. Thus, the best-damped points of G-ADC model are universal for a particular topology, such as two-level converters or three-level converters.
3) G-ADC model has more strict mathematical foundations than L/C-ADC model. L/C-ADC is a heuristic approach to emulate switches with the charging or discharging RLC circuits. However, G-ADC is an analytical method which fits the ideal response of switches with the parameterized discrete system. By analyzing the corresponding discrete system, a variety of numerical stability information including stability boundary and damping index of the switching emulation models can be provided. Therefore, it is easy to show that, in theory, the almost ideal performance of the optimized G-ADC model can be guaranteed.

The simulation results also show that the proposed G-ADC model is capable of improving the accuracy of the switching emulation for power electronics converters using high switching frequency without losing the strengths of fixed equivalent admittance and flexibility of ADC technique.

II. Generalization of the ADC Switch Model

A. L/C-ADC Model

The basic idea of L/C-ADC model is representing the switch as a small inductor when it is ON and representing as a small capacitor with a series resistor when it is OFF, as shown in Fig. 1(a) and (b). In the widely-used Electromagnetic Transient Program (EMTP) algorithm proposed by Dommel [24], the branch components are discretized into an equivalent admittance associated with a history current source. The L/C-ADC model can also be described by this discrete form, as shown in Fig. 1(c).

The equivalent admittances of inductor branch and capacitor/resistor branch are set to be the same by adjusting the inductance L_{sw}, capacitance C_{sw}, and resistance R_{sw}. For example, if the L/C-ADC model is discretized by backward Euler (BE) method, these three parameters should satisfy

$$Y_{sw} = Y_L = \frac{\Delta t}{L_{sw}} = Y_{\mathrm{CR}} = \frac{C_{sw}}{C_{sw}R_{sw} + \Delta t} \tag{1}$$

while the history current expressions of inductor branch and capacitor/resistor branch are as follows:

$$\begin{cases} I_{h\_L}(t) = -I(t - \Delta t) \\ I_{h\_\mathrm{CR}}(t) = Y_{sw}U(t - \Delta t) - R_{sw}Y_{sw}I(t - \Delta t). \end{cases} \tag{2}$$

When the switch state changes, only the history current expression changes while the equivalent admittance remains fixed. Therefore, the admittance matrix of the simulated system can be prestored and there is no need to reform the admittance matrix whenever the switch state changes during the simulation. As the reformation and inversion of matrix raise the cost such as computational time or/and hardware resources, this fixed-equivalent-admittance model can remarkably improve the computational efficiency. However, because L/C-ADC model introduces the virtual dynamics of the charging and discharging behavior of the LC circuits, L/C-ADC model suffers from the nonuniversality of parameter settings, and the virtual power loss problem in high-frequency applications.

B. G-ADC Model

Inspired by the L/C-ADC model, we first come up with a more general idea of the ADC model, i.e., representing the switch with an ON-state emulating circuit when it is ON and representing with an OFF-state emulating circuit when it is OFF, as shown in Fig. 2(a) and (b).

The ON-state emulating circuit and the OFF-state emulating circuit can be any circuit as long as they satisfy these two following requirements:

1) The equivalent admittances of these two circuits should have the same value to make sure there is no need to reform the admittance matrix after switching actions.
2) The steady-state characteristics and transient-state characteristics of these circuits should be close to those of the ideal switches.

No matter what these ON-state emulating circuit and OFF-state emulating circuit are, their corresponding discrete circuits have the identical form, as shown in Fig. 2(c). Therefore, it is more general to define the G-ADC model by an equivalent admittance Y_{ON} associated with a history current source I_{h_ON} at ON state and Y_{OFF} associated with I_{h_OFF} at OFF state, respectively. For

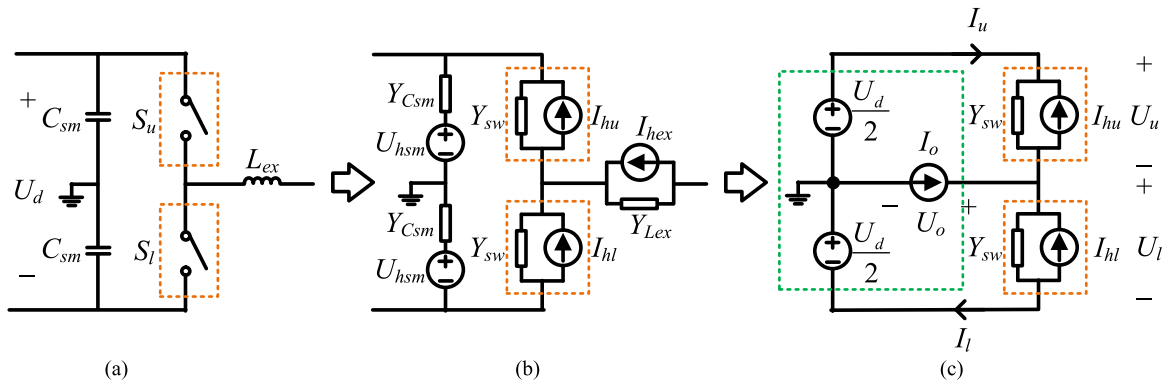

Fig. 3. Basic half-bridge circuit. (a) Analog form. (b) Discrete form. (c) Equivalent form.

the sake of generality, the history current expressions of this generalized model are formulated by

$$\begin{cases} I_{h\_\mathrm{on}}(t) = \alpha_{\mathrm{on}} U(t-\Delta t) + \beta_{\mathrm{on}} I(t-\Delta t) \\ I_{h\_\mathrm{off}}(t) = \alpha_{\mathrm{off}} U(t-\Delta t) + \beta_{\mathrm{off}} I(t-\Delta t). \end{cases} \tag{3}$$

Different with the L/C-ADC model whose parameters to be set are the RLC values of the analog circuits, it is the discrete circuit parameters of G-ADC model, i.e., the equivalent admittances $Y_{\mathrm{ON}}, Y_{\mathrm{OFF}}$, the history current coefficients, $\alpha_{\mathrm{off}}, \beta_{\mathrm{off}}, \alpha_{\mathrm{on}}, \beta_{\mathrm{on}}$, which are to be set by the users.

So the first requirement of ON-state emulating circuit and OFF-state emulating circuit, is easy to be satisfied by directly setting their equivalent admittances Y_{ON} and Y_{OFF} equal to the same value Y_{sw}.

As for the second requirement, the steady-state characteristics and transient-state characteristics are both determined by the history current expressions. How to constrain the history current coefficients to make sure the G-ADC model can well emulate the ideal switch will be discussed in the following sections.

III. Feasible Parameter Space of G-ADC Model for Two-Level Converters

The proposed G-ADC model in the last section is a parameterized switch model with five parameters undetermined, including the equivalent admittance of switch, Y_{sw}, and the coefficients of history current expressions, $\alpha_{\mathrm{off}}, \beta_{\mathrm{off}}, \alpha_{\mathrm{on}}, \beta_{\mathrm{on}}$. In this section, the impacts of these parameters on the steady-state and transient-state characteristics of the switch are analyzed and the feasible parameter space is explored and discussed when the G-ADC model is applied to two-level converters. In this feasible parameter space, the best-damped models with the fastest damping speed of transient errors are proposed.

A. Assumptions

The characteristic analysis of G-ADC model for two-level converters is based on the following assumptions:

1) The two-level converter can be decomposed into the half-bridge circuit in Fig. 3(a) and the switches to be modeled work in the opposite ON/OFF states.
2) The filter inductor can be seen as an independent current source, and the smoothing capacitor can be seen as an independent voltage source.

The first assumption is satisfied for both half-bridge and full-bridge converters, which are the basic topologies of two-level converters. The second assumption is also easy to be satisfied when the dynamics of filter inductor and capacitor are much slower than the switching actions, which will be further elaborated in the Appendix. With these assumptions, the switching dynamics of two-level converters can be analyzed with the basic circuit unit in Fig. 3(c), which is independent of the external circuit.

B. Steady-State Characteristic Constraints

In most cases, the ideal switch model is accurate enough for the system-level simulation. To emulate the ideal switch, the G-ADC model is supposed to have the steady-state characteristics as follows:

1) When the switch state is ON, no matter what the branch current is, there is no branch voltage over this switch.
2) When the switch state is OFF, no matter what the branch voltage is, there is no branch current through this switch.

To determine the parameters of G-ADC model, we need to find the constraints of history current coefficients equivalent to these descriptions above. Take the upper switch S_u in Fig. 3(a) for example, its branch current at ON state is

$$\begin{aligned} I_u(t) &= Y_{sw} U_u(t) - I_{h\_\mathrm{ON}}(t) \\ &= Y_{sw} U_u(t) - \alpha_{\mathrm{on}} U_u(t-\Delta t) - \beta_{\mathrm{on}} I_u(t-\Delta t). \end{aligned} \tag{4}$$

Its branch current at OFF state is

$$\begin{aligned} I_u(t) &= Y_{sw} U_u(t) - I_{h\_\mathrm{OFF}}(t) \\ &= Y_{sw} U_u(t) - \alpha_{\mathrm{off}} U_u(t-\Delta t) - \beta_{\mathrm{off}} I_u(t-\Delta t). \end{aligned} \tag{5}$$

When the upper switch is ON and reaches a steady state, its voltage and current should satisfy

$$\begin{cases} U_u(t) = U_u(t-\Delta t) = 0 \\ I_u(t) = I_u(t-\Delta t). \end{cases} \tag{6}$$

When the upper switch is OFF and reaches a steady state, its voltage and current should satisfy

$$\begin{cases} U_u(t) = U_u(t-\Delta t) \\ I_u(t) = I_u(t-\Delta t) = 0. \end{cases} \tag{7}$$

By substituting (6) into (4) and substituting (7) into (5), we can conclude that only if the following equations are satisfied, the G-ADC model can have the ideal steady-state characteristics:

$$\begin{cases} \alpha_{\text{off}} = Y_{sw} \\ \beta_{\text{on}} = -1. \end{cases} \tag{8}$$

C. Transient-State Characteristic Constraints

There are two working modes of the half-bridge circuit in Fig. 3(a), i.e., S_u is OFF while S_l is ON and S_u is ON while S_l OFF. After a mode change, the simulated half-bridge in Fig. 3(c) can be regarded as a discrete time system with the nonzero initial state. To better emulate the transient processes of the ideal switch, the zero-input responses of the discrete system should converge to the steady-state values as soon as possible.

As the half-bridge circuit is a symmetrical topology, the zero-input responses of both mode changes turn out to have the symmetrical expressions. Hence, only the zero-input responses of the former mode (S_u is OFF while S_l is ON) is derived below.

First, we can list the KCL equations of Fig. 3(c) in the complex frequency domain

$$\begin{cases} 0 = I_u(z) + I_{hu}(z) - Y_{sw}U_u(z) \\ 0 = I_l(z) + I_{hl}(z) - Y_{sw}U_l(z) \\ 0 = I_u(z) - I_l(z) - I_o. \end{cases} \tag{9}$$

With α_{off} and β_{on} determined by (8), the history currents of the upper and lower switches can be expressed by

$$\begin{cases} I_{hu}(z) = z^{-1}\left(Y_{sw}U_u(z) + \beta_{\text{off}}I_u(z)\right) \\ I_{hl}(z) = z^{-1}\left(\alpha_{\text{on}}U_l(z) - I_l(z)\right) \end{cases} \tag{10}$$

where

$$\begin{cases} U_u(z) = \frac{1}{2}U_d - U_o(z) \\ U_l(z) = \frac{1}{2}U_d + U_o(z). \end{cases} \tag{11}$$

Substituting (10) and (11) into (9), we can obtain three equations with $I_u(z)$, $I_l(z)$, and $U_o(z)$ unknown. Solving these equations, we can acquire;

1) the zero-input response of I_u, I_l, and U_o in the complex frequency domain (12) shown at the bottom of this page, and
2) the characteristic equation of the discrete system (13)

$$P(z) = Y_{sw}(z-1)^2 + (z+\beta_{\text{off}})(Y_{sw}z - \alpha_{\text{on}}). \tag{13}$$

According to the Jury Stability Criterion [25], the second−order discrete system is stable if the conditions $P(1) > 0$, $P(-1) > 0$ and $|a_2| < a_0$ are all satisfied, where a_2 and a_0 are the coefficients of z^0 and z^2 in (13), respectively. Therefore, we can make sure the half-bridge modeled by G-ADC is stable, if and only if α_{on} and β_{off} satisfy the following constraints:

$$\begin{cases} \left(\frac{\alpha_{\text{on}}}{Y_{sw}} + 1\right)(\beta_{\text{off}} - 1) < 4 \\ \frac{\alpha_{\text{on}}}{Y_{sw}}\beta_{\text{off}} > -1 \\ \frac{\alpha_{\text{on}}}{Y_{sw}} < 1 \\ \beta_{\text{off}} > -1. \end{cases} \tag{14}$$

The constraints (14) and (8) are utilized together to describe the feasible parameter space of G-ADC model for two-level converters.

D. Best-Damped G-ADC Models in Feasible Parameter Space

Typically, for a stable discrete time system, the speed of response of the system is captured by the modulus of the largest eigenvalue. All the moduli are much closer to zero, in other word, the discrete system is much more stable. Therefore, to quantify the stability margin and the damping degree, we define an index of the max modulus of poles, $MMoP$ as

$$MMoP = \max\left(|p_1|, |p_2|\right) \tag{15}$$

where the poles p_1 and p_2, can be obtained according to (13) as shown in (16) at the bottom of this page.

With this index, how the coefficients α_{on} and β_{off} significantly impact on the stability and damping can be shown intuitively by Fig. 4. The *z*-axis represents the $MMoP$, the *x*-axis represents $\alpha_{\text{on}}/Y_{sw}$, and the *y*-axis represents β_{off}. The black bold line is the stability boundary of G-ADC model for two-level converters. Within the feasible parameter space described by (14), there are two lowest parameter points shown in Fig. 4 where $MMoP$ is

$$\begin{cases} I_u(z) = \frac{Y_{sw}U_d(Y_{sw}z-\alpha_{\text{on}})(z-1) - Y_{sw}I_o(z-1)^2}{Y_{sw}(z-1)^2 + (z+\beta_{\text{off}})(Y_{sw}z-\alpha_{\text{on}})} \\ I_l(z) = \frac{Y_{sw}U_d(Y_{sw}z-\alpha_{\text{on}})(z-1) + I_0(z+\beta_{\text{off}})(Y_{sw}z-\alpha_{\text{on}})}{Y_{sw}(z-1)^2 + (z+\beta_{\text{off}})(Y_{sw}z-\alpha_{\text{on}})} \\ U_o(z) = \frac{2I_o(z-1)(z+\beta_{\text{off}}) + U_dY_{sw}(-\beta_{\text{off}}z - 2z + 1) + U_d\alpha_{\text{on}}(z+\beta_{\text{off}})}{Y_{sw}(z-1)^2 + (z+\beta_{\text{off}})(Y_{sw}z-\alpha_{\text{on}})} \end{cases} \tag{12}$$

$$\begin{cases} p_1 = \frac{1}{4}\frac{-Y_{sw}\beta_{\text{off}} + 2Y_{sw} + \alpha_{\text{on}} + \sqrt{Y_{sw}^2\beta_{\text{off}}^2 - 4Y_{sw}^2\beta_{\text{off}} + 6Y_{sw}\alpha_{\text{on}}\beta_{\text{off}} - 4Y_{sw}^2 + 4Y_{sw}\alpha_{\text{on}} + \alpha_{\text{on}}^2}}{Y_{sw}} \\ p_2 = \frac{1}{4}\frac{-Y_{sw}\beta_{\text{off}} + 2Y_{sw} + \alpha_{\text{on}} - \sqrt{Y_{sw}^2\beta_{\text{off}}^2 - 4Y_{sw}^2\beta_{\text{off}} + 6Y_{sw}\alpha_{\text{on}}\beta_{\text{off}} - 4Y_{sw}^2 + 4Y_{sw}\alpha_{\text{on}} + \alpha_{\text{on}}^2}}{Y_{sw}} \end{cases} \tag{16}$$

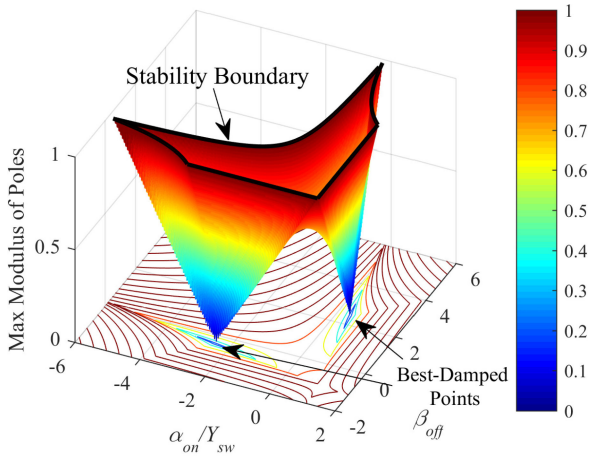

Fig. 4. Max modulus of poles ($MMoP$) with different $\alpha_{\rm on}/Y_{sw}$ and $\beta_{\rm off}$.

equal to zero. That means, all the poles are zero, and the zero-input responses of these two models converge to the steady-state values with the fastest speed. In this paper, we called these two models the best-damped G-ADC models.

The history current expressions of these best-damped G-ADC models, termed as Types I and II, respectively, are as follows:

History current expressions of Type I

$$\begin{cases} I_{h\_\rm on}\left(t\right) = \left(-1-\sqrt{2}\right) Y_{sw} U\left(t-\Delta t\right) - I\left(t-\Delta t\right) \\ I_{h\_\rm off}\left(t\right) = Y_{sw} U\left(t-\Delta t\right) + \left(1-\sqrt{2}\right) I\left(t-\Delta t\right). \end{cases} \tag{17}$$

History current expressions of Type II

$$\begin{cases} I_{h\_\rm on}\left(t\right) = \left(-1+\sqrt{2}\right) Y_{sw} U\left(t-\Delta t\right) - I\left(t-\Delta t\right) \\ I_{h\_\rm off}\left(t\right) = Y_{sw} U\left(t-\Delta t\right) + \left(1+\sqrt{2}\right) I\left(t-\Delta t\right). \end{cases} \tag{18}$$

Due to the best-damped characteristic, the transient process time of switching actions is shortened thus the virtual power loss can be remarkably reduced.

Comparing with the L/C-ADC model, another merit of these best-damped G-ADC models is that all the derivations are independent of the operating conditions and external circuit parameters if the previous two assumptions are satisfied. Hence, the best-damped G-ADC models are theoretically insensitive to the external system.

IV. Feasible Parameter Space of G-ADC Model for Three-Level Converters

In this section, the feasible parameter space and the best-damped model of G-ADC model for three-level converters are discussed.

A. Assumptions

The characteristic analysis of G-ADC model for three-level converters is based on the following assumptions:

1) The three-level converter can be equivalent to the surrogate circuit shown in Fig. 5(b).
2) The second assumption is same with that of the two-level converter.

The surrogate circuit is able to supply three different output voltages ($\frac{U_d}{2}$, 0, and $-\frac{U_d}{2}$). Therefore, it is used to replace the three-level neutral point clamped (NPC) converter in real-time simulation [28]. With these assumptions, the switch dynamics of three-level NPC converters can be analyzed with the basic circuit unit shown in Fig. 5(c), which is also independent from the external circuit.

B. Steady-State Characteristic Constraints

The steady-state characteristic constraints are independent of the converter topology. Therefore, $\alpha_{\rm off}$ and $\beta_{\rm on}$ of G-ADC model for three-level converters adopt the same values with those for two-level converters.

C. Transient-State Characteristic Constraints

The zero-input responses of all the modes in Table I are derived in the similar way of Section III-C. The zero-input responses of all the mode changes share the same characteristic equation

$$\begin{aligned} \Delta = \big(&Y_{sw}\beta_{\rm off} z + 3Y_{sw} z^2 - 4Y_{sw} z \\ &- \alpha_{\rm on}\beta_{\rm off} - \alpha_{\rm on} z + 2Y_{sw}\big)\left(\beta_{\rm off} + z\right). \end{aligned} \tag{19}$$

According to the Jury Stability Criterion of the third−order discrete system, we can make sure the surrogate circuit modeled by G-ADC is stable, if and only if $\alpha_{\rm on}$ and $\beta_{\rm off}$ satisfy the following constraints:

$$\begin{cases} \left(\frac{\alpha_{\rm on}}{Y_{sw}} + 1\right)\left(\beta_{\rm off} - 1\right) < 8 \\ \frac{\alpha_{\rm on}}{Y_{sw}}\beta_{\rm off} > -1 \\ \frac{\alpha_{\rm on}}{Y_{sw}} < 1 \\ 1 > \beta_{\rm off} > -1. \end{cases} \tag{20}$$

The constraints (20) and (8) are utilized together to describe the feasible parameter space of G-ADC model for three-level NPC converters.

$$\begin{cases} p_1 = \frac{1}{6}\frac{-Y_{sw}\beta_{\rm off} + 4Y_{sw} + \alpha_{\rm on} + \sqrt{Y_{sw}^2\beta_{\rm off}^2 - 8Y_{sw}^2\beta_{\rm off} + 10Y_{sw}\alpha_{\rm on}\beta_{\rm off} - 8Y_{sw}^2 + 8Y_{sw}\alpha_{\rm on} + \alpha_{\rm on}^2}}{Y_{sw}} \\ p_2 = \frac{1}{6}\frac{-Y_{sw}\beta_{\rm off} + 4Y_{sw} + \alpha_{\rm on} - \sqrt{Y_{sw}^2\beta_{\rm off}^2 - 8Y_{sw}^2\beta_{\rm off} + 10Y_{sw}\alpha_{\rm on}\beta_{\rm off} - 8Y_{sw}^2 + 8Y_{sw}\alpha_{\rm on} + \alpha_{\rm on}^2}}{Y_{sw}} \\ p_3 = -\beta_{\rm off} \end{cases} \tag{21}$$

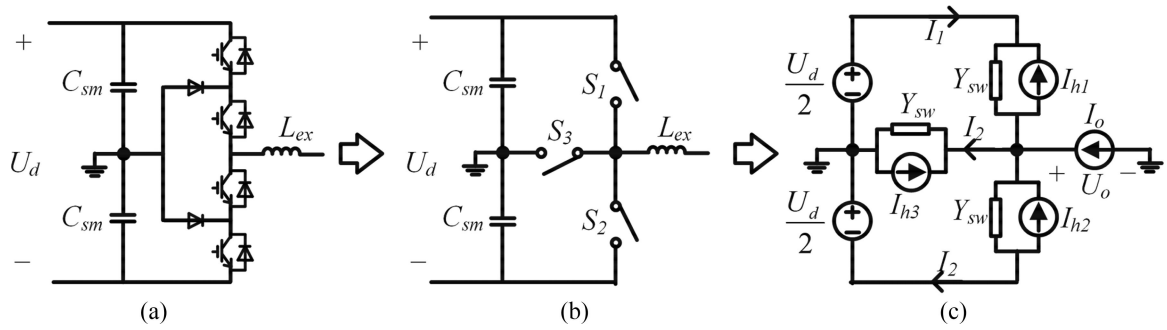

Fig. 5. Typical NPC converter. (a) Original circuit. (b) Surrogate circuit. (c) Equivalent circuit.

TABLE I
COMBINATION STATES OF EQUIVALENT TOPOLOGY OF THREE-LEVEL CONVERTERS

	Mode 1	Mode 2	Mode 3
Switch S_1	OFF	OFF	ON
Switch S_2	ON	OFF	OFF
Switch S_3	OFF	ON	OFF
Output voltage U_o	$-\frac{U_d}{2}$	0	$\frac{U_d}{2}$

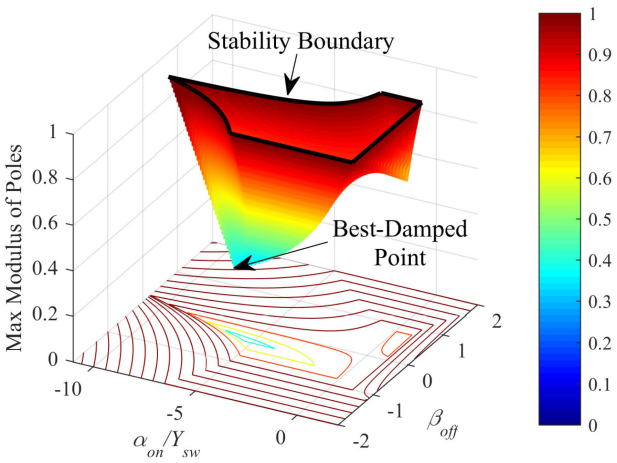

Fig. 6. Max modulus of poles ($MMoP$) with different $\alpha_{\text{on}}/Y_{sw}$ and β_{off}.

D. Best-Damped G-ADC Models in Feasible Parameter Space

The three poles of the third-order discrete system can be derived according to (19), as shown in (21) shown at the bottom of previous page.

With these poles, the $MMoP$ can be calculated and how the coefficients α_{on} and β_{off} impact on the stability and damping can be shown intuitively by Fig. 6.

Different with two-level converters, the minimum $MMoP$ for three-level converters shown in Fig. 6 is always larger than zero. It is because two coefficients of α_{on} and β_{off} cannot make all three poles equal to zero simultaneously. However, the best-damped parameter point can still be found numerically with the minimum average modulus of (21) when the approximated coefficients are $\alpha_{\text{on}} = -5.04Y_{sw}$ and $\beta_{\text{off}} = -0.39$.

V. SUMMARY OF THE ADC MODELS

A. Relationship of L/C-ADC and G-ADC

Since the ON-state emulating circuit and OFF-state emulating circuit of G-ADC model can be any circuit as long as they satisfy the two requirements in Section II-B. Actually, the inductor branch and capacitor/resistor branch of L/C-ADC model also satisfy these requirements. Hence, the L/C-ADC model is a special case of the G-ADC model. From the history current expressions of L/C-ADC model discretized by BE method and trapezoidal (TP) method, we can find its relationship with the G-ADC model as shown in Table II, where L_{sw}, C_{sw}, and R_{sw} are the values of small inductor, small capacitor, and series resistor of the L/C-ADC model, respectively. α_{off} and β_{on} of the history current expression are all the same for both L/C-ADC and G-ADC models. The main difference is the ranges of α_{on} and β_{off}.

In the $\alpha_{\text{on}}/Y_{sw} - \beta_{\text{off}}$ plane of Fig. 7, the relationship between L/C-ADC model and G-ADC model is more intuitive. The vertical lines represent the feasible parameter space of L/C-ADC model discretized by TP method and BE method, respectively. This figure indicates that the G-ADC model has a higher dimension of feasible parameter space than the L/C-ADC model. That means the G-ADC model is able to describe more transient characteristics. The two crossing points shown in Fig. 7(a) are corresponding to the best-damped G-ADC models for two-level converters, while the crossing point shown in Fig. 7(b) is for the three-level converter. They are all out of the feasible parameter space of L/C-ADC models, which implies that the best-damped G-ADC models cannot be achieved by the L/C-ADC model only through parameter settings.

B. Generality of the G-ADC Method

As mentioned in the Introduction, the parameter settings of L/C-ADC model are related to the operating conditions and circuit parameters of the external system. While in this paper, G-ADC switch models in the basic circuit unit are decoupled from the external circuit by regarding the filter inductance and smoothing capacitor as a current source and a voltage source, respectively. Therefore, the derived feasible parameter space, as well as best-damped point(s), are independent of the external system and can apply to the converters which share the same basic circuit units. In other words, two-level converters which can

TABLE II
SUMMARY OF THE ADC MODELS

		Y_{sw}	α_{off}	β_{off}	α_{on}	β_{on}
G-ADC for two-level converters	Feasible parameter space	$\frac{\Delta t}{L_{ex}} = Y_{sw} = \frac{C_{sm}}{\Delta t}$	Y_{sw}	Satisfy (14)		-1
	Best-damped point I	$\sqrt{\frac{C_{sm}}{L_{ex}}}$	Y_{sw}	$1-\sqrt{2}$	$\left(-1-\sqrt{2}\right)Y_{sw}$	-1
	Best-damped point II	$\sqrt{\frac{C_{sm}}{L_{ex}}}$	Y_{sw}	$1+\sqrt{2}$	$\left(-1+\sqrt{2}\right)Y_{sw}$	-1
G-ADC for three-level converters	Feasible parameter space	$\frac{\Delta t}{L_{ex}} = Y_{sw} = \frac{C_{sm}}{\Delta t}$	Y_{sw}	Satisfy (20)		-1
	Best-damped point (approximated)	$\sqrt{\frac{C_{sm}}{L_{ex}}}$	Y_{sw}	-0.39	-5.04 Y_{sw}	-1
L/C-ADC	Backward Euler method	$Y_{sw} = \frac{\Delta t}{L_{sw}} = \frac{C_{sw}}{\Delta t + C_{sw}R_{sw}}$	Y_{sw}	$-R_{sw}Y_{sw}$	0	-1
	Trapezoidal method	$Y_{sw} = \frac{\Delta t}{2L_{sw}} = \frac{2C_{sw}}{\Delta t + 2C_{sw}R_{sw}}$	Y_{sw}	$1-2R_{sw}Y_{sw}$	- Y_{sw}	-1

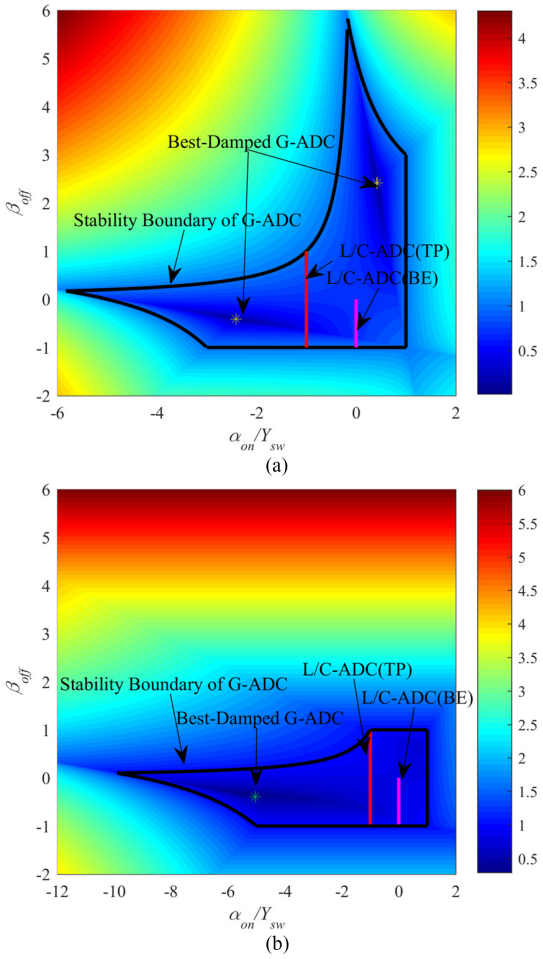

Fig. 7. Feasible parameter space of G-ADC model. (a) Two-level converters. (b) Three-level converters.

TABLE III
GENERALITY OF L/C-ADC MODEL AND G-ADC MODEL

	L/C-ADC model	G-ADC model
Independent of operation point of external systems	*No*	*Yes*
Independent of circuit parameter of external systems	*No*	*Yes*
Independent of converter topology	*No*	*No*
Practicable in high switch frequency applications	*No*	*Yes*

be decomposed and simplified into Fig. 3(c), share the common set of best-damped parameters. Similarly, three-level converters which can be decomposed and simplified into Fig. 5(c) share another set. The other topologies which cannot be classified into these two categories can be analyzed using the similar process of Sections III and IV. Besides, the best-damped G-ADC model almost has no virtual power loss, which makes it still accurate in high switch frequency applications. Therefore, the generality of L/C-ADC model and G-ADC model can be summarized in Table III.

VI. FPGA IMPLEMENTATION OF REAL-TIME SIMULATION

A. NI-PXIe-Based Real-Time Simulation Platform

We implement the G-ADC-based real-time simulation on a universal platform of National Instruments shown in Figs. 8 and 9. This self-built simulation platform mainly consists of a real-time CPU module, an FPGA module, a host-PC, and other external devices. The real-time CPUs simulate the control system which receives the real-time measured signals from the FPGA

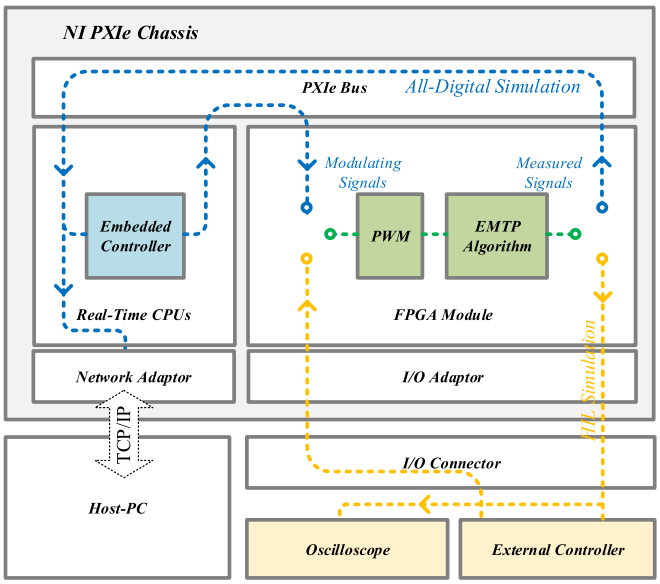

Fig. 8. Structure of the real-time simulation platform.

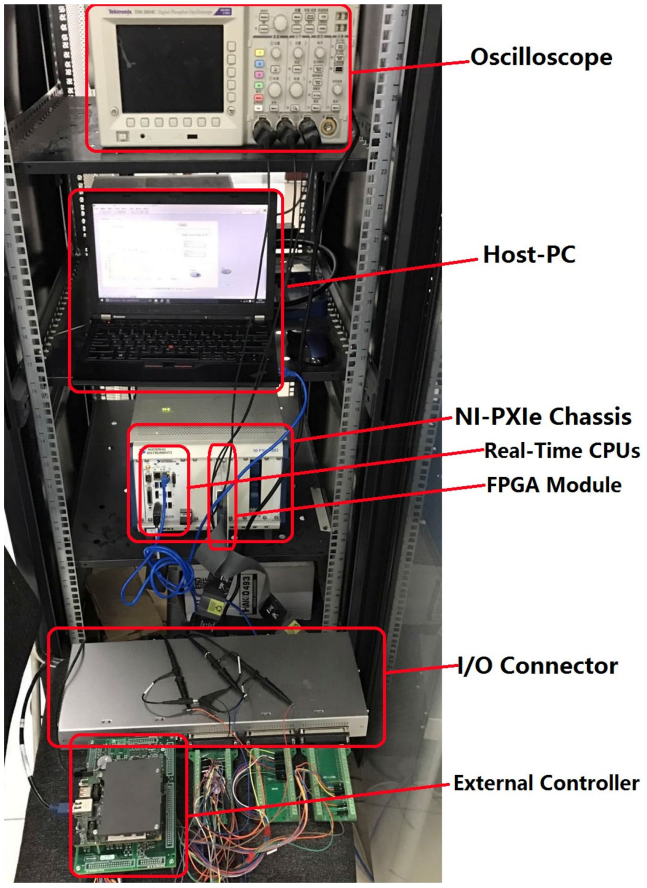

Fig. 9. Platform setup.

module and sends the modulating signals to the FPGA module through the PXIe bus. The FPGA module performs the EMTP algorithm with the switch modeled by ADC model, which will be elaborated in Section VI-B. Besides, the PWM generation is also implemented on the FPGA. As for the host-PC, it provides the development environment and works as the human-machine interface during simulating. This simulation platform also provides an I/O interface with the external controller in the applications of HIL simulation.

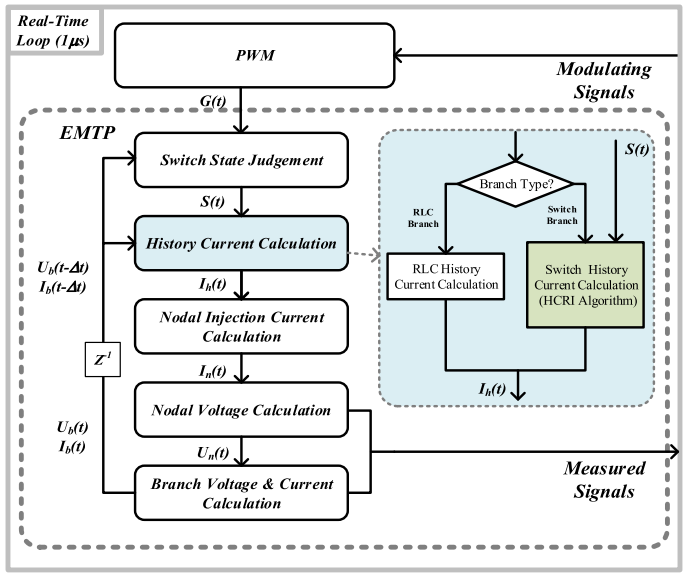

Fig. 10. Flow chart of the ADC-based EMTP algorithm on FPGA.

B. G-ADC-Based EMTP Algorithm Implemented on FPGA

Fig. 10 shows the flow chart of ADC-based EMTP algorithm in one simulation loop. The procedure consists of five steps, to judge the switch states, to calculate the history currents, nodal injection currents, nodal voltages, branch voltages, and currents in turns. Details about the ETMP algorithm can be found in [24] and the FPGA implementation can be found in [26] and [27]. Especially, the history currents of switch branches are directly calculated with branch voltages and branch currents of the last step except at the first step after switching actions. As for the first step after switching actions, the history current reinitialization (HCRI) algorithm is adopted to reduce the initial errors.

C. HCRI Algorithm

The zero-input response in the time domain is related to not only the z-transformation functions but also the initial states. In order to further reduce the virtual power loss, the initial states after switching actions should also be considered. Some researchers have tried to solve the virtual power loss problems by the reinitialization techniques [28]. The compensation source technique [20] can also be seen as another form of the reinitialization techniques. However, these techniques are all for L/C-ADC models, thus, the reduced initial errors still cannot be well damped in the following simulation steps.

The main idea of the HCRI algorithm is to minimize the initial errors after switching actions by making sure the history current at the first step after switch turning ON equal to the history current at the final step of last ON state. Similarly, the history current at the first step after switch turning OFF should be equal to the history current at the final step of the last OFF state. The

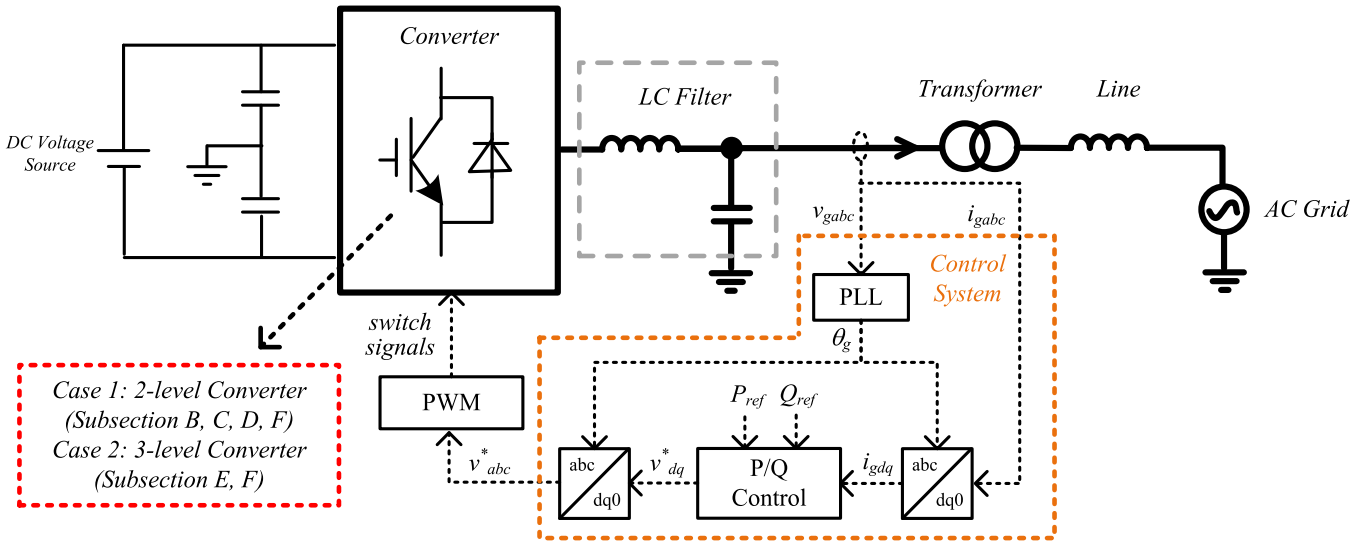

Fig. 11. Testing system with a three-phase VSC.

procedure of history current calculation with HCRI algorithm is as follows:

HCRI Algorithm:

If $S_i(t) = S_i(t - \triangle t)$
  If $S_i(t) = 1$ Calculate $I_{h\_swi}(t) = I_{h\_\text{ON}}(t)$;
  Else Calculate $I_{h\_swi}(t) = I_{h\_\text{OFF}}(t)$;
  End
Else
  If $S_i(t) = 1$ Calculate $I_{h\_swi}(t) = I_{h\_\text{ON}}(t_{\text{last\_action}})$;
  Else Calculate $I_{h\_swi}(t) = I_{h\_\text{OFF}}(t_{\text{last\_action}})$;
  End
  Update $t = t_{\text{last\_action}}$;
End

where $S_i(t)$ denotes the ON/OFF state of the ith switch and $t_{\text{last\_action}}$ denotes the time when last switching action happens.

VII. Case Study

A. Testing System Configurations

The real-time simulation of a testing system with a three-phase voltage source converter (VSC) shown in Fig. 11 is performed on the NI-PXIe platform. The converter of two-level topology (Case 1) is simulated and discussed in Section VII-B, C, D, and F. The converter of three-level topology (Case 2) is simulated and discussed in Section VII-E and F.

The dc voltage source is 750 V and the RMS of ac grid voltage is 220 V. The inductance of LC filter is 1.5 mH and the capacitance is 50 μF. The smoothing capacitors on the dc side are 4000 μF. The equivalent inductance of the transformer and line is 2.3 mH. The carrier frequency of PWM is 10 kHz. The three-phase VSC is equipped with a P/Q controller. P_{ref} is set to 40 kW and Q_{ref} is set to zero.

B. Comparison of the Best-Damped G-ADC Model and the Optimized L/C-ADC Model

Two ADC models are compared in the EMTP simulation implemented on the FPGA: 1) an optimized L/C-ADC model with the parameters set by the method adopted in RTDS small-time-step model library [21] and 2) the best-damped G-ADC model of Type I. The same testing system is also built in PSCAD/EMTDC, serving as a benchmark model.

Fig. 12 shows the turning-OFF and turning-ON processes of one switch in one switch period. Although the parameters of L/C-ADC model are optimized, the voltage and current waveforms still have obvious transient errors after switching actions, as shown in Fig. 12(a) and (b). These errors take too many steps to be damped. As a result, the L/C-ADC has large power/energy loss after switching actions, as shown in Fig. 12(c) and (d). On the other hand, the best-damped G-ADC model has small initial errors, and these errors are damped in two steps after switching actions. Therefore, the G-ADC model has little power/energy loss. As the two-value-resistor model in PSCAD has a small leak current during ON-state and a small forward voltage drop during OFF-state, the energy loss accumulates slightly during the whole switch period, as shown in Fig. 12(d). Overall, the waveforms of best-damped G-ADC model are more close to the offline waveforms of PSCAD comparing with the L/C-ADC.

C. Virtual Power Loss Ratios Under Different Carrier Frequencies

In Fig. 12(a), it takes more than 10 μs for the switch voltage of L/C-ADC model to converge to the steady state, while it takes about 2 μs for the G-ADC model. When the carrier frequency is higher, i.e., the switching period becomes shorter, the L/C-ADC model may switch to a new state before its voltage reaches the steady state, as shown in Fig. 13. However, in high frequency, the best-damped G-ADC model still has an ideal waveform.

To measure the accuracy of switch model, the virtual power loss ratio is defined, which is the total virtual power loss of all

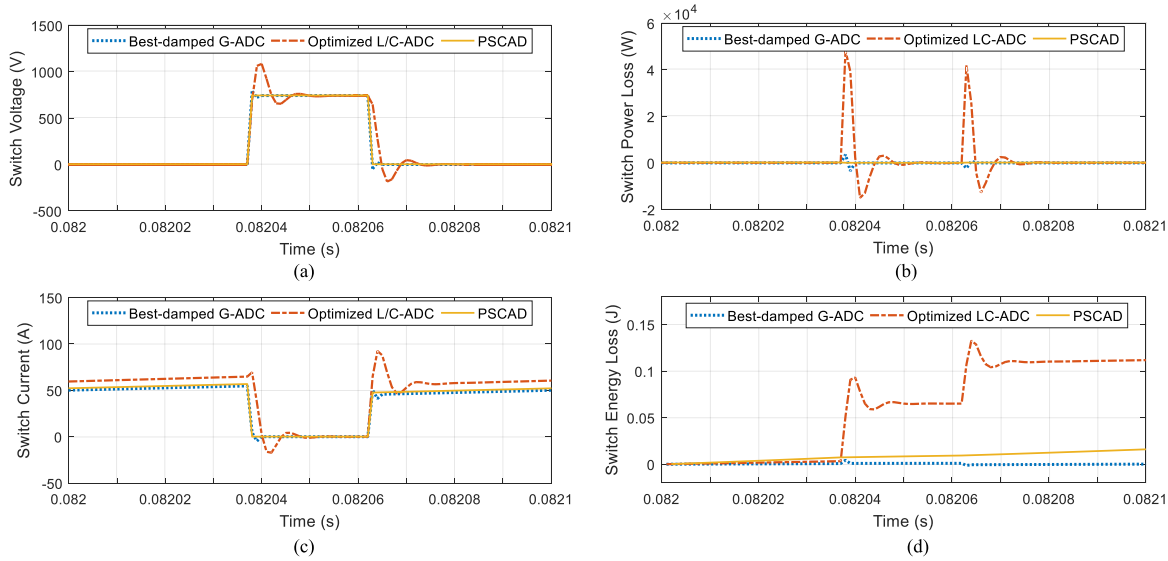

Fig. 12. Comparison of the best-damped G-ADC and L/C-ADC. (a) Switch voltage. (b) Switch power loss. (c) Switch current. (d) Switch energy loss.

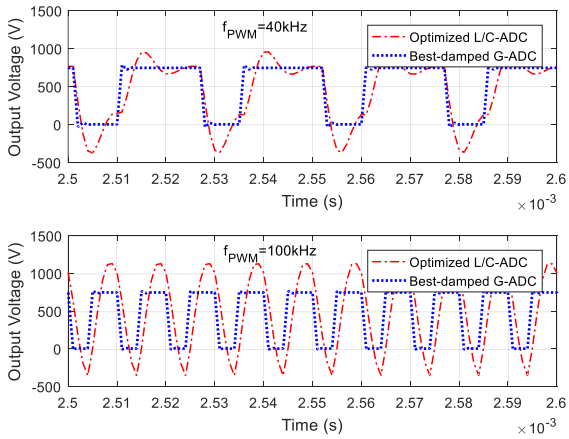

Fig. 13. Switch voltage waveforms under the carrier frequencies of 40 kHz and 100 kHz.

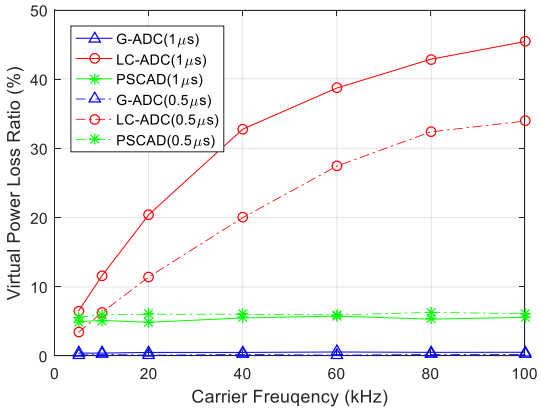

Fig. 14. Virtual power loss ratios under different carrier frequencies.

the six switches divided by the input power of the converter. In one switch period, the energy loss is mainly dependent on the transient errors of switch voltage/current. While in a larger time scale, the virtual power loss ratio also depends on the switching frequency and time step for the ADC model. Fig. 14 shows the virtual power loss ratios under different carrier frequencies.

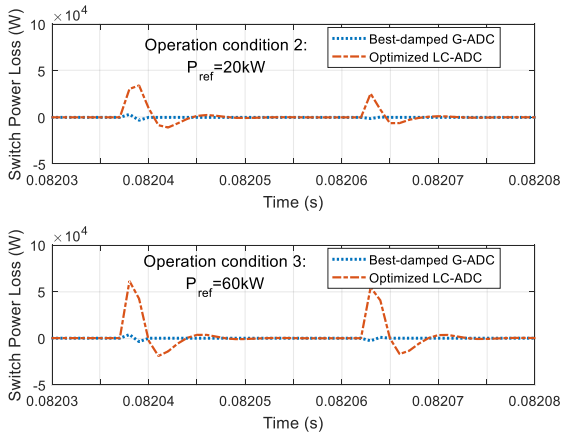

Fig. 15. Virtual power loss under different operating conditions.

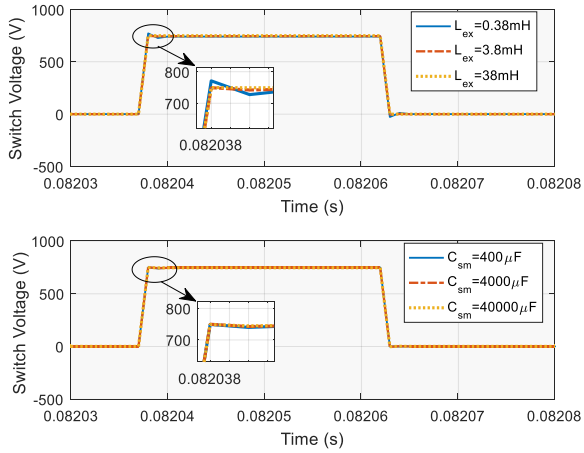

Fig. 16. Voltages of best-damped G-ADC model under different external circuit parameters.

For the L/C-ADC model, the virtual power loss ratio is approximately proportional to the carrier frequency in low frequency, as the virtual power loss is mainly generated during switching actions. The virtual power loss ratio will be unaccept-

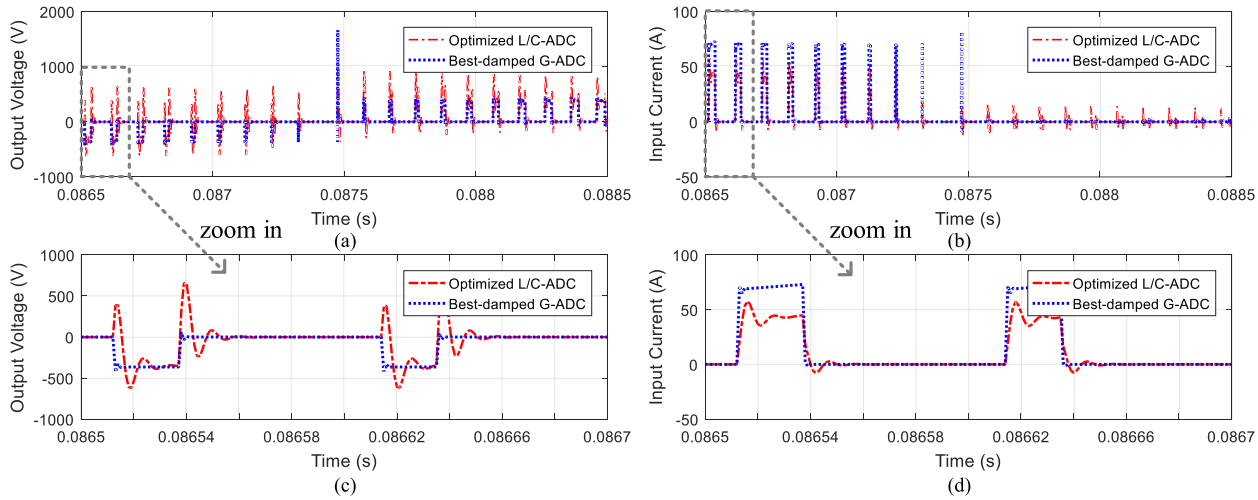

Fig. 17. Comparison of the best-damped G-ADC and L/C-ADC for three-level converters. (a) Output voltages U_o of best-damped G-ADC model. (b) Input currents I_1 of best-damped G-ADC model. (c) Zoomed-in output voltages U_o of best-damped G-ADC model. (d) Zoomed-in input currents I_1 of best-damped G-ADC model.

able when the switching frequency increases. The only method to reduce the power loss ratio of L/C-ADC model is adopting a smaller time step. However, a smaller time step means a stricter real-time requirement.

As for the two-value-resistor model of PSCAD, it accumulates the energy loss slightly at a constant speed during the whole switch period, thus, has a small virtual power loss almost independent of switch frequency and time step, as shown in Fig. 14.

As the voltage and current waveforms of best-damped G-ADC model is very close to those of the ideal switch model, no matter what the switching frequency is, the virtual power loss ratio of the best-damped model remains at a tiny degree.

D. Simulations Under Different Operating Conditions and External Circuit Parameters

One problem with the L/C-ADC model is that the parameter setting depends on the current operating conditions and external circuit parameters. However, the derivation of best-damped G-ADC models is independent of the operating conditions and external circuit parameters. Therefore, the best-damped characteristic applies to a wide range of simulation situations, theoretically.

To validate the universality of best-damped G-ADC model under different operating conditions, we reset the P_{ref} of the P/Q controller to change the active power output by the VSC. Together with the power loss curves of 40 kW, as shown in Fig. 12(c), Fig. 15 indicates that the best-damped G-ADC model is still almost lossless under different operating conditions, compared with the L/C-ADC model.

To validate the universality of best-damped G-ADC model under different external circuit parameters, we empirically set the external inductance L_{ex} and smoothing capacitor C_{sm}, as shown in Fig. 11 to be one tenth of the original values. And the process is repeated to set L_{ex} and C_{sm} to be ten times of the original values. Fig. 16 indicates that the best-damped G-ADC model switch model can keep the quasi-ideal switch characteristics in a variety of the external circuit parameters.

E. Simulations of the Three-Level NPC Converter

In this section, a three-level NPC converter is simulated under the phase-disposition PWM modulation. Fig. 17 shows the waveforms of the output voltage U_o, shown in Fig. 5(c), and input current I_1, shown in Fig. 5(c). The output voltage and input current of best-damped G-ADC model have much smaller initial transient errors after switching actions and these errors decay in much fewer steps comparing with optimized L/C-ADC model. It implies that the G-ADC model also has obvious advantages over the L/C-ADC model in three-level converter switch modeling.

F. HIL Simulation of the Two-Level Converter and Three-Level Converter

The real-time simulations in the case study are all-digital simulation. Actually, this simulation platform is also capable of the HIL simulation, as shown in Fig. 8. A preliminary test of the HIL is given here. Both L/C-ADC model and G-ADC model are simulated. Fig. 18 is the screen shot of the oscilloscope with channel 1 displaying the switch voltage of two-level converters and channel 2 displaying the switch current. Fig. 19 is the screen shot of the oscilloscope with channel 1 displaying the output voltage U_o, shown in Fig. 5(c), of three-level converters and channel 2 displaying the input current I_1, shown in Fig. 5(c).

Both Figs. 18 and 19 show that the best-damped G-ADC model has an obvious advantage on model accuracy over the L/C-ADC model, which is consistent with the conclusions of the previous sections. To further compare the efficiency of switch models, the average execution time per step (1 μs) is shown in Table IV and the FPGA resource consumption is shown in Table V.

From Tables IV and V, we can see that the G-ADC model almost cost the same execution time and FPGA resource with the L/C-ADC model. Both the L/C-ADC model and G-ADC model satisfy the real-time requirement. The extra 0.012 μs G-ADC model cost has few influences on the real-time performance, and the extra resource G-ADC model consumes is very small con-

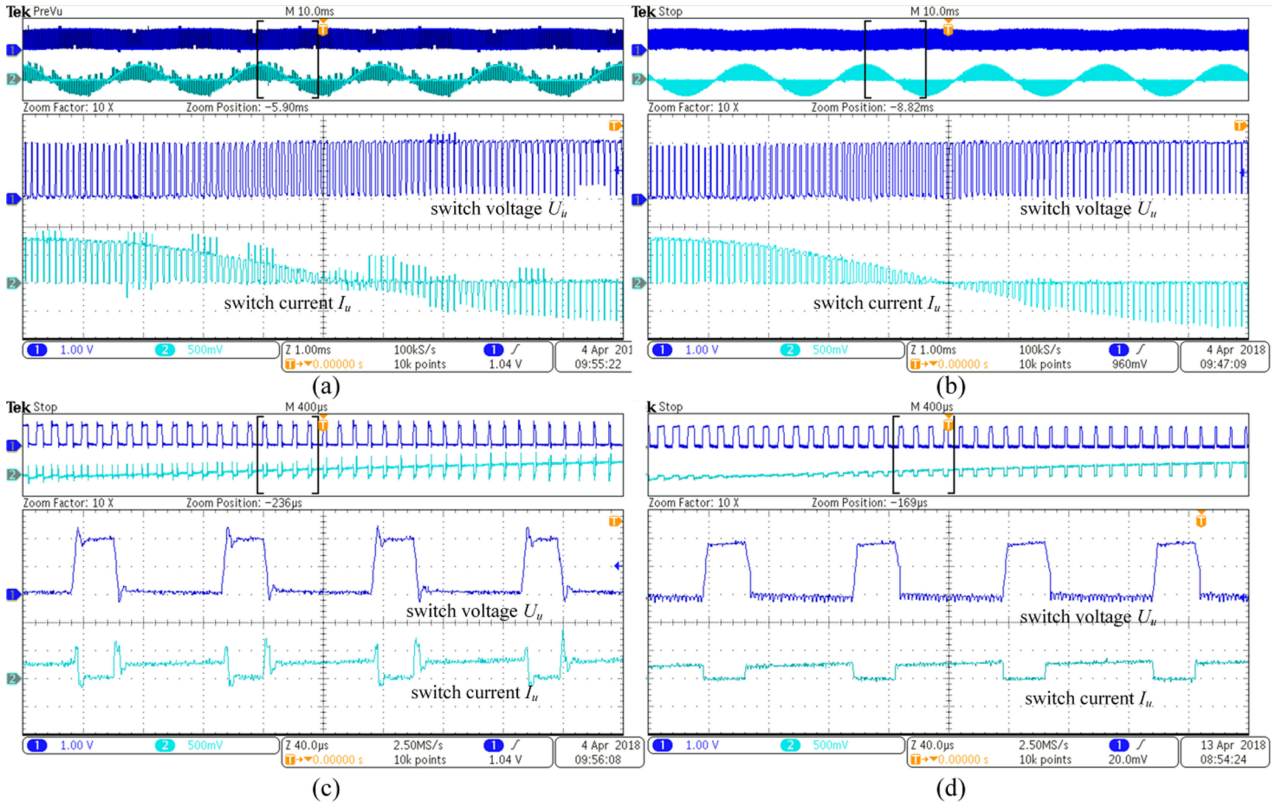

Fig. 18. Switch voltage and switch current of two-level converters (channel 1: switch voltage, channel 2: switch current). (a) Waveforms of L/C-ADC model. (b) Waveforms of G-ADC model. (c) Zoomed-in waveforms of L/C-ADC model. (d) Zoomed-in waveforms of G-ADC model.

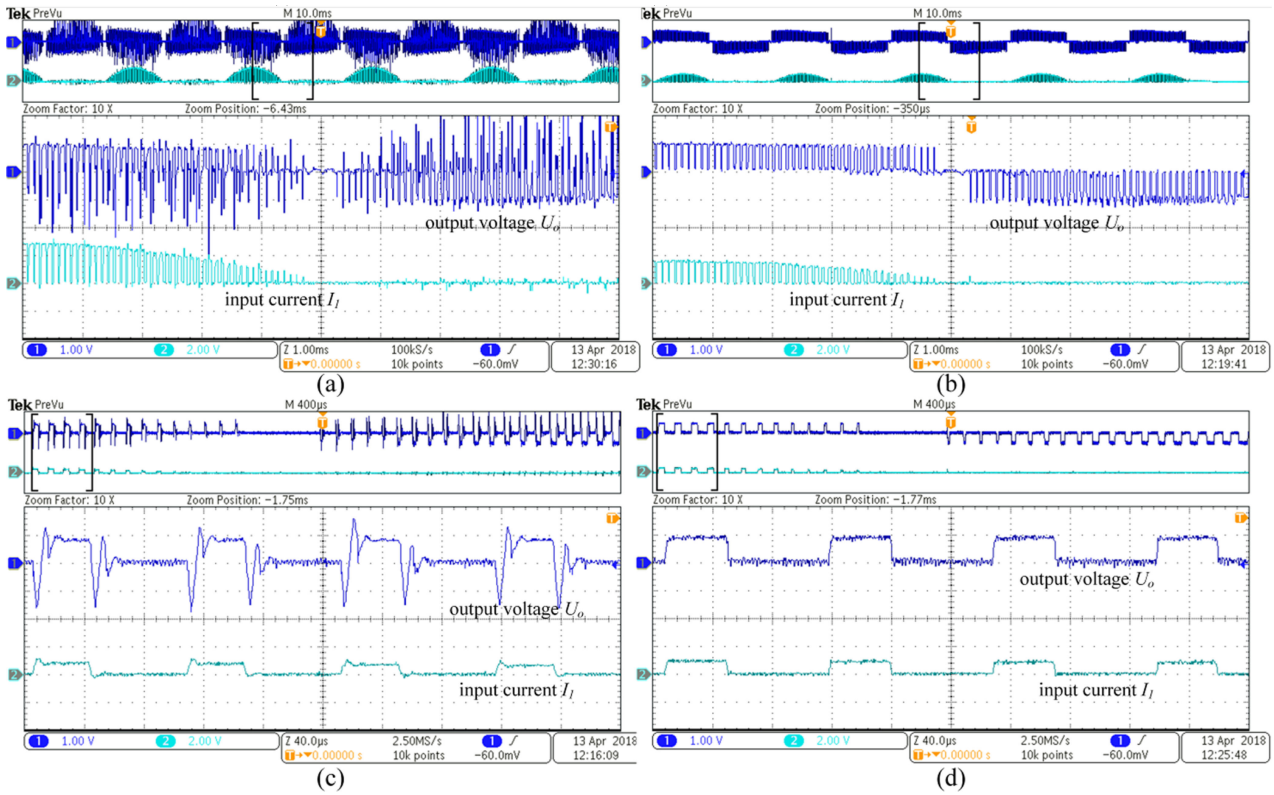

Fig. 19. Output voltage and input current of three-level converters (channel 1: switch voltage, channel 2: switch current). (a) Waveforms of L/C-ADC model. (b) Waveforms of G-ADC model. (c) Zoomed-in waveforms of L/C-ADC model. (d) Zoomed-in waveforms of G-ADC model.

TABLE IV
AVERAGE EXECUTION TIME PER STEP (1 μS) OF THE SWITCH MODELS

	Average Execution Time per Step (1μs)		
	L/C-ADC model	G-ADC model	Two-value-resistor model
Off-line simulation on PC	*178*μs	*181*μs	*940*μs
Real-time simulation on FPGA	*0.463*μs	*0.475*μs	/

TABLE V
FPGA RESOURCE CONSUMPTION OF TWO ADC MODELS FOR TWO-LEVEL CONVERTERS

Resource Type	Total Available Resource	Resource Consumption	
		L/C-ADC model	G-ADC model
Flip-Flops	*508400*	*10.2% (51874)*	*10.5% (53350)*
LUTs	*254200*	*19.0% (48374)*	*20.0% (50734)*
Block RAM	*795*	*11.4% (91)*	*11.4% (91)*
DSP48 Slices	*1540*	*10.2% (157)*	*13.7%(211)*

sidering the total resource of FPGA. In conclusion, it is already shown that the best-damped G-ADC model achieves better accuracy and flexibility of parameter setting than the traditional L/C-ADC model with almost the same computational cost and efficiency.

VIII. CONCLUSION

This paper proposes a general G-ADC model. The offline and real-time results of a three-phase VSC testing system show that the best-damped G-ADC model has more ideal waveforms and cause much less virtual power loss than the optimized L/C-ADC model. Simulations under a variety of carrier frequencies, time steps, operating conditions, and external circuit parameters show that these best-damped G-ADC models are insensitive to the operating conditions and external system parameters. HIL simulation results performed on an NI-PXIe-based real-time platform validate the feasibility and effectiveness of the proposed method. However, there are still many works to be done, such as the parameter settings of more complex topologies, the emulation of actual switch power loss, and other nonlinearities in power system.

APPENDIX

The properties and conclusions of G-ADC model in Section III only apply to the power electronic devices satisfying the first assumption in Section III-A. Luckily, the half bridge and full-bridge, two common topologies which compose most of the important two-level ac/dc converters, perfectly meet this requirement. Therefore, the G-ADC model can be applied to the typical ac/dc VSCs. As for the dc/dc converter, such as buck circuit and boost circuit, the combination of IGBT and diode can be seen as a generalized half bridge. As them also work in opposite states for most time, the G-ADC model can also be applied to them.

With regards to the second assumption, this requirement is actually very easy to be satisfied in the small time step simulation. Intuitively, the transient process of the switch model is much faster than that of the filter inductor and smoothing capacitor, thus, the filter inductor and smoothing capacitor of course can be seen as an independent current source and voltage source, respectively. To confirm our guess, we take the half bridge, shown in Fig. 3, for example. The equivalent admittances of the external impedance L_{ex} and smoothing capacitor C_{sm} are

$$\begin{cases} Y_{Lex} = \frac{\Delta t}{L_{ex}+\Delta t R_{ex}} \approx \frac{\Delta t}{L_{ex}} \\ Y_{Csm} = \frac{C_{sm}}{\Delta t}. \end{cases} \tag{A1}$$

Thus, to satisfy the requirement of the second assumption, Y_{sw} needs to be much larger than Y_{Lex} and much smaller than Y_{Csm}

$$\frac{\Delta t}{L_{eq}} \ll Y_{sw} \ll \frac{C_{sm}}{\Delta t}. \tag{A2}$$

Considered that the time step Δt of FPGA-based real-time simulation is usually less than 2 μs, and the filter inductor and smoothing capacitor are on the level of mH and μF, there is a wide range of Y_{sw} to be selected to satisfy (A2). Besides, the VSC usually has smoothing capacitor(s) and filter inductor(s) on each side. L_{ex} could be very small, as long as Y_{sw} that satisfies (A2) exists. If there is no inductance in the analyzed topology, the feasible parameter space and best-damped point derived in this paper will be no longer appropriate.

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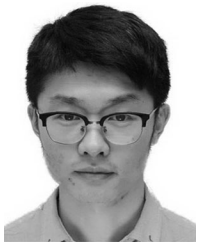

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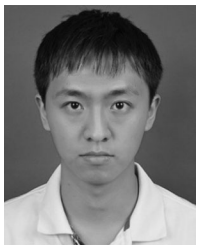

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