Letters

500 °C SiC PWM Integrated Circuit

Saleh Kargarrazi, *Member, IEEE*, Hossein Elahipanah, *Member, IEEE*, Stefano Saggini, *Member, IEEE*, Debbie Senesky, *Member, IEEE*, and Carl-Mikael Zetterling, *Senior Member, IEEE*

***Abstract*—This letter reports on a high-temperature pulsewidth modulation (PWM) integrated circuit microfabricated in 4H-SiC bipolar process technology that features an on-chip integrated ramp generator. The circuit has been characterized and shown to be operational in a wide temperature range from 25 to 500 °C. The operating frequency of the PWM varies in the range of 160 to 210 kHz and the duty cycle varies less than 17% over the entire temperature range. The proposed PWM is suggested to efficiently and reliably control power converters in extreme environments.**

***Index Terms*—Bipolar junction transistor (BJT), high-temperature integrated circuit (IC), pulsewidth modulator (PWM), silicon carbide.**

I. Introduction

WIDE-bandgap devices have been matured over the last decade [1]–[8] and led to design and fabrication of devices and integrated circuits (ICs) that can operate in extreme environments (aviation, downhole exploration, and space). In particular, implementation of high-temperature ICs in SiC (silicon carbide) CMOS (complementary metal–oxide–semiconductor) [9]–[11], metal–semiconductor field-effect transistor [12], junction gate field-effect transistor [6], and BJT (bipolar junction transistor) [13]–[16] technologies has been demonstrated. Moreover, large-scale integration of SiC electronics on chip has viably been accelerated in recent years with efforts to integrate complex circuits [17]–[19], passives [20], and more recently lateral high-current devices and ICs [21], [22].

Today's complex and mobile electrified systems (e.g., electric automobiles and aircraft) urge for power electronics that meet the high power density and wide temperature range requirements of such systems. Although much research has been focused on power converters benefiting wide-bandgap technologies [e.g., SiC and GaN (gallium nitride)], the control, protection, and

Manuscript received May 25, 2018; revised June 26, 2018; accepted July 22, 2018. Date of publication July 24, 2018; date of current version February 5, 2019. *(Corresponding author: Saleh Kargarrazi.)*

S. Kargarrazi and D. Senesky are with the Department of Aeronautics and Astronautics, Stanford University, Stanford, CA 94305 USA (e-mail:

-

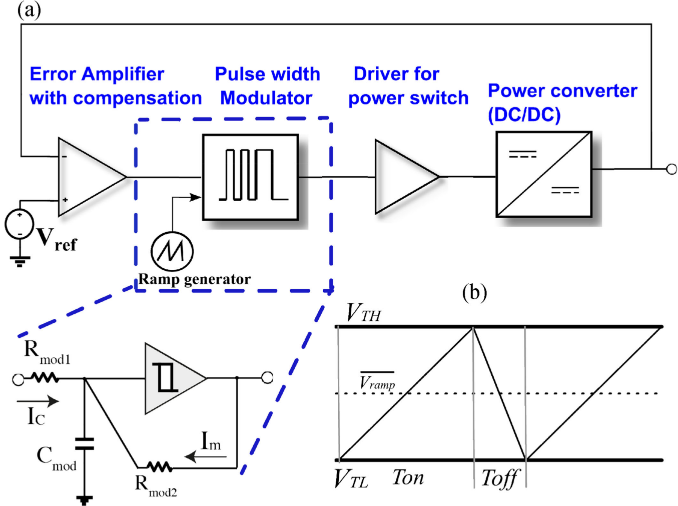

Fig. 1. (a) DC–DC controller schematic: The proposed hysteretic PWM and the ramp generator are indicated with the dashed lines. (b) PWM ramp signal.

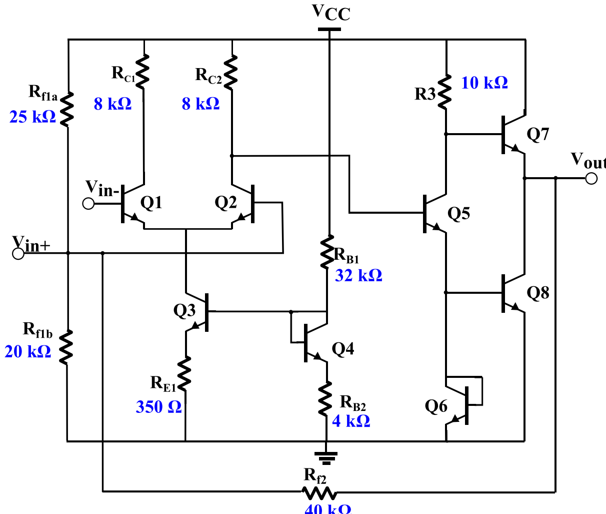

Fig. 2. Schmitt trigger schematic.

a capacitor with a reference current obtained, for example, by mirroring the current that is flowing in an external pin polarized by a reference voltage. Choosing large ramp amplitude in classical PWM architecture increases the immunity of the controller to the switching noise, and therefore a comparator with large input dynamic range is required. However, a classical approach to design a PWM cannot be applied to design a bipolar SiC PWM. The large input dynamic range over the wide temperature range is hard to attain due to the lack of p-n-p transistors with high enough current drive in the bipolar SiC technology. Also, the relatively low gain of the BJTs in this technology (<50) results in high loading effect of each subcircuit. Without the complementary transistor, i.e., p-n-p, the ramp cannot be generated starting from a reference current but a simpler generation based on a resistor is required. The proposed modulation technique in this letter is based on a *hysteretic* architecture, where the oscillator ramp is merged with the comparator, and a comparator with reduced input dynamic range (due to the nature of SiC BJTs) can be used. In contrast to standard hysteretic controllers [31], this letter does not use current ripple as the ramp signal. Instead, in order to have a large enough ramp to reduce the jitter noise, the ramp is generated using an RC ramp generator.

The PWM's gain is defined as the variation of the duty cycle with respect to the variation of the voltage appeared at the input of the PWM. It can be described as $\frac{\Delta D}{\Delta V} = \frac{1}{\Delta V_{\text{ramp}}}$, where ΔV_{ramp} is the ramp's amplitude. In general, this amplitude is chosen sufficiently large to guarantee a sufficient power supply noise rejection ratio on the duty cycle. In the case of the SiC control circuit, the amplitude must be large enough to guarantee the operation of the circuit over a wide range of temperature variation and process uncertainties.

The proposed hysteretic modulator comprises a comparator with hysteresis function (a Schmitt trigger) as shown in Fig. 2, and an RC network to generate a ramp. C_{mod} charges and discharges in each cycle through R_{mod1} and R_{mod2}. The comparator provides two threshold levels, V_{TH} and V_{TL}, which define the maximum and minimum levels of the ramp signal [see Fig. 1(b)].

By choosing the appropriate positive-feedback resistors (R_{f1a}, R_{f1b}, and R_{f2}), the comparator-threshold levels, V_{TH} and V_{TL} can be set. The resistor values were selected based on following equations:

$$V_{\text{TH}} = \frac{R_{f1b}}{R_{f1b} + (R_{f1a}||R_{f2})} \cdot V_{CC} \tag{1}$$

$$V_{\text{TL}} = \frac{R_{f1b}||R_{f2}}{(R_{f1b}||R_{f2}) + R_{f1a}} \cdot V_{CC}. \tag{2}$$

The ramp's amplitude and its average can be expressed as $\Delta V_{\text{ramp}} = V_{\text{TH}} - V_{\text{TL}}$ and $\overline{V_{\text{ramp}}} = (V_{\text{TH}} + V_{\text{TL}})/2$.

The ON time (T_{on}) of the PWM, and hence the power switch, can be expressed as a function of the ramp amplitude and the mean current flowing in R_{mod1} and R_{mod2}. Therefore,

$$T_{\text{on}} = \frac{C_{\text{mod}} \Delta V_{\text{ramp}}}{\left(\frac{\overline{V_{\text{ramp}}} - V_{\text{OL}}}{R_{\text{mod2}}} - \overline{I_c}\right)} \tag{3}$$

where V_{OL} is the minimum voltage level at the output of the PWM. By using similar equations to define the OFF time of the PWM, the switching period T_{sw} can be calculated as

$$T_{\text{sw}} = \left(1 + \frac{\left(\frac{\overline{V_{\text{ramp}}} - V_{\text{OL}}}{R_{\text{mod2}}} - \overline{I_c}\right)}{\left(\frac{V_{\text{OH}} - \overline{V_{\text{ramp}}}}{R_{\text{mod2}}} + \overline{I_c}\right)}\right) T_{\text{on}} \tag{4}$$

where V_{OH} is the maximum voltage level at the output of the PWM. Assume, for the sake of simplicity, that the charge and discharge currents are equal

$$\overline{I_m} = \frac{V_{\text{OH}} - \overline{V_{\text{ramp}}}}{R_{\text{mod2}}} = \frac{\overline{V_{\text{ramp}}} - V_{\text{OL}}}{R_{\text{mod2}}}. \tag{5}$$

Hence,

$$T_{\text{on}} = \frac{C_{\text{mod}} \Delta V_{\text{ramp}}}{(\overline{I_m} - \overline{I_c})} \quad \text{and} \tag{6}$$

$$T_{\text{sw}} = \left(\frac{2\overline{I_m}}{(\overline{I_m} + \overline{I_c})}\right) T_{\text{on}}. \tag{7}$$

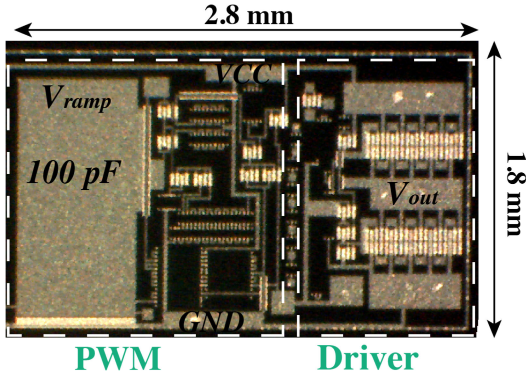

Fig. 3. Optical photo of the PWM and the driver.

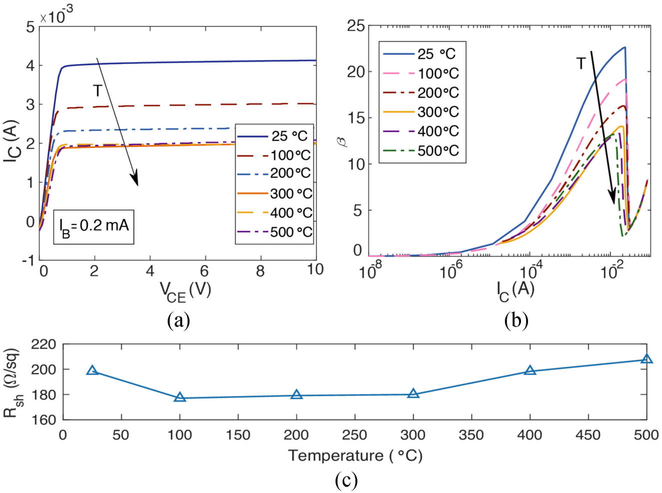

Fig. 4. (a) Output characteristics of the SiC single BJTs. (b) Forward current gain β at $V_{BC} = 0$. (c) Sheet resistance of the collector epi layer.

Since output stage of the *error amplifier* and *Schmitt trigger* have the same topology [18], the ratio of the currents as appeared in (7) depends on the ratio of the corresponding resistors [$\frac{R_{\text{mod1}}}{(R_{\text{mod1}}+R_{\text{mod2}})}$]. Considering the same temperature dependence of the resistors implemented on collector epi layer and their appearance as ratio, the switching-frequency variation over temperature is mitigated.

C. Chip Layout

An optical photo of the microfabricated 4H-SiC PWM and the driver is shown in Fig. 3. The blocks are connected to the same power supply and ground (GND) nodes. Also, all the BJTs have the same orientation to mitigate the process variation.

III. Experimental Results and Discussions

The chip was placed on a temperature-controlled hot stage and tested at different temperatures up to 500 °C. Initially, SiC BJTs and resistors, as the elements of the PWM circuit, were characterized over the temperature range. The maximum current gain $\beta_{\max}$ decreases from 23 down to 13 (see Fig. 4), as the temperature rises due to the ionization of the dopants. A slight improvement of the current gain in the range between 300 and 500 °C is observed because of the increased carrier lifetime.

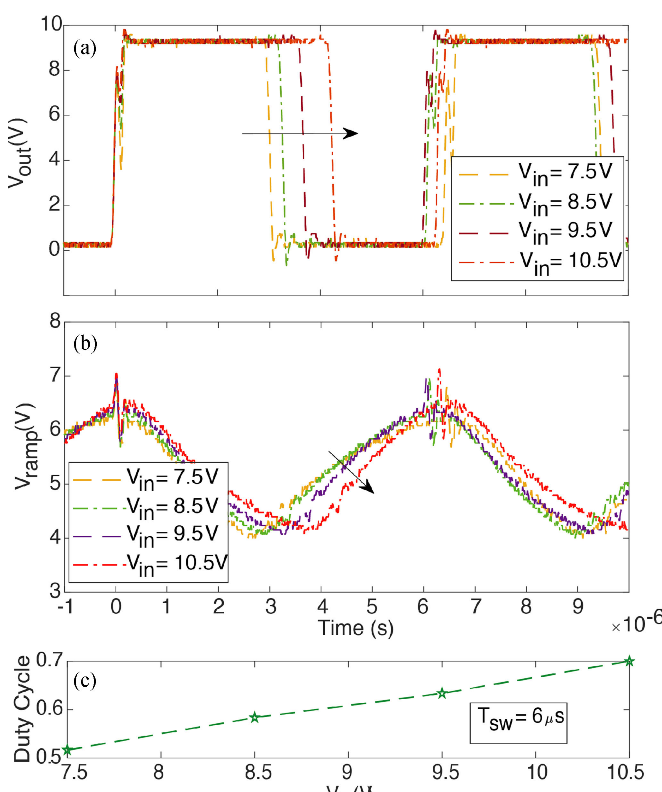

Fig. 5. (a) Pulsewidth modulated signal at the output of the driver. (b) Ramp signal. (c) Duty cycle of the PWM over variation of the input signal.

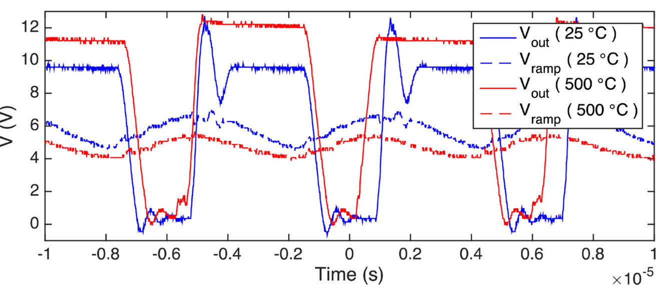

Fig. 6. Generated ramp and the pulse at the output of the driver while driving a 4.7 nF capacitive load at 25 and 500 °C ($V_{\text{in}} = 8.5$ V).

Moreover, the sheet resistance decreases as the temperature rises up to 100 °C due to the ionization of dopants and then increases due to the reduced mobility of carriers [8].

First, measurement of the PWM circuit was conducted at room temperature. A voltage varying between 7.5 and 10.5 V was injected to the input of the PWM. This voltage represents the amplified error of the converter that appears at the output of the error amplifier. The pulsewidth-modulated pulse at the output of the driver and the generated ramp is characterized and illustrated in Fig. 5. Also, the variation of the duty cycle of the PWM over the input-voltage variation is derived. The switching period is $\sim$6 μs and the turn-ON variation in the range of 3.1–4.2 μs is obtained as the input voltage varies.

Fig. 6 shows the ramp and output voltages at 25 and 500 °C for a typical case of $V_{\text{in}} = 8.5$ V while the driver in driving a 4.7 nF capacitor. A 1200-V CREE SiC MOSFET has an input ca-

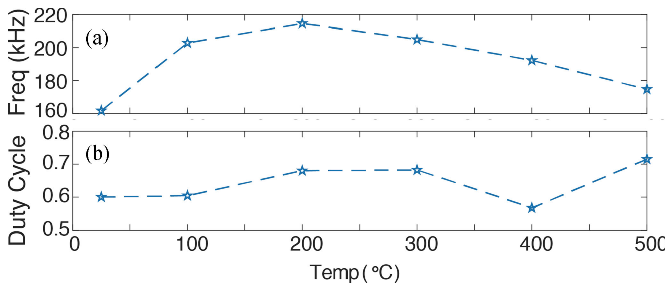

Fig. 7. (a) Ramp frequency. (b) Duty cycle of the PWM up to 500 °C ($V_{\rm in}$ = 8.5 V).

TABLE I
COMPARISON OF THIS WORK WITH RECENT WIDE-BANDGAP PWM ICS

	GaN PWM IC [28]	CMOS SiC PWM IC [29]	Bipolar SiC PWM IC (*This work*)
Operating Temperature	$25-250$°C	$25-400$°C	$25-500$°C
PWM Architecture	Hysteretic control External sawtooth generator	Digitally controlled External clock generator	Hysteretic control Integrated ramp generator
Operating Frequency	1 MHz	200 kHz	160 - 210 kHz
Chip size	$\sim$ 1.6 mm^2	3.9 mm^2	5 mm^2

pacitance of ~2.8 nF. The capacitive load chosen in this letter is far beyond the gate capacitance of commercial power switches, indicating that the PWM is suitable for various sizes of power switches. The ramp and output curves at room temperature and 500 °C differ mainly due to the variation of the BJTs current gain β and the base-emitter voltage $V_{\rm BE}$ over temperature. Reduction of β at elevated temperatures, among its overall influence on the biasing levels of the BJTs, reduces the current in $R3$–$Q5$–$Q6$ branch in Fig. 2. Moreover, $V_{\rm BE}$ in Q_6 is also reduced at elevated temperatures. Both these phenomena result in higher output voltage in ON state at 500 °C as compared to room temperature.

The operating frequency of the PWM has been determined based on a study to control a DC–DC 15–30 V boost converter, as described in full details in [18]. It has also been estimated during the simulation of the closed-loop PWM controller/converter design, using the device models that have been extracted from a previous fabrication run. The variation of the frequency of the PWM pulse and the ramp over temperature is illustrated in Fig. 7(a) showing the nonmonotonous variation of the frequency over temperature, with a maximum of 210 kHz at 200 °C. This observation is related to the nonmonotonous variation of the sheet resistances realized in collector layer. This phenomenon has been previously discussed in SiC bipolar technology[8]. Moreover, the variation of the duty cycle of the PWM at $V_{\rm in}$ = 8.5 V is shown in Fig. 7 (b) showing variation of the duty cycle in the range of 0.55 to 0.7 over the temperature range between 25 and 500 °C. Table I compares the proposed bipolar SiC PWM IC with the recent wide-bandgap PWM ICs. It has to be noted that, unlike the other designs, the bipolar SiC PWM IC has an integrated ramp generator. Therefore, its operating frequency is dictated by the value of the integrated resistor and capacitor and follows their variation over temperature.

Future work includes design of temperature-insensitive circuitry to reduce the frequency and duty-cycle variation over temperature. Furthermore, implementation of a PWM circuits with an integrated reference voltage as well as other PWM architectures in bipolar SiC could be investigated.

IV. CONCLUSION

In this letter, a fully integrated high-temperature PWM and ramp generator circuit in SiC BJT technology is demonstrated. The characteristics of the circuit is discussed over temperature range between 25 and 500 °C. Using a voltage reference at the input of the PWM varying in the range of 7.5 to −10.5 V, as the amplified error of the error amplifier, the duty cycle can be set between 0.5 and 0.7. Due to the variation of the integrated resistors, the ramp-generator frequency varies with temperature; however, the operating frequency is in the range of 160 to 210 kHz over the entire temperature range (up to 500 °C). The high-temperature PWM IC enables controlling power converter at elevated temperatures.

ACKNOWLEDGMENT

The authors would like to thank Knut and Alice Wallenberg Foundation for their support.

REFERENCES

[1] K. D. Chabak et al., "Strained AlInN/GaN HEMTs on SiC With 2.1-A/mm output current and 104-GHz cutoff frequency," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 561–563, Jun. 2010.

[2] P. Herfurth et al., "GaN-on-insulator technology for high-temperature electronics beyond 400 °C," *Semicond. Sci. Technol.*, vol. 28, no. 7, 2013. Art. no. 074026. [Online]. Available: http://stacks.iop.org/0268-1242/28/i=7/a=074026

[3] A. J. Suria, A. S. Yalamarthy, H. So, and D. G. Senesky, "DC characteristics of ALD-grown Al2O3 /AlGaN/GaN MIS-HEMTs and HEMTs at 600 °C in air," *Semicond. Sci. Technol.*, vol. 31, no. 11, 2016, Art. no. 115017. [Online]. Available: http://stacks.iop.org/0268-1242/31/i=11/a=115017

[4] D. Clark et al., "High temperature digital and analogue integrated circuits in silicon carbide," in *Mater. Sci. Forum*, vol. 740, pp. 1065–1068, 2013.

[5] D. J. Spry, P. G. Neudeck, L. Chen, D. Lukco, C. W. Chang, and G. M. Beheim, "Prolonged 500 °C Demonstration of 4H-SiC JFET ICs with two-level interconnect," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 625–628, May 2016.

[6] P. G. Neudeck, D. J. Spry, L. Chen, N. F. Prokop, and M. J. Krasowski, "Demonstration of 4H-SiC digital integrated circuits above 800 °C," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1082–1085, Aug. 2017.

[7] W. C. Lien, N. Damrongplasit, J. H. Paredes, D. G. Senesky, T. J. K. Liu, and A. P. Pisano, "4H-SiC N-Channel JFET for operation in high-temperature environments," *IEEE J. Electron Devices Soc.*, vol. 2, no. 6, pp. 164–167, Nov. 2014.

[8] L. Lanni, B. Malm, M. Östling, and C.-M. Zetterling, "500 °C Bipolar integrated OR/NOR gate in 4H-SiC," *IEEE Electron Device Lett.*, vol. 34, no. 9, pp. 1091–1093, Sep. 2013.

[9] A. Rahman et al., "High-Temperature SiC CMOS comparator and op-amp for protection circuits in voltage regulators and switch-mode converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 935–945, Sep. 2016.

[10] P. Shepherd, A. Rahman, S. Ahmed, A. M. Francis, J. Holmes, and H. A. Mantooth, "500 kHz – 5 MHz phase-locked loops in high-temperature silicon carbide CMOS," *Additional Conf.(Device Packaging, HiTEC, HiTEN, & CICMT)*, vol. 2014, no. HITEC, pp. 000 076–000 083, 2014. [Online]. Available: https://doi.org/10.4071/HITEC-TP15

[11] M. Barlow, A. M. Francis, N. Chiolino, J. Holmes, A. Abbasi, and H. A. Mantooth, "SiC-CMOS digital circuits for high temperature power conversion," in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl.*, Nov. 2016, pp. 223–227.

[12] M. Alexandru *et al.*, “SiC integrated circuit control electronics for high-temperature operation,” *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3182–3191, May 2015.

[13] C.-M. Zetterling *et al.*, “Bipolar integrated circuits in SiC for extreme environment operation,” *Semicond. Sci. Technol.*, 2017. [Online]. Available: http://iopscience.iop.org/10.1088/1361-6641/aa59a7

[14] S. Kargarrazi, L. Lanni, and C.-M. Zetterling, “Design and characterization of 500 °C Schmitt trigger in 4H-SiC,” in *Mater. Sci. Forum*, vol. 821, 2015, pp. 897–901.

[15] S. Kargarrazi, L. Lanni, S. Saggini, A. Rusu, and C. M. Zetterling, “500 °C Bipolar SiC Linear Voltage Regulator,” *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1953–1957, Jun. 2015.

[16] S. Kargarrazi, L. Lanni, and C. M. Zetterling, “A study on positive -feedback configuration of a bipolar SiC high temperature operational amplifier,” *Solid-State Electron.*, vol. 116, pp. 33–37, 2016. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110115003470

[17] Y. Tian, R. Hedayati, and C. M. Zetterling, “SiC BJT Compact DC Model With Continuous- Temperature Scalability From 300 to 773 K,” *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3588–3594, Sep. 2017.

[18] S. Kargarrazi, “High temperature bipolar SiC power integrated circuits,” Ph.D. dissertation, School Inf. Commun. Technol., KTH Roy. Inst. Technol., Stockholm, Sweden, 2017. [Online]. Available: http://urn.kb.se/resolve?urn=urn:nbn:se:kth:diva-201618

[19] M. H. Weng *et al.*, “Recent advance in high manufacturing readiness level and high temperature CMOS mixed-signal integrated circuits on silicon carbide,” *Semicond. Sci. Technol.*, vol. 32, no. 5, 2017, Art. no. 054003. [Online]. Available: http://stacks.iop.org/0268-1242/32/i=5/a=054003

[20] J. Colmenares, S. Kargarrazi, H. Elahipanah, H. P. Nee, and C. M. Zetterling, “High-temperature passive components for extreme environments,” in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl.*, Nov. 2016, pp. 271–274.

[21] H. Elahipanah, S. Kargarrazi, A. Salemi, M. Östling, and C. M. Zetterling, “500 °C High current 4H-SiC lateral BJTs for high-temperature integrated circuits,” *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1429–1432, Oct. 2017.

[22] S. Kargarrazi, H. Elahipanah, S. Rodriguez, and C. M. Zetterling, “500 °C, High current linear voltage regulator in 4H-SiC BJT technology,” *IEEE Electron Device Lett.*, vol. 39, no. 4, pp. 548–551, Apr. 2018.

[23] Navitas Semiconductor, 2018. [Online]. Available: https://www.navitassemi.com/

[24] A. M. H. Kwan, Y. Guan, X. Liu, and K. J. Chen, “Integrated over-temperature protection circuit for GaN smart power ICs,” *Japanese J. Appl. Physics*, vol. 52, no. 8S, 2013, Art. no. 08JN15. [Online]. Available: http://stacks.iop.org/1347-4065/52/i=8S/a=08JN15

[25] K. Y. Wong, W. Chen, and K. J. Chen, “Integrated voltage reference and comparator circuits for GaN smart power chip technology,” in *Proc. 21st Int. Symp. Power Semicond. Devices IC’s*, Jun. 2009, pp. 57–60.

[26] X. Liu and K. J. Chen, “GaN single-polarity power supply bootstrapped comparator for high-temperature electronics,” *IEEE Electron Device Lett.*, vol. 32, no. 1, pp. 27–29, Jan. 2011.

[27] S. Kargarrazi, L. Lanni, A. Rusu, and C. M. Zetterling, “A monolithic SiC drive circuit for SiC Power BJTs,” in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices IC’s*, May 2015, pp. 285–288.

[28] H. Wang, A. M. H. Kwan, Q. Jiang, and K. J. Chen, “A GaN pulse width modulation integrated circuit for gan power converters,” *IEEE Trans. Electron Devices*, vol. 62, no. 4, pp. 1143–1149, Apr. 2015.

[29] S. Roy *et al.*, “A SiC CMOS digitally controlled PWM generator for high-temperature applications,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8364–8372, Oct. 2017.

[30] L. Lanni, R. Ghandi, B. Malm, C.-M. Zetterling, and M. Östling, “Design and characterization of high-temperature ECL-based bipolar integrated circuits in 4H-SiC,” *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1076–1083, Apr. 2012.

[31] C. Yuan, L. Xinquan, and D. Hanxiao, “Ultra-low startup voltage low output ripple high-efficiency hysteretic current mode step-up DC-DC converter,” *IET Power Electron.*, vol. 8, no. 7, pp. 1238–1245, 2015.