Ultralow Input–Output Capacitance PCB-Embedded Dual-Output Gate-Drive Power Supply for 650 V GaN-Based Half-Bridges

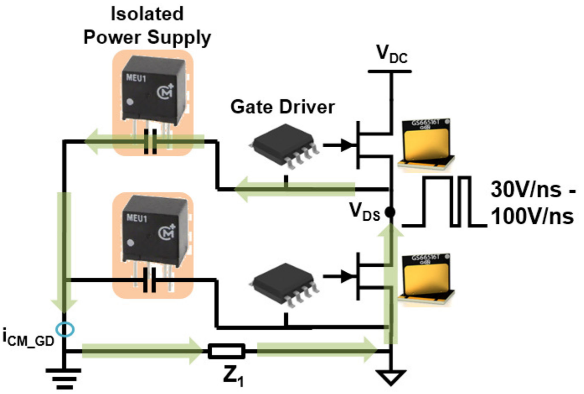
Bingyao Sun, *Student Member, IEEE*, Rolando Burgos, *Member, IEEE*, and Dushan Boroyevich, *Fellow, IEEE*

***Abstract*—Wide-bandgap devices have been widely used to reduce the size and increase the efficiency of power converters by operating at a high switching frequency, at the expense of heightened radiated and conducted electromagnetic inference (EMI) emissions, of which the latter circulates through the power loop and ancillary circuitry. In effect, the parasitic isolation capacitance C_i of the gate-driver power supply represents a key EMI propagation path to be controlled in order to ensure the operational integrity of power converters. To this end, this paper proposes an integrated, dual-output gate-drive power supply for gallium-nitride (GaN) 650 V, 60 A, half-bridge phase legs, rated at 2 W (2 × 1 W), 15 to 2 × 7 V, featuring an ultralow C_i of 1.6 pF, an output-to-output parasitic capacitance of 1.6 pF, a power density of 72 W/in^3, and an efficiency of 85%. All this is attained using an active-clamp flyback converter switching at 1 MHz using 65 V GaN high-electron-mobility transistor devices and Schottky output rectifiers, and a Pareto-optimized transformer design minimizing its interwinding capacitances, volume, and losses. Finally, the transformer is fully embedded in a printed circuit board (PCB) material, doubling as a substrate for the topside active layer of the power supply. The paper presents the complete design procedure, processing, and experimental demonstration of the proposed integrated power supply, evaluating as well the reliability impact of the magnetic-PCB material interface in high ambient temperature applications ($>$200 °C).**

***Index Terms*—Gate drive, gallium nitride (GaN), isolation capacitor, power supply, printed-circuit-board (PCB)-embedded.**

I. INTRODUCTION

WIDE-BANDGAP (WBG) devices, like silicon-carbide (SiC) metal-oxide semiconductor field-effect transistors and gallium-nitride (GaN) high-electron-mobility transistors (HEMTs), have been increasingly used in power converters for numerous applications. Thanks to their distinct advantages over silicon (Si) devices, such as faster switching speed, lower switching loss, and higher switching frequency, converters based on WBG devices achieve higher efficiency and higher power



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The authors are with the Center for Power Electronics Systems, Bradley Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061 USA (e-mail:

TABLE I
STATE-OF-THE-ART 2 W ISOLATED POWER SUPPLY CHARACTERISTICS

Reference	**[7]**	**[8]**	**[9]**	**[10]**	**[11]**
Part No.	Ampere Lab	SC02S1205A	MEJ2S0509SC	R05P205S	LTM8068
Output No.	2	1	1	1	1
Switching frequency /Hz	1.2M	80k	45k	50k	250k
Isolation capacitance /pF	0.9	15	4	1.5 ~ 10	13.5
Efficiency	75%	82%	76%	73%	70%
Size/mm	23 x18 x2.8	19.6x10.5x7.2	19.6 x12.6x10	19.5 x12.5x9.8	11.3 x9 x4.9
Power density/ W/in^3	26.7	22.11	13.2	13.7	59
Isolation voltage	--	1kVdc	5.2kVdc	6.4kVdc	2kVac
Temperature/℃	200	100	85	95	125

(input-output) capacitances in the gate-driver power supply, showing how this conducted CM emission could distort the output of the gate-driver power supply and gate-drive [6]. Accordingly, to protect the gate-driver from the increased EMI emission, a small isolation capacitance is necessary to attenuate the EMI emission within the gate-driver loop [4]–[6].

Generally, in order to have a small isolation capacitance in the isolated power supply, the distance between the primary and secondary sides of the transformer in question should be as large as possible. As a result, the power supply would suffer from low power density. Table I lists the isolation capacitance, the typical efficiency, and the volume of 2 W state-of-the-art isolated power supplies recently developed at universities and industry. The input voltages of the listed converters range from 5 to 15 V, and the output voltages are within 5–7 V. In Table I, [7] has an ultralow isolation capacitance, but also a large volume or a low power density with a high switching frequency. From the comparison among [8]–[11], it is found that the power supplies with isolation capacitances smaller than 10 pF have a power density less than 13.7 W/in^3. This represents one of the key challenges tackled in this work; namely, how to minimize the effect of this tradeoff to attain both an ultralow isolation capacitance and high power density in gate-drive power supplies for GaN power semiconductors.

Besides the above-mentioned tradeoff, efficiency is also a key design variable affected by the power supply volume. For instance, though [8] achieved a higher efficiency than [11], while both featured comparable isolation capacitances, the former had a larger volume than the latter. In general, to achieve high efficiency and simultaneously high power density, high switching frequency operation is essential in order to reduce the size, and consequently the losses, of all passive components. Then, to counteract the resultant increase in losses due to the higher switching frequency operation, a soft-switching technique can be adopted, at the expense of a limited selection of power converter topologies. Consequently, all these tradeoffs must be judiciously handled throughout the entire design process.

Further, the printed-circuit-board (PCB)-embedded technique has been demonstrated to be an effective way to increase the integration level of power converters. PCB is a widely used and low-cost substrate in the converter design, which can be manufactured based on a standard lamination process. Thanks to it, the converter can be fabricated following an automated and high-volume production process. Though the PCB is thin, there is still space to embed some components seeking to reduce the total converter size. As an example, a transformer with an air core was implemented into a PCB in [12] for a 27.14 MHz resonant *LLC*-type converter. In [13] and [14], a low-temperature cofired ceramic inductor was embedded into a PCB, which also doubled as a substrate for a point-of-load converter, increasing the power density to 800 W/in^3. A comparative 2 W gate-driver power supply design in [7] and [15] succeeded embedding the UI-shape magnetic ferrite core and copper-trace windings into the PCB, which verified the feasibility of building a complex transformer structure within a PCB using a standard lamination process. Furthermore, the dies of the Si insulated-gate bipolar transistor and diode were also embedded into a PCB in [16] and [17]. It was found in [16] that the thermal resistance of the PCB-embedded devices was reduced by 30–44% compared with the traditional method and the insulation strength of the PCB-embedded module could be as high as 41–50 kVrms/mm. Studies in [17] explained the detailed die-embedding process. In [18], an investigation concerning the failure of PCB-embedded electrical components and electronics was presented, analyzing and predicting the main phenomenon observed, namely, the crack initiation propagation within the PCB-embedded structure. Finally, seeking to extend the application range of the isolated power supply, Studies in [15] evaluated the feasibility of operating at ambient temperatures of up to 200 °C, focusing on possible reliability effects of the PCB-embedded transformer. Along these lines, a novel PCB-embedded transformer structure is investigated in this paper seeking to achieve the maximum possible power density for the gate-driver power supply at hand.

In this paper, a gate-drive power supply is designed for 650 V, GaN HEMT devices in a half-bridge configuration. Accordingly, the power supply features two isolated 7 V, 1 W outputs, feeding from a 15 V input bus. The main challenge, as described, is to find simultaneously an appropriate design approach to achieve maximum power density, minimum isolation capacitance, and high efficiency. Accordingly, a PCB-embedded transformer structure is proposed to fully utilize the PCB substrate, whose dimensions are optimized to achieve a small transformer loss, isolation capacitance, and volume. GaN devices from EPC are selected, switching at 1 MHz. To eliminate turn-on loss to ensure high efficiency, the topology with the zero voltage switching (ZVS) is adopted. Furthermore, the transformer operation at high temperature is evaluated conducting thermal cycling test

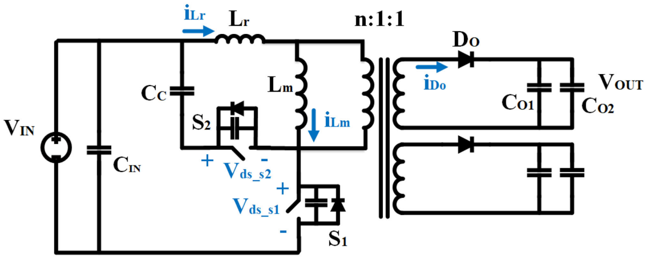


Fig. 2. Active-clamp flyback topology.

TABLE II
TOPOLOGY COMPARISON SUMMARY

	Flyback	**Active-clamp flyback**	**LLC (center-type)**
Primary switch No.	1	2	2
Secondary diode No.	2	2	4
Winding No.	3	3	5
Simulated Efficiency	69%	88%	90%

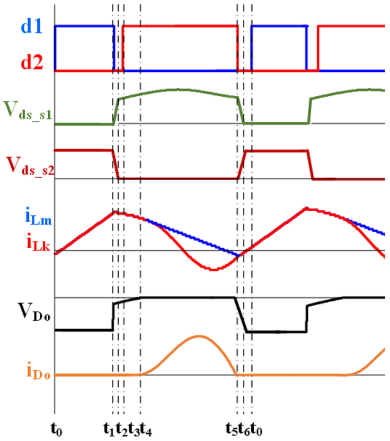


Fig. 3. Resonant operation mode in active-clamp flyback.

at 200 °C, showing the benefits of using high-temperature-rated PCB materials.

To design the targeted gate-driver power supply, the paper presents first the circuit design, including the topology selection, operation mode analysis, and active and passive component selections. The design optimization of the PCB-embedded transformer is then presented, including the core and PCB material selection. Based on the optimized dimensions, the transformer is built, and the fabrication process, including the standard lamination procedure and converter assembly, is presented. The transformer and the converter hardware are then characterized, showing the results of experimental tests conducted to verify the efficiency, isolation voltage, isolation capacitance, total volume, and the impact of high-temperature operation.

II. CIRCUIT DESIGN

A. Topology Selection

As the work presented targeted isolated dc–dc conversion at very low power with high power density, the topology candidates had to be simple and fairly efficient under the high switching frequency, such as the classic flyback, active-clamp flyback, and *LLC* resonant converters. Before the selection, one fact had to be taken into consideration that the leakage inductance in the proposed PCB-embedded transformer structure was found to be around 50% of the magnetizing inductance. This was found in the finite element analysis (FEA) numerical calculations and verified later on by hardware measurements.

Accordingly, if the classic flyback topology were selected, a critical current mode (CRM) should be used to achieve soft turn-on of the main switch [19]; however, when the main switch turns off, the large leakage inductor induces a large turn-off voltage overshoot, resulting in a high turn-off loss when operating at the high switching frequency. Also, the output diodes cannot turn off with zero current in the classic flyback. To solve these issues, the active-clamp flyback converter adds a clamp capacitor and a series switch, as shown in Fig. 2, effectively clamping the voltage of the main switch S_1 and avoiding the large turn-off voltage overshoot. The clamp capacitor C_C role is to collect the leakage inductor L_r energy and release it to the secondary side while inducing a resonance with L_r and the magnetizing inductor L_m. Thanks to this resonant operation [20]–[23], S_1 and S_2 have ZVS, and the secondary diodes achieve zero-current switching (ZCS). In the simulation with the same switching devices, the active-clamp flyback had an 88% estimated efficiency, which was 19% higher than the classic flyback. The *LLC* resonant converter is another option for the high-efficiency dc–dc converter design, which attained a 90% estimated efficiency in simulation at full power. However, with the center-type secondary side, the two isolated outputs require four diodes and five transformer windings (one primary and four secondary windings), increasing the transformer volume significantly. If the full bridge is selected for the secondary sides, there are three transformer windings required with the eight diodes, leading to a large footprint of the circuit layer. All aforementioned are summarized in Table II. In conclusion, the active-clamp flyback was finally selected thanks to its simple topology, relatively high efficiency, and small transformer size as it will be demonstrated.

B. Resonant Operating Mode

In order to perform soft switching in the active-clamp flyback, the resonant operating mode was explained in detail in [20] and [21] and is illustrated in Fig. 3. According to [20], the transformer first works in the CRM. Before S_1 turns on at t_0, the negative current in the magnetizing inductor can discharge the S_1 junction capacitor during t_5–t_6, with which the soft turn-on of S_1 is achieved. When S_1 is turned off at t_1, L_r and L_m discharge the junction capacitor of S_2 during t_1–t_2, before it turns on at t_3, with which S_2 achieves zero-voltage turn-on. During t_2–t_5, C_C resonates with L_m and L_r before t_4, and solely with L_r after t_4. At the instant that S_2 turns off at t_5, L_r has almost the same current as L_m and the secondary-side

TABLE III
S_1 CANDIDATE LOSS ESTIMATION

Part Number	**Vds /V**	**Rds(on) /mΩ**	**Id /A**	**Qoss/ nC**	**Loss/mW**		
					Conduction	***Turn-off***	***Total***
EPC2020	60	2	60	50	0.84	372.41	373.26
EPC8009	65	130	2.7	0.94	54.76	8.34	63.09
EPC8002	65	530	2	0.344	223.24	2.16	225.40
EPC2021	80	2.5	60	63	1.05	496.55	497.61

current is almost zero. As a result, the secondary-side diodes achieve zero-current turn-off.

According to the circuit analysis in [20], the negative magnetizing inductor current $|i_{Lr}(t_5)|$, at the moment S_2 turns off, was calculated with (1) to be smaller than –0.2 A in order for S_1 to achieve ZVS, where $C_{S1/2}$, t_{DT}, *n*, V_{IN}, and V_{OUT} are, respectively, the junction capacitor of S_1 and S_2, the dead time between S_1 and S_2, the turns ratio of the transformer, the input voltage, and the output voltage. In (1), $C_{S1/2}$ is estimated as 20 pF, t_{DT} takes 25 ns, and *n* is 1. If the turns ratio *n* is larger than 1, the corresponding $|i_{Lr}(t_5)|$ is smaller than 0.2 A so that "$|i_{Lr}(t_5)| = 0.2$ A" is also an appropriate estimation for *n* larger than 1.

The corresponding maximum magnetizing inductance L_m needed was calculated to be 6 μH according to (2) [20], where L_r, L_m, *P*, *D*, and *f* are, respectively, the leakage inductance, the magnetizing inductance, the total output power, the duty ratio, and the switching frequency. The switching frequency of the design was fixed to 1 MHz due to the high temperature limits of the switch module from [7]

$$|i_{Lr}(t_5)| \geq 2C_{S1/2}\frac{V_{\mathrm{IN}}+\frac{V_{\mathrm{OUT}}}{n}}{t_{\mathrm{DT}}} \tag{1}$$

$$L_m = \frac{V_{\mathrm{IN}}\frac{D^2}{f^2} - 2L_r\left(\frac{P}{V_{\mathrm{IN}}f}+|i_{Lr}(t_5)|\frac{D}{f}\right)}{\left(\frac{P}{V_{\mathrm{IN}}f}+|i_{Lr}(t_5)|\frac{D}{f}\right)}. \tag{2}$$

According to (1) and (2), the magnetizing inductance should be smaller than 6 μH. The clamp capacitor can be selected after the leakage inductance is finalized after the transformer fabrication. If L_r is around 2 μH, the clamp capacitor can be selected to be 10 nF in order to achieve ZCS for the diodes.

C. Active Component Selection

With the selected L_m and C_C, the two switches S_1 and S_2, and the output diodes can be selected based on the estimated rms current, the turn-off transient current and voltage, and the maximum voltage during the resonant operation.

In consideration of a small total switch loss, including the turn-off loss and conduction loss, S_1 and S_2 utilized EPC GaN devices. The maximum voltage of the two devices was simulated to be less than 30 V, considering there could be 1 nH power loop parasitic inductance. The devices with 60–80 V maximum junction voltage were selected. The estimated loss using the selected devices for S_1 is listed in Table III. From Table III, the device EPC8009 has the smallest total loss thanks to its small on-resistance and small output capacitor, compared with other candidates. To this end, EPC8009 was selected for S_1. A similar loss estimation was performed for S_2 and its results are summarized in Table IV, based on which the device EPC8009 was selected for S_2.

TABLE IV
S_2 CANDIDATE LOSS ESTIMATION

Part Number	**Vds /V**	**Rds(on) /mΩ**	**Id /A**	**Qoss/ nC**	**Loss/mW**		
					Conduction	***Turn-off***	***Total***
EPC2020	60	2	60	50	0.58	330.19	330.77
EPC8009	65	130	2.7	0.94	37.77	7.39	45.16
EPC8002	65	530	2	0.344	153.98	1.92	155.89

TABLE V
COMPONENT LIST

S_1	EPC8009	**C_c**	10 nF (0603)
S_2	EPC8009	**C_{o1}**	10 µF (0603)
D_o	STPS0560Z	**C_{o2}**	0.33 µF (0402)
Gate drive	LM5113	**C_{in}**	10 µF (0603)

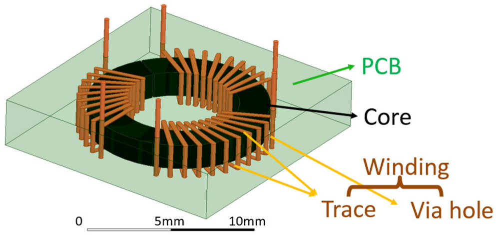


Fig. 4. PCB-embedded transformer structure illustration.

Furthermore, the Si Schottky diode STPS0560Z was selected as an output diode. The gate drives for S_1 and S_2 used the highly integrated chip LM5113, where the bootstrap circuit is embedded to drive the high-side switch S_2. The input and output capacitors were also selected based on the ripple requirements. The summary of the component selections is presented in Table V.

III. TRANSFORMER DESIGN AND OPTIMIZATION

A. PCB-Embedded Transformer Structure

The proposed transformer structure is shown in Figs. 4 and 5, where the toroidal core is shown in black color and the three windings—one primary and two secondary sides—are wound around the core symmetrically. The top and bottom sides of the windings are laid out as PCB traces, whereas the vertical connection between the top and bottom turns is constructed using vias. There are six vias with longer length above the transformer, which are used to connect the transformer to the circuit layer. The material surrounding the transformer is the PCB. In order to increase the isolation voltage among the windings, PCB material covers the top and bottom PCB traces as well, which is

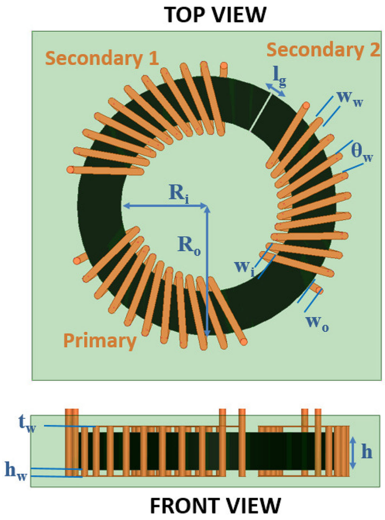


Fig. 5. Top and front view of the PCB-embedded transformer.

TABLE VI
DIMENSIONS OF THE PCB-EMBEDDED TRANSFORMER

	Description	Optimized Value
R_i/mm	Core inner radius	3.7
R_o/mm	Core outer radius	5.65
h/mm	Core thickness	1.8
l_g/mm	Air gap width	0.1
w_w/mm	Turn width	0.2
w_i/mm	Space between winding and core at inner circle	0.5
w_o/mm	Space between winding and core at outer circle	0.5
h_w/mm	Space between winding and core in the vertical direction	0.1
ϑ_w/degree	Angle between turns	2.86
t_w/mm	Winding copper thickness	0.0343
N	Turn number	10

illustrated clearly in the front view of Fig. 5. The air gap locates in the middle of the two secondary windings, as shown in the top view of Fig. 5. This ensures the symmetric inductance and the balanced output voltage for the two output channels. Besides, the air gap is placed far from the windings to avoid any fringing effect and reduce the ac winding loss. In the structure, only one air gap is allowed because two or more air gaps would separate the core into several pieces. This multipiece core structure would require the precise horizontal alignment of the pieces during the lamination process, complicating the manufacturing process significantly.

In addition, the leakage inductance of the transformer would increase even more exceedingly the already high 50% of the total inductance. The large leakage is the result of the loose structure of the windings. For example, the part of the magnetic flux generated by the outer via-holes goes into the surrounding PCB material, instead of circulating in the core. If there is a need to reduce the leakage inductance, the winding structure would have to be changed, for instance, flat and wide traces instead of the wire-type traces. The leakage value here, however, is not a problem. On the contrary, it is needed to ensure soft switching for S_1 for all operating condition.

In terms of the core material selection, the core material chosen is P61 from ACME, whose Curie temperature is 280 °C and the core loss coefficient is 150 kW/m^3 at 50 mT, 100 °C, 1 MHz. The core loss coefficient of P61 is lower compared with other commercial MnZn ferrite materials [23]. The highest temperature during the standard PCB lamination process is 190 °C, and the highest operating temperature is 200 °C, both of which are safely within the capabilities of the material in question, eliminating the risk of possibly affecting its magnetic properties.

Two different PCB materials were selected, one for standard temperature range applications (<100 °C) and one for 200 °C applications. FR4 is a low-cost commonly used PCB material suitable for the first case, and as such was selected to test with the structure in room temperature. However, at 200 °C, FR4 has delamination problems. The coefficient of thermal expansion (CTE) of FR4 is 70 ppm/°C, large enough that it could break the ferrite core at 200 °C. To this end, MEGTRON2 (R-1577) from Panasonic is a better option to build the high-temperature version, which has a smaller CTE of 34 ppm/°C.

The winding trace material is copper, whose thickness can be selected either 1 or 2 oz. Copper of 2 oz can reduce the winding conduction loss thanks to a smaller dc resistance; however, it increases the clearance distance between two turns. Copper clearance of 1 oz is 10 mils (0.254 mm) according to the PCB manufacture requirements, and 2 oz clearance is twice of that of 1 oz. Assuming ten turns are used in one winding, 2 oz copper has at least 100 mils (2.54 mm) wider windings than those of 1 oz copper. If the core size is fixed, a wider winding leads to a larger isolation capacitance due to the closer distance between the windings. If the same isolation capacitance is expected, the core with 2 oz copper winding should accordingly have a larger radius than that with 1 oz copper winding. As a result, in the consideration of the minimum transformer volume and isolation capacitance, 1 oz copper is preferred. Accordingly, the thickness of the copper trace t_w was fixed to be 0.0356 mm.

The parameters defining the winding and core dimensions are illustrated in Fig. 5 and are described in Table VI. Specifically, the core has four dimensions: the inner radius R_i, the outer radius R_o, the thickness h, and the air gap length l_g. As for the windings, the trace width w_w, thickness t_w, the turn number N, and the angles between two turns θ_w are used to describe them. The angles between two turns θ_w is directly related to the clearance distance between the neighbor inner vias w_m, the inner radius of the core R_i, and the via diameter w_w, as shown in (3). In order to quantify the space between the winding and the core, h_w, w_o, and w_i describe, respectively, the space from the core to the top or bottom layer copper trace, to the inner via-holes, and to the outer via-hole. These three parameters are limited by the PCB manufacturing ability. If w_i and w_o are too small, the via-holes may hit and break the core during the fabrication. On the contrary, large w_i and w_o result in a large leakage inductance for the transformer. h_w is fixed due to the smallest PCB laminate layer thickness of the selected PCB material. In this design, w_i and w_o were fixed to be 0.5 mm, and h_w was fixed to be 0.1 mm

$$\theta_w = \arctan\left(\frac{w_m/2}{R_i - w_i - w_w/2}\right). \tag{3}$$

B. Transformer Model and Optimization

There are three targets the transformer optimization focuses on: the transformer volume V, the transformer loss P_t, and the isolation capacitance C_i. To perform the optimization, there are three steps. The first step is to define the optimized parameters and their varying range. Then, the models are constructed describing the relationship between the targets and the optimized parameters. Based on the models, a Pareto surface is plotted to illustrate the relationships among the three targets. One design point on the Pareto optimal-solution surface satisfying all three characteristics is finally picked as the optimized transformer design.

The optimized parameters include R_i, R_o, h, l_g, w_w, and N. To ensure enough space for the circuit on the transformer substrate, R_o was set to be larger than 4 mm; h was set to be smaller than 2.5 mm because a thick PCB may suffer from delamination issues; and l_g was limited by the core saturation flux density and L_m.

The models describing the relationship among the target V, P_t, C_i, and the optimized parameters were built. V was calculated using (4). P_t was separated into the core loss P_{core} and winding loss P_{winding}; the core loss was estimated with (5), where $(\text{FWC})_{\text{sq}}$ is the flux waveform coefficient and is approximately $\pi/4$ in this case [24]. The core loss coefficient P_v in (5) is provided by the magnetic manufacturer. The winding loss was calculated using (6), where R_{dc} was calculated based on the winding length and width using (7). $I_{p\text{-rms}}$ and $I_{s\text{-rms}}$ in (6) are the rms current of the transformer primary and secondary sides, respectively. The ac winding loss was hard to estimate here given that the magnetic field around the turns was very complex and hard to calculate. FEA calculations were used instead to estimate a close value for R_{ac}, which in this case was $0.4R_{\text{dc}}$

$$V = (2(R_o + w_o + w_w))^2(2h_w + h) \tag{4}$$

$$P_{\text{core}} = (\text{FWC})_{\text{sq}} P_v V \tag{5}$$

$$P_{\text{winding}} = \left(I^2_{p-\text{rms}} + 2I^2_{s-\text{rms}}\right)(R_{\text{dc}} + R_{\text{ac}}) \tag{6}$$

$$\begin{aligned} l_{\text{winding1}} &= 2N(R_o - R_i + w_i + w_o) \\ S_{\text{Cu1}} &= t_w w_w \\ l_{\text{winding2}} &= 2N(h + 2h_w) \\ S_{\text{Cu2}} &= \pi\left(\frac{w_w}{2}\right)^2 \\ R_{\text{dc}} &= \rho_{\text{Cu}}\left(\frac{l_{\text{winding1}}}{S_{\text{Cu1}}} + \frac{l_{\text{winding2}}}{S_{\text{Cu2}}}\right). \end{aligned} \tag{7}$$

The isolation capacitance model is very complex to build due to its dependence on the large number of variables. To simplify the models, the isolation capacitance was separated into two parts: C_{w-w}, the winding-to-winding capacitance, assuming there is no core, and C_{w-c-w}, the equivalent capacitance from the winding to the core, and then from the core to the winding, as illustrated in Fig. 6. Each kind of capacitance was analyzed using Q3D simulations. If there are only two windings in the PCB material and no core, C_{w-w} is mostly dependent on the shortest distance between the windings and the facing surface area. The curve-fitting method was used to get C_{w-w}. C_{w-c} was estimated by calculating the winding surface area, and the distance from the winding to the core, as (8) shows. R_c in Fig. 6 is the resistance of the core between the two windings. Then, the equivalent isolation capacitance C_i can be calculated according to the equivalent circuit in Fig. 6.

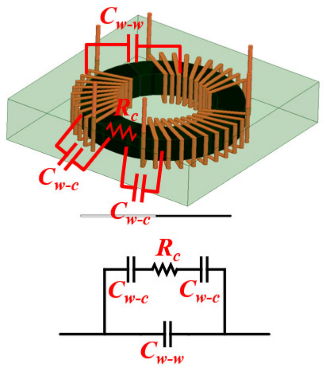


Fig. 6. Isolation capacitance illustration in the structure.

$$C_{w-c} = C_{c-w} = \varepsilon_{\text{PCB}}\left(\frac{l_{\text{winding1}} w_w}{h_w} + \frac{l_{\text{winding2}} w_w}{w_i}\right). \tag{8}$$

The error of the transformer C_i model between the simulation and the practical measurement was 0.5 pF. This extra 0.5 pF may be the result of the extra measurement cable connected on the power supply and the circuit layer on the transformer substrate.

C. Optimization Results

With the models described, the optimization process was implemented in the optimization software CADES. To get a Pareto surface among P_t, V, and C_i, there are three steps in the software. The software first finds the solutions of the transformer dimensions to the given V and C_i. The second step is to find the solution, which comes up with the smallest P_t among the first-step results. This solution is marked as the best design with the given V and C_i. The final step in the software is to sweep values of V and C_i and to find the best design points for each V and C_i combination. The output of the software is plotted in Fig. 7.

As observed in Fig. 7, when V comes smaller with a fixed C_i, the transformer loss increases because the maximum flux density increases when the core size reduces. It is also concluded from the surface that when the volume is fixed, the larger the isolation capacitance, the smaller the loss. This is caused by the winding width variation. In effect, when the winding width is larger, the winding resistance reduces and with it its associated loss. However, with wider-trace windings on a fixed core, the

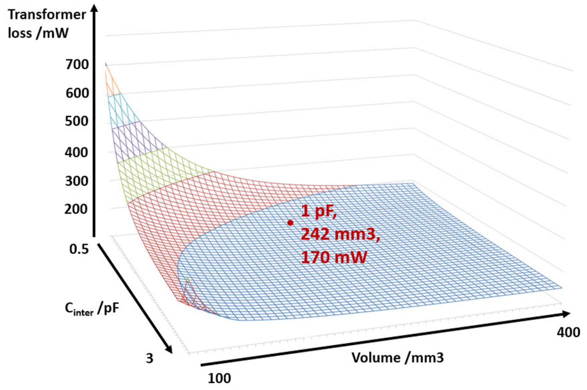


Fig. 7. Pareto surface within loss, isolation capacitance, and volume for the transformer design.

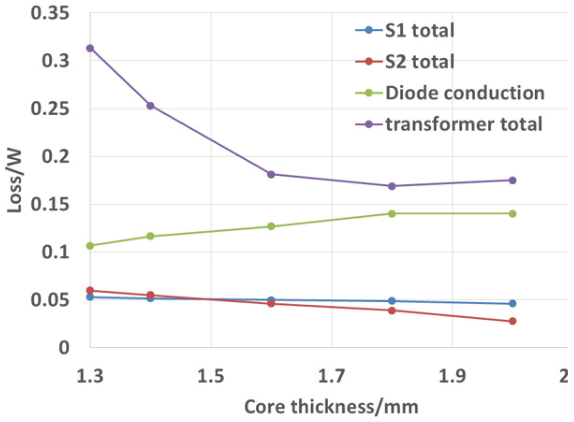


Fig. 8. Loss analysis for different h, with 1 MHz switching frequency.

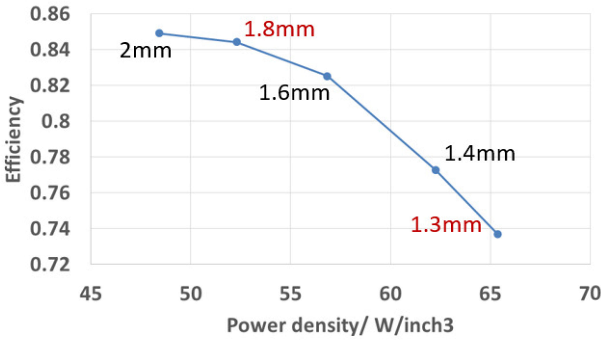


Fig. 9. Efficiency estimation versus power density for different h, with 1 MHz switching frequency.

distance between the windings diminishes and the facing area is larger, yielding a larger isolation capacitance. On the Pareto surface, one design with estimated 1 pF isolation capacitance, 170 mW transformer loss with the size of 242 mm^3 was selected to fabricate and test. The optimized dimensions are listed in Table VI.

With the selected design point, the magnetizing inductance L_m is 3.7 μH. With a 1.8-mm-thick core, an 84% efficiency was expected. Almost half of the total loss was dissipated on the transformer, with the diodes taking 30% of the total loss. To verify the design point, several detailed designs were then investigated around the 1.8 mm thickness case. Figs. 8 and 9 show the loss breakdown and the estimated efficiency for a core thickness varying from 1.3 to 2 mm, whose inner and outer radius was the same as the value shown in Table VI. When the core thickness increases, the cross-sectional area of the toroidal core becomes larger and therefore the core loss reduces. With a fixed turn number $N = 10$ and a fixed air gap $l_g = 0.1$ mm, the magnetizing inductance increases as well, so the rms and the turn-off current magnitudes of the switches reduce, in turn reducing the conduction and turn-off switching losses. As a penalty of the reduced loss, the volume of the PCB containing the transformer increases, decreasing the overall power density of the converter.

IV. TRANSFORMER FABRICATION AND CONVERTER ASSEMBLY

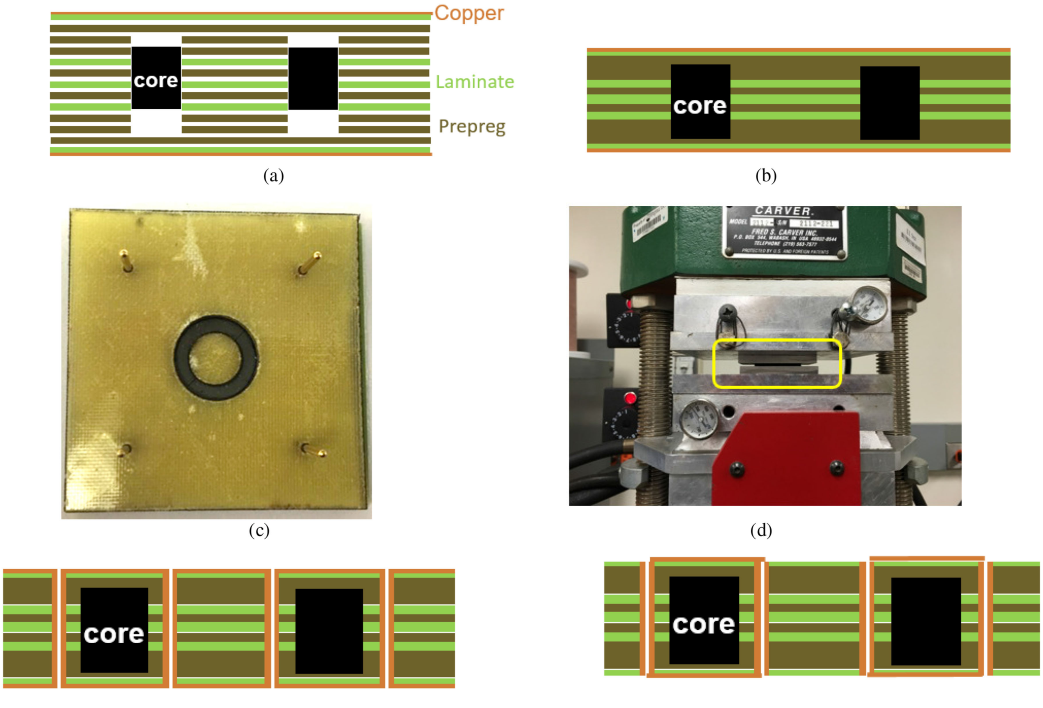
With the design parameters listed in Table VI, the PCB-embedded transformer was constructed based on a standard PCB lamination process. To compare the selected design featuring 1.8 mm thickness, another sample with a 1.3 mm thick core was built as well. Afterward, the converter was built by connecting the transformer and the circuit layers undergoing one more lamination step.

A. *Embedding of Transformer Core*

To connect several laminate layers with copper into one board, a PCB lamination process is carried out. In the dual-stage pressure cycle, the prepreg material is melted to connect the laminate layers, and the air within the layers is extracted. In order to embed the magnetic core within the PCB material, before the dual-stage pressure cycle, the laminate and prepreg material are first cut with the shape of the core, and the core is put into the "sandwiched" layer stack composed of the laminate and prepreg material. These steps are illustrated in Fig. 10(a). The middle layers of the laminate material should have similar thickness as the core in order to relieve the vertical pressure on the core during the dual-stage pressure cycle. As the ferrite is easy to break under imbalanced pressure on the surface, it is better to put several prepreg layers between the middle laminate layers and the top and bottom laminate layers as a pressure buffer for compliance purposes. After the lamination, the core is fixed within the PCB material, as Fig. 10(b) shows. The air gap of the core is also filled with the prepreg material. The relative permeability of the prepreg material is almost the same as that of air, so the magnetic parameters of the transformer remain constant after lamination. Fig. 10(c) and (d) show one sample under the layer stack before lamination and during the lamination process.

B. *Winding Fabrication*

With the core embedded in the PCB, the transformer windings are fabricated around the core. First, the vias are constructed, as Fig. 10(e) shows. Then, the copper, except for the winding traces on the top and bottom layer, is removed. The resultant PCB is shown in Fig. 10(f). The constructed transformer is shown in Fig. 11, where the vias, the PCB traces, and the air gap are clearly seen. The finished thickness of the transformer in Fig. 11 is 2.1 mm. The primary magnetizing inductance is 3.7 μH and the leakage inductance is 1.7 μH.



(a) (b) (c) (d) (e) (f)

Fig. 10. (a) Layer stack before PCB lamination. (b) PCB after lamination. (c) One sample during layer stack before lamination. (d) One sample under dual-stage pressure cycle. (e) Via-hole construction after PCB lamination. (f) Winding construction.

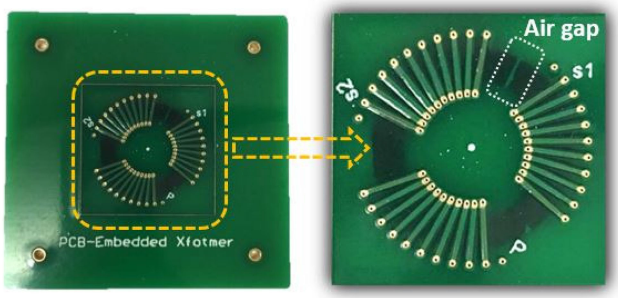


Fig. 11. PCB-embedded transformer.

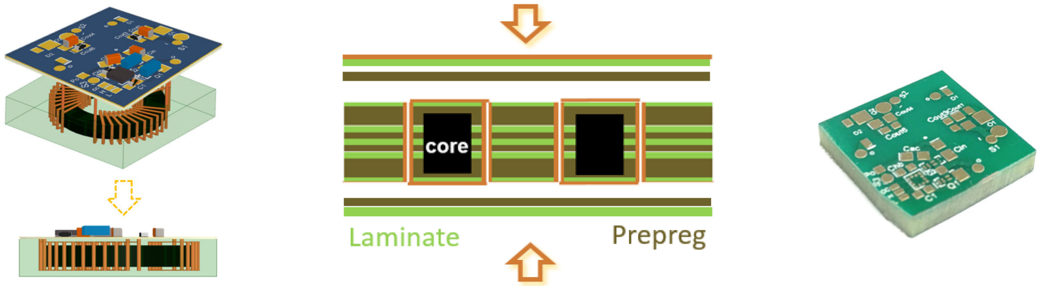
C. Converter Assembly

With the fabricated transformer, the circuit layer is connected to the transformer with a second lamination process, shown in Fig. 12(a) and (b). The six winding terminals can connect to the circuit layer by vias. In this way, the PCB-embedded transformer works as a substrate of the converter, rather than taking space on the circuit layer. The converter after assembly is shown in Fig. 12(c). It is seen in Fig. 12(b) that both the winding top and bottom traces are covered by the PCB material, which helps increase the isolation voltage among the three windings. Otherwise, the electrical breakdown through air may happen under high-voltage difference conditions between the input and the output side of the power supply. It is also suggested to coat the circuit with an insulation material to avoid the electrical breakdown along the converter surface.

The proposed PCB-embedded transformer structure and fabrication process can be applicable in other low-power isolated power converter design, with the similar leakage inductor requirement. The adoption of the high-power converter can be limited by the large size of the core, larger inductor or transformer loss, high temperature, and manufacture, which is more challenging. Furthermore, the Curie temperature of the magnetic material should be higher than the temperature used during the PCB lamination process. The discussion above is also applicable for other PCB-embedded transformer structures, like the planar core with PCB windings [15].

The steps to design a PCB-embedded transformer in the proposed structure for a given topology and working condition are summarized as follows.

1) Select devices based on loss estimation and determine the bounds for the magnetic inductance and leakage inductance.
2) Considering manufacturing limitations, design the winding structure, select PCB and core material.
3) Define dimensions to be optimized, set design targets, such as loss, efficiency, volume, power density, isolation capacitance, current ripple, etc.
4) Build model or equation between the optimized parameter and the targets, extract a Pareto-front or Pareto-surface.
5) With the selected design dimensions, fabricate transformer, including embedding core, constructing via-holes and winding traces.
6) Design the circuit layer and connect the circuit layer to the transformer.



(a) (b) (c)

Fig. 12. (a) Converter assembly with the transformer substrate. (b) PCB lamination to connect the transformer and the circuit. (c) Converter after the assembly.

TABLE VII
CHARACTERISTICS OF 2 W ISOLATED POWER SUPPLY WITH THE PCB-EMBEDDED TRANSFORMER

Sample No.	Core thickness/mm	Switching frequency /MHz	Efficiency	Volume /mm^3	Isolation capacitance /pF	Power density / W/in^3	Isolation voltage
1	1.3	1	73%	321	1.5	91.6	2kV AC >1min
2	1.8	1	85%	405	1.6	72	

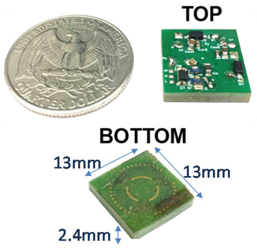


Fig. 13. Active-clamp flyback with the PCB-embedded transformer substrate.

V. EVALUATION OF THE GATE-DRIVE POWER SUPPLY

A. Electrical Characteristics

Based on the fabrication procedures mentioned above, the final converter hardware was built and shown in Fig. 13, whose characteristics are listed in Table VII. The total size of the converter with a 1.3-mm-thick core (sample 1) is 321 mm^3 (13 mm × 13 mm × 1.9 mm), and it is 405 mm^3 (13 mm × 13 mm × 2.4 mm) for sample 2, with a 1.8-mm-thick core. With 2 W output, the overall power density of the converter is 91.6 W/in^3 for sample 1 and 72 W/in^3 for sample 2. The isolation voltage between the windings was measured to be 2 kV at 60 Hz. After 5 min of high-voltage excitation, there was no partial discharge or breaking down phenomena observed. The isolation capacitance was measured to be 1.5 pF for sample 1 and 1.6 pF for sample 2. It is also found in the measurement that the capacitance between the two secondary windings was 1.5 pF in sample 1 and 1.6 pF in sample 2. These small capacitance values guarantee a negligible interference from the high-side gate driver to the low-side gate driver through the power supply. The overall efficiency of sample 2 with 2 W load was measured to be 85%. The thermal distribution of the circuit layer, shown in Fig. 14, under full load with 25 °C room temperature is illustrated in Fig. 15, where the GaN devices reach 41.1 °C and the diode temperature is 59.6 °C. The efficiency under different load condition was measured and is depicted in Fig. 16. When the load drops to

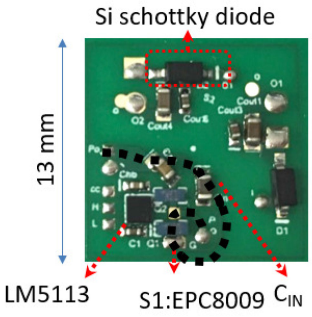


Fig. 14. Circuit layer and the power loop (black dashed line) when S_1 turns off.

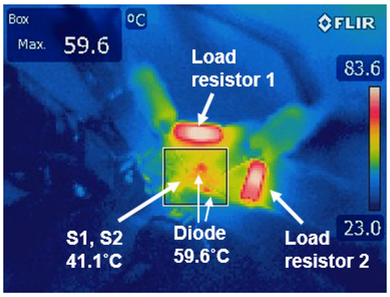


Fig. 15. Thermal distribution under full load.

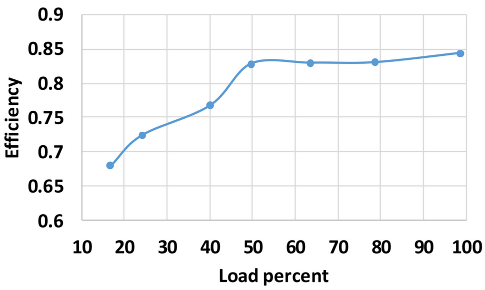


Fig. 16. Efficiency under different loads.

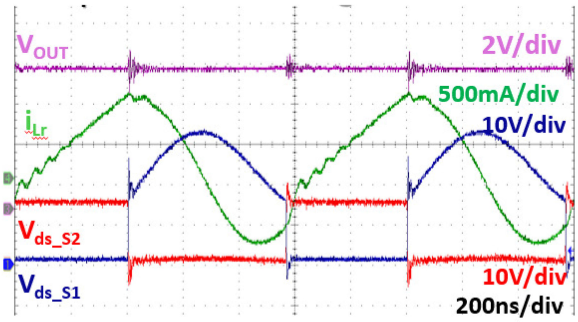


Fig. 17. Experimental waveforms of the gate-drive power supply with 1 MHz switching frequency and 2 W output power.

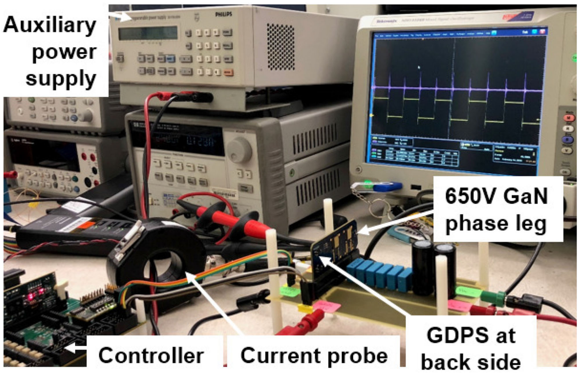


Fig. 18. Setup to measure $i_{\text{CM\_GD}}$ with 650 V GaN HMETs.

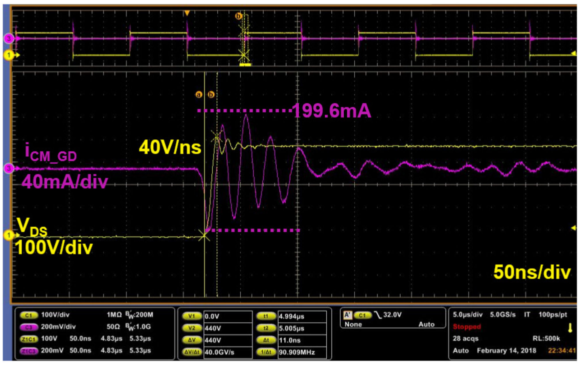


Fig. 19. Transient waveforms using MEJ2S0509SC.

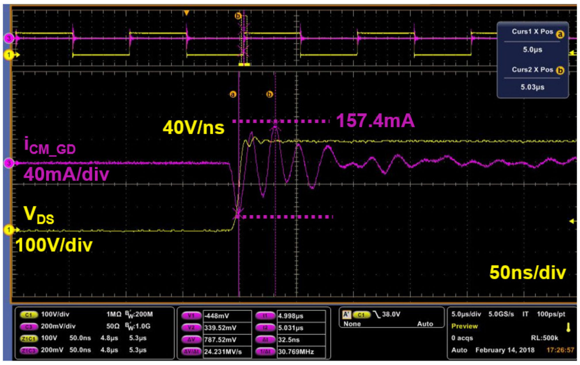


Fig. 20. Transient waveforms using the proposed gate-driver power supply.

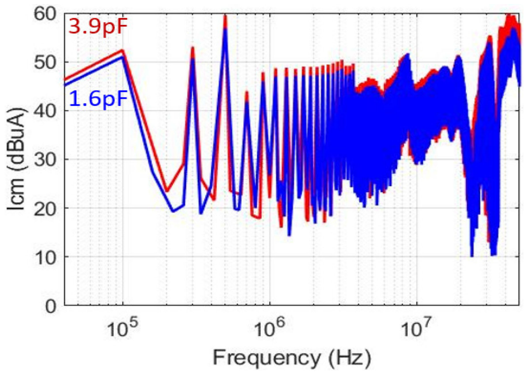


Fig. 21. $i_{\text{CM\_GD}}$ comparison using the proposed design and MEJ2S0509SC.

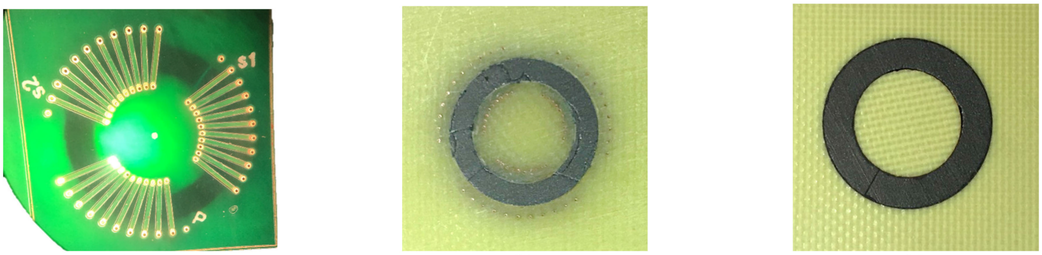
15% (0.3 W), the efficiency decreases to 68% and the duty cycle of S_1 needs to drop from 33% to 31% to maintain 7 V output voltage.

Finally, the pulsewidth modulation (PWM) gate signals of the converter were created by a function generator, as the PWM controller implementation was out of the immediate scope of this work. Nonetheless, the control circuitry was planned to be implemented on the bottom layer of the power supply shown in Fig. 13, minimizing the impact on the converter power density. Sufficient space was left for its implementation. One suitable controller for the design is UCC28780, an adaptive zero-voltage switching active-clamp flyback controller [26], whose maximum switching frequency is 1 MHz with peak-current mode control, soft-startup, and short-circuit protection. When the load current is zero, referring to the condition that the supported 650 V GaN HEMT does not switch, the controller enters in "standby power mode" to maintain the output voltage with minimum switching cycles [26].

Before the converter assembly, the circuit was tested with the PCB-embedded transformer connected by wires. In this way, the transformer current could be measured simultaneously with the drain–source voltage V_{ds} of S_1 and S_2, whose transient waveforms were captured in Fig. 17. The waveforms in Fig. 17 follow the same pattern as Fig. 3. In addition, there are some oscillations observed in the transformer primary-side current, which are caused by the oscillation between the diode junction capacitor and the transformer leakage inductor. When S_1 turns off, there is an obvious voltage overshoot, which is induced by the parasitic power loop inductance of the PCB layout. As the circuit is built on a single-layer PCB, the power loop between the primary transformer terminals is long, which is highlighted in Fig. 14 as the black dash line, and it introduces a large parasitic inductance. If a two-layer PCB is utilized for the circuit layer, the power loop inductance could be minimized at the expense of a total PCB thickness increase by 0.1–0.2 mm.

B. EMI Measurement

To verify the effect from the isolation capacitance on the EMI emission in the gate-driver loop, $i_{\text{CM\_GD}}$ highlighted in Fig. 1 was measured with the designed power supply and the state-of-the-art power supply MEJ2S0509SC [9]. Typical gate-driver power supplies with reinforced solution have an isolation capacitance in the 10 pF. MEJ2S0509SC with 4 pF is unique in the market.



(a) (b) (c)

Fig. 22. (a) FR sample image before the thermal cycling test. (b) FR4 sample image after the thermal cycling test. (c) MEGTRON 2 sample image after the thermal cycling test.

To drive two HEMTs in a phase leg, two MEJ2S0509SC are adopted. The experimental setup is shown in Fig. 18. One phase leg with 650 V, 60 A GaN HEMTs is switching with 100 kHz 50% duty cycle, with no load and 400 V input voltage. The drain–source voltage of the low-side HEMT V_{DS} was captured by a high-voltage differential probe. The CM current within the gate-driver loop $i_{\mathrm{CM\_GD}}$ was measured by a 100 MHz high-bandwidth current probe.

Fig. 19 shows the transient waveforms of V_{DS} and $i_{\mathrm{CM\_GD}}$ using MEJ2S0509SC. *dv/dt* of the 650 V GaN HEMTs is 40 V/ns during turn-off, generating the CM emission $i_{\mathrm{CM\_GD}}$ with a 199.6 mA magnitude in the gate-driver loops. With the replacement by the proposed power supply, $i_{\mathrm{CM\_GD}}$ magnitude is reduced to 157.4 mA, corresponding to a 27% reduction in CM current, depicted in Fig. 20. The spectra of $i_{\mathrm{CM\_GD}}$ in the two experiments are plotted and compared in Fig. 21. It is found that the conducted EMI emission in the gate-driver loop is reduced by 3 dB from 100 kHz to 10 MHz from replacing MEJ2S0509SC by the designed gate-driver power supply.

C. *Thermal Reliability*

A thermal cycling test was performed to explore the thermal reliability of the embedded transformer structure. The main concern here was that the core may break under the differing thermal expansions between the PCB material and the core when the operating temperature varies from –50 to 200 °C. To this end, a total of 150 one-hour temperature cycles was conducted on six samples; three of them were made of FR4 and the rest of MEGTRON2 (R-1577). Before the test, the FR4 samples were visually inspected to ensure that there was no damage around that the core and the air gap were clearly seen. One sample before the test is shown in Fig. 22(a). The MEGTRON samples could not be visually inspected due to the nontransparent nature of the laminate material.

The resultant core images after the thermal cycling tests were conducted are shown in Fig. 22(b) and (c). To get the images, the top PCB layer covering the core was polished. In Fig. 22(b), it is seen that the core within FR4 is completely cracked. The large thermal expansion from the PCB material puts so much pressure on the ferrite core that the core cannot withhold it. On the other hand, the core embedded in the MEGTRON2 sample, shown in Fig. 22(c), looked the same after the tests, showing no evidence of cracking. This simple test pointed out the importance of selecting the right PCB material for power supplies intended to operate at high ambient temperature conditions, demonstrating as well the desirable properties of the MEGTRON2 material. To fully assess the lifetime of the power supply operating under such conditions an extended number of cycles would be required.

VI. SUMMARY AND CONCLUSION

This paper presented the design of an integrated dual-output gate-driver power supply with a PCB-embedded transformer based on GaN HEMT devices operating at a switching frequency of 1 MHz. With careful design, the constructed converter with two 1-W isolated outputs was demonstrated to achieve 85% overall efficiency, featuring a minimal 1.6 pF isolation capacitance, both primary-to-secondary and secondary-to-secondary, achieving a power density of 72 W/in^3. An optimization of the transformer dimension was performed and presented to identify the key tradeoffs among the transformer loss, interwinding capacitance, and volume, with which a solution on the Pareto-optimal surface was found. The designed PCB-embedded transformer was then fabricated and effectively embedded into the PCB material, being finally integrated with a top active circuit layer hosting the GaN devices and passive components. Experimental tests were conducted to demonstrate its operation and attained performance. Furthermore, thermal cycling tests with alternative PCB materials were conducted to assess the feasibility of operating at a high ambient temperature (200 °C), where the MEGTRON 2 material from Panasonic showed superior qualities matching the ferrite material used for the transformer core. Finally, the proposed optimization design approach and the proposed power supply structure demonstrated the feasibility of simultaneously achieving high power density and high efficiency when utilizing the PCB-embedded transformer as a substrate for GaN-based power converters.

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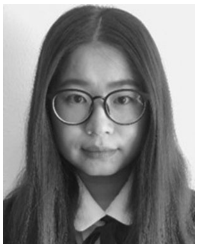


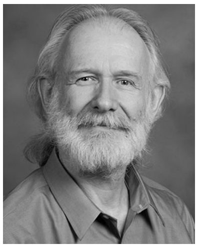
Bingyao Sun (S'14) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2013, and the M.S. degree in electrical engineering in 2015 from Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, USA, where she is currently working toward the Ph.D. degree in electrical engineering at the Center for Power Electronics Systems (CPES).

From 2013 to 2018, she is a Research Assistant with the CPES, Virginia Tech. Her research interests include the high switching frequency power converter design using wide-bandgap devices, development of the gate driver for wide-bandgap semiconductors, electromagnetic interference modeling, and filter design for power converters.

Rolando Burgos (S'96–M'03) received the B.S. degree in electronics engineering, the Electronics Engineering Professional degree, and the M.S. and Ph.D. degrees in electrical engineering from the University of Concepción, Concepción, Chile, in 1995, 1997, 1999, and 2002, respectively.

In 2002, he joined, as a Postdoctoral Fellow, the Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, VA, USA, becoming a Research Scientist in 2003 and a Research Assistant Professor in 2005. In 2009, he joined ABB Corporate Research, Raleigh, NC, where he was a Scientist (2009–2010) and a Principal Scientist (2010–2012). In 2010, he was appointed as an Adjunct Associate Professor with the Electrical and Computer Engineering Department, North Carolina State University, working ad honorem with the Future Renewable Electric Energy Delivery and Management Systems Center. In 2012, he returned to Virginia Tech, where he is currently an Associate Professor with The Bradley Department of Electrical and Computer Engineering, a CPES Faculty, and a Member of the CPES Executive Board. His research interests include wide-bandgap semiconductor based power conversion, electromagnetic interference and electromagnetic compatibility, multiphase multilevel power converters, grid power electronics systems, stability of ac and dc power systems, and modeling and control of power electronics converters and systems.

Dr. Burgos is a Member of the IEEE Power Electronics Society, where he currently serves the Chair of the Power and Control Core Technologies Committee, as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE POWER ELECTRONICS LETTERS, and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is also a Member of the IEEE Industry Applications Society, the IEEE Industrial Electronics Society, and the IEEE Power and Energy Society.



Dushan Boroyevich (S'81–M'86–SM'03–F'06) received the Dipl. Ing. degree from the University of Belgrade, Belgrade, Serbia, in 1976, the M.S. degree from the University of Novi Sad, Novi Sad, Serbia, in 1982, and the Ph.D. degree from Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, VA, USA, in 1986.

From 1986 to 1990, he was an Assistant Professor and the Director of the Power and Industrial Electronics Research Program with the Institute for Power and Electronic Engineering, University of Novi Sad. He then joined the Bradley Department of Electrical and Computer Engineering, Virginia Tech, as an Associate Professor. He is currently the University Distinguished Professor and the Associate Vice President for Research and Innovation in Energy Systems with Virginia Tech, and the Director of the Center for Power Electronics Systems. He is an Honorary Professor with the Xi'an Jiaotong University, Xi'an, China, and a K.T. Li Chair Professor with the National Cheng Kung University, Tainan, Taiwan. He has led numerous research projects in the areas of multiphase power conversion, electronic power distribution systems, modeling and control, and multidisciplinary design optimization. He has advised more than 40 Ph.D. and 40 M.S. students to graduation and has coauthored with them more than 700 papers.

Dr. Boroyevich was the President of the IEEE Power Electronics Society (PELS) for 2011–2012. He was a recipient of numerous awards, including the IEEE William E. Newell Power Electronics Technical Field Award, the IEEE PELS Harry A. Owen Distinguished Service Award, European Power Electronics Association Outstanding Achievement Award, and the Award for Outstanding Achievements and Service to Profession by the European Power Electronics and Motion Control Council. He was elected to the US National Academy of Engineering in 2014 for advancements in control, modeling, and design of electronic power conversion for electric energy and transportation.