Letters

Three-Phase ZVR Topology and Modulation Strategy for Transformerless PV System

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***Abstract*—Leakage current reduction is crucial for operating transformerlss photovoltaic (PV) systems. In this letter, a new three-phase topology and modulation strategy is proposed. It is derived from the single-phase zero-voltage state rectifier topology, but the operation mechanism is quite different. Therefore, a new modulation strategy based on the Boolean logic function is proposed to achieve the constant common-mode voltage, so as to eliminate the leakage current. Finally, the experimental tests are carried out to verify the feasibility and effectiveness of the proposed solution.**

***Index Terms*—Inverter, leakage current, modulation, transformerless PV system.**

I. Introduction

PULSEWIDTH modulated inverters have been typically used for transformerless photovoltaic (PV) system applications [1], [2]. However, the conventional three-phase six-switch inverter suffers from high-frequency common-mode voltage, which results in the high leakage current [3]. High leakage current results in grid current distortion, electromagnetic interference, and potential safety issues [4], [5]. That is the reason why many attempts have been done to reduce the leakage current in grid connected PV systems. Many interesting solutions have been presented in literature. In general, these can be classified into two groups. One group is the topology-based method [6]–[12], and the other is the modulation-based one. The latter is mainly for three-phase systems. Cavalcanti *et al.* presented an improved modulation strategy [13], [14]. It can achieve a constant common mode voltage to leakage current, but the modulation index is limited. Lee *et al.* proposed a modified modulation [15]. The idea is interesting and insightful, but

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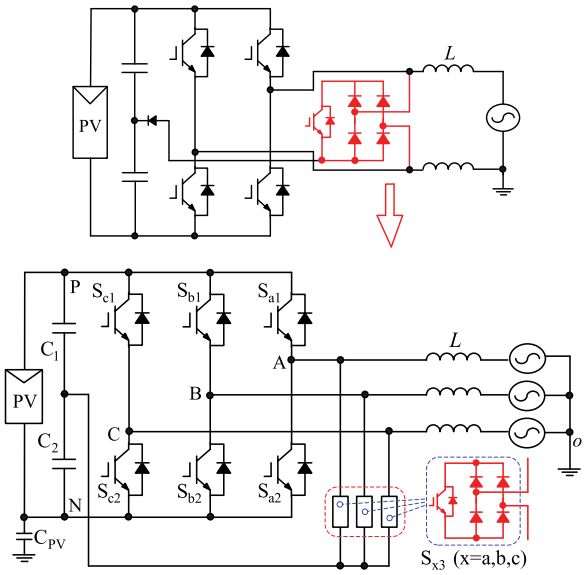


Fig. 1. Schematic diagram of three-phase ZVR topology.

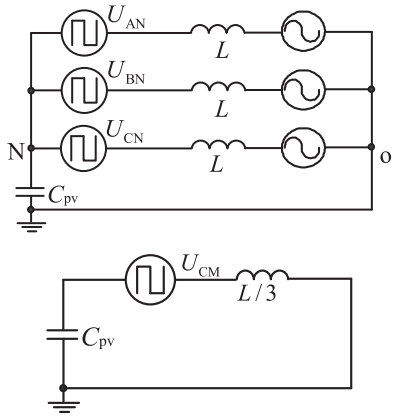


Fig. 2. Simplified diagram.

lower than that without ZVR, since the voltage stresses of three more power devices is only half of the dc bus voltage, which is much lower than those of previous six switches. Furthermore, the conventional inverter without ZVR fails to reduce the leakage current. Therefore, the proposed three-phase ZVR topology is attractive for transformerless PV systems.

The three-phase ZVR inverter can be simplified as shown in Fig. 2, where common-mode voltage is defined in (1). More details about the simplified diagram can be found in [13]. It can be observed that the leakage current can be eliminated if the common-mode voltage is constant

$$U_{CM} = \frac{U_{AN} + U_{BN} + U_{CN}}{3}. \tag{1}$$

Different from the conventional three-phase six-switch topology, the phase voltage of U_{AN}, U_{BN}, and U_{CN} have three states, depending on the switching pattern, as shown in (2), where U_d is the dc bus voltage and x = a, b, c. And the states of 2, 1, and 0 are also defined in (2)

$$U_{xN} = \begin{cases} U_d, & ''2''\ S_{x1}\ \text{on},\ S_{x2}\ \text{and}\ S_{x3}\ \text{off} \\ U_d/2, & ''1''\ S_{x3}\ \text{on},\ S_{x1}\ \text{and}\ S_{x2}\ \text{off} \\ 0, & ''0''\ S_{x2}\ \text{on},\ S_{x1}\ \text{and}\ S_{x3}\ \text{off}. \end{cases} \tag{2}$$

TABLE I
COMMON-MODE VOLTAGE AND SWITCHING STATES

Group	Switching sates	CMV
1	222	U_d
2	221, 212, 122	$5U_d/6$
3	220, 202, 022, 211, 121,112	$2U_d/3$
4	210, 201, 120, 102, 012, 021, 111	$U_d/2$
5	110, 101, 011, 200, 020, 002	$U_d/3$
6	100, 010, 001	$U_d/6$
7	000	0

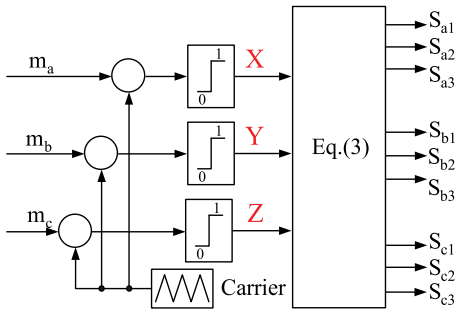


Fig. 3. Proposed modulation strategy.

Table I shows the switching states and their corresponding common mode potential. It can be observed that there are seven groups of switching states. Note that the common-mode voltage should be constant to eliminate the leakage current, so group 4 is selected in this letter. In order to achieve the switching states of group 4, a new modulation strategy is proposed as shown in Fig. 3. First, three modulating signals, (c.f. m_a, m_b, and m_c) are compared with one carrier to get the three logic signals (c.f. X, Y, and Z in Table II). Second, three logic signals pass through the (3) to get the switching signals, as shown in Table II, where 9 variables of $\mathrm{S}_{a1} \sim \mathrm{S}_{c3}$ are defined as follows. For example, $\mathrm{S}_{a1} = 1$ means the switch is on. While $\mathrm{S}_{a1} = 0$ means the switch is OFF

$$\begin{aligned} S_{a1} &= X\bar{Y}, \quad S_{a2} = \bar{X}Y, \quad S_{a3} = XY + \bar{X}\bar{Y} \\ S_{b1} &= Y\bar{Z}, \quad S_{b2} = \bar{Y}Z, \quad S_{b3} = YZ + \bar{Y}\bar{Z} \\ S_{c1} &= \bar{X}Z, \quad S_{c2} = X\bar{Z}, \quad S_{c3} = XZ + \bar{X}\bar{Z}. \end{aligned} \tag{3}$$

It should be noted that for the proposed strategy in (3) and Fig. (4), the classical duty cycles are modified so that the generated common-mode voltage is kept constant. Therefore, the duty cycles are modified, and the applied voltages at

TABLE II
DETAILED SWITCHING LOGICS OF FIG. 4

XYZ	S_{a1}	S_{a2}	S_{a3}	S_{b1}	S_{b2}	S_{b3}	S_{c1}	S_{c2}	S_{c3}	group 4
100	1	0	0	0	0	1	0	1	0	210
010	0	1	0	1	0	0	0	0	1	021
001	0	0	1	0	1	0	1	0	0	102
101	1	0	0	0	1	0	0	0	1	201
110	0	0	1	1	0	0	0	1	0	120
011	0	1	0	0	0	1	1	0	0	012
000 111	0	0	1	0	0	1	0	0	1	111

the output of the three-phase ZVR inverter are different from those of the conventional three-phase inverter, where the common mode voltage cannot be kept constant with the classic modulation.

Take line 2 of Table II for example, in case of X = 1, Y = 0, Z = 0, and

$$S_{a1} = X\bar{Y} = 1, \quad S_{a2} = \bar{X}Y = 0, \quad S_{a3} = XY + \bar{X}\bar{Y} = 0$$
$$S_{b1} = Y\bar{Z} = 0, \quad S_{b2} = \bar{Y}Z = 0, \quad S_{b3} = YZ + \bar{Y}\bar{Z} = 1$$
$$S_{c1} = \bar{X}Z = 0, \quad S_{c2} = X\bar{Z} = 1, \quad S_{c3} = XZ + \bar{X}\bar{Z} = 0. \quad (4)$$

According to definition of (2), $S_{a1} = X\bar{Y} = 1$, $S_{a2} = \bar{X}Y = 0$, and $S_{a3} = XY + \bar{X}\bar{Y} = 0$ means "2." $S_{b1} = Y\bar{Z} = 0$, $S_{b2} = \bar{Y}Z = 0$, and $S_{b3} = YZ + \bar{Y}\bar{Z} = 1$ means "1." $S_{c1} = \bar{X}Z = 0$, $S_{c2} = X\bar{Z} = 1$, and $S_{c3} = XZ + \bar{X}\bar{Z} = 0$ means "0." Therefore, when XYZ = 100, the output will be "210" as shown in group 4. It is in agreement with the result in Table II. Other cases are similar and not duplicated here for simplicity. In this way, the common-mode voltage can be kept constant with the proposed modulation strategy of the new three-phase ZVR topology. Note that the proposed topology is similar to the conventional three-phase six-switch one, except for the additional ZVR branch. So the design procedure is almost the same as that of the conventional one, and thus, the following only provides the design procedure for the additional ZVR branch. As can be seen from the experimental results, the current stress of the ZVR is the same as that of the conventional six switches, but the voltage stress of the ZVR is much lower than that of the conventional six switches. Therefore, the design procedure is almost the same with conventional six switches, except for voltage stress. That is a low voltage rating ZVR can be designed for the proposed topology. The following will present the experimental evaluation.

III. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed solution, the hardware experimental prototype is built and tested. The experimental parameters are listed below. The dc bus voltage is 120 V, the switching frequency is 10 kHz, filter inductor is 5 mH, filter capacitors are 9.4 uF, and the stray capacitor is 300 nF. As shown in Fig. 4, the reference currents of $I^*_{\mathrm{REF}\alpha} = I^*_{\mathrm{ref}} \sin\theta$ and

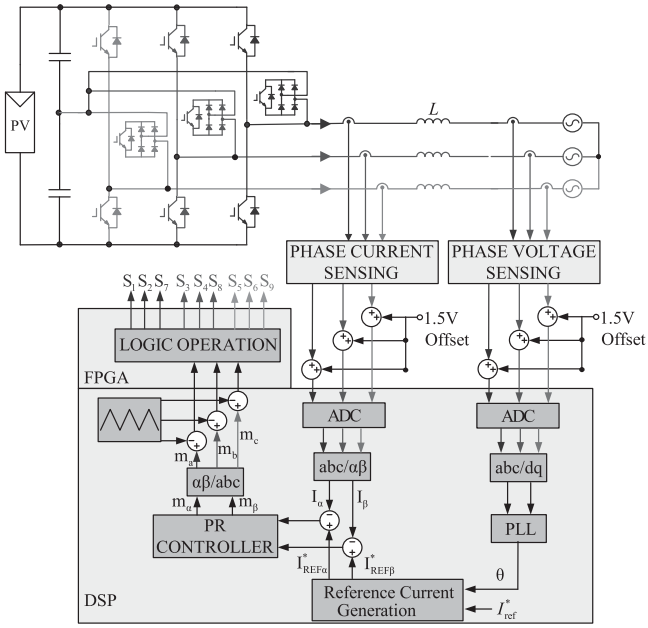


Fig. 4. Close-loop control structure.

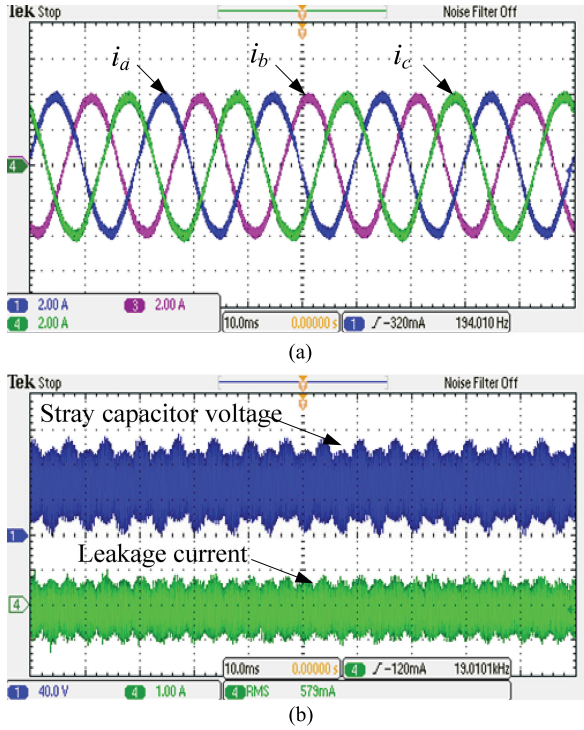
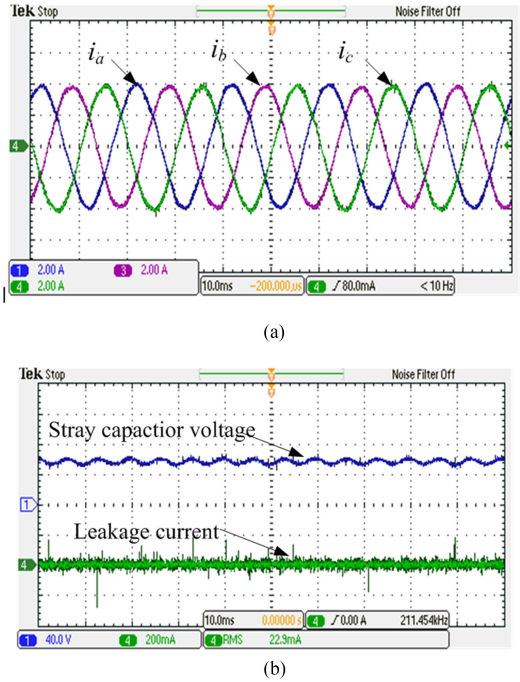


Fig. 5. Experimental results with the dual-carrier modulation. (a) Grid current. (b) Stray capacitor voltage and leakage current.

$I^*_{\mathrm{REF}\beta} = I^*_{\mathrm{ref}} \cos\theta$ are generated by the reference current amplitude of I^*_{ref} and phase angular θ, which is the output of phase-locked loop. The current is control by proportional-resonant controller [17]. The modulation algorithms are implemented in TMS320F28335 digital signal processor, and the logic operations are programmed with XC3S400 FPGA.

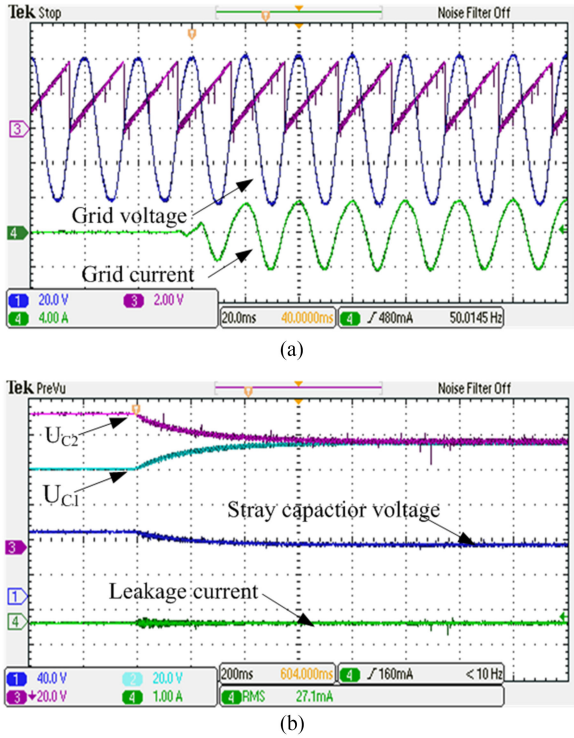
Fig. 5 shows the experimental results with the dual-carrier modulation (c.f., Fig. 3) of three-phase ZVR topology. It can



(a)

(b)

Fig. 6. Experimental results with proposed modulation. (a) Grid current. (b) Stray capacitor voltage and leakage current.



(a)

(b)

Fig. 7. Dynamic experiments with proposed modulation. (a) Phase_a grid voltage and current. (b) Dc-link capacitor voltages, stray capacitor voltage, and leakage current

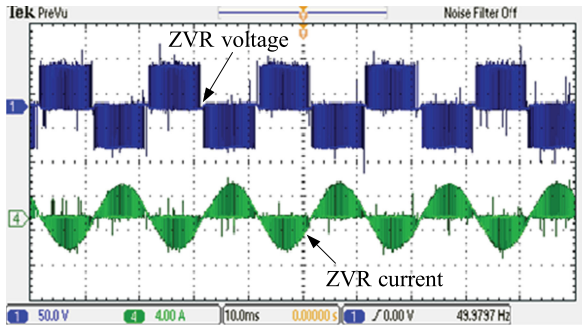


Fig. 8. current and voltage through the ZVR.

be observed that the grid current consists of the high-frequency harmonics, which are the results of the leakage current. The total harmonic distortion (THD) is 5.9%, which fails to meet the requirements of the IEEE Standard (c.f. THD $<$ 5%). Fig. 5(b) shows the stray capacitor voltage and leakage current. Obviously, the stray capacitor voltage consists of high-frequency components. It leads to the high leakage current. The peak value of the leakage current is far beyond 300 mA, as specified in VDE-0126-1-1 standard.

Fig. 6 shows the experimental results with the proposed modulation (c.f. Fig. 4) of three-phase ZVR topology. It can be observed that the high-frequency harmonics of the grid is significantly reduced. The reason behind it is that the grid current consists of the common-mode and differential-mode currents. In this case, the high-frequency common-mode leakage current is small. So the total harmonic distortion of the grid current is as low as 3.5%, which is meet the requirements of the IEEE Standard (c.f. THD $<$ 5%). Fig. 5(b) shows the stray capacitor voltage and leakage current. Obviously, the stray capacitor voltage is free of any high-frequency components. Therefore, the leakage current is significantly reduced. The peak value of the leakage current is well below 300 mA, which meets the VDE-0126-1-1 standard. Note that the zero sequence injection is used for the proposed carried-based modulation for the better utilization of the dc-link voltage. That is the reason why a small zero sequence component is on stray capacitor. Note that this frequency of variation is very low, so the leakage current would not be affected, as shown in Fig. 6.

In order to further validate the effectiveness of the proposed method, the dynamic experiments are carried out in Fig. 7, where the triangular waveform is the grid synchronization signal from the phase-locked loop. In this case, the grid current changes 0 to 4 A. The dc-link capacitor voltages of C_1 and C_2 are well balanced. The comprehensive theoretical analysis of the capacitor voltage balancing mechanism of the proposed solution is beyond the scope of this letter. And the leakage current is well below 300 mA. The dynamic tests further verify the effectiveness of the proposed solution.

The current and voltage through the ZVR are shown in Fig. 8. It can be observed that the current stress of the ZVR is the same as that of the conventional six switches, but the voltage stress of the ZVR is much lower than that of the conventional six switches. Therefore, the power losses are lower than that of the conventional six switches. Note that the additional switches $S_{a3} \sim S_{c3}$ and their drive circuits are needed, but the leakage current can be well suppressed, and no bulky, costly and low-efficient EMI filter is needed. Therefore, the overall performance is better than the conventional solution.

IV. Conclusion

This letter has presented the analysis and experimental verification of a new three-phase ZVR topology and its modulation strategy to eliminate the leakage current for transformerless PV systems. The findings reveal that the leakage current can be effectively reduced well below 300 mA by selecting the switching states of new three-phase ZVR topology. Aside from that, the proposed modulation is easy to implement. Therefore, it is attractive for three-phase transformerless PV systems. The future research is toward the comprehensive theoretical analysis the capacitor voltage balancing mechanism of the proposed solution.

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