Power-Efficient VLC Transmitter Based on Pulse-Width Modulated DC–DC Converters and the Split of the Power

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***Abstract*—Visible light communication (VLC) has gained relevance during the last few years. It consists in using high-brightness LEDs (HB-LEDs) both for lighting and transmitting information by changing the light intensity rapidly. However, there are some bottlenecks that are slowing down the deployment of this technology. One of the most important problems is that the HB-LED drivers proposed for addressing high data rates in VLC achieve poor power efficiency. Since these HB-LED drivers must be able to reproduce fast current waveforms, the use of linear power amplifiers has been adopted, which clearly damages the power efficiency of HB-LED lighting. In order to alleviate this problem, an HB-LED driver made up of two DC–DC power converters is presented in this work. One of them is responsible for performing the communication functionality by operating at high switching frequency (10 MHz), whereas the second converter fulfills the illumination functionality by ensuring a certain biasing point. The split of the power allows us to minimize the power delivered by the fast-response DC–DC power converter, which suffers from high switching losses. Thus, the overall efficiency can be maximized for each particular communication scenario and for scenarios with changing conditions (i.e., mobile transmitter and/or receiver, presence of mobile obstacles, etc.). In this sense, how the lighting level and the communication signal power affect both the power efficiency and the communication efficiency is deeply analyzed in the experimental section. The implemented prototype achieves an overall efficiency around 90%. In addition, the proposed VLC transmitter is able to reproduce a wide range of digital modulation schemes, including the preferred one for wireless communications: orthogonal frequency division multiplexing.**

***Index Terms*—High switching frequency, high-brightness LED (HB-LED), orthogonal frequency division multiplexing (OFDM), output-series connection, visible light communication (VLC).**

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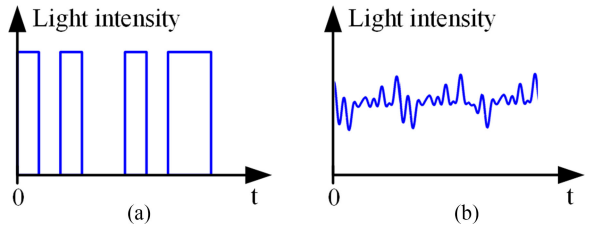


Fig. 1. Example of light intensity waveforms in VLC. (a) Pulse-based modulation scheme. (b) Advanced modulation scheme.

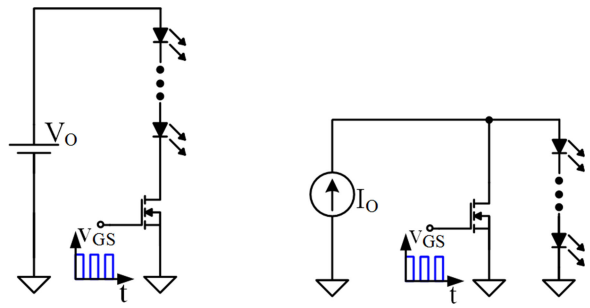


Fig. 2. HB-LED drivers for reproducing pulse-based modulation schemes. (a) MOSFET in series with the HB-LED string. (b) MOSFET in parallel with the HB-LED string.

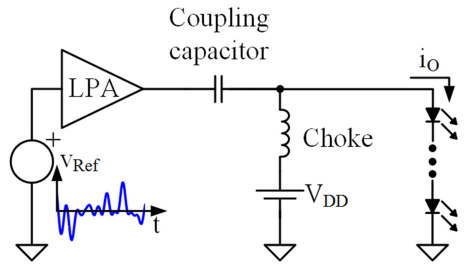


Fig. 3. Power-inefficient HB-LED driver for reproducing advanced modulation schemes.

which implies that they cannot achieve high bit rates when the available bandwidth is as limited as in the case of HB-LEDs.

The second approach is based on reproducing advanced modulation schemes that provide a higher data rate than pulse-based modulation schemes for the same bandwidth [see Fig. 1(b)]. The drawback is that this method jeopardizes the main advantage of HB-LED lighting: the power efficiency. The reason is that the HB-LED drivers that have been proposed for reproducing this kind of modulation scheme use a linear power amplifier (LPA) for delivering the AC component, while a DC–DC power converter determines the DC component (see Fig. 3). The use of this kind of HB-LED driver for VLC is reported in [5] and [16]–[26]. The problem is that a class A or AB LPA offers very low power efficiency (between 10% and 40%). It is important to note that the overall efficiency of the HB-LED driver for VLC is determined by both the LPA and the DC–DC power converter, which actually achieves high power efficiency (similar to a conventional HB-LED driver for lighting applications). Therefore, the straightforward method for increasing the efficiency is to reduce power delivered by the LPA in order to mitigate the impact of its low efficiency on the overall efficiency. However, this strategy is counterproductive because reducing the communication signal power strongly jeopardizes the range of the communication system. A cleverer method is to design advanced modulation schemes that demand less communication signal power for achieving the same range [27], [28]. Nevertheless, this benefit is obtained at the expense of damaging other characteristics and the improvement is not as high as desired. Another approach can be found in [29], where a digital-to-analog converter (DAC) is used as the HB-LED driver for VLC. However, since the proposed DAC is made up of several transistors that operate in a linear mode (i.e., similar to an LPA), the efficiency is lower than 70%.

As a conclusion, reproducing advanced modulation schemes is mandatory for enabling the massive data traffic predicted for upcoming years. However, increasing the efficiency of the HB-LED driver is an important target that must be addressed. Some recent works have studied the issue [30]–[36]. In [30], [31], several VLC transmitters fully or partially based on the use of DC–DC power converters are proposed. However, there is a lack of technical analysis and experimental results. In addition, some important issues, such as the dependence of the HB-LED behavior on the operating temperature, are not considered. In [32] and [33], a two-phase synchronous buck converter able to reproduce single-carrier digital modulation schemes by controlling its output voltage ripple is presented. Since the first switching harmonic acts as the carrier of the reproduced modulation scheme, the approach provides the highest ratio between the bit rate and the required switching frequency. The major drawback of this method is that it is not able to reproduce multicarrier digital modulation schemes, such as orthogonal frequency division multiplexing (OFDM), which are preferable in some scenarios [37]–[40].

In the present work, a VLC transmitter able to reproduce both single-carrier and multicarrier digital modulation schemes is presented. The architecture is made up of two DC–DC power converters in output-series connection [35], [36]. The first one is a fast-response DC–DC converter that achieves a bandwidth high enough to reproduce the communication signal. The second converter fulfills the illumination functionality by ensuring a certain biasing point.

The paper is organized as follows. The operating principle of a VLC transmitter and the driving requirements are explained in Section II. The proposed HB-LED driver together with other approaches are described in Section III. The experimental results are given in Section IV, and finally, the conclusions are gathered in Section V.

II. Driving HB-LEDs for Performing VLC

The VLC transmitter must be able to generate a light intensity waveform (s_O) made up of a DC component (s_{O-DC}) that determines the lighting level and an AC component (s_{O-AC}) that represents the transmitted information. The study of the relationship among s_O, the current through the HB-LED string (i_O), and the applied voltage (v_O) is essential to properly design the HB-LED driver. The behavior depends on the particular HB-LED that is used, but certain general characteristics can be

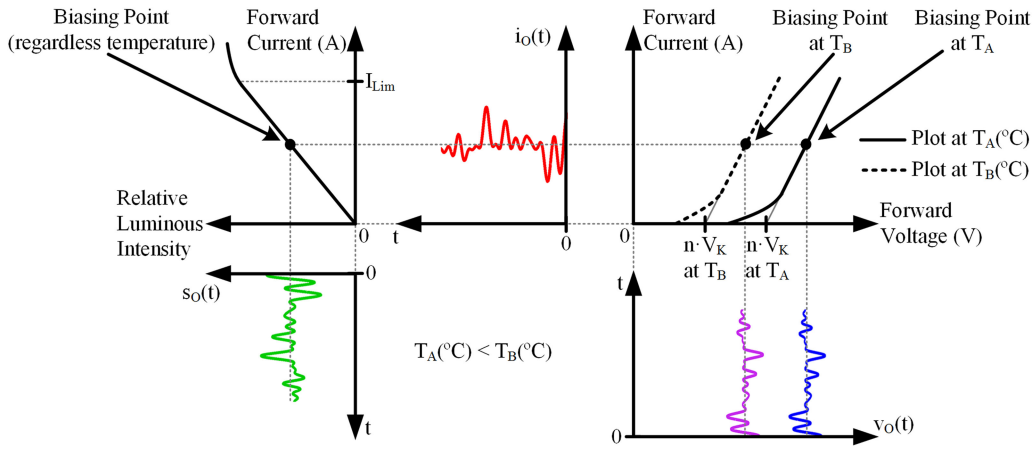


Fig. 4. Driving a string of n HB-LEDs in series connection for performing VLC by considering the L–I and I–V curves.

identified. Fig. 4 shows the main waveforms involved in the process of performing VLC with an HB-LED string considering both the light intensity versus current (L–I) curve and the current versus voltage (I–V) curve. Note that n represents the number of HB-LEDs in series connection. A linear relationship between light intensity and current is assumed when the last one is lower than a certain limit value (I_{Lim}). Then, the relationship in the desired operation region (i.e., the linear region) can be modeled as

$$s_O = n \cdot K_{L-I} \cdot i_O \quad \text{if } i_O < I_{Lim} \tag{1}$$

where K_{L-I} is the proportionality coefficient of each HB-LED. Regarding the I–V curve, the behavior of a single HB-LED has been traditionally modeled as an ideal diode (D) in series with the dynamic resistance (R_D) and a constant voltage source that represents the knee voltage (V_K). Fig. 4 also shows the dependence of the voltage waveform on the junction temperature of the HB-LEDs (T_J). Basically, V_K falls when T_J rises while R_D remains constant [41]–[43]. Consequently, ensuring a certain voltage level does not guarantee the desired lighting level. Taking into account all these facts, the relationship between current and voltage in the desired operation region (i.e., the linear region) can be modeled as

$$i_O = \frac{1}{n \cdot R_D} \left(v_O - n \cdot V_K(T_J)\right) \quad \text{if } v_O > n \cdot V_K(T_J). \tag{2}$$

Considering the previous facts, the desired features of the HB-LED driver based on the use of DC–DC converters can be stated as follows.

Capability to reproduce a fast current reference. In order to maximize the bit rate, the HB-LED driver must exploit all the bandwidth provided by the HB-LEDs. Consequently, the HB-LED driver must be based on the use of a fast-response DC–DC power converter able to reproduce current waveforms of several MHz.

High output voltage accuracy. As Fig. 4 shows, the current through the HB-LEDs does not start until the applied voltage overcomes $n \cdot V_K$. After that, a small increase of the voltage is translated into a high increase of the current, and consequently, a high increase of the light intensity. Then, the HB-LED driver must be able to perform very small voltage variations in comparison to the DC voltage that it must provide. In addition, it must minimize the output voltage ripple to reduce signal distortion.

Temperature compensation. As was previously explained, the relation among s_O, i_O, and v_O strongly depends on T_J. Therefore, implementing some kind of current feedback loop is mandatory to ensure the proper reproduction of the target light intensity waveform.

Low/medium power. The power that the HB-LED driver must deliver strongly depends on the application scenario. For instance, the power of an HB-LED bulb for the office environment is in the order of tens of watts, whereas it can attain thousands of watts in the case of a football stadium.

High efficiency. Low power dissipation in the HB-LED driver is essential to extend the use of VLC for providing services such as Internet connection. In this sense, a 90% efficiency target seems to be reasonable.

Dimming capability. This last feature is recommended, but not mandatory.

III. Proposed HB-LED Driver for Reproducing Advanced Modulation Schemes

In order to support the explanation of the VLC transmitter presented in this work and to highlight its advantages, the ideas contemplated by the authors before achieving the definitive approach are explained below.

A. Controlling the Whole Current Through the HB-LEDs

Since the relation between v_O and s_O strongly depends on T_J, the straightforward approach to implement the VLC transmitter consists in controlling i_O (see Fig. 5). In this way, the DC–DC power converter drives the HB-LEDs with a current proportional to the desired light intensity waveform according to (1).

The light intensity reference (s_{O-Ref}) is made up of the lighting level reference $(s_{O-DC\text{-}Ref})$ and the communication component reference $(s_{O-AC\text{-}Ref})$. Then, the current reference (i_{O-Ref}) is obtained according to (1), and after that, i_{O-Ref} is compared

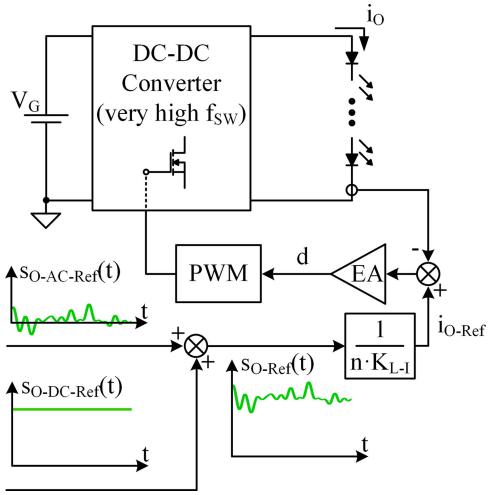


Fig. 5. HB-LED driver approach based on controlling i_O.

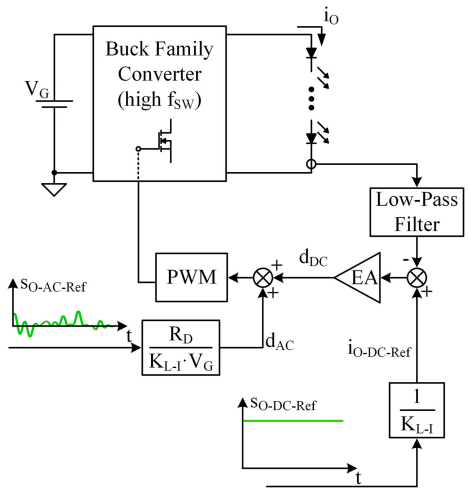


Fig. 6. HB-LED driver approach based on controlling i_{O-DC}.

to i_O. The result is processed by the error amplifier (EA), and finally, the pulse-width modulation block generates the gate signal of the MOSFETs according to the received control action (i.e., the duty cycle d).

The simplicity constitutes the major advantage of this approach. Unfortunately, the high switching frequency (f_{SW}) required for implementing this method is a significant problem. Take into account that f_{SW} must be high enough to ensure a bandwidth equal or higher than the maximum frequency of s_O (f_{S-Max}). The ideal minimum value of f_{SW} is twice f_{S-Max} according to the Nyquist–Shannon sampling theorem. However, this limit rises when the reactive elements of the power stage and the dynamics related to the current feedback loop, such as the EA response, are considered. Therefore, f_{SW} would be much higher than f_{S-Max} in practice. The key point is that since f_{S-Max} is in the order of MHz, f_{SW} would be extremely high, which will be translated into unaffordable switching losses.

Another drawback is the high output voltage accuracy required for reproducing s_{O-AC} properly. It can be easily understood with an example based on the I–V curve depicted in Fig. 4. Consider a string of *n* HB-LEDs acting as load and pay attention to V_K and the voltage that determines I_{Lim} (V_{Lim}). Taking into account these two voltages, the maximum variation of v_O can be defined as

$$\Delta v_O = n \cdot [V_{Lim}(T_J) - V_K(T_J)]. \quad (3)$$

The high output voltage accuracy required by this approach arises when the ratio between Δv_O and v_{O-DC} is evaluated. For instance, if the target i_{O-DC} is $0.5 \cdot I_{Lim}$, v_{O-DC} is equal to

$$v_{O-DC} = n \cdot V_K(T_J) + 0.5 \cdot \Delta v_O. \quad (4)$$

Then, the ratio is equal to

$$\frac{\Delta v_O}{v_{O-DC}} = \frac{2 \cdot [V_{Lim}(T_J) - V_K(T_J)]}{V_{Lim}(T_J) + V_K(T_J)}. \quad (5)$$

Typically, V_K and V_{Lim} are around 3 and 3.5 V when T_J is 25 °C, respectively, which is translated into a very low ratio (i.e., 1/6.5). In summary, the HB-LED driver must be able to perform very small voltage variations in comparison to the DC voltage that it must provide. Consequently, the DC–DC converter must achieve high duty cycle accuracy.

B. Controlling the Average Current Through the HB-LEDs

As previously mentioned, the impact of the feedback loop on the converter bandwidth leads to an unaffordable f_{SW} when i_O is controlled. Fortunately, this drawback can be overcome by analyzing in detail how T_J affects the HB-LED behavior. As explained in Section II, V_K falls when T_J rises while R_D remains constant. The key point is to study how the voltage waveform required for tracking a certain s_O changes with T_J. In this sense, Fig. 4 exemplifies this fact considering two particular T_J values. It can be seen that the DC component of v_O (i.e., v_{O-DC}) depends on T_J because of the change of V_K. However, since R_D does not depend on T_J, the AC component of v_O (i.e., v_{O-AC}) does not change. As a conclusion, a current loop is actually needed, but controlling the average current through the HB-LEDs (i.e., i_{O-DC}) instead of the whole current waveform is enough for ensuring the proper operation. Thus, the feedback loop does not limit the speed of the HB-LED driver for reproducing the AC component of the current through the HB-LED string (i.e., i_{O-AC}). Therefore, the required f_{SW} can be reduced in comparison to the approach described in Section III-A.

Taking into account the previous considerations, a VLC transmitter based on a DC–DC converter that controls i_{O-DC} instead of i_O can be addressed (see Fig. 6). In this case, the output current is sensed and filtered to measure i_{O-DC}. Since this value determines the lighting level, the DC component of the output current reference $(i_{O-DC-Ref})$ is obtained from $s_{O-DC-Ref}$ by using (1), and then, $i_{O-DC-Ref}$ is compared to i_{O-DC}. Thus, the EA provides a constant control action (d_{DC}) that ensures the desired lighting level. After that, the AC component of the control action (d_{AC}), which is responsible for the communication signal, is added. At this point, the function that models the relationship between light intensity changes and duty cycle changes when the HB-LED string operates in the linear region (f_{d-s}) must be ob-

tained. This function allows us to calculate d_{AC} from $s_{O-AC\text{-}Ref}$. Then, the L–I curve and the I–V curve must be considered in order to obtain f_{d-s}. Equation (1) is valid to obtain the relationship between light intensity changes and current changes. The relationship between current changes and voltage changes can be deduced from (2)

$$v_{O-AC} = n \cdot R_D \cdot i_{O-AC}. \tag{6}$$

Finally, the relationship between the output voltage and the duty cycle must be used. Then, f_{d-s} depends on the particular DC–DC converter topology selected for the implementation. For instance, if the approach is implemented with a buck converter, the function is equal to

$$f_{d-s}(s_{O-AC-Ref}) = \frac{R_D}{K_{L-I} \cdot V_G} s_{O-AC-Ref} \tag{7}$$

where V_G is the input voltage of the DC–DC converter. It is important to note that the low-pass filter of the feedback loop must reject the frequency components of i_O related to the communication signal in order to achieve the proper operation. This enables the sum of d_{AC} without interfering with the EA operation.

This method avoids the bandwidth limitation caused by the feedback loop. Therefore, the bandwidth of the DC–DC converter is only limited by the reactive elements of the power stage, alleviating the main problem of the previous approach. However, the required f_{SW} keeps being significantly high, and consequently, the HB-LED driver will suffer from high switching losses when the highest data rates (i.e., highest f_{S-Max} values) are addressed. In addition, the required duty cycle accuracy keeps being a problem.

C. Controlling the Average Current Through the HB-LEDs and Splitting the Power

The definitive approach is focused on both increasing the power efficiency and reducing the demanded duty cycle accuracy. The proposed HB-LED driver is made up of two DC–DC power converters in output-series connection (see Fig. 7) and each one is designed to meet different objectives. The low-side converter (LSC) operates in close-loop controlling i_{O-DC}. Regarding the high-side converter (HSC), it operates in open-loop performing the small voltage variations. The set of DC–DC converters works in the following way. The HSC provides v_{O-AC} (i.e., the voltage component responsible for the communication) plus a certain DC voltage (v_{O-H-DC}) required for the proper operation of the DC–DC converter. Note that v_{O-H-DC} is mandatory to ensure that the total output voltage of the HSC (v_{O-H}) never reaches zero or negative values (i.e., $v_{O-AC} + v_{O-H-DC} > 0\,V$). The remaining DC voltage that is required for achieving the desired lighting level is provided by the LSC. Therefore, the LSC controls i_{O-DC} by adjusting its output voltage (v_{O-L}) to ensure that the total DC output voltage of the HB-LED driver (i.e., $v_{O-DC} = v_{O-L} + v_{O-H-DC}$) achieves the desired biasing point regardless v_{O-H-DC} and the V_K variations with T_J. Then, the total output voltage of the HB-LED driver is

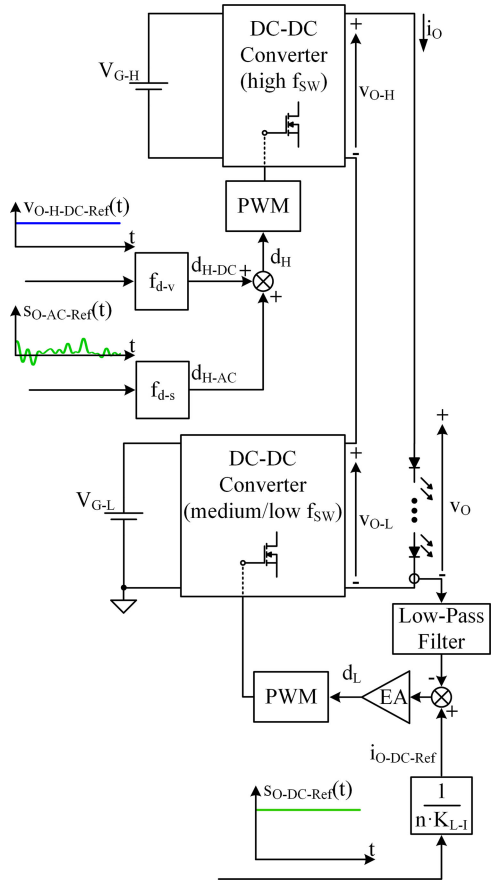


Fig. 7. HB-LED driver approach based on controlling i_{O-DC} and splitting the power.

$$\begin{aligned} v_O &= v_{O-L} + v_{O-H} \\ &= v_{O-L} + v_{O-H-DC} + v_{O-H-AC} \\ &= v_{O-DC} + v_{O-H-AC}. \end{aligned} \tag{8}$$

It should be noted that f_{d-v} (see Fig. 7) models the relationship between the duty cycle of the HSC (d_H) and v_{O-H}. Then, this function depends on the particular DC–DC converter topology selected for the HSC implementation. As Fig. 7 shows, f_{d-v} is used to obtain the DC component of the HSC duty cycle (d_{H-DC}). The AC component of the HSC duty cycle (d_{H-AC}) can be calculated using f_{d-s}. As in the previous approach, this function depends on the particular DC–DC converter topology.

The HSC is the only DC–DC converter that must ensure a bandwidth equal or higher than f_{S-Max}. As a result, its switching frequency (f_{SW-H}) is high. Theoretically, the required f_{SW-H} is equal to the required f_{SW} of the approach described in Section III-B because, as in that case, the feedback loop does not limit the converter bandwidth. Therefore, the lowest f_{SW-H} value that can be used is determined only by the reactive elements of the power stage. If a very fast topology is used, f_{SW-H} can be reduced to a value that ranges between 3 and 6 times the f_{S-Max} value. As in the previous approach, the HSC will suffer

from high switching losses when the data rate requirement demands a communication signal with high bandwidth and, as a consequence, a high f_{SW-H}. However, the key point is that since the HSC only delivers the part of the power determined by the communication signal, which is significantly lower than the total power, the impact of those switching losses in the overall efficiency is mitigated. The rest of the power is delivered by the LSC, which can achieve high efficiency because the selection of its switching frequency (f_{SW-L}) is not subject to a high bandwidth requirement. Therefore, f_{SW-L} can be significantly lower than f_{SW-H}. Note that since the LSC only needs to track a constant current reference ($i_{O-DC\text{-}Ref}$), its design and efficiency are similar to those of a conventional HB-LED driver for lighting applications. In practice, the LSC will typically operate with f_{SW-L} in the range of hundreds of kHz, while the HSC will operate with f_{SW-H} in the MHz range. In summary, the power delivered by the HSC must be minimized in order to maximize the overall efficiency. It can be performed by selecting v_{O-H-DC} barely higher than the one that always ensures $v_{O-H} > 0$ V.

Another advantage of this approach is that the output-series connection enables an accurate reproduction of v_{O-AC} with relative ease. Since the HSC is focused on performing the small voltage variations while the LSC provides most of v_{O-DC}, the required duty cycle accuracy for each converter is not as critical as in the previous approaches.

Regarding the drawbacks, the two isolated input voltages required for the implementation (i.e., V_{G-H} and V_{G-L}) are the weakest point of the approach.

D. Selected DC–DC Converter Topologies

In this paper, a multi-phase asynchronous buck converter with P phases (P-phase buck converter) and a single-phase synchronous buck converter are considered as HSC and LSC, respectively (see Fig. 8). The multi-phase buck topology [44] was conceived to be used as voltage regulator modules for supplying microprocessors due to the high efficiency and bandwidth achieved [45], [46]. In addition, this topology is widely used as an envelope amplifier when the envelope tracking (ET) technique is used to increase the efficiency of a RF power amplifier [47]–[54]. These applications have some similarities with the HSC of the proposed VLC transmitter architecture: the output voltage level is low, the demanding bandwidth is very high, very low output voltage ripple is mandatory, and in the case of both ET and VLC, a certain voltage reference must be tracked. It is important to note that an M^{th} order low-pass filter is considered at the output of the P-phase buck converter. The use of a fourth or higher order output filter was already proposed in ET for reducing the output voltage ripple [51]–[59].

It is well known that driving floating MOSFET is difficult when f_{SW} is high. This problem appears in the conventional P-phase buck converter, where the MOSFETs source terminals are connected to nonconstant voltage points. However, in the proposed configuration, the MOSFETs source terminals are connected to the input voltage source negative terminal of the HSC (see Fig. 8). Thus, the MOSFETs driving task becomes easier if V_{G-H} is used

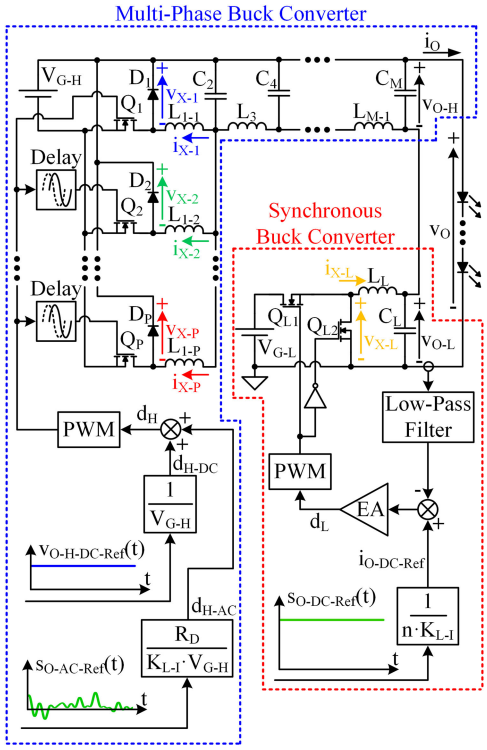


Fig. 8. HB-LED driver made up of a P-phase buck converter with an M^{th} order low-pass filter (HSC) and a single-phase synchronous buck converter a with second-order low-pass filter (LSC).

to supply the MOSFETs drivers of the HSC. Note that the position of the other HSC elements should be modified in order to properly perform the buck converter function.

Regarding the LSC, its requirements are less challenging than in the case of the HSC because it operates similar to a conventional HB-LED driver for lighting applications. In this sense, a single-phase synchronous buck converter with second-order low-pass filter provides all the characteristics required to fulfill the LSC target. As major advantages of this topology, the power stage is made up of few elements, it achieves high efficiency and its averaged model is very simple.

E. Steady-State Operation

Fig. 9(a) shows the equivalent circuit of the proposed HB-LED driver modeling $v_{X-1}, v_{X-2}, \ldots, v_{X-P}$ (i.e., the switch-node voltages of the HSC) and v_{X-L} (i.e., the switch-node voltage of the LSC) as ideal pulse voltage sources. Note that this assumption is valid when the HSC operates in a continuous conduction mode. In the case of the P-phase buck converter (i.e., the HSC), there are P switch-node voltages (i.e., $v_{X-1}, v_{X-2}, \ldots, v_{X-P}$) and each one has a particular delay (i.e., $t_{d-1}, t_{d-2}, \ldots, t_{d-P}$) with respect to the switch-node voltage of the first phase (i.e., v_{X-1}). Then, each ideal pulse voltage source can be modeled as

$$v_{X-i}\ (t) = v_{X-1}\ (t - t_{d-i})\,. \tag{9}$$

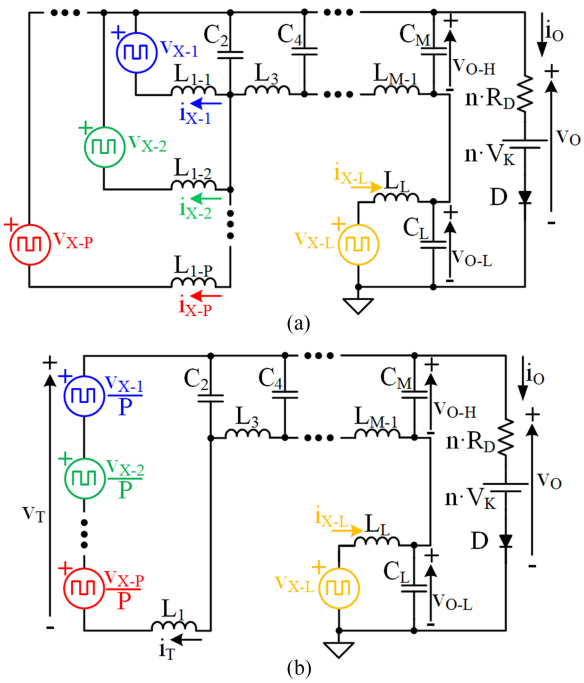


Fig. 9. Equivalent circuits of the proposed HB-LED driver. (a) Modeling $v_{X-1}, v_{X-2}, \ldots, v_{X-P}$ and v_{X-L} as ideal pulse voltage sources. (b) Applying the superposition and Thevenin's theorems.

Using a suitable delay pattern leads to a reduction of the output voltage ripple. In this way, the benefit of the P-phase structure arises when the delay pattern defined as follows is used:

$$t_{d-i} = \frac{(i\ -\ 1)\cdot T_{SW-H}}{P} \tag{10}$$

where T_{SW-H} is the switching period of the HSC.

In order to show the output voltage ripple reduction achieved by the P-phase structure, the superposition and Thevenin's theorems are applied to obtain the schematic depicted in Fig. 9(b). Note that it is assumed that $L_{1-1}, L_{1-2}, \ldots, L_{1-P}$ are identical, and consequently, L_1 is equal to L_{1-1}/P. In this way, an equivalent voltage source at the input of the equivalent HSC filter can be defined as

$$v_T(t) = \frac{1}{P}\sum_{i=1}^{P} v_{X-i}(t) = \frac{1}{P}\sum_{i=1}^{P} v_{X-1}(t - t_{d-i}). \tag{11}$$

Fig. 10 shows the main voltage waveforms of the proposed HB-LED driver assuming steady-state conditions. Note that T_{SW-L} is the switching period of the LSC. It can be seen that that due to the delay pattern indicated in (10), v_T has lower harmonic content than the switch-node voltages, and moreover, it is placed at higher frequencies. Thus, the filtering task is easier than in the case of a single-phase approach.

Another important point is that, as Fig. 10 shows, the total output voltage ripple is made up of the output voltage ripple of both converters (i.e., the P-phase buck converter and the synchronous buck converter). Then, it is essential to reduce not only the output voltage ripple of the HSC, but also the output voltage ripple of the LSC in order to minimize the distortion of the reproduced signal.

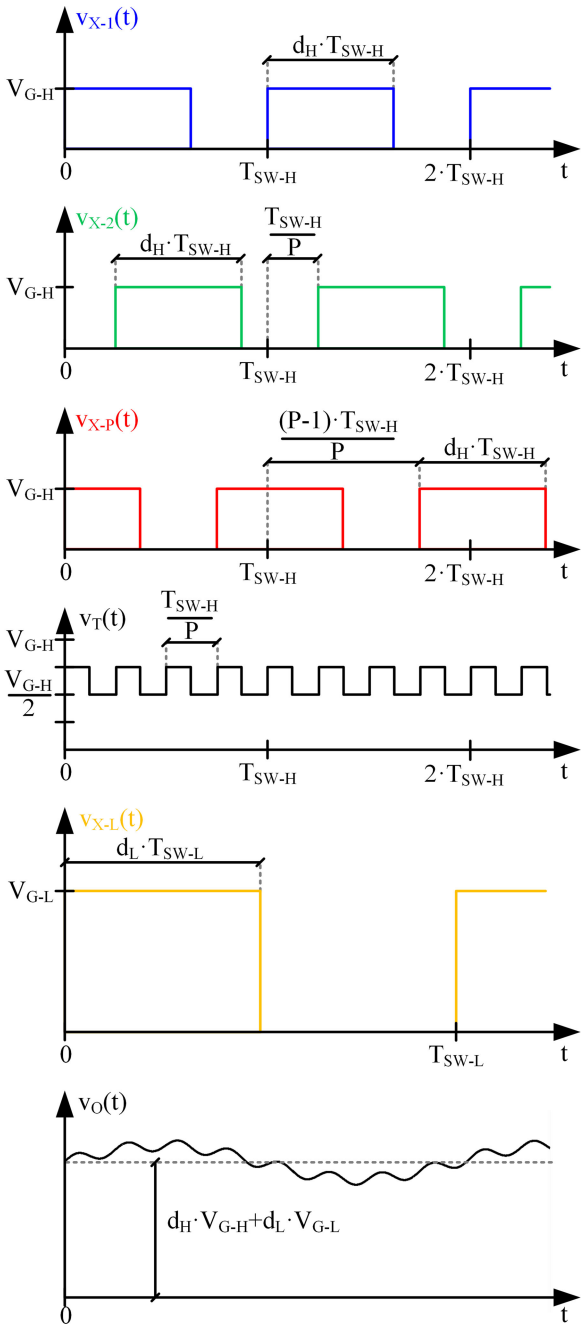


Fig. 10. Main voltage waveforms of the proposed HB-LED driver assuming steady-state conditions.

The reduction of the output voltage ripple achieved by the P-phase buck converter can also be understood from the main current waveforms. As Fig. 11 shows, the current delivered by each converter is identical (i.e., equal to i_O) due to the output-series connection. Moreover, it is very important to analyze the current of each HSC phase (i.e., $i_{X-1}, i_{X-2}, \ldots, i_{X-P}$) in order to understand the reduction of the output voltage ripple achieved by the P-phase structure. Assuming that all phase inductances are identical, the current ripple of each HSC phase will be equal.

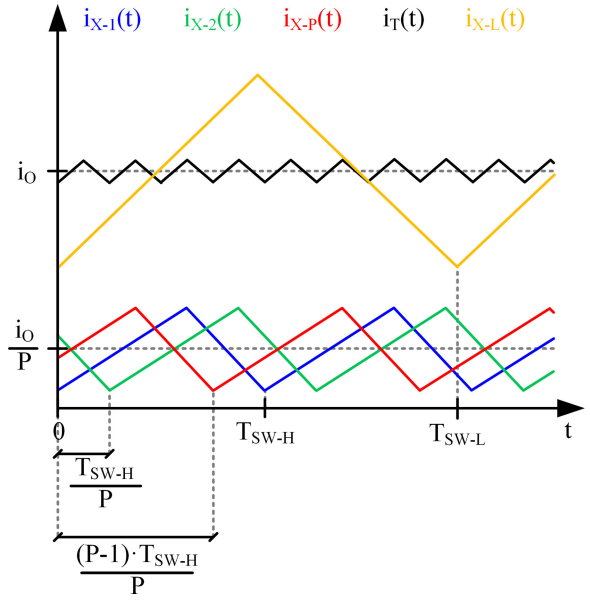


Fig. 11. Main current waveforms of the proposed HB-LED driver assuming steady-state conditions.

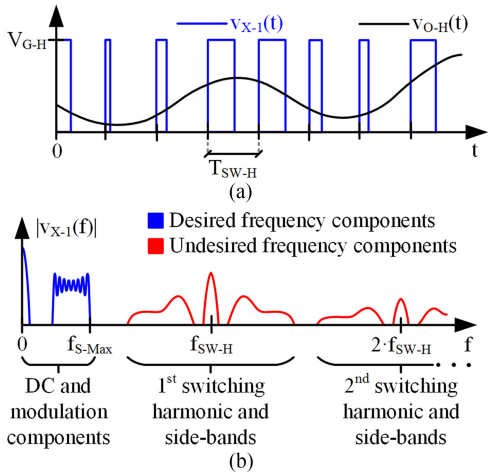


Fig. 12. Analysis of the relationship between the pulse-width modulated voltage at the first switch-node of the P-phase buck converter (i.e., v_{X-1}) and v_{O-H}. (a) Time-domain analysis. (b) Frequency-domain analysis.

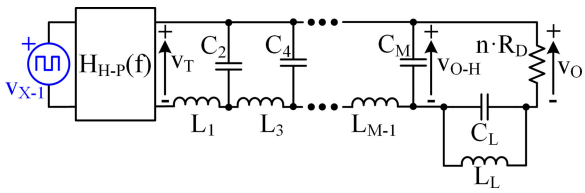


Fig. 13. Equivalent circuit of the proposed HB-LED driver that can be used to obtain $H_H(f)$.

In addition, the DC component of each phase current is i_O/P if the equivalent series resistances of all phase inductors are identical. Then, the inductor current of the i^{th} phase is delayed t_{d-i} with respect to the inductor current of the first phase (see Fig. 11). As a result, the sum of all phase currents (i.e., $i_T = i_{X-1} + i_{X-2} + \cdots + i_{X-P}$) has a lower ripple than in the case of a single phase.

F. Frequency-Domain Analysis

The steady-state analysis is a suitable initial step to study the general operating principle of the proposed HB-LED driver. However, the frequency-domain analysis must be carried out in order to deeply understand the P-phase buck converter operation, the synchronous buck converter operation, and their joint operation as a single HB-LED driver.

As previously explained, the P-phase buck converter is responsible for reproducing the communication signal with high accuracy. The operating principle is based on providing the desired v_{O-AC} from v_{X-1} [see Fig. 12(a)] by carefully filtering this pulse-width modulated voltage. Therefore, the transfer function between v_{X-1} and v_O [i.e., $H_H(f) = v_O(f)/v_{X-1}(f)$] must be analyzed. It is important to note that $H_H(f)$ must reject the switching harmonics together with their sidebands [see Fig. 12(b)]. Moreover, this transfer function must meet some additional requirements in order to avoid distortion when reproducing the signal reference. First, its magnitude must be flat in the desired frequency bands. Note that these frequency bands include the DC component and the frequency components that appear due to the duty cycle variation over time (i.e., the frequency components related to the modulation scheme that is being reproduced). Second, the phase-shift of $H_H(f)$ must be linear with the frequency in those regions, ensuring a constant group delay.

$H_H(f)$ will show the effect of the P-phase structure, the effect of the M^{th} order low-pass filter and the impact of the synchronous buck converter on the P-phase buck converter

$$H_H(f) = H_{H-P}(f) \cdot H_{H-F}(f) \cdot H_{H-L}(f) \qquad (12)$$

where $H_{H-P}(f)$ is the transfer function between v_{X-1} and v_T (i.e., the effect of the P-phase structure), $H_{H-F}(f)$ is the transfer function between v_T and v_{O-H} (i.e., the effect of the M^{th} order low-pass filter), and $H_{H-L}(f)$ is the transfer function between v_{O-H} and v_O (i.e., the impact of the synchronous buck converter). The equivalent circuit depicted in Fig. 13 can be used to analyze $H_H(f)$.

Starting with the M^{th} order low-pass filter, it is well known that it causes a magnitude drop for frequencies higher than the cutoff frequency (f_{C-H}). Therefore, f_{C-H} must be higher than the highest frequency component of the signal (i.e., f_{S-Max}). There is an important trade-off among f_{C-H}, f_{SW-H}, f_{S-Max}, and the order of the filter. f_{C-H} must be high enough to not distort the frequency components of the signal, and at the same time, it must be low enough to ensure enough rejection of the switching harmonics and their sidebands. In order to alleviate this problem, f_{SW-H} can be increased in exchange for higher switching losses. Another option consists in increasing the filter order. However, this is translated into higher complexity and cost. This issue has been deeply studied in [51] and [57] for the ET application, and the design guidelines included in these works are valid for the P-phase buck converter of the proposed HB-LED driver. As in

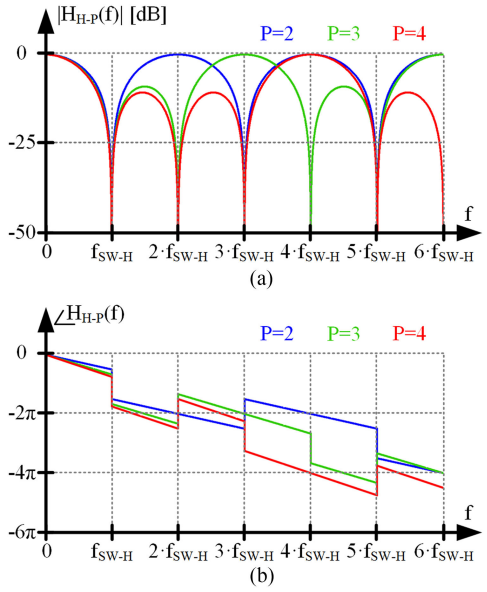


Fig. 14. $H_{H-P}(f)$ analysis. (a) Magnitude. (b) Phase.

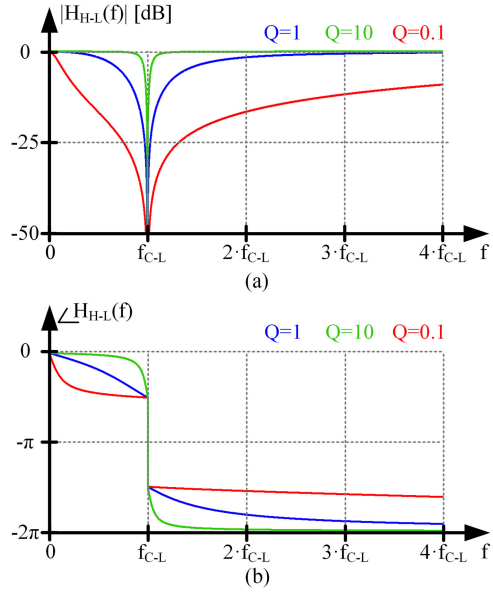


Fig. 15. $H_{H-L}(f)$ analysis. (a) Magnitude. (b) Phase.

[51] and [57], the source impedance of the filter is 0 Ω, and consequently, proper filter tables must be used. In this case, $n \cdot R_D$ must be considered as the load impedance of the filter.

Regarding $H_{H-P}(f)$ and according to (9)–(11), it can be defined as

$$H_{H-P}(f) = \frac{v_T(f)}{v_{X-1}(f)} = \frac{1}{P}\frac{\sin(\pi \cdot f \cdot T_{SW-H})}{\sin\left(\pi \cdot f \cdot \frac{T_{SW-H}}{P}\right)} e^{-j\cdot\pi\cdot f\cdot T_{SW-H}\cdot\left(\frac{P-1}{P}\right)}. \quad (13)$$

Then, the multi-phase structure introduces notch filters at some switching frequency harmonics, contributing to reduce the output voltage ripple. As Fig. 14 shows, the higher the number of phases, the higher the number of notch filters and the lower the output voltage ripple.

Regarding the impact of the synchronous buck converter on the P-phase buck converter, the output filter of the LSC also introduces a notch filter at its cutoff frequency (f_{C-L}). Fig. 15 shows $H_{H-L}(f)$ for different Q values of the synchronous buck converter filter keeping the same f_{C-L}. Note that the expression utilized for the Q factor evaluation is

$$Q = n \cdot R_D \cdot \sqrt{\frac{C_L}{L_L}}. \quad (14)$$

Finally, Fig. 16(a) shows $|H_H(f)|$ highlighting the different effects. This figure considers different number of phases and different LSC filter designs that keep the same f_{C-L} but change the Q factor. It is important to note that f_{Ref} represents the central frequency of the modulation scheme that is going to be reproduced. The rest of the signal components would be placed around f_{Ref}. It can be seen that the available frequency band for the communication signal depends on the Q factor of the LSC filter. Note that in Fig. 16(a), the identification of the available frequency band only considers the amplitude distortion. However, the phase distortion also plays an important role [see Fig. 16(b)]. Therefore, the relative variation of the group delay with respect to the group delay at f_{Ref} [i.e., $\tau_{R-Ref}(f)$] must be evaluated

$$\tau_{R-Ref}(f) = \frac{[\tau(f) - \tau(f_{Ref})]}{\tau(f_{Ref})} \quad (15)$$

where $\tau(f)$ is the group delay of $H_H(f)$. The actual available frequency band is the smallest of both approaches (i.e., considering the amplitude and the phase distortion) and it depends on the limits employed to identify the bands. In other words, the maximum attenuation permitted in the case of the amplitude distortion and the maximum relative variation of the group delay permitted in the case of the phase distortion. In any case, it can be concluded that a high Q factor is desirable for maximizing the available frequency band. Moreover, f_{C-L} must be placed between the DC component and the lowest harmonic of the reproduced modulation scheme.

Regarding the synchronous buck converter, how it is affected by the P-phase buck converter when it tries to control i_O must be analyzed. There are several transfer functions that can be calculated in order to address this point. In this paper, the transfer function between the duty cycle (i.e., d_L) and i_O [$G_{dL-i}(f)$] is obtained and studied by using the equivalent circuit depicted in Fig. 17.

Fig. 18 shows $G_{dL-i}(f)$ for different Q values of the synchronous buck converter filter, highlighting the impact of the P-phase buck converter. It can be seen that the output impedance of the HSC introduces certain notch filters at high frequencies. Fortunately, this fact has a minor impact on the current feedback loop, and consequently, the synchronous buck converter can be designed similarly to a conventional HB-LED driver for lighting applications. It is important to note that the low-pass filter of the feedback loop must be taken into account for designing the regulator. The cutoff frequency of this low-pass filter should

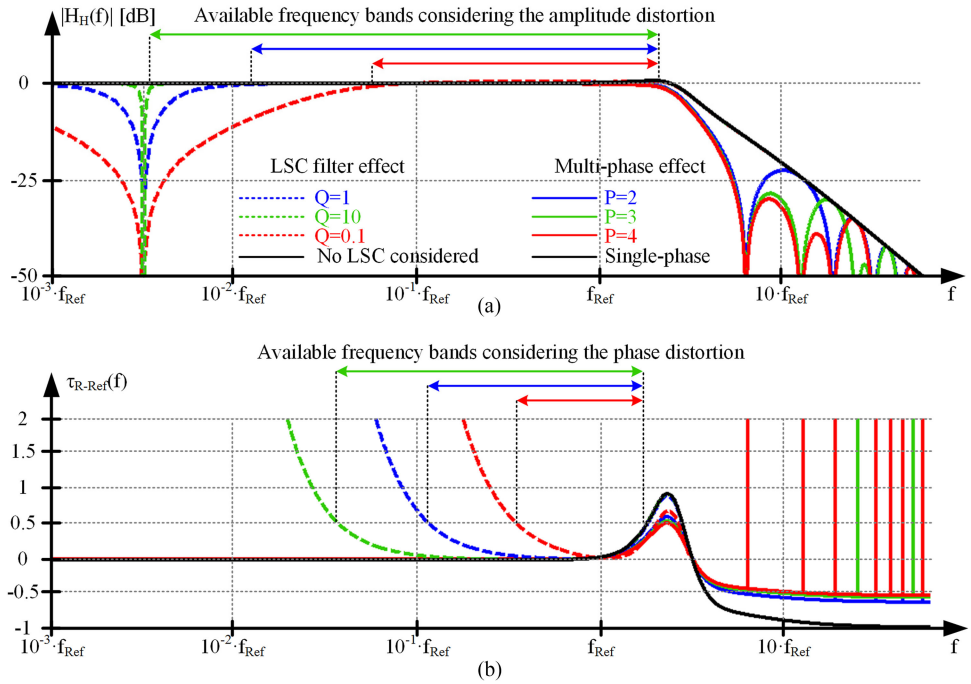


Fig. 16. $H_H(f)$ analysis. (a) Magnitude. (b) Relative variation of the group delay with respect to the group delay at f_{Ref}.

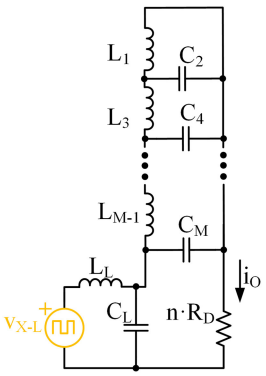


Fig. 17. Equivalent circuit of the proposed HB-LED driver that can be used to obtain $G_{dL-i}(f)$.

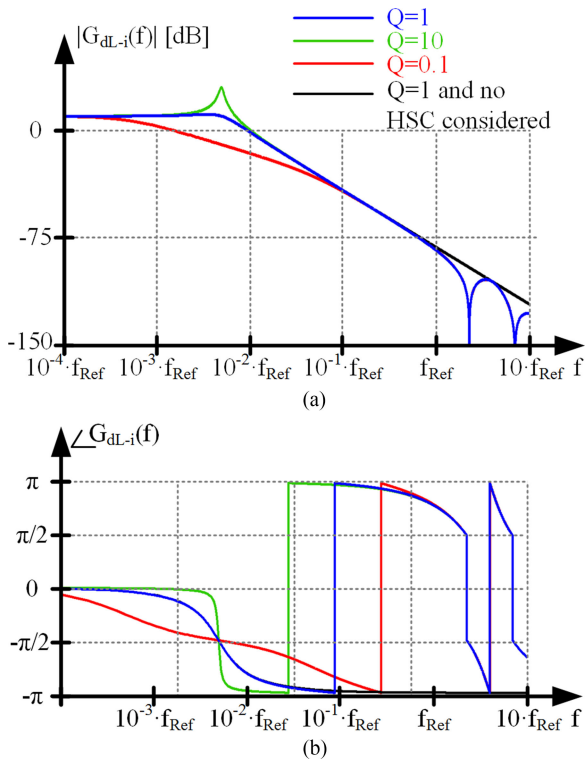


Fig. 18. $G_{dL-i}(f)$ analysis. (a) Magnitude. (b) Phase.

be as low as possible, but at the same time, high enough to not jeopardize excessively the bandwidth of the feedback loop. In general, this point is not an issue, and in practice, a cutoff frequency similar to f_{C-L} fulfills the application requirements.

G. Design Guidelines

The recommended steps for the design of the proposed VLC transmitter are described in this section. The design specifications should include the maximum lighting level ($s_{O-DC-Max}$) and the modulation scheme that must be reproduced together with the maximum power of the communication signal, thus defining s_{O-AC} for the highest communication power. It is important to note that the modulation scheme does not determine the communication signal power because it only determines the shape of the signal. The same signal can be transmitted with different power levels (i.e., more or less amplification) depending on the particular application requirements.

Step 1: Dimensioning the HB-LED string. The number of HB-LEDs of the string (i.e., n) can be calculated by taking into account $s_{O-DC-Max}$, the dynamic resistance (i.e., R_D),

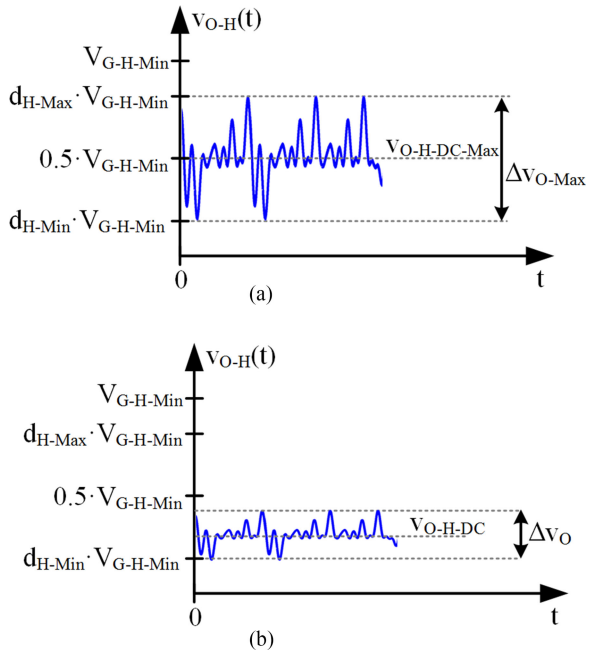


Fig. 19. v_{O-H} for two communication power levels using $V_{G-H} = V_{G-H-Min}$. (a) Maximum communication power. (b) Lower communication power.

and the knee voltage (i.e., V_K) of the HB-LEDs selected for the implementation.

Step 2: Characterization of i_{O-AC} *and* v_{O-AC} *for the highest communication power*. i_{O-AC} and v_{O-AC} for the highest communication power ($i_{O-AC-Max}$ and $v_{O-AC-Max}$, respectively) can be obtained by considering (1), (2), and the equivalent dynamic resistance of the HB-LED string selected in step 1 (i.e., $n{\cdot}R_D$). After that, the peak-to-peak value of v_O (Δv_O) for the highest communication power (Δv_{O-Max}) can be calculated from $v_{O-AC-Max}$.

Step 3: Determining V_{G-H}. It is important to note that the lower the V_{G-H} value, the lower the duty cycle accuracy required to generate v_{O-H}, and as a consequence, the lower the demanded time resolution of the field programmable gate array (FPGA). Therefore, it is essential to determine the minimum V_{G-H} value ($V_{G-H-Min}$) that could to be used. The duty cycle of the P-phase buck converter (i.e., d_H) must be always lower than a maximum value (d_{H-Max}) and higher than a minimum value (d_{H-Min}) that are established due to safety reasons. For the sake of simplicity, the same safety margin is considered for both duty cycle limits (i.e., $d_{H-Min} = 1 - d_{H-Max}$). Note that Fig. 19 can be used to understand the reasoning related to step 3. Under the aforementioned considerations and when the converter operates with the maximum communication power, the following equation can be used to determine $V_{G-H-Min}$:

$$d_{Max} \cdot V_{G-H-Min} = d_{Min} \cdot V_{G-H-Min} + \Delta v_{O-Max}. \tag{16}$$

Therefore, V_{G-H} must satisfy the following condition:

$$V_{G-H} \geq V_{G-H-Min} = \frac{\Delta v_{O-Max}}{1 - 2 \cdot d_{Min}}. \tag{17}$$

It is important to note that v_{O-H-DC} is defined as

$$v_{O-H-DC} = d_{Min} \cdot V_{G-H} + \frac{\Delta v_O}{2}. \tag{18}$$

As a result, the following condition is always satisfied:

$$v_{O-H} \geq d_{Min} \cdot V_{G-H} > 0\ V. \tag{19}$$

The maximum value of v_{O-H-DC} is reached when the communication power is the highest one

$$v_{O-H-DC-Max} = 0.5 \cdot V_{G-H-Min}. \tag{20}$$

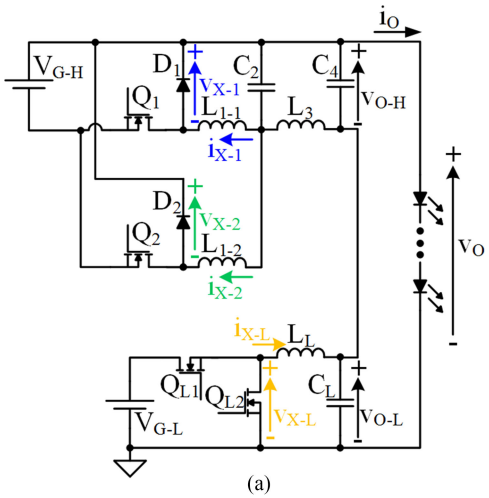
Step 4: Selecting the number of phases (i.e., P) and the order of the filter (i.e., M*)*. As is explained in Section III-F, both the multi-phase effect and the high-order output filter contribute to reduce the output voltage ripple. Therefore, both points must be addressed together. Obviously, the higher the number of phases, the lower the required order of the filter and vice versa. As a consequence, there are several solutions (i.e., several combinations of P and M) that, showing similar complexity (which could be evaluated using P + M), ensure a certain level of output voltage ripple rejection. In order to select the most appropriate solution for the particular requirements of the VLC transmitter, parameters that are difficult to be measured, such as the dependence of the cost or of the size on P and M, must be taken into account. In any case, it is recommendable to follow the directions of [51] and [57] for determining M and the cutoff frequency of the filter (i.e., f_{C-H}) once P is selected.

Step 5: Designing the synchronous buck converter. In the case of the synchronous buck converter, the input voltage (i.e., V_{G-L}) can be selected according to standard voltage values such as 24 or 48 V. As is explained in Section III-F, the cutoff frequency of the filter (i.e., f_{C-L}) should be lower than the minimum frequency of the communication signal that the P-phase buck converter is going to reproduce. In addition, the Q value of the filter should be high enough to avoid the distortion of the communication signal. The design of the feedback loop is straightforward.

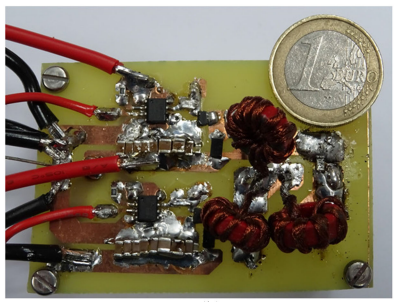
IV. Experimental Results

A. Prototype Details

A two-phase asynchronous buck converter and a single-phase synchronous buck converter were built to test experimentally the proposed HB-LED driver (see Fig. 20). The switching frequency of the two-phase buck converter and the synchronous buck converter is 10 MHz and 250 kHz, respectively. The output filter of the HSC is a fourth-order Butterworth filter with a cutoff frequency equal to 4 MHz. In the case of the LSC, the cutoff frequency of the second-order filter is 20.5 kHz and the Q value is 1.56. Table I shows the passive components used for the filters. The inductors of the HSC are implemented with iron powder cores (T50-2) from Micrometals. A SER1390-333 MLB inductor from Coilcraft is used for the inductor of the LSC. The low-pass filter of the feedback loop is implemented with an RC filter whose cutoff frequency is 15.9 kHz. Silicon MOSFETs are



(a)



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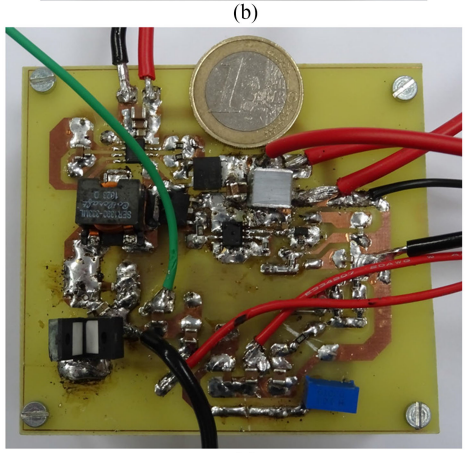

(c)

Fig. 20. Two-phase buck converter with a fourth-order Butterworth filter in output-series connection with a synchronous buck converter. (a) Schematic circuit of the implemented HB-LED driver. (b) Two-phase buck converter prototype. (c) Synchronous buck converter prototype.

used in both converters: SSM3K336R in the two-phase buck converter and TK7S10N1Z in the synchronous buck converter. In both cases, the MOSFETs are driven by EL7156 ICs. Schottky diodes DB2430500L are used in the HSC. The load is made up of six HB-LEDs (W42180 Seoul Semiconductor) connected in series. The input voltage of the two-phase buck converter and the synchronous buck converter is 8.5 and 24 V, respectively. PDA10A-EC is used as the receiver of the VLC setup. Since this device is made up of a photodiode and a transconductance amplifier, its output signal is a voltage waveform proportional to the received light intensity.

TABLE I
PASSIVE COMPONENTS USED FOR THE OUTPUT FILTERS

Component	$L_{1\text{-}1}$ (nH)	$L_{1\text{-}2}$ (nH)	C_2 (nF)	L_3 (nH)	C_4 (nF)	L_L (μH)	C_L (μF)
Value	812	812	9.4	287.1	2.3	33	1.818

Regarding the communication signal, a 64-QAM-OFDM scheme that is made up of 29 carriers is reproduced. It is important to note that the maximum frequency component of the reproduced modulation scheme (i.e., f_{S-Max}) is around 3 MHz. The sequence of duty cycle values that the HSC requires to reproduce the communication signal (i.e., d_H) is stored in the FPGA that controls the two-phase buck converter.

B. Evaluation of the Trade-off Between Communication Efficiency and Power Efficiency

In order to deeply evaluate the performance of the HB-LED driver prototype, it is tested under different operating conditions. The test target is to study how the lighting level and the communication signal power affect both the power efficiency and the communication efficiency. Obviously, the lighting level depends on the average current through the HB-LED string (i.e., i_{O-DC}). Regarding the communication signal power, it can be controlled by adjusting the peak-to-peak value of v_O (i.e., Δv_O).

Two lighting levels (determined by $i_{O-DC} = 300$ and 500 mA) and two levels of the communication signal power (determined by $\Delta v_O = 4.1$ and 2.2 V) are considered. As a result, there are four possible situations (see Table II). It is important to note that the distance between the transmitter and the receiver is 20 cm in all situations. Fig. 21 exemplifies the performed test and facilitates the understanding of the reasoning that will appear in this section.

Fig. 22 shows the main waveforms of the VLC system for each situation. Note that v_{RX} is the receiver signal. The DC component of v_{RX} (v_{RX-DC}) measures the lighting level, while the peak-to-peak value (Δv_{RX}) is determined by the received communication signal power. Table II indicates both the DC component and the peak-to-peak value of each waveform. Note that Δi_O is the peak-to-peak value of i_O. In addition, it shows the amount of power delivered by the two-phase buck converter (P_{O-H}) and by the synchronous buck converter (P_{O-L}), the efficiency of the two-phase buck converter (η_H), the efficiency of the synchronous buck converter (η_L), the overall efficiency (η), and a figure-of-merit for evaluating the communication efficiency that will be introduced below.

In situation 1, i_{O-DC} and Δv_{O-AC} are 500 mA and 4.1 V, respectively. Note that as indicated in Section II, v_{O-AC} is small in comparison to v_{O-DC}. It can be seen that most of v_{O-DC} is delivered by the synchronous buck converter. In this situation, the power of the HB-LED driver is 10.1 W, 81% of the power

TABLE II
MAIN PARAMETERS OF THE TEST PERFORMED TO EVALUATE THE TRADE-OFF BETWEEN COMMUNICATION EFFICIENCY AND POWER EFFICIENCY

	$i_{O\text{-}DC}$ (mA)	Δi_O (mA)	$v_{O\text{-}DC}$ (V)	Δv_O (V)	$v_{O\text{-}L}$ (V)	$v_{RX\text{-}DC}$ (mV)	Δv_{RX} (mV)	$P_{O\text{-}L}$ (W)	$P_{O\text{-}H}$ (W)	P_O (W)	η_L (%)	η_H (%)	η (%)	EVM_{RMS} (%)
Situation 1	500	750	19.9	4.1	16.1	34	29	8.19	1.24	10.1	92.8	79.2	91.3	22.3
Situation 2	300	575	19	4.1	15.2	23	25	4.64	1.23	5.87	89.7	84.5	88.6	27.6
Situation 3	500	350	19.9	2.2	18.2	34	15	9.56	0.52	10.08	94.8	75.7	93.6	23.2
Situation 4	300	300	19	2.2	17.3	23	15	5.31	0.51	5.82	92.4	81.3	91.3	24

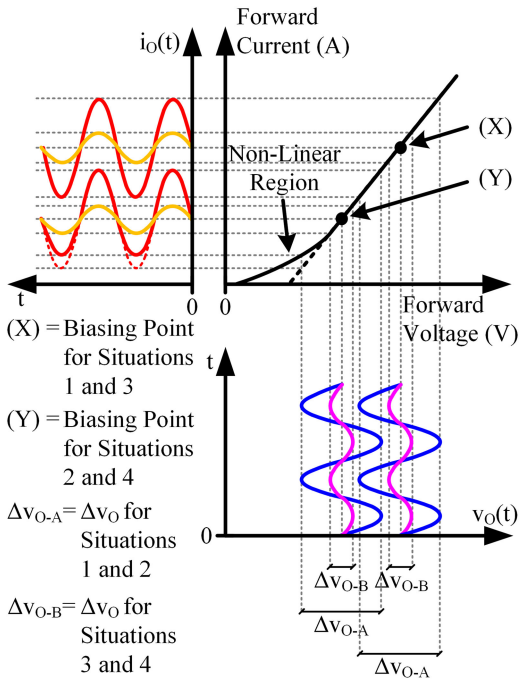

Fig. 21. Graphical description of the test considering the I–V curve of the HB-LED string and sinusoidal waveforms.

is provided by the synchronous buck converter, and the overall efficiency is 91.3%.

Comparing situation 2 to situation 1 allows us to study the impact of decreasing the lighting level on the power efficiency of the HB-LED driver (i_{O-DC} falls from 500 to 300 mA). In order to achieve the lower biasing point, the synchronous buck converter decreases its output voltage, and as a result, the amount of power delivered by this converter falls. It is important to note that since the communication signal power is the same, the peak-to-peak values of the waveforms are the same as in situation 1, and consequently, the operating conditions of the two-phase buck converter are almost the same. Actually, Δi_O and Δv_{RX} slightly change because the transmitter partially works in the nonlinear region of the HB-LED string. It can be easily understood seeing Fig. 21. How this fact affects the communication will be addressed below. Taking into account all these considerations, the weight of the synchronous buck efficiency on the

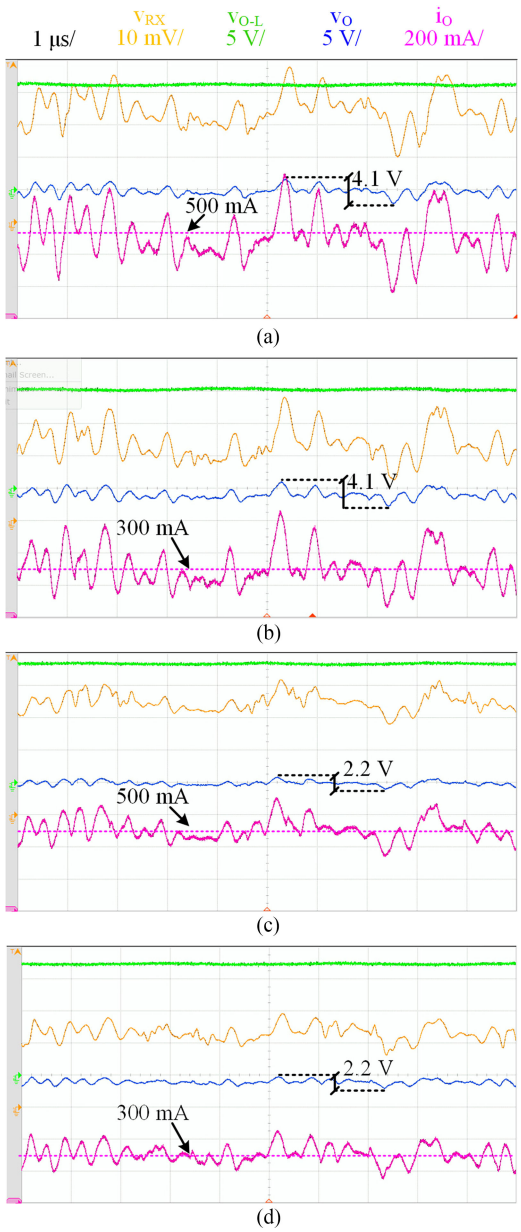

Fig. 22. Main experimental waveforms of the VLC system during the test performed to evaluate the trade-off between communication efficiency and power efficiency. (a) Situation 1. (b) Situation 2. (c) Situation 3. (d) Situation 4.

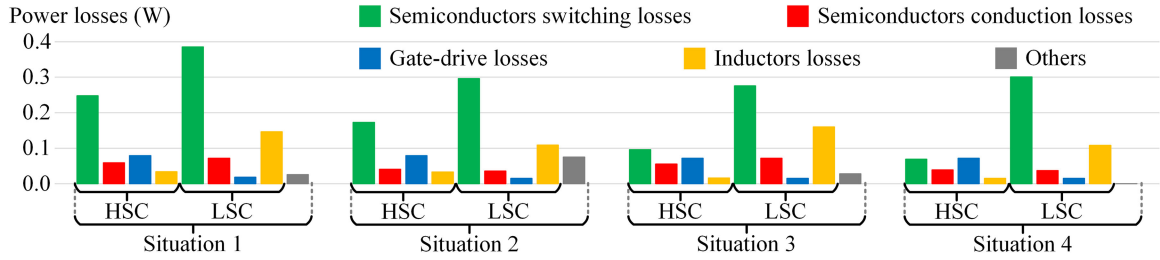

Fig. 23. Estimation of the power losses distribution in the components of the experimental VLC transmitter for each operating situation.

overall efficiency is lower in situation 2 than in situation 1, and consequently, the overall efficiency falls.

In order to study the impact of reducing the communication signal power on the power efficiency of the HB-LED driver, situation 3 can be compared to situation 1 (Δv_{O} falls from 4.1 to 2.2 V). All the peak-to-peak values of the waveforms change, while the values of i_{O-DC}, v_{O-DC}, and v_{RX-DC} are the same as in situation 1. However, it is important to note that the output voltage of the synchronous buck converter is higher in the case of situation 3. It is because the AC voltage provided by the two-phase buck converter is lower in this situation, so its DC voltage is reduced to minimize the power that it delivers. Consequently, the synchronous buck converter increases its output voltage to achieve the desired lighting level. As Table II shows, the total power of the HB-LED driver is almost the same in situation 1 and in situation 3, but the power share is different. It can be seen that in situation 3, the power provided by the synchronous buck converter (94.8% of the total power) is higher than in situation 1, and as a result, the overall efficiency rises.

Finally, the remaining case appears in situation 4, where both the lighting level and the communication signal power fall (i_{O-DC} falls from 500 to 300 mA and Δv_{O} falls from 4.1 to 2.2 V). In this situation, the power of the HB-LED driver is 5.82 W, the synchronous buck converter delivers 91.2% of the total power, and the overall efficiency is 91.3%.

Fig. 23 shows an estimation of the losses distributed in the components of the experimental prototype for each operating situation. It can be seen that although P_{O-H} is much lower than P_{O-L} in all operating situations (see Table II), the semiconductor switching losses of the two-phase buck converter are one of the major sources of power losses.

In summary, minimizing the communication signal power and maximizing the lighting level are the best strategy for achieving the highest power efficiency. This conclusion fits in with the efficiency of the convereters because the strategy leads to minimize the power delivered by the HSC and to maximize the power delivered by the LSC. In this way, the overall efficiency of the HB-LED driver is mainly determined by the LSC efficiency.

However, the impact of both the lighting level and the communication signal power on the communication efficiency must also be evaluated to show a more general vision of the VLC transmitter performance. Basically, the communication efficiency depends on two parameters: the distortion and the power of the received signal. In general, the higher the power of the received signal, the higher the communication efficiency because the signal can be demodulated easier. Obviously, the higher the signal distortion, the lower the communication efficiency.

The error vector ($\bar{e}$) is employed to measure the accuracy of the communications system

$$\bar{e} = \bar{W} - \bar{V} \tag{21}$$

where $\bar{W}$ is the received symbol and $\bar{V}$ is the ideal symbol. Note that a symbol is a vector whose magnitude and direction are determined by the amplitude and the phase of a certain sinusoid. The modulation scheme defines the possible symbols (i.e., the amplitude and phase combinations that the sinusoid can have) and the bit sequence that univocally identify each one. In this way, the transmission of a particular symbol leads to the transmission of a particular bit sequence and, consequently, the transmission of information. The reproduced 64-QAM-OFDM scheme is made up of several carriers (i.e., sinusoidal waveforms with different frequencies), and each one transmits a symbol (i.e., each one has a particular amplitude and a particular phase) during a certain time interval, which is referred as symbol period (T_{Sym}). The $\bar{e}$ calculation is used to evaluate the performance of the communication system by evaluating the error vector magnitude (EVM_{RMS}) [60]. This widely used figure-of-merit evaluates $\bar{e}$ for each carrier during a sequence of several symbol periods considering the average power of the involved symbols

$$EVM_{RMS} = \sqrt{\frac{\sum_{n=1}^{N}\sum_{k=1}^{C}|\overline{e_{n,k}}|^2}{\sum_{n=1}^{N}\sum_{k=1}^{C}|\overline{V_{n,k}}|^2}} \tag{22}$$

where N is the number of symbols periods and C is the number of carriers. The lower the EVM_{RMS} value, the higher the communication efficiency. Typically, a value around 5–15% is required to fulfill the requirements of commercial wireless communication systems. Table II shows the EVM_{RMS} value obtained in each situation. It can be seen that the measured values do not accomplish with the communication standards. However, as explained in Section IV-C, this issue can be solved by adjusting the communication speed to the particular communication scenario where the VLC system is evaluated.

The best result is obtained when i_{O-DC} is 500 mA and Δv_{O} is 4.1 V (i.e., situation 1). If the lighting level is considerably reduced (i.e., the situation changes from 1 to 2), EVM_{RMS} rises dramatically although the communication signal power is the same. The reason is that the HB-LED string must be operating in the current–voltage linear region to properly reproduce

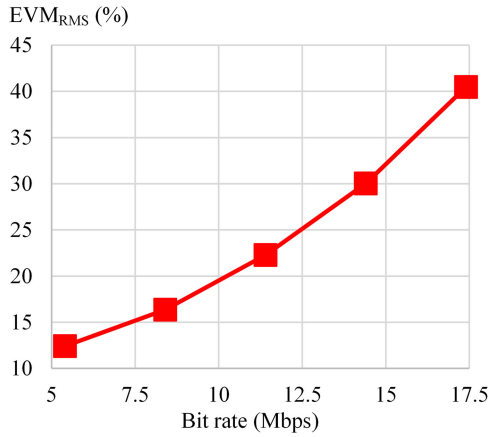

Fig. 24. EVM_{RMS} for different bit rates when the VLC system is evaluated in the laboratory setup and it operates in situation 1.

the communication signal. However, Δv_O is too high for the i_{O-DC} value considered in situation 2 (Fig. 21 may help to understand this phenomena). Thus, the HB-LEDs operate close to V_K, where the nonlinear current–voltage relation causes high signal distortion. Then, the communication signal power should be reduced when considering the lighting level of situation 2 in order to avoid the nonlinear region. In this way, EVM_{RMS} can be improved by reducing Δv_O. It is equivalent to move from situation 2 to situation 4. It can be seen that, as expected, EVM_{RMS} is lower than in the case of situation 2 because it reduces the distortion caused by the nonlinear operation. However, since the communication signal power is lower than in the case of situation 1, EVM_{RMS} is not as low as in that situation. Finally, EVM_{RMS} can be reduced a bit by increasing the lighting level (i.e., moving from situation 4 to situation 3) in order to completely avoid the nonlinear operation.

As a conclusion, there is trade-off between power efficiency and communication efficiency. For a particular lighting level, the communication signal power must be the maximum possible without operating in the nonlinear region in order to maximize the communication efficiency. However, from the power efficiency perspective, the best results are obtained when the communication signal power is minimized.

C. Bit Rate Evaluation

The reproduced 64-QAM-OFDM scheme is made up of 29 carriers. The lowest carrier frequency and the highest carrier frequency are 200 kHz and 3 MHz, respectively. Each carrier provides a bit rate equal to 600 kbps, and consequently, the maximum bit rate achieved by this modulation scheme is 17.4 Mbps. However, the speed of the communication signal must be evaluated together with EVM_{RMS} in order to show a consistent result. It is important to note that, in general, the higher the communications speed, the higher the number of transmission errors. However, the actual values of these two parameters depend on the communication scenario, which, in addition, changes over time. One of the advantages of OFDM schemes is that the communication speed can be dynamically

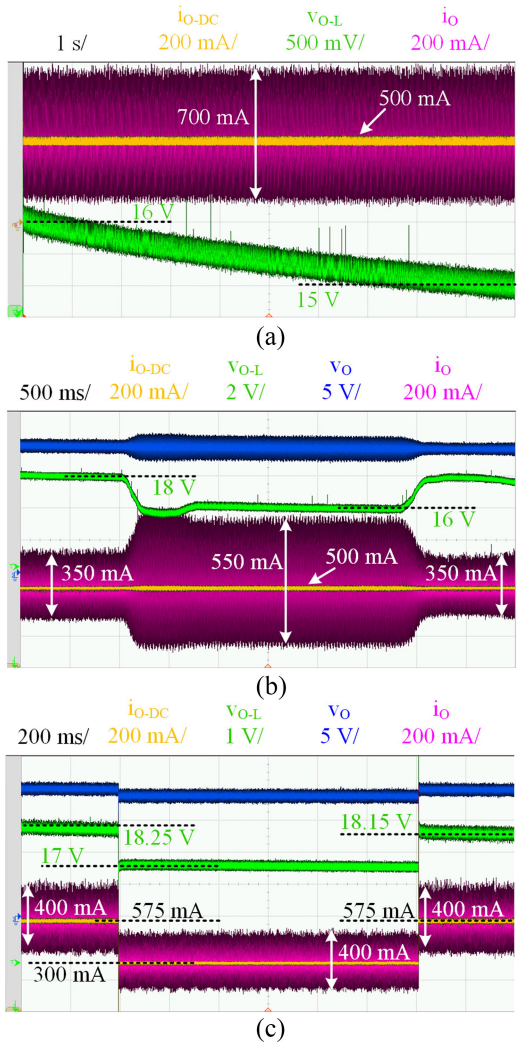

Fig. 25. Main experimental waveforms of the VLC system during the feedback loop tests. (a) Compensation of the V_K fall with T_J. (b) Response to two changes of the communication signal power. (c) Response to two changes of the lighting level.

adjusted to reduce EVM_{RMS}. This is performed by deactivating the carriers that are causing more transmission errors.

Fig. 24 shows the measured relationship between EVM_{RMS} and bit rate when the VLC system is evaluated in the laboratory setup and it operates in situation 1. It can be seen that EVM_{RMS} is too high for the maximum speed. Therefore, for this particular communication scenario, a bit rate lower than 7.5 Mbps should be used to accomplish with most extended communication standards (i.e., $EVM_{RMS} \leq 15\%$).

D. Feedback Loop Tests

Several tests have been carried out in order to check the feedback loop behavior of the implemented HB-LED driver. Fig. 25(a) shows how the synchronous buck converter reduces its output voltage in order to compensate the fall of V_K with T_J. Thus, both i_{O-DC} and Δi_O remain constant over time. Note that for this test, the HB-LEDs heatsink was removed to see a considerable change during a short period of time.

Fig. 25(b) shows the results when two changes in the communication signal power are performed. When the increase of the communication signal power occurs, the two-phase buck increases not only the AC component of its output voltage but also the DC component. Remember that the DC component of the two-phase buck converter output voltage is adjusted to provide the minimum value that enables the reproduction of the AC component. As a consequence, the synchronous buck converter reduces its output voltage to compensate the change.

Finally, Fig. 25(c) shows the results when two changes in the lighting level are performed. It can be seen how the synchronous buck converter modifies its output voltage to track the desired lighting level.

V. Conclusion

Although VLC is an application with high potential for alleviating the congestion of the RF spectrum, it has some bottlenecks that are slowing down its deployment. One of the most important problems is the low power efficiency of the HB-LED drivers proposed for reproducing advanced modulation schemes. The use of DC–DC converters seems to be the solution for solving the problem. However, the high bandwidth required for reproducing waveforms of several MHz causes that conventional HB-LED drivers for lighting applications cannot be directly adopted.

An HB-LED driver made up of a multi-phase buck converter with a high-order output filter in output-series connection with a synchronous buck converter is presented and deeply evaluated in this work. The multi-phase buck converter achieves high bandwidth operating in open-loop with high switching frequency. In this way, it is responsible for performing the small voltage variations (i.e., the communication signal component). On the other hand, the synchronous buck converter operates in close-loop ensuring that the desired lighting level is achieved. The split of the power enables the maximization of the power efficiency by minimizing the power that the multi-phase buck converter must deliver in each possible communication scenario. Moreover, the output-series connection enables an accurate reproduction of the communication signal with relative ease.

The joint operation of both converters is studied, focusing the attention on the multi-phase effect, the high-order output filter effect, and the impact of each converter on the other. It is concluded that the multi-phase structure supports the filtering task by reducing the output voltage ripple, whereas high Q factors of the synchronous buck converter filter are desirable for reducing the signal distortion. Moreover, the multi-phase buck converter has a minor impact on the synchronous buck operation, and consequently, its design is similar to conventional HB-LED drivers for lighting applications.

The wide experimental section allows us to analyze the trade-off that exists between communication efficiency and power efficiency. The key point is that for a particular lighting level, the power efficiency falls when the communication signal power rises. However, from the communication perspective, the communication signal power must be the maximum possible without operating in the nonlinear region.

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