# Nonisolated High-Step-up DC–DC Converter With Minimum Switch Voltage Stress

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***Abstract*—A new high-step-up dc–dc converter topology combining a charge pump mechanism with a standard inductor-based buck cell is presented here. Its main advantages are minimum switch voltage stress, given by the input voltage, and reduced energy in the magnetic element compared to a conventional boost converter designed for the same voltage gain. The proposed topology is derived through a modification of the basic voltage-doubler charge pump cell that, thanks to a coupled inductor, allows to make the flying capacitor voltages dependent on the switch duty cycle. Both capacitor charging and discharging paths benefit from the inherent leakage inductance of the coupled inductor, with consequent soft diode turn OFF with no reverse recovery problems and ringing free operation. A proper design of the buck inductance permits a quasi-square-wave operation, thus allowing a zero-voltage turn ON of the switches. Suitable design criteria are proposed so as to achieve the desired converter operation mode, without need for any iterative process. Experimental results based on a 44–400 V, 300−W prototype confirm the theoretical analysis and expectations, showing a quite flat efficiency curve that stays above 90% down to one tenth of the nominal power.**

***Index Terms*—Boost converters, charge pump circuits, high-step-up dc–dc converters.**

## I. Introduction

THE need for high-step-up dc–dc converters to be used as interfaces between low-voltage, high-current renewable energy sources, such as fuel cells and photovoltaic modules, and a common high-voltage dc bus in distributed generation systems, has boosted the research efforts toward solutions capable of overcoming the limitations of the conventional boost topology. The high voltage gain can be achieved exploring different approaches, such as using charge pump circuits, voltage multiplier cells, magnetic coupling, voltage lift, etc. A quite vast overview of the different techniques can be found in [1]–[6].

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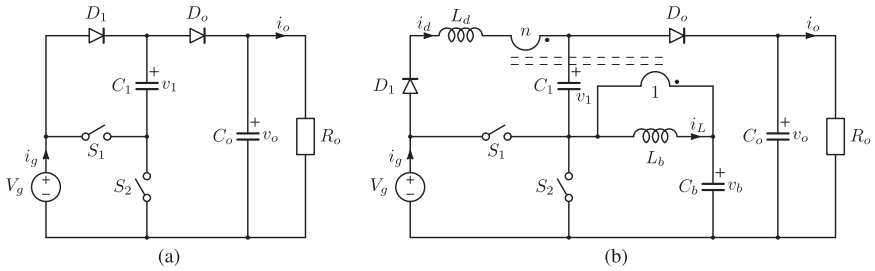


Fig. 1. Topology derivation. (a) Basic voltage-doubler SC cell. (b) Modified topology for higher voltage gains.

proposed topology useful for interfacing single photovoltaic panels with a high dc-link voltage in microinverter applications.

In Section II, the derivation of the proposed converter is outlined, while Section III describes in detail its operation. Section IV derives useful equations to estimate component current and voltage stresses, and Section V reports a simple, noniterative design procedure to calculate all the component values.

Experimental results, taken on a 44–400 V, 300 W prototype, are included in Section VI showing the performance of the proposed high-step-up topology.

## II. Topology Derivation

Starting from the basic voltage-doubler SC cell shown in Fig. 1(a), the first step toward the proposed high-step-up topology is shown in Fig. 1(b). In order to charge $C_1$ to a voltage dependent on the switch $S_1$ duty cycle $D$, an $L_b$–$C_b$ filter is added in parallel to $S_2$, thus forming an equivalent buck cell, and a secondary winding is coupled to the filter inductor, with turns ratio $n$, and put in series with $D_1$. In this way, an equivalent voltage source, represented by the transformer secondary winding, is added in the $C_1$ charging path during $S_2$ ON interval. This voltage is a function of the converter duty cycle, being related to the buck capacitor voltage $v_b$. Assuming a unity efficiency and neglecting the transformer leakage inductance, the capacitor average voltages are $V_b = DV_g$ and $V_1 = (1 + nD)V_g$. Consequently, the ideal voltage gain results

$$M = \frac{V_o}{V_g} = \frac{V_g + V_1}{V_g} = 2 + nD. \tag{1}$$

Moreover, the *charge balance* condition at a steady state for the capacitors yields $\bar{i}_{Do} = \bar{i}_d = I_o$ and $\bar{i}_L = nI_o$.

In the circuit shown in Fig. 1(b), the coupled windings introduce a nonnegligible leakage inductance $L_d$ that helps to shape the $C_1$ charging current during the $S_2$ conduction interval. However, in the output capacitor charging phase ($S_1$ conduction interval), only component and layout parasitic inductors in the current path are present: the associated small value is not enough to limit the current peak during this phase, unless huge capacitance values are used. Even more problematic is the high-frequency resonance that starts, at the $D_1$ turn-OFF instant, between the diode junction capacitance and the coupled inductor leakage inductance $L_d$, that causes a severe voltage stress and EMI generation.

For these reasons, the topology is modified as shown in Fig. 2, adding one more capacitor–diode branch $C_2$–$D_2$. In this way,

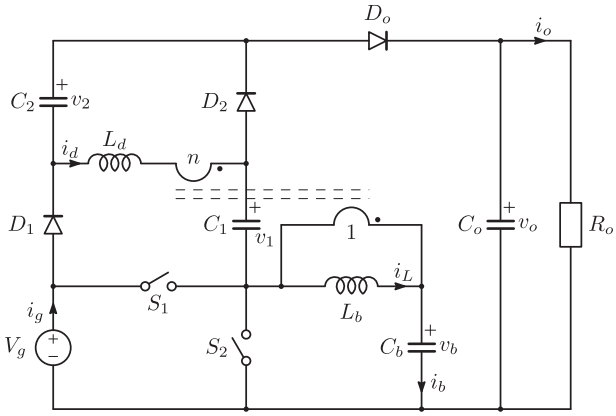

Fig. 2. Proposed high-step-up topology derived from Fig. 1(b).

the secondary winding is in series with both charging and discharging current paths, as it will be clarified in the following section, and all diode voltages are clamped, thus eliminating the parasitic oscillations. Assuming that the conduction intervals of diodes $D_o$ and $D_{1,2}$ are always lower than the corresponding switch conduction intervals of $S_1$ and $S_2$, respectively, the converter main waveforms in a switching period appear, as shown in Fig. 3. The voltage gain, under the above-mentioned assumptions, results from the charge pump actions according to which capacitors $C_1$ and $C_2$ are charged to $V_1 = (1 + nD)V_g$ and $V_2 = nDV_g$, respectively, during the $S_2$ conduction interval, while $C_o$ is charged to $V_o = V_1 + V_2 + V_g + n(1 - D)V_g$, during the $S_1$ conduction interval. Accordingly, the voltage gain results

$$M = \frac{V_o}{V_g} = 2 + n(1 + D). \tag{2}$$

This expression reveals the previously mentioned topology limitation in terms of voltage gain variation capability, compared with boost-based structures. Moreover, considering the constraints imposed by the desired converter operation according to Fig. 3, the duty-cycle variation is limited. This aspect is further clarified in Section V.

Once again, the *charge balance* condition at a steady state for the capacitors yields $\bar{i}_{Do} = \bar{i}_{D1} = \bar{i}_{D2} = \bar{i}_d = I_o$, and $\bar{i}_L = I_L = nI_o$. Thus, compared with an equivalent gain boost converter, the average value of the coupled inductor magnetizing current is reduced by a factor $n/M \ll 1$.

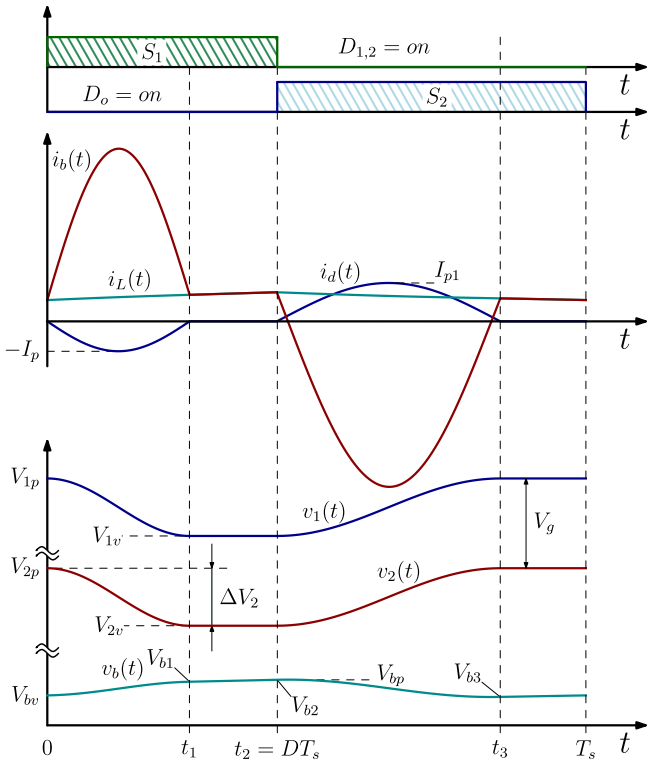


Fig. 3. Main waveforms in a switching period.

## III. Converter Operation

In order to simplify the analysis, let us neglect the magnetizing current ripple assuming $i_L(t) \approx I_L = nI_o$. The output voltage is also considered constant, i.e., $v_o(t) \approx V_o$. The converter operation is divided into four subintervals, described in Fig. 4.

### A. *Interval* $0 \le t \le t_1$ *[see Fig. 4(a)]*

When the switch $S_1$ is turned ON, a resonant tank is formed involving $C_1$, $C_2$, $C_b$, and $L_d$ with initial conditions $i_d(0) = 0$, $v_1(0) = V_{1p}$, $v_2(0) = V_{2p}$, and $v_b(0) = V_{bv}$ (see Fig. 3). The simplified scheme is reported in Fig. 5 with the following parameters: $C_A = C_1C_2/(C_1 + C_2)$, $C_B = C_b/n^2$, $v_A(0) = v_B(0) = 0$, and $V_k = V_o - (n + 1)V_g + nV_{bv} - V_{1p} - V_{2p}$. The resonant current and voltages are as follows:

$$i_d(t) = \frac{V_k}{Z_r}\sin(\omega_r t) + \frac{n^2 C_r}{C_b} I_o\,(1 - \cos(\omega_r t)) \tag{3}$$

$$v_{1,2}(t) = V_{1,2p} + \frac{C_r}{C_{1,2}} V_k\,(1 - \cos(\omega_r t)) - \frac{n^2 C_r^2}{C_b C_{1,2}} Z_r I_o \sin(\omega_r t) + \frac{n^2 C_r}{C_b C_{1,2}} I_o t \tag{4}$$

$$v_b(t) = V_{bv} - \frac{nC_r}{C_b} V_k\,(1 - \cos(\omega_r t)) + \frac{n^3 C_r^2}{C_b^2} Z_r I_o \sin(\omega_r t) - \frac{nI_o}{C_b}\left(\frac{n^2 C_r}{C_b} - 1\right) t \tag{5}$$

where

$$C_r = \frac{1}{\dfrac{1}{C_1} + \dfrac{1}{C_2} + \dfrac{n^2}{C_b}}, \quad \omega_r = \frac{1}{\sqrt{L_d C_r}}, \quad Z_r = \sqrt{\frac{L_d}{C_r}}. \tag{6}$$

This phase ends at instant $t_1$ as soon as the resonant current $i_d(t)$ reaches zero, i.e., from (3) as follows:

$$t_1 = \frac{2}{\omega_r}\tan^{-1}\left(-\frac{V_k}{I_o}\frac{\omega_r C_b}{n^2}\right) \approx \frac{\pi}{\omega_r}. \tag{7}$$

In fact, as it will be clear later on, the sine term in (3) is dominant, thus making the interval duration practically equal to half the resonance frequency. Using such approximation, the resonant current peak value ($I_p$ in Fig. 3) is approximated as

$$I_p \approx -i_d\left(\frac{T_r}{4}\right) = -\frac{V_k}{Z_r} - \frac{n^2 C_r}{C_b} I_o. \tag{8}$$

Thus, approximately after half the resonant cycle, diode $D_o$ turns OFF, and only the buck stage remains operating, as shown in Fig. 4(b).

### B. *Interval* $t_1 \le t \le t_2 = DT_s$ *[see Fig. 4(b)]*

In the remaining part of the main switch ON time, neglecting the magnetizing current ripple, the capacitor $C_b$ continues to be charged almost linearly according to

$$v_b(t) = V_{b1} + \frac{nI_o}{C_b}(t - t_1) \tag{9}$$

where $V_{b1}$ is the value reached at the end of the previous subinterval, i.e., (5) calculated at $t = t_1$ (see Fig. 3). At the end of this subinterval, the voltage across $C_b$ is $V_{b2} = V_{b1} + (nI_o/C_b)(t_2 - t_1)$.

### C. *Interval* $DT_s \le t \le t_3$ *[see Fig. 4(c)]*

In this interval $S_2$, $D_1$, and $D_2$ are conducting, thus recharging $C_1$ and $C_2$ in a resonant manner. The simplified circuit is the same as in Fig. 5, with different expressions for $C_A = C_1 + C_2$ and $V_{k1} = -V_{2v} + nV_{b2}$, while $C_B = C_b/n^2$ remains the same (now voltage $V_k$ was renamed as $V_{k1}$ to avoid confusion with the previous resonance phase). The resonant current and voltages are

$$i_d(t) = \frac{V_{k1}}{Z_{r1}}\sin(\omega_{r1}(t - t_2)) + \frac{n^2 C_{r1}}{C_b} I_o\,(1 - \cos(\omega_{r1}(t - t_2))) \tag{10}$$

$$v_{1,2}(t) = V_{1,2v} + \frac{C_{r1}}{C_1 + C_2} V_{k1}\,(1 - \cos(\omega_{r1}(t - t_2))) - \frac{n^2 C_{r1}^2}{C_b(C_1 + C_2)} Z_{r1} I_o \sin(\omega_{r1}(t - t_2)) + \frac{n^2 C_{r1}}{C_b(C_1 + C_2)} I_o(t - t_2) \tag{11}$$

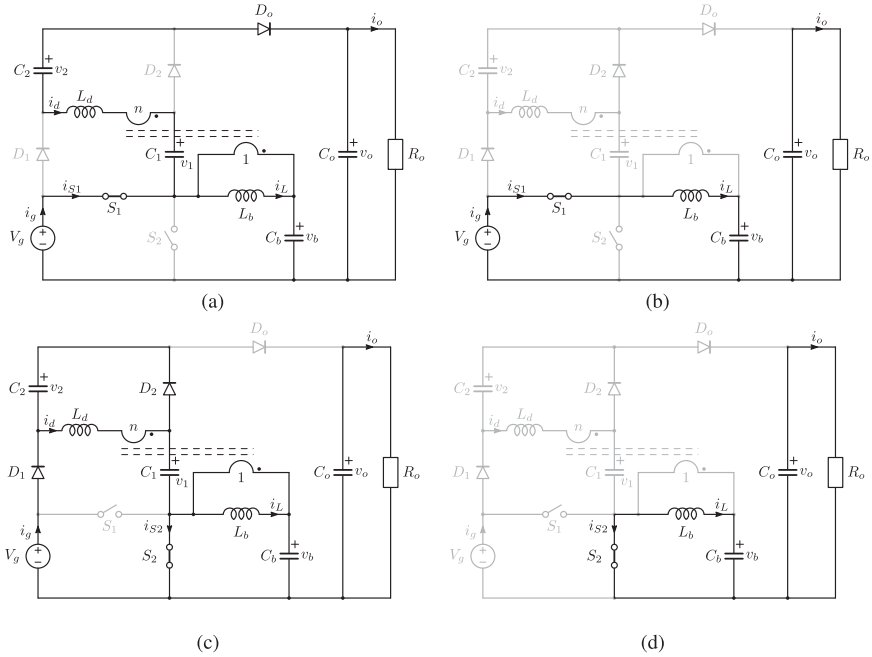


Fig. 4. Subtopologies in a switching period. (a) Interval $0 \le t \le t_1$. (b) Interval $t_1 \le t \le t_2 = DT_s$. (c) Interval $t_2 \le t \le t_3$. (d) Interval $t_3 \le t \le T_s$.

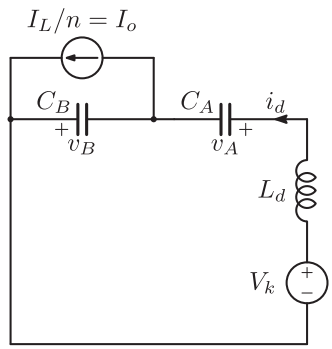


Fig. 5. Simplified resonant circuit during intervals $[0, t_1]$ and $[t_2, t_3]$.

$$v_b(t) = V_{b2} - \frac{nC_{r1}}{C_b} V_{k1} \left(1 - \cos(\omega_{r1}(t - t_2))\right) + \frac{n^3 C_{r1}^2}{C_b^2} Z_{r1} I_o \sin(\omega_{r1}(t - t_2)) - \frac{nI_o}{C_b} \left(\frac{n^2 C_{r1}}{C_b} - 1\right)(t - t_2) \quad (12)$$

where

$$C_{r1} = \frac{1}{\dfrac{1}{C_1 + C_2} + \dfrac{n^2}{C_b}}, \quad \omega_{r1} = \frac{1}{\sqrt{L_d C_{r1}}}, \quad Z_{r1} = \sqrt{\frac{L_d}{C_{r1}}}. \quad (13)$$

The turn OFF of diodes $D_1$ and $D_2$ at instant $t_3$, when the resonant current $i_d(t)$ goes to zero, concludes this phase. From (10), the interval duration is calculated as

$$t_3 - t_2 = \frac{2}{\omega_{r1}} \left(\pi - \tan^{-1}\left(\frac{V_{k1}}{I_o} \frac{\omega_{r1} C_b}{n^2}\right)\right) \approx \frac{\pi}{\omega_{r1}}. \quad (14)$$

Once again, the sine term in (10) is dominant, and using this approximation, the resonant current peak value ($I_{p1}$ in Fig. 3) simplifies as

$$I_{p1} \approx i_d\left(t_2 + \frac{T_{r1}}{4}\right) = \frac{V_{k1}}{Z_{r1}} + \frac{n^2 C_{r1}}{C_b} I_o. \quad (15)$$

### *D. Interval $t_3 \le t \le T_s$ [see Fig. 4(d)]*

In the last fraction of the switching period, the freewheeling phase of the buck section continues, and capacitor $C_b$ discharges according to the following relation:

$$v_b(t) = V_{b3} - \frac{nI_o}{C_b}(t - t_3) \quad (16)$$

where $V_{b3}$ is the voltage at the end of the previous subinterval (see Fig. 3).

## IV. Components Current and Voltage Stress

In this section, the device voltage and current stresses are determined under the assumption of a negligible magnetizing current ripple. In order to estimate the current RMS values in different components, the following approximation of the resonant current was considered:

$$i_d(t) \approx \begin{cases} -I_p \sin(\omega_r t) & \text{for } 0 \le t \le t_1 \approx \frac{\pi}{\omega_r} \\ I_{p1} \sin(\omega_{r1}(t - t_2)) & \text{for } t_2 \le t \le t_3 \approx t_2 + \frac{\pi}{\omega_{r1}} \\ 0 & \text{otherwise} \end{cases}. \quad (17)$$

### *A. Diode* $\mathrm{D_o}$

This diode carries the resonant current $i_{Do}(t) = -i_d(t)$ during interval $[0, t_1]$. Consequently, its peak value is given by (8).

Here, $V_k$ can be estimated by observing that, for the capacitor *charge balance*, $\bar{i}_{Do} = I_o$. Thus, from (3), we have

$$I_o = -\frac{1}{T_s}\int_0^{t_1} i_d(t)dt \;\;\Rightarrow\;\; V_k = -Z_r I_o \pi \left(\frac{T_s}{T_r} + \frac{n^2 C_r}{2C_b}\right). \tag{18}$$

As far as the diode voltage stress is concerned, from Fig. 4(c), we get

$$V_{Do} = V_o - V_{1v} \approx V_o - \left(V_1 - \frac{\Delta V_1}{2}\right) \tag{19}$$

where the capacitor voltage variation $\Delta V_1$ is calculated considering that the charge the capacitors $C_1$ and $C_2$ deliver to the output in a switching period is equal to the load current integrated over the switching period, i.e.,

$$\Delta V_{1,2} = \frac{I_o T_s}{C_{1,2}}. \tag{20}$$

Considering the approximation (17), the diode current rms value is given by

$$I_{Do_{\text{RMS}}} = \frac{I_p}{2}\sqrt{\frac{T_r}{T_s}}. \tag{21}$$

### B. Diodes $\text{D}_{1,2}$

These devices conduct during interval $[t_2, t_3]$, where current $i_d(t)$ is shared between $C_1$ and $C_2$, i.e., $i_{D1,2}(t) = i_d(t)C_{1,2}/(C_1 + C_2)$. The diode current peak value in the charging phase is equal to $I_{p1}C_{1,2}/(C_1 + C_2)$. Once again, from the condition $\bar{i}_d = I_o$, an expression for $V_{k1}$ in the interval $[t_2, t_3]$ is found as follows:

$$V_{k1} = Z_{r1} I_o \pi \left(\frac{T_s}{T_{r1}} - \frac{n^2 C_{r1}}{2C_b}\right). \tag{22}$$

The maximum diode voltage stress can be inferred from Fig. 4(a), and results $V_{D1,2} = V_o - V_g - V_{2,1v} \approx V_o - V_g - (V_{2,1} - \frac{\Delta V_{2,1}}{2})$. Considering the approximation (17), the diode current RMS value is given by

$$I_{D1,2_{\text{RMS}}} = \frac{I_{p1}}{2}\frac{C_{1,2}}{C_1 + C_2}\sqrt{\frac{T_{r1}}{T_s}}. \tag{23}$$

### C. Switch $\text{S}_1$

The current flowing into the main switch $S_1$, during interval $[0, t_2 = DT_s]$, from Fig. 4(a), is $i_{S1}(t) = i_L(t) - (1 + n)i_d(t) = i_{Cb}(t) - i_d(t)$. Thus, its peak value is given by $I_{S1_{pk}} = nI_o + (1 + n)I_p$. The switch voltage stress is clearly given by the input voltage, while the switch RMS current value results

$$I_{S1_{\text{RMS}}} = I_o\sqrt{\frac{I_p}{I_o}\frac{n+1}{\omega_r T_s}\left(4n + (n+1)\frac{\pi}{2}\frac{I_p}{I_o}\right) + n^2 D}. \tag{24}$$

### D. Switch $\text{S}_2$

The instantaneous switch current, in the interval $[t_2 = DT_s, T_s]$, is given by $i_{S2}(t) = i_{C1}(t) - i_{Cb}(t) = -i_L(t) + (C_1/(C_1 + C_2) + n)i_d(t)$. Consequently, its peak value is calculated as $I_{S2_{pk}} = -nI_o + (C_1/(C_1 + C_2) + n)I_{p1}$. Like $S_1$, the voltage stress is given by the input voltage. Its RMS current value is calculated as

$$I_{S2_{\text{RMS}}} = I_o\sqrt{\frac{I_{p1}}{I_o}\frac{n+\xi}{\omega_{r1}T_s}\left(-4n + (n+\xi)\frac{\pi}{2}\frac{I_{p1}}{I_o}\right) + n^2(1-D)} \tag{25}$$

where $\xi = C_1/(C_1 + C_2)$.

### E. Capacitors $\text{C}_{1,2}$

The RMS current value through $C_1$ and $C_2$ is totally determined by the resonant current. Considering the approximation (17), we obtain

$$I_{C1,2_{\text{RMS}}} = \sqrt{\frac{I_p^2}{2}\frac{T_r}{2T_s} + \frac{I_{p1}^2}{2}\frac{T_{r1}}{2T_s}\left(\frac{C_{1,2}}{C_1 + C_2}\right)^2}. \tag{26}$$

The maximum capacitor voltage is $V_{C1,2} \approx V_{1,2} + \Delta V_{1,2}/2$.

### F. Capacitor $\text{C}_b$

The current through capacitor $C_b$ is $i_{Cb}(t) = i_L(t) - ni_d(t)$. Considering (17), we get

$$I_{Cb_{\text{RMS}}} = nI_o\sqrt{\frac{\frac{I_{p1}}{I_o}\frac{1}{\omega_{r1}T_s}\left(-4 + \frac{I_{p1}}{I_o}\frac{\pi}{2}\right)}{+\frac{I_p}{I_o}\frac{1}{\omega_r T_s}\left(4 + \frac{I_p}{I_o}\frac{\pi}{2}\right) + 1}}. \tag{27}$$

The average voltage across the capacitor $C_b$ is simply equal to $V_{Cb} = DV_g$.

### G. Coupled Inductor

The coupled inductor primary winding carries the same current as $C_b$, while the secondary current RMS value is

$$I_{d_{\text{RMS}}} = \sqrt{\frac{I_p^2}{2}\frac{T_r}{2T_s} + \frac{I_{p1}^2}{2}\frac{T_{r1}}{2T_s}}. \tag{28}$$

## V. Design Constraints

In this section, guidelines for the selection of the main converter components are given. The considered specifications are listed in Table I. In the following, we consider $C_1 = C_2 = C_x$.

### A. Turns Ratio n

The main idea under the choice of the coupled inductor turns ratio is to guarantee the converter operation, as described in the previous section, i.e., $t_1 < DT_s$ and $t_3 - t_2 < (1 - D)T_s$. Considering the approximations (7) and (14), and taking into account the input voltage variation, we can write the following:

$$\frac{\pi}{\omega_r} \le D_{\min} T_s \tag{29}$$

$$\frac{\pi}{\omega_{r1}} \le (1 - D_{\max})\, T_s. \tag{30}$$

TABLE I
CONVERTER SPECIFICATIONS

| Parameter | Symbol | Value | |
|---|---|---|---|
| Minimum input voltage | $V_{g_{min}}$ | 40 | V |
| Nominal input voltage | $V_{g_{nom}}$ | 44 | V |
| Maximum input voltage | $V_{g_{max}}$ | 48 | V |
| Nominal output voltage | $V_o$ | 400 | V |
| Nominal output power | $P_o$ | 300 | W |
| Switching frequency | $f_s$ | 200 | kHz |

Considering the equal sign in (29) and (30) as boundary conditions and taking the ratio, we get:

$$\frac{1+\lambda}{1+4\lambda}=\left(\frac{D_{\min}}{1-D_{\max}}\right)^2 \tag{31}$$

where $\lambda = C_b/(2n^2C_x)$. Deriving parameter $\lambda$ from the above-presented equation, we get

$$\lambda=\frac{1-\left(\frac{D_{\min}}{1-D_{\max}}\right)^2}{4\left(\frac{D_{\min}}{1-D_{\max}}\right)^2-1}. \tag{32}$$

Being $\lambda$ positive, from (31) and (32), the condition $(1-D_{\max})/2 < D_{\min} < 1-D_{\max}$ must be satisfied. Thus, using (2), the following constraint is found:

$$n_{\min}=\frac{M_{\min}+M_{\max}-4}{3}<n<n_{\max}=\frac{2M_{\min}+M_{\max}-6}{4}. \tag{33}$$

The above-presented relation reveals the mentioned limitation in terms of the allowed input voltage range, since applying the condition $n_{\min} \le n_{\max}$ yields the following constraint:

$$M_{\max} \le 2\left(M_{\min}-1\right). \tag{34}$$

The selected value for $n$, from expression (33), is

$$n=\frac{n_{\min}+n_{\max}}{2}=\frac{10M_{\min}+7M_{\max}-34}{24}. \tag{35}$$

### B. Magnetizing Inductance $L_b$

Even if the above-presented analysis considers a negligible buck inductor current ripple, the latter has a modest effect on the converter voltage gain. On the other hand, a high inductor current ripple may have a beneficial effect in terms of inductor size and reduction of switching losses, especially if a *quasi-square-wave* operation is achieved (i.e., the current $i_L$ is negative at the end of $S_2$ conduction interval). In this case, zero-voltage turn ON of both switches is achieved, provided that the current value at the commutation instants is enough to completely charge/discharge the switching node capacitance. Please note that this soft-switching condition is independent of the resonant current $i_d$, since the latter is always zero at the commutation instants. By imposing this constraint and assuming a piecewise linear current ripple, the following limit value is found:

$$L_{b\max}=\frac{V_o-(2+n)V_{g\max}}{2n^2I_of_s}. \tag{36}$$

A suitable margin should be considered in choosing an inductance value lower than the limit (36), considering that the voltage ripple on $v_b$ may not be so negligible, a fact that would make the hypothesis of a piecewise linear inductor current not well verified.

### C. Leakage Inductance $L_d$

Instead of imposing a value for the coupled inductor leakage inductance, the value measured on the implemented transformer is used. This approach avoids the complexity of building a transformer with a precise value of the total leakage inductance. Clearly, this approach is allowed by the many degrees of freedom the topology has, as the two resonance frequencies $\omega_r$ and $\omega_{r1}$ are functions of five parameters, namely $L_d$, $C_1$, $C_2$, $C_b$, and $n$ [see (6) and (13)]. In any case, no particular winding arrangements are necessary, considering that a standard winding configuration with primary layers on top of the secondary layers generates a leakage inductance in the range of few percent ($2 \div 10\%$) of the magnetizing one (referred to the same winding).

### D. Capacitors $C_b$ and $C_x = C_1 = C_2$

From (32), parameter $\lambda$ is calculated, and from (29), we get

$$C_b=n^2\frac{1+4\lambda}{L_d}\left(\frac{D_{\min}}{\pi f_s}\right)^2. \tag{37}$$

Then, from $\lambda$ definition, $C_1 = C_2 = C_b/(2n^2\lambda)$.

## VI. PROTOTYPE DESIGN AND EXPERIMENTAL RESULTS

In order to verify the above-presented theoretical analysis and the performance of the proposed high-step-up topology, a prototype was designed and built according to the specifications listed in Table I. The active devices are: $S_1 = S_2 =$ IPB010N06N (60 V, 180 A) from Infineon, $D_1 = D_2 =$ IDD03SG60C from Infineon, and $D_o =$ C3D03060E from Cree. The SiC diodes have been used just for their immediate availability in the lab, even if their voltage rating is much higher than needed.

From (33), being $8.33 \le M \le 10$, the transformer turns ratio $n$ should be selected in the range $4.78 \div 5.17$; thus, $n = 5$ was chosen. The maximum magnetizing inductance value to guarantee the *quasi-square-wave* operation from (36) is 8.5 $\mu$H , and the selected value was much lower in order to have enough negative current at $S_2$ turn OFF to charge the parasitic capacitance of the switching node up to the input voltage before $S_1$ is turned ON. The value measured at primary side on the wounded RM10 core was $L_b = 3.74$ $\mu$H. The total secondary leakage inductance is $L_d = 4.3$ $\mu$H. Once this value is referred to the primary side, it gives a leakage-to-magnetizing inductance ratio of 4.65%. The primary winding layer consists of three turns of Litz wire (400 strands of 71 $\mu$m diameter) positioned on top of a two-layers secondary winding, made by 15 turns of Litz wire

TABLE II
CONVERTER PARAMETERS

| Parameter | Symbol | Value | |
|---|---|---|---|
| Primary turns number | $N_p$ | 3 | |
| Secondary turns number | $N_s$ | 15 | |
| Magnetizing inductance | $L_b$ | 3.7 | µH |
| Secondary leakage inductance | $L_d$ | 4.3 | µH |
| Flying capacitors | $C_1 = C_2$ | 100 | nF |
| Buck capacitor | $C_b$ | $6 \times 0.68$ | µF |
| Output capacitor | $C_o$ | 1 | µF |
| Input capacitor | $C_{in}$ | $3 \times 2.2$ | µF |

TABLE III
CALCULATED VOLTAGE AND CURRENT STRESS AT NOMINAL OPERATING POINT

| Parameter | $D_o$ | $D_1$ | $D_2$ | $S_1$ | $S_2$ | $C_1$ | $C_2$ | $C_b$ | $C_{in}$ |
|---|---|---|---|---|---|---|---|---|---|
| $I_{peak}$ [A] | 4.72 | 4.72 | 4.72 | 32 | 21 | 4.72 | 4.72 | 27.3 | 32 |
| $I_{RMS}$ [A] | 1.68 | 0.98 | 0.98 | 11.9 | 8.9 | 1.95 | 1.95 | 13 | 12 |
| $V_{stress}$ [V] | 281 | 281 | 237 | 44 | 44 | 155 | 111 | 18.5 | 44 |

(200 strands of 50 $\mu$m diameter). Like any inductor carrying a nonzero average current, also the coupled inductor used in this topology needs a suitable air-gap that, in the used RM10 core has a thickness of 150 $\mu$m, in both central and lateral legs. From (32), parameter $\lambda$ is equal to 0.714; consequently, from (37), $C_b$ should be 4 $\mu$F. Considering the high RMS current flowing in this capacitance, which based on (27) was estimated equal to 13 A, six 0.68 $\mu$F film capacitors were connected in parallel. Finally, from $\lambda$ definition, $C_{1,2}$ should be 114 nF, and the standard 100 nF value was used. The input capacitor is $C_{in} = 3 \times 2.2$ $\mu$F, while the output one is $C_o = 1$ $\mu$F. All converter parameter values are listed in Table II. With the selected component values, the calculated current and voltage stress at the nominal operating point, using the expressions developed in Section IV, are listed in Table III. The photo of the implemented prototype is reported in Fig. 6 and it shows the main active and passive components.

The converter main waveforms at two different input voltage values and for nominal output voltage and power are reported in Fig. 7. Please note that, despite the currents in the switches are not directly measured, the relative information can be easily gathered from the displayed waveforms since $i_{S1}(t) = i_{Cb}(t) - i_{C1}(t)$, during interval $[0, t_2 = DT_s]$, while $i_{S2}(t) = i_{C1}(t) - i_{Cb}(t)$, during interval $[t_2 = DT_s, T_s]$. Looking at these experimental waveforms, we can highlight two main aspects. The first one has to do with the delay between the $S_1$ turn-OFF instant and the instant $C_1$ starts to be charged: this is due to the different charging current paths the resonant current $i_d(t)$ divides in, one involving $C_1$, $D_1$, $S_2$, and $C_{in}$, and the other involving just $C_2$ and $D_2$. It happens that, when $S_2$ turns ON, $D_1$ and $D_2$ turn ON at different instants ($D_2$ first), so

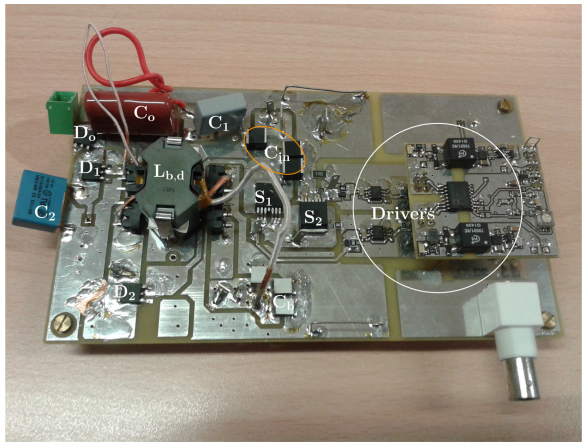


Fig. 6. Photo of the prototype showing the main components.

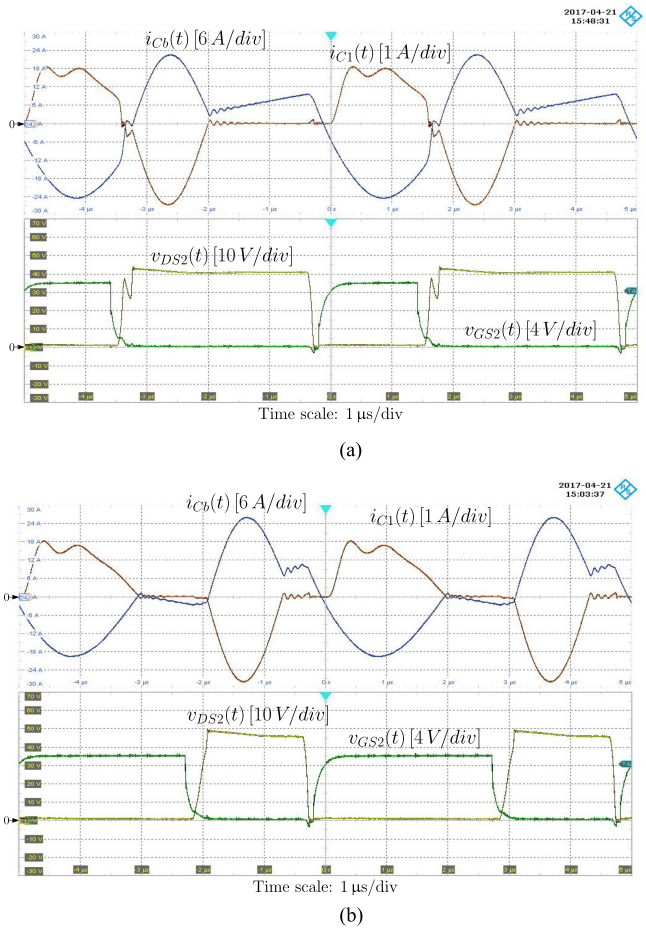


Fig. 7. Measured converter main waveforms at nominal output voltage and power. (a) $V_g = 42$ V. (b) $V_g = 48$ V.

that, at the beginning, the resonance involves just $C_2$, and only when $D_1$ turns ON, also $C_1$ comes into play. This phenomenon is better appreciated looking at the measures shown in Fig. 8, taken at nominal conditions, that reports the flying capacitor voltages $v_{C1}(t)$ and $v_{C2}(t)$: in this operating point, the delay is about 380 ns.

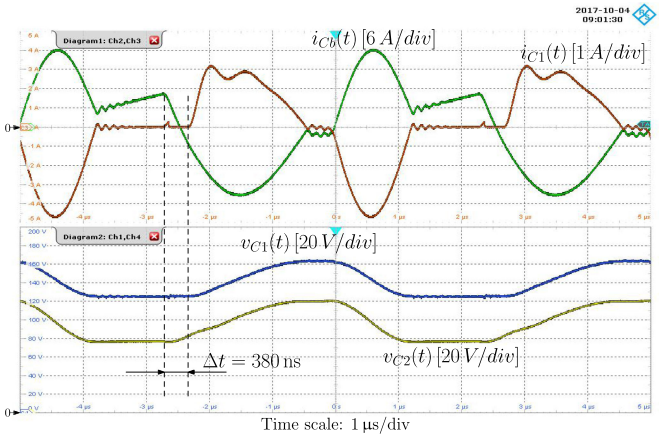


Fig. 8. Measured converter main waveforms at nominal condition showing the delay between the $S_1$ turn-OFF instant and the instant $C_1$ starts to be charged.

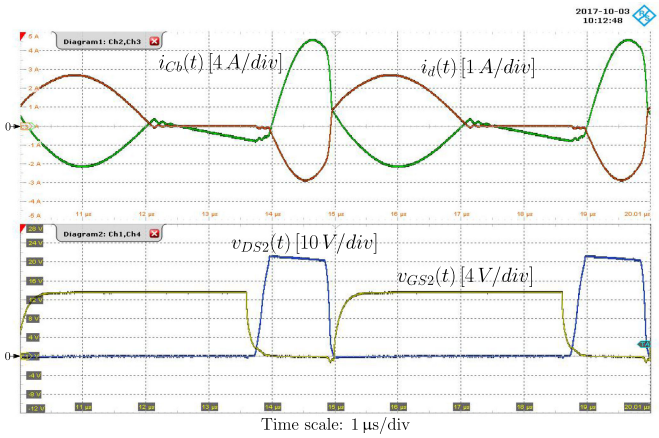


Fig. 9. Measured converter main waveforms at $V_g = 52$ V and nominal output voltage and 160 W of output power.

The second consideration is that at the minimum input voltage the condition $T_{r1}/2 < (1 - D_{\max})T_s$ is not met, as revealed by the current waveforms in Fig. 7(a) taken at $V_g = 42$ V. This is caused by four main factors: the aforementioned double resonance, that affects the $t_3 - t_2$ interval, the high magnetizing current ripple that affects the overall voltage gain, the nonunity converter efficiency, and the input voltage ripple ($\Delta V_g = 2.8$ V) both calling for a higher duty-cycle value compared with the theoretical one. Being the design done considering boundary equations, it cannot cope with any deviation from the theoretical analysis. Nonetheless, violating the condition (30) does not cause any harm to the converter operation, being the diode current rate of change always limited by the transformer leakage inductance $L_d$. This remains true also for low duty-cycle values where condition (29) might not be satisfied. In this case, another topological state appears with a higher rate of change of current $i_d(t)$, as can be seen from the measure taken at $V_g = 52$ V ($P_o = 160$ W) reported in Fig. 9.

The $S_2$ gate-to-source and drain-to-source voltages, shown in Fig. 7, demonstrate that the ZVS condition at turn ON is always satisfied for $S_2$, and almost satisfied for $S_1$. In any case,

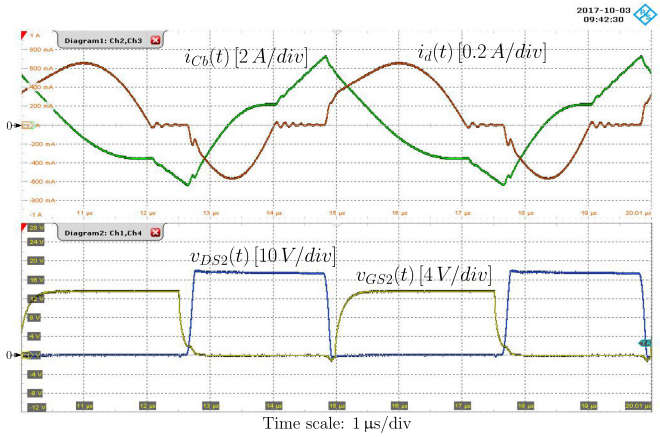


Fig. 10. Measured converter main waveforms at nominal input and output voltages and 40 W of output power.

TABLE IV
COMPARISON BETWEEN THEORETICAL EXPECTATIONS AND EXPERIMENTAL RESULTS AT THE NOMINAL OPERATING POINT

| | **D** | $\mathbf{V_{1v}}$ [V] | $\mathbf{V_{1p}}$ [V] | $\mathbf{V_{2v}}$ [V] | $\mathbf{V_{2p}}$ [V] | $\mathbf{I_p}$ [A] | $\mathbf{I_{p1}}$ [A] | $\mathbf{I_{S1_p}}$ [A] | $\mathbf{I_{S2_p}}$ [A] |
|---|---|---|---|---|---|---|---|---|---|
| Theory | 0.42 | 117 | 155 | 73 | 111 | 4.72 | 4.45 | 32 | 21 |
| Measure | 0.5 | 126 | 165 | 77 | 121 | 5.2 | 4.69 | 29 | 24 |

the switching node voltage appears clean and ringing free. At reduced output power, the converter enters deeply into the *quasi-square-wave* operation, thus guaranteeing ZVS commutations even at light load. This is demonstrated by the measure shown in Fig. 10 that was taken at 40 W of output power ($V_g = 44$ V, $V_o = 400$ V). The comparison between some calculated quantities and the corresponding measured values is shown in Table IV: despite the rough approximations used in the analysis, the matching is quite good, and the main discrepancy is caused by the higher duty-cycle value of the experimental setup (see comments above). Note that the peak current value in the switches is overestimated for $S_1$ and underestimated for $S_2$. This is due to the constant magnetizing current $i_L$ assumed in the analysis, opposed to the designed high current ripple ($\Delta i_{L_{pk-pk}} > 2\bar{i}_L$) for the *quasi-square-wave* operation.

The comparison between measured and theoretical duty cycle as a function of the voltage conversion ratio at nominal output voltage and power is shown in Fig. 11. As we can see, the measured behavior follows the theoretical expectation from (2), except for a translation to higher values due to the circuit losses. The last point corresponding to the minimum input voltage (maximum voltage gain) tends to deviate from the linear behavior predicted by (2) because of the different operating condition mentioned above (i.e., $T_{r1}/2 > (1 - D_{\max})T_s$).

The conversion efficiency (power stage only) was calculated measuring input and output powers using digital multimeters (Keysight 34461A), for input/output voltages and output current, while the input current was read directly on the dc power supply Chroma 62050P-100-100. The overall relative error on

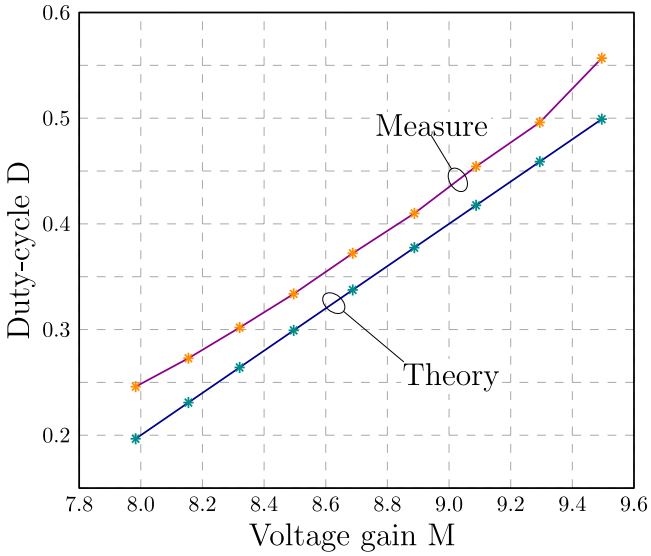


Fig. 11. Comparison between measured and theoretical duty cycle as a function of the voltage conversion ratio (nominal output voltage and power).

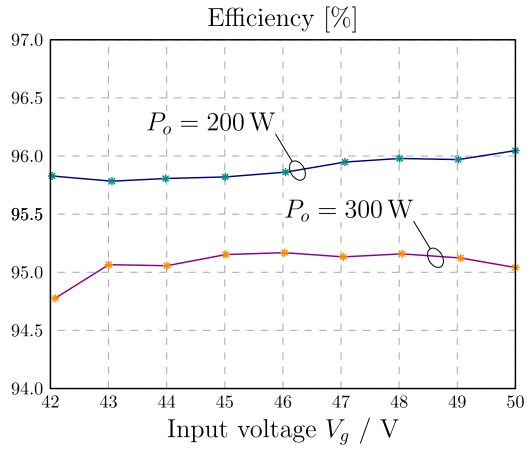


Fig. 12. Conversion efficiency as a function of input voltage for two different output power levels.

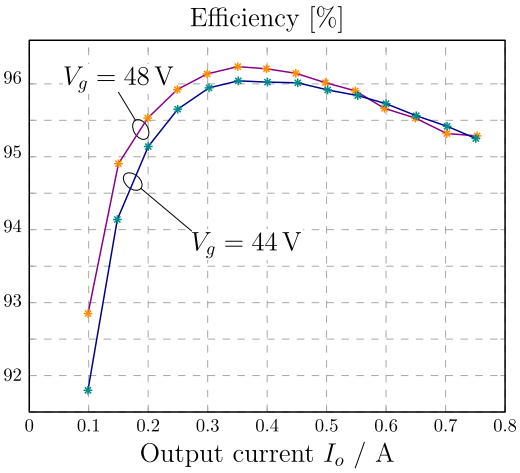


Fig. 13. Conversion efficiency as a function of the output current for two different input voltage values.

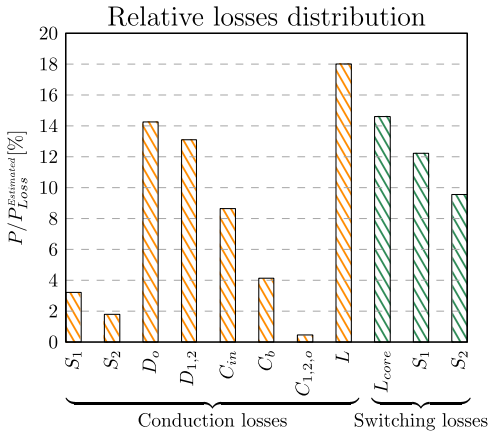


Fig. 14. Calculated relative losses distribution among the main components (estimated overall losses at nominal condition $P_{\text{Loss}}^{\text{Estimated}} \approx 10$ W). Notation $D_{1,2}$ means the sum of $D_1$ and $D_2$ conduction losses, while $C_{1,2,o}$ means the sum of $C_1$, $C_2$ and $C_o$ conduction losses.

the efficiency calculation is lower than 0.5%, the main contribution coming from the input current measurement (0.1% of reading plus 0.1% of range). The measured efficiency at different input voltage values and for two different power levels is shown in Fig. 12: values above 95% are achieved at nominal power except at the lower part of the input voltage range ($V_g = 42$ V). Here, the slight efficiency reduction is caused by the different operating condition mentioned above according to which $T_{r1}/2 > (1 - D_{\max})T_s$, that is, causing an increase of $S_1$ turn-ON losses, as revealed by the $v_{DS2}(t)$ waveform in Fig. 7(a). At lower output current values, the efficiency remains above 90% down approximately to one tenth of the nominal power, as revealed by the measurement reported in Fig. 13 for two different input voltage values ($V_g = 44$ V and $V_g = 48$ V). The relative losses distribution between the different components was calculated based on the stress analysis reported in Section IV at the nominal operating point, and the result is shown in Fig. 14. The total power loss was estimated as $P_{\text{Loss}}^{\text{Estimated}} = 10$ W, lower than the measured one $P_{\text{Loss}}^{\text{Measured}} = 15.8$ W. As we can see, turn-OFF switching losses have been considered too, even if the commutation time intervals are very difficult to predict. This is because the switching node transition is affected by the huge MOSFET's output capacitance (roughly 3.4 nF each) that acts as a lossless snubber, especially at the $S_2$ turn OFF, where the switched current is quite low ($\approx -2.5$ A from Fig. 8). However, the forecasted total $S_1$ losses of 1.37 W are not unrealistic, since the temperature measured on the device package in the same operating point was 83 °C without forced air circulation (ambient temperature $T_A \approx 20$ °C). With a thermal resistance from junction to ambient of the TO263-7 package ranging between 40 K/W with 6 cm$^2$ of cooling area and 62 K/W with minimal footprint, it means a dissipated power in the range $1 \div 1.6$ W. Turn-ON switching losses have been neglected for both switches, thanks to the *quasi-square-wave* operation imposed by a proper selection of the magnetizing inductance $L_b$, even if this condition is not completely met for $S_1$, as can be inferred from the rising edge of voltage $v_{DS2}(t)$ in Fig. 7(b). However, the

small switched current and residual voltage ($\approx 10$ V) give a negligible contribution to the overall losses. The core loss was estimated based on the manufacturer data of the used N87 ferrite material. The high RMS current value flowing in the devices, which is the price to pay for having the minimum switch voltage stress, makes the control of any parasitic resistance in the current path crucial in order to limit the conduction losses. This is the reason why the input and the buck-stage capacitances were implemented by connecting in parallel more lower value capacitors, as revealed in Table II. For the same reasons, the SiC diodes used in the experimental prototype are not the best choice for this circuit, where they are naturally turned OFF by the resonant current $i_d$. Looking at their voltage stress (see Table III), lower voltage rating and, consequently, lower voltage drop Si devices could be used for a better overall efficiency.

## VII. Conclusion

This paper presented a high-step-up topology featuring minimum switch voltage stress as well as reduced magnetic energy, compared with an equivalent gain conventional boost converter. The conversion process explores both a magnetic coupling and a charge pump mechanism to efficiently transfer energy to the output. The leakage inductance of the coupled inductors is explored to shape the capacitor charging/discharging current so as to achieve soft diode commutations.

A detailed design procedure was described to easily calculate the needed passive component values. The *quasi-square-wave* operation allows ZVS turn ON of all switches. Experimental results taken on a 300-W prototype confirmed the theoretical analysis and expectations.

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