Minimizing Inverter Capacity Design and Comparative Performance Evaluation of SVC-Coupling Hybrid Active Power Filters

Lei Wang, *Member, IEEE*, Chi-Seng Lam, *Senior Member, IEEE*, and Man-Chung Wong, *Senior Member, IEEE*

***Abstract*—In this study, a minimizing inverter capacity design is proposed, and the characteristics and performance of static VAR compensator (SVC) coupling hybrid active power filters (SVC-HAPFs) are analyzed. The cost of the SVC part is much lower than that of the active inverter part, and thus, the reduction of inverter part capacity can lead to a decrease in the total cost of SVC-HAPF. To demonstrate the advantages of the proposed minimizing inverter capacity design of SVC-HAPF, comparisons are given between the conventional and the proposed SVC-HAPF designs. Comparisons are also provided among active power filters (APFs), HAPFs, and the proposed SVC-HAPF in terms of dc-link voltage, compensation range, and performance. Finally, simulation and laboratory-scale experimental results are given to validate the minimizing inverter capacity design, and to verify the characteristics and compensation performances of APF, HAPF, and the proposed SVC-HAPF.**

***Index Terms*—Active inverter, active power filters (APFs), dc-link voltage, hybrid active power filters (HAPFs), static VAR compensator (SVC).**

	Year	Resonance prevention capability	Comp. range	Tracking performance	Inverter rating	Power loss	Cost
PPF [1]	1940s	Week	Narrow	Poor	--	Low	Low
SVC [2]-[12]	1960s	Week	Wide	Medium	--	Low	Low
APF [13]- [19]	1976	Strong	Wide	Good	High	High	High
HAPF [20], [21]	2003	Strong	Narrow	Poor	Low	Medium	Medium
SVC//APF [22]	2003	Strong	Wide	Good	Medium	High	High
PPF//APF [23], [24].	2010	Strong	Wide	Good	Medium	High	High
TCR//RITHAPF [25]	2012	Medium	Medium	Good	Low-Medium	Medium	High
Conventional SVC-HAPFs [26]-[31]	2014	Strong	Wide	Good	Medium	Medium	Medium
Proposed SVC-HAPF	2017	Strong	Wide	Good	Low-Medium	Low-Medium	Medium

I. Introduction

CURRENT quality compensators can be installed to solve current quality problems, such as a low power factor (PF), harmonic current pollution, and unbalanced problems. A historical review of the various compensators is given below and summarized in Table I.

To compensate for reactive power, low-cost passive power filters (PPFs) [1] and static VAR compensators (SVCs) [2]–[4], were proposed in the 1940s and 1960s, respectively. In practical applications, PPFs and SVCs suffer from the potential resonance problem [5], [6] due to system frequency variation [7], parameter (inductor and capacitor) values changes [7], [8], nonlinear dynamics characteristics in thyristor (SVCs only) [9]–[12], etc. To overcome the resonance problem and to improve performance, active power filters (APFs) were proposed in 1976 [13], [14]. For medium-voltage applications, APF requires costly multilevel structures [15]–[19] to reduce the voltage across the dc-link capacitor and power switches. To reduce the voltage capacity of the inverter, large *LC*-impedance coupling hybrid active power filters (HAPFs) were proposed in 2003 [20]. However, HAPFs have a narrow compensation range, which limits their compensation ability [20], [21]. In the same year, Dixon *et al.* [22] proposed an SVC structure in parallel with APF (SVC//APF). The SVC part of SVC//APF is used to compensate for most of the reactive power, thus the current rating of the APF can be significantly reduced. However, the voltage rating of the APF part remains high, so the SVC//APF still requires a costly multilevel structure for medium-voltage level applications. Another hybrid structure of PPF in parallel with APF (PPF//APF) was proposed after 2010 in [23] and [24]. The PPF part of PPF//APF can share the large compensating current, and thus, the current rating of APF can be reduced. However, when the loading reactive power is capacitive or has a wide reactive power variation, the APF loses its small current rating characteristic. In 2012, Luo *et al.* [25] proposed a novel hybrid system consisting of a thyristor-controlled reactor (TCR) and a resonant impedance-type hybrid active power filter (RITHAPF) (TCR//RITHAPF).

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L. Wang is with the Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macao 999078, China.

C.-S. Lam is with the State Key Laboratory of Analog and Mixed Signal VLSI, University of Macau, Macao 999078, China (e-mail:

The RITHAPF part is an APF crossing over a matching transformer connected in parallel with a fundamental series resonant circuit. As most of the loads are inductive and the TCR part is also inductive, the RITHAPF part is required to provide a large capacitive compensating current for inductive loads compensation so that the current/power rating of RITHAPF can be high. However, the matching transformer in TCR//RITHAPF can also drive up the total system cost. After 2014, SVC-coupling hybrid active power filters (SVC-HAPFs) were widely studied [26]–[31], which have the characteristics of a wider compensation range than HAPF and a lower dc-link voltage than the APF. Of these compensators, the PPF and HAPF have poor dynamic reactive power tracking performance compared to the others, and the tracking performances of APF, SVC//APF, PPF//APF, TCR//RITHAPF, and SVC-HAPFs are better than those of SVC.

The structure of SVC-HAPF was first proposed in [26], and the different aspects of SVC-HAPFs discussed in [27]–[31]. The control strategies of SVC-HAPFs for balanced loads compensation have been discussed in [26] and for unbalanced loads in [27]. To overcome the potential overcapacity problem of the SVC-HAPFs, the selective compensation control method was proposed in [28] for harmonic distortion, and unbalanced and reactive power. The focus of [26]–[28] is on the control methods, while the focus of [29] and [30] is on the system design of the SVC-HAPFs. Although the final selected parameters are the same in [29] and [30], the SVC-HAPF design approaches differ. In [29], the SVC-HAPF design was for unbalanced loads compensation. In [30], the SVC-HAPF was designed to compensate for fundamental reactive power, while the current harmonic components were not taken into consideration. The hardware implementation of the SVC-HAPF was discussed in [31]. The minimizing inverter capacity design of the SVC-HAPF was not considered in [26]–[31], although a reduction in SVC-HAPF inverter capacity can bring about decreases in the compensation device capacity, power loss, and cost. Therefore, the parameter design procedures for reducing the dc-link operation voltage of the SVC-HAPFs are explored in this study. The proposed SVC-HAPF design is also compared with the conventional designs in [29] and [30].

Based on the limitations of the conventional SVC-HAPFs in [27]–[31], this study aims the following.

1) Enable a reduction in the power rating ratio between the active inverter part and the SVC part through mathematical analysis.
2) Propose a minimizing dc-link voltage design for SVC-HAPFs reactive power and harmonic currents compensation (see Section III).
3) Compare the conventional design of the SVC-HAPFs [29], [30] with the proposed one through analysis and simulations (see Section III).
4) Perform a comprehensive study of dc-link voltage, compensation, and tracking performances of the APF, conventional HAPF, and SVC-HAPF (see Section IV).
5) Provide power loss and efficiency analyses of the APF, the conventional HAPF, and the proposed SVC-HAPF (see Section V).

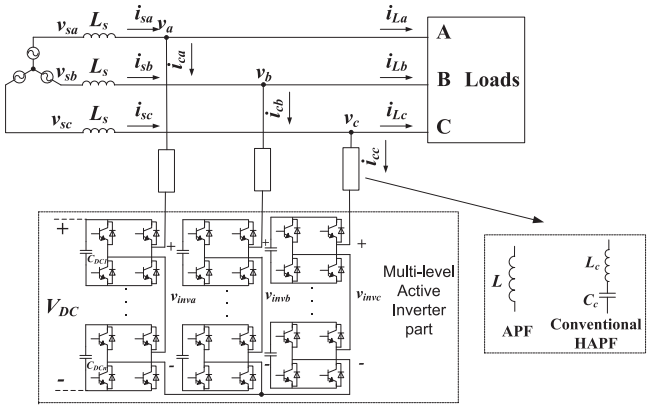

Fig. 1. Structure of the conventional multilevel APF and HAPF.

The layout of this paper is as follows. In Section II, the structures, modeling, and control are introduced for the APF, HAPF, and SVC-HAPF. In Section III, the power rating ratio analysis is proposed between the active inverter part and the coupling SVC part of the SVC-HAPF, based on the structures and modeling. The required dc-link voltage is also deduced and analyzed for both the conventional and the proposed SVC-HAPFs. The conventional HAPF and the proposed SVC-HAPF are compared in Section IV. The experimental verifications are provided in Section V for the conventional HAPF and the proposed SVC-HAPF. Finally, a summary is given in Section VI.

II. Structures, Modeling, and Control of HAPF and SVC-HAPF

Figs. 1 and 2 show the structures of the APF, HAPF, and the SVC-HAPF. The subscript "x" stands for phases a, b, and c in the following analysis. v_{sx} and v_x are the source and load voltages; and i_{sx}, i_{Lx}, and i_{cx} are the source, load, and compensating currents, respectively. L_s is the transmission line impedance. In Fig. 1, L is the coupling inductor of APF, and L_c and C_c are the coupling inductor and capacitor of HAPF, respectively. L_c, $L_{\rm PF}$, and $C_{\rm PF}$ in Fig. 2 are the coupling inductor, SVC part inductor, and capacitor, respectively.

Fig. 1 shows that the inverter voltage of APF is high due to the small coupling inductive impedance L. The coupling LC part (L_c and C_c) of HAPF is used to provide the fixed reactive power compensation, and the active inverter part is used to enlarge the reactive power compensation range and compensate the harmonic current. Compared with HAPF, the SVC part of SVC-HAPF provides a wide and continuous inductive and capacitive reactive power compensation range, which is controlled by the firing angles (α_x) of the thyristors. As the SVC part can provide the fundamental voltage drop, the rating of the active inverter part can be small and the use of a costly multilevel structure is, thus, avoided [29]. In addition, the isolation transformer is used to protect the active inverter part from the inrush current.

The control model of the SVC-HAPF for simulation and experiments is provided in Fig. 2. The inputs are load voltage v_x, load current i_{Lx}, and compensating current i_{cx}, and the

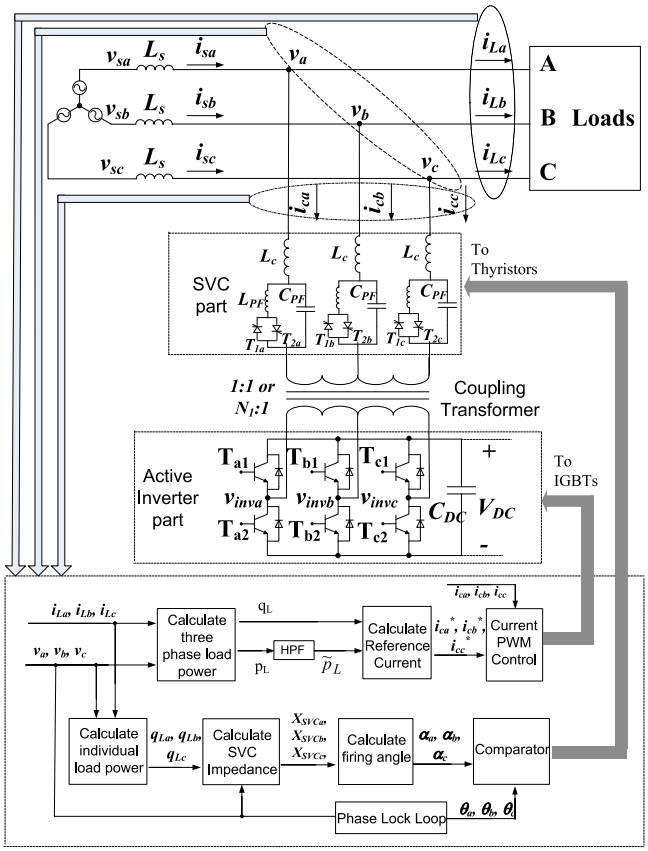

Fig. 2. Structure and control method of the SVC-HAPF.

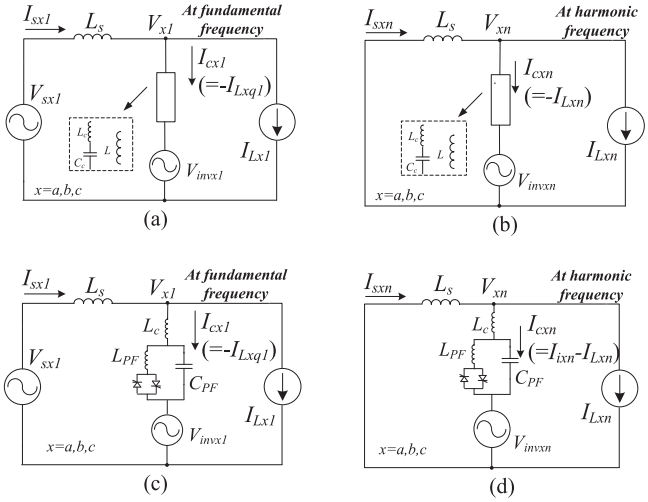

Fig. 3. Single-phase equivalent circuit models. (a) APF/HAPF fundamental frequency model. (b) HAPF harmonic frequency model. (c) SVC-HAPF fundamental frequency model. (d) SVC-HAPF harmonic frequency model.

outputs are the trigger signals for the thyristors in the SVC part and IGBTs in the active inverter part. For the SVC part control, the first step is to calculate the load reactive power q_{Lx} via the single-phase instantaneous p-q theory [19], [20]. The required fundamental impedance $X_{\mathrm{SVC}x}$ of the SVC part can then be obtained based on the load reactive power q_{Lx} and load voltage v_x. The corresponding firing angle α_x of the SVC part can then be obtained. Finally, by comparing the firing angle α_x with the phase angle of the load voltage θ_x, the trigger signals for the thyristor of the SVC can be obtained.

The active inverter part is used to limit the compensating current i_{cx} to its reference i_{cx}^*, which includes the harmonic component and reactive power component. By using the instantaneous p-q theory [13], the instantaneous active power and reactive power in $\alpha-\beta$ frame can be calculated from the load voltage and current (v_x and i_{Lx}). The obtained reactive power and harmonic active power can then be used to calculate the reference i_{cx}^*. Through the current hysteresis pulsewidth modulation (PWM) control method, the trigger signals for the active inverter part can be generated by comparing i_{cx} with i_{cx}^*. Discussions of the tradeoffs of different PWM control methods are included in the Appendix.

Fig. 3 shows the single-phase equivalent fundamental and harmonic frequency circuit models of the APF, HAPF, and SVC-HAPF. The coupling impedances of the models are found to be different. For the harmonic models in Fig. 3(b) and (d), the L part of APF and the LC part of the HAPF cannot generate the harmonic current, while the SVC part of SVC-HAPF can produce the harmonic current I_{ixn}. Therefore, the compensating current I_{cxn} of SVC-HAPF includes both the load harmonic current I_{Lxn} and the SVC part harmonic current I_{ixn}.

III. Rating Ratio of the Active Inverter Part and the SVC Part, and the Minimum Required DC-Link Voltage of SVC-HAPF

Based on the circuit analysis in Fig. 2, the power rating in the active inverter part can be calculated as $V_{\mathrm{inv}x}I_{cx}$, while the power rating of the SVC part can be calculated as $V_{\mathrm{SVC}}I_{cx}$. Accordingly, the power rating ratio of the active inverter and the SVC parts ($S_{\mathrm{inv}x}/S_{\mathrm{SVC}x}$) can be expressed as

$$R_{\mathrm{tot}} = \frac{S_{\mathrm{inv}x}}{S_{\mathrm{svc}x}} = \frac{V_{\mathrm{inv}x}\cdot I_{cx}}{V_{\mathrm{svc}x}\cdot I_{cx}} = \frac{V_{\mathrm{inv}x}}{V_{\mathrm{svc}x}} \tag{1}$$

where $S_{\mathrm{inv}x}$ and $S_{\mathrm{SVC}x}$ are the ratings of the phase active inverter part and the SVC part; $V_{\mathrm{inv}x}$ and $V_{\mathrm{SVC}x}$ are the phase root-mean-square (RMS) voltages of the active inverter part and the SVC part, and I_{cx} is the phase RMS compensating current. The required dc-link voltage $V_{\mathrm{DC\_tot}}$ can be expressed as [28]–[30]

$$V_{\mathrm{DC\_tot}} = \sqrt{6}\cdot V_{\mathrm{inv}x}. \tag{2}$$

As shown in Fig. 3(c) and (d), the current passing through the SVC-HAPFs includes both fundamental and harmonic components. Therefore, the $V_{\mathrm{SVC}x}$ and $V_{\mathrm{inv}x}$ in (1) and (2) can be expressed by using Ohm's law as

$$V_{\mathrm{SVC}x} = \sqrt{V_{\mathrm{SVC}x1}^2 + \sum_{n=2}^{\infty} V_{\mathrm{SVC}xn}^2} = \sqrt{\left(X_{\mathrm{SVC}1}\cdot I_{cx1}\right)^2 + \sum_{n=2}^{\infty}\left(X_{\mathrm{SVC}n}\cdot I_{cxn}\right)^2} \tag{3}$$

$$V_{\mathrm{inv}x} = \sqrt{V_{\mathrm{inv}x1}^2 + \sum_{n=2}^{\infty} V_{\mathrm{inv}xn}^2} = \sqrt{V_{\mathrm{inv}x1}^2 + \sum_{n=2}^{\infty} \left(X_{\mathrm{SVC}n} \cdot I_{cxn}\right)^2}. \quad (4)$$

Combining (1)–(4), the R_{tot} and $V_{\mathrm{DC\_tot}}$ can also be expressed in terms of fundamental and harmonic components as

$$\mathrm{R_{tot}} = \sqrt{\frac{V_{\mathrm{inv}x1}^2}{V_{\mathrm{SVC}x1}^2 + \sum_{n=2}^{\infty} V_{\mathrm{SVC}xn}^2} + \frac{\sum_{n=2}^{\infty} V_{\mathrm{inv}xn}^2}{V_{\mathrm{SVC}x1}^2 + \sum_{n=2}^{\infty} V_{\mathrm{SVC}xn}^2}} = \sqrt{R_{\mathrm{tot}1}^2 + \sum_{n=2}^{\infty} R_{\mathrm{tot}n}^2} \quad (5)$$

$$V_{\mathrm{DC\_tot}} = \sqrt{6 \cdot V_{\mathrm{inv}x1}^2 + 6 \cdot \sum_{n=2}^{\infty} V_{\mathrm{inv}xn}^2} = \sqrt{V_{\mathrm{DC\_tot}1}^2 + \sum_{n=2}^{\infty} V_{\mathrm{DC\_tot}n}^2}. \quad (6)$$

In (1)–(6), the subscript "n" stands for the fundamental ($n = 1$) and harmonic ($n \geq 2$) frequency components. X_{SVC1} and $X_{\mathrm{SVC}n}$ are the impedance of the SVC part at the fundamental and at each harmonic frequency order. $V_{\mathrm{inv}x1}$ and $V_{\mathrm{inv}xn}$ are the fundamental and harmonic inverter output voltage. I_{cx1} and I_{cxn} are the fundamental and harmonic compensating currents. The I_{cxn} includes two parts: I_{ixn} and I_{Lxn}. I_{ixn} represents the self-harmonic injection current components by SVC and I_{Lxn} represents the loading harmonic current components. R_{tot1} and $V_{DC\_\mathrm{tot}1}$ along with $R_{\mathrm{tot}n}$ and $V_{\mathrm{DC\_tot}n}$ are the fundamental and harmonic components of the power rating ratio R_{tot} and the dc-link voltage of $V_{\mathrm{DC\_tot}}$, respectively.

In the following analysis, the R_{tot} in (5) and $V_{\mathrm{DC\_tot}}$ in (6) is deduced, compared, and discussed through six parts, described as follows.

1) *In Section III-A:* The parameter design and characteristics of SVC (X_{SVC1} and $X_{\mathrm{SVC}n}$) are proposed and discussed.
2) *In Section III-B:* The fundamental components (R_{tot1} and $V_{DC\_\mathrm{tot}1}$) of R_{tot} and $V_{\mathrm{DC\_tot}}$ are deduced.
3) *In Section III-C:* The harmonic components ($R_{\mathrm{tot}n}$ and $V_{\mathrm{DC\_tot}n}$) of R_{tot} and $V_{\mathrm{DC\_tot}}$ are obtained.
4) *In Section III-D:* The required R_{tot} and $V_{\mathrm{DC\_tot}}$ are deduced and discussed.
5) *In Section III-E:* Simulation case studies are provided.
6) *In Section III-F:* A section summary is drawn.

The calculation of the parameters in R_{tot} (5) and $V_{\mathrm{DC\_tot}}$ (6) are explained in Sections III-A–III-C. In Section III-D, the deduced R_{tot} in (5) and $V_{\mathrm{DC\_tot}}$ in (6) are plotted in Figs. 8 and 9 discussions of R_{tot} and $V_{\mathrm{DC\_tot}}$ are also included. The simulation case studies are provided in Section III-E to verify the analysis in Sections III-A–III-D. Finally, a section summary is drawn in Section III-F.

A. Parameter Design and Characteristics of SVC

The expressions of impedance of SVC ($X_{\mathrm{SVC}n}$) at fundamental ($n = 1$) and harmonic frequency order ($n = 2, 3, 4 \ldots$) can be given as

$$X_{\mathrm{SVC}n}(\alpha) = \left| \frac{\pi(n\omega L_{\mathrm{PF}})}{(2\pi - 2\alpha + \sin 2\alpha) - \pi(n\omega)^2 \cdot L_{\mathrm{PF}} C_{\mathrm{PF}}} + n\omega L_c \right| \quad (7)$$

where α is the firing angle, ω is the angular frequency ($\omega = 2\pi f$), and f is the fundamental frequency.

At the fundamental frequency, the compensating reactive power by the SVC part (Q_{cx_SVC}) can be expressed as

$$Q_{cx\_\mathrm{SVC}} = \frac{V_{x1}^2}{X_{\mathrm{SVC1}}(\alpha)} \quad (8)$$

where V_{x1} is the RMS value of the fundamental load voltage, and X_{SVC1} can be obtained from (7) with $n = 1$.

From Figs. 2 and 3, the impedance SVC part is controlled by back-to-back connected thyristors T_{1x} and T_{2x} through the firing angle α. When $\alpha = 180^\circ$, the SVC part provides the maximum capacitive compensating reactive power $Q_{cx\_\mathrm{SVC(MaxCap)}}$ for inductive load reactive power compensation. However, when $\alpha = 90^\circ$, the SVC part provides the maximum inductive reactive power $Q_{cx\_\mathrm{SVC(MaxInd)}}$ for capacitive load reactive power compensation. Based on (7) and (8), the L_{PF} and C_{PF} of the SVC part can be designed as

$$C_{\mathrm{PF}} = \frac{Q_{Lx(\mathrm{MaxInd})}}{\omega^2 \cdot Q_{Lx(\mathrm{MaxInd})} \cdot L_c - \omega \cdot V_{x1}^2} \quad (9)$$

$$L_{\mathrm{PF}} = \frac{V_{x1}^2 - \omega L_c Q_{Lx(\mathrm{MaxCap})}}{\omega \cdot Q_{Lx(\mathrm{MaxCap})} - \omega^3 \cdot L_c \cdot C_{PF} \cdot Q_{Lx(\mathrm{MaxCap})} + \omega \cdot V_{x1}^2 \cdot C_{\mathrm{PF}}} \quad (10)$$

where $Q_{Lx(\mathrm{MaxInd})}$ and $Q_{Lx(\mathrm{MaxCap})}$ are the load maximum inductive and capacitive reactive power, respectively.

Based on (7), the design criteria of L_c can be expressed as

$$L_c = \frac{1}{(\omega n_1)^2 C_{\mathrm{PF}}} (X_{\mathrm{SVC}}(n) = 0, \text{ with } \alpha = 180^\circ)$$
$$L_c = \frac{1}{(\omega n_2)^2 C_{\mathrm{PF}} - 1/L_{\mathrm{PF}}} (X_{\mathrm{SVC}}(n) = 0, \text{ with } \alpha = 90^\circ). \quad (11)$$

According to the research in [29], the L_c in the SVC part is to filter out the current ripple caused by the power switches of the active inverter part. In [30], the L_c is designed to tune the n_1 and n_2 away from the dominated harmonic orders. In [27]–[31], the zero harmonic impedance point is in fact tuned at around the 3.7th harmonic order ($X_{\mathrm{SVC}}(n) = 0$ at $n_1 \approx n_2 \approx n \approx 3.7$) [27]–[31].

In this study, the proposed fifth-harmonic order ($X_{\mathrm{SVC}}(n) = 0$ at $n_1 \approx n_2 \approx n \approx 5$) is based on the general comparative performance evaluation (in Fig. 4) and the minimized R_{tot} inverter design (in Fig. 5).

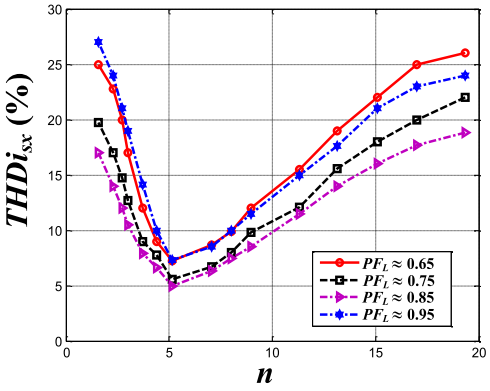

Fig. 4. Simulated source current THD_{isx} with different PF_L and tuned at different n after SVC-HAPF compensation ($V_{\text{DC\_tot}} = 2500$ V).

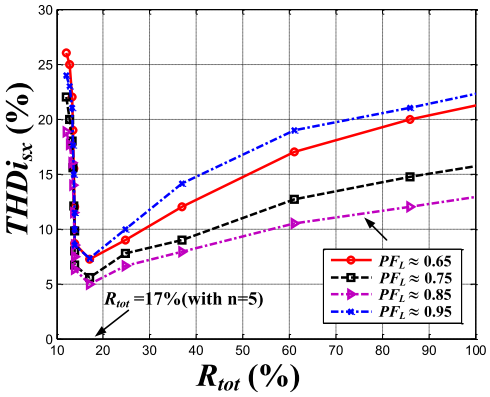

Fig. 5. Simulated source current THD_{isx} with different load power factor (PF_L) after SVC-HAPFs compensation with different R_{tot}.

Fig. 4 shows that the SVC-HAPF with $X_{\text{SVC}}(n) = 0$ at $n = 5$ can provide the best compensation results. The performance of SVC-HAPF becomes worse with $X_{\text{SVC}}(n) = 0$ at $n < 5$ or $n > 5$. Fig. 5 shows that the SVC-HAPF with $R_{\text{tot}} = 17\%$ can provide the relatively best THD_{isx} performance. In addition, the corresponding zero impedance point for $R_{\text{tot}} = 17\%$ is $n \approx 5$.

In the following, two different designs for the SVC part with $X_{\text{SVC}}(n) = 0$ at $n \approx 3.7$ [27]–[31] and the proposed $X_{\text{SVC}}(n) = 0$ at $n \approx 5$ are discussed.

B. Fundamental Frequency Analysis of R_{tot1} and V_{DCtot1}

From Fig. 3(c), the fundamental inverter voltage V_{invx1} can be expressed as

$$V_{\text{invx1}} = V_{x1} - X_{\text{SVC1}}(\alpha) \cdot I_{cx1} \tag{12}$$

where V_{x1}, I_{cx1}, and X_{SVC1} are the fundamental load voltage, fundamental compensating current, and fundamental SVC part impedance, respectively. The load reactive power can be expressed as

$$Q_{\text{Lx}} = V_{x1} \cdot I_{Lxq1} = V_{x1} \cdot (-I_{cx1}) \tag{13}$$

where Q_{Lx} is the loading reactive power and I_{Lxq1} is the load fundamental reactive current, which is equal to $-I_{cx1}$ during

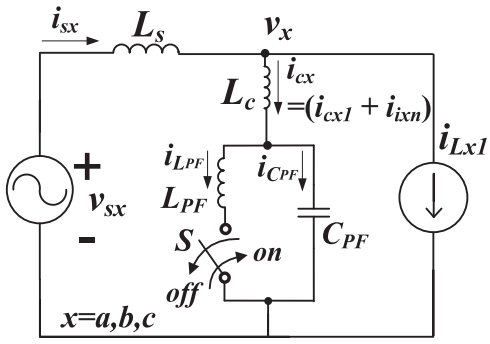

Fig. 6. SVC equivalent single-phase model for harmonic currents rejection analysis.

compensation. Combining (2), (8), (12), and (13), the R_{tot1} and $V_{\text{DC\_tot1}}$ can be expressed as

$$R_{\text{tot1}} = \frac{V_{\text{invx1}}}{V_{\text{SVC1}}} = \left| \frac{|Q_{\text{Lx}}| - |Q_{cx\_\text{SVC}}|}{Q_{Lx}} \right| \tag{14}$$

$$V_{\text{DC\_tot1}} = \sqrt{6} \cdot V_{\text{invx1}} = \sqrt{6} \cdot V_{x1} \left| \frac{|Q_{\text{Lx}}| - |Q_{cx\_\text{SVC}}|}{Q_{cx\_\text{SVC}}} \right|. \tag{15}$$

In (14) and (15), Q_{cx_SVC} and Q_{Lx} are the compensating reactive power by the SVC part and the load reactive power, respectively.

C. Harmonic Frequency Analysis of R_{totn} and $V_{\text{DC\_totn}}$

As shown in Fig. 3(d), the harmonic compensating current can be expressed as

$$I_{cxn} = I_{ixn} + (-I_{\text{L}xn}) \tag{16}$$

where I_{ixn} is the self-harmonic injection current by SVC and I_{Lxn} is the load harmonic current.

In this section, the required R_{totn} and $V_{\text{DC\_totn}}$ are discussed separately in two sections. In Section III-C1, the required R_{totn} and $V_{\text{DC\_totn}}$ to compensate i_{ixn} injected by the SVC part are deduced under assumptions of $I_{cxn} = I_{ixn}$ and $I_{Lxn} = 0$ (linear loading condition). In Section III-C2, the total required R_{totn} and $V_{\text{DC\_totn}}$ are obtained so that both current I_{Lxn} and I_{ixn} ($I_{cxn} = I_{ixn} + (-I_{Lxn})$) can be compensated for the nonlinear loading condition.

1) R_{totn} and $V_{\text{DC\_totn}}$ for Compensating Self-Harmonic Injection Current by SVC Part (i_{ixn}) Only: In this section, the required R_{totn} and $V_{\text{DC\_totn}}$ can be obtained to compensate for i_{ixn} injected by the SVC part. To clearly illustrate the i_{ixn} problem, the loading is assumed to be linear ($i_{Lxn} = 0$). The equivalent single-phase self-harmonic current rejection analysis model is provided in Fig. 6.

In Fig. 6, the thyristors (T_{1x} and T_{2x}) in each phase of the SVCs can be considered as a pair of bidirectional switches, which can generate the low-order harmonic current i_{ixn}. As the switch S turns ON and OFF, the two differential equations of

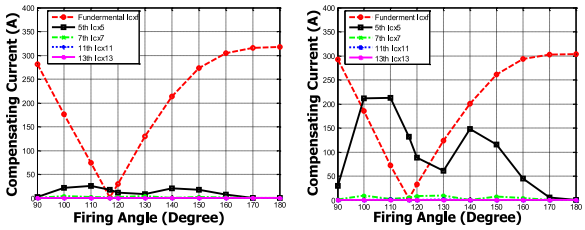

Fig. 7. Simulated fundamental and harmonic compensating currents at different firing angles under linear loading with: (a) SVC with ($X_{\rm SVC}(n) = 0$ at $n \approx 3.7$) [27]–[31] and (b) SVC with ($X_{\rm SVC}(n) = 0$ at $n \approx 5$)

$i_{cx}(t)$ ($i_{cx\_\rm off}$ and $i_{cx\_\rm on}$) can be obtained as

$$i_{cx\_\rm off} = i_{cx1} + i_{ixn} = A_1 \sin(\omega t - \alpha) + K_1 \sin(\omega_{n1} t + \varphi_{\rm n1}) \quad \text{Fundamental} \quad \text{Harmonic} \tag{17}$$

$$i_{cx\_on} = i_{cx1} + i_{ixn} = A_2 \sin(\omega t + \alpha) + K_2 \cos(\omega_{\rm n2} t + \varphi_{n2}) + K_3 \quad \text{Fundamental} \quad \text{Harmonic} \tag{18}$$

where A_1 and A_2 are the peak values of the fundamental compensating current during each turn off and turn on; K_1, K_2, K_3, ϕ_{n1}, and ϕ_{n2} are constants during each switching cycle and depend on the initial conditions of the compensating current and capacitor voltages; and ω_{n1} and ω_{n2} are the harmonic angular frequencies, which can be expressed as

$$\omega_{\rm n1} = \frac{1}{\sqrt{(L_s + L_c) \cdot C_{\rm PF}}} \left(n_1 = \frac{\omega_1}{2\pi f} = \frac{1}{2\pi f \sqrt{(L_s + L_c) \cdot C_{\rm PF}}} \right) \tag{19}$$

$$\omega_{\rm n2} = \sqrt{\frac{L_s + L_c + L_{\rm PF}}{(L_s + L_c) \cdot L_{\rm PF} C_{\rm PF}}} \left(n_2 = \frac{\omega_2}{2\pi f} = \frac{1}{2\pi f} \sqrt{\frac{L_s + L_c + L_{\rm PF}}{(L_s + L_c) \cdot L_{\rm PF} C_{\rm PF}}} \right) \tag{20}$$

where L_s is the system inductor, which is typically a small value, and the L_c, $L_{\rm PF}$, and $C_{\rm PF}$ are parameters in the SVC part.

Fig. 7 shows the fundamental and harmonic compensating current at different firing angles of two SVC-HAPFs. For a three-phase three-wire system, the common harmonic orders are $6n \pm 1$ (≥ 5) with $n = 1, 2, 3 \ldots$. Based on Fig. 7(a), (19), and (20), if the SVC part is with $X_{\rm SVC}(n) = 0$ at $n \approx 3.7$, the generated harmonic current can be significantly reduced as the possible generated harmonic orders n_1 and n_2 are far from the $6n \pm 1$ order. From Fig. 7(b), for the SVC part with $X_{\rm SVC}(n) = 0$ at $n \approx 5$, the significant fifth-order harmonic current can be generated when n_1 and n_2 are designed close to 5.

2) $R_{\rm totn}$ and V_{DC_totn} for Compensating Both Load Harmonic Current (i_{Lxn}) and Self-Harmonic Injection Current (i_{ixn}): As the SVC has poor harmonic compensation ability, the active inverter part of SVC-HAPF is designed to compensate load harmonic current i_{Lxn} and to absorb the SVC self-generated i_{ixn} (already discussed in Section III-C1) simultaneously.

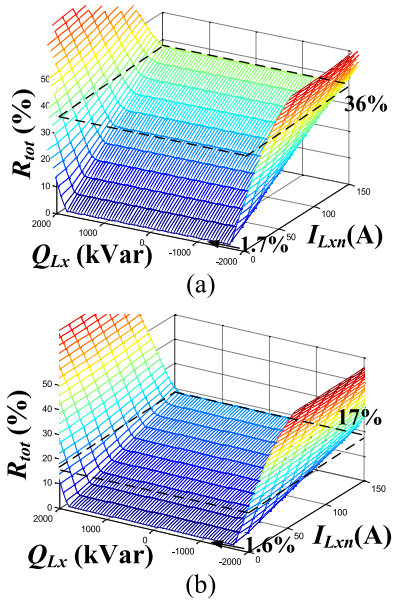

Fig. 8. Ratio of $R_{\rm tot}$ with varying Q_{Lx} and I_{Lxn}. (a) SVC-HAPF with ($X_{\rm SVC}(n) = 0$ at $n \approx 3.7$) [27]–[31] and (b) SVC-HAPF with ($X_{\rm SVC}(n) = 0$ at $n \approx 5$).

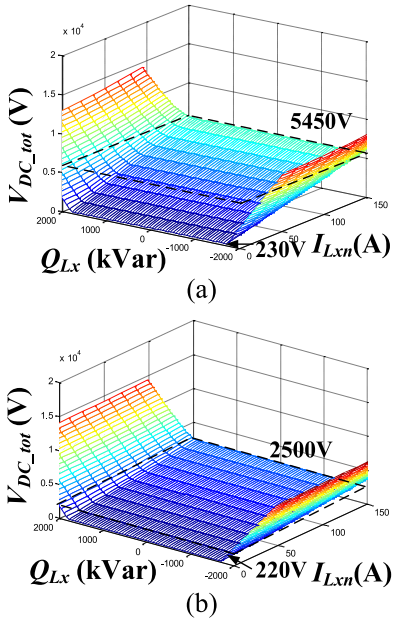

Fig. 9. $V_{\rm DC\_tot}$ with varying Q_{Lx} and I_{Lxn}. (a) SVC-HAPF with ($X_{\rm SVC}(n) = 0$ at $n \approx 3.7$) [27]–[31]. (b) SVC-HAPF with ($X_{\rm SVC}(n) = 0$ at $n \approx 5$).

In this study, the six-pulse rectifier nonlinear loads are considered as the worst case of the three-phase three-wire harmonic loads ($I_{Lxn} = I_{Lx1}/n$). As the rating of a nonlinear loading is 10 kV to 500 A, the total required $R_{\rm totn}$ and $V_{\rm DC\_totn}$ of SVC-HAPFs for compensating both i_{ixn} and i_{Lxn} can be plotted as in Figs. 8 and 9.

D. Minimizing Inverter Capacity Design of $R_{\rm tot}$ and $V_{\rm DC\_tot}$

In this section, minimizing the inverter capacity design of SVC-HAPF is discussed, including the fundamental compo-

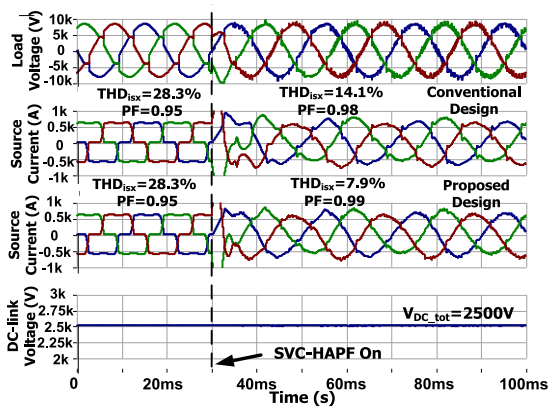

Fig. 10. Simulated load voltage, source current under SVC-HAPF ($X_{\rm SVC}(n \approx 3.7) = 0$) compensation [27]–[31], and source current under SVC-HAPF($X_{\rm SVC}(n \approx 5) = 0$) compensation.

nent (discussed in *Section III-B*) and harmonic components (discussed in Section III-C). The $R_{\rm tot}$ in (5) and $V_{\rm DC\_tot}$ in (6) are plotted in Figs. 8 and 9, which also show the $R_{\rm tot}$ and $V_{\rm DC\_tot}$ with varying Q_{Lx} and I_{Lxn} (also including I_{ixn}) for different SVC-HAPFs.

From Figs. 8 and 9, at $I_{Lxn} = 0$, it can be seen that the SVC-HAPF still requires the $R_{\rm tot}$ and $V_{\rm DC\_tot}$ to absorb the self-harmonic injection currents by the SVC part, which is consistent with the discussions in *Section III-C1*. With I_{Lxn} increasing, the required $R_{\rm tot}$ and $V_{\rm DC\_tot}$ are also increasing. When the Q_{Lx} is outside of the designed Q_{cx_SVC} range, the designed $R_{\rm tot}$ and $V_{\rm DC\_tot}$ can further enlarge the reactive power compensation range of the SVC part, which is consistent with the analysis in *Section III-B*. As the SVC-HAPF ($X_{\rm SVC}(n) = 0$ at $n \approx 5$) requires a lower dc-link voltage for nonlinear loading compensation ($I_{Ln} > 0$), the following discussions focus on SVC-HAPF ($X_{\rm SVC}(n) = 0$ at $n \approx 5$).

E. Simulated Comparison Between the Conventional SVC-HAPF and the Proposed SVC-HAPF

In this section, simulation case studies are conducted using PSCAD/EMTDC. Fig. 10 illustrates the load voltage (and its ripple), the source current, load current, and dc-link voltage waveforms for 10 kV to 500 A six-pulse rectifier nonlinear load before and after different SVC-HAPF compensations.

Based on Fig. 9, the required dc-link voltage of the SVC-HAPF ($X_{\rm SVC}(n) = 0$ at $n \approx 5$) is lower than the SVC-HAPF ($X_{\rm SVC}(n) = 0$ at $n \approx 3.7$) for nonlinear loads compensation. The dc-link voltage of 2500 V is designed based on the SVC-HAPF tuned at the fifth-harmonic order ($X_{\rm SVC}(n) = 0$ at $n \approx 5$) as in Fig. 10. Thus, the SVC-HAPF ($X_{\rm SVC}(n) = 0$ at $n \approx 5$) can provide better THD and PF performance [see Fig. 10(b)] than the SVC-HAPF tuned at the 3.7th harmonic order, which is due to insufficient dc-link voltage [see Fig. 10(a)], as verified by Fig. 9. The detailed descriptions of compensation performance are given below.

From Fig. 10, after the SVC-HAPF compensation, the PF is improved to ≥0.98 for both SVC-HAPFs under the same dc-link voltage. However, the source current THDi_{sx} is improved to 14.1% for the design of $X_{\rm SVC}(n \approx 3.7) = 0$ case, while THDi_{sx} is improved to less than 8% for the design of $X_{\rm SVC}(n \approx 5) = 0$ case. Therefore, the SVC-HAPF ($X_{\rm SVC}(n \approx 5) = 0$) has better compensating performance.

TABLE II
COMPARISON AMONG THE CONVENTIONAL DESIGN AND THE PROPOSED DESIGN SVC-HAPFS

		SVC-HAPF ($X_{SVC}(n)$ =0 at n≈3.7)	SVC-HAPF ($X_{SVC}(n)$ =0 at n≈5)
Required V_{DC_tot} and R_{tot}	Linear loads comp. (Fig. 7)	Low	Low
	Nonlinear loads comp. (Fig. 10)	Medium	Low
Performance Evaluation (Fig. 4)		Normal	Good

F. Summary of the Conventional SVC-HAPF and the Proposed SVC-HAPF

Based on the above discussions, a brief summary is drawn in Table II. This shows that the SVC-HAPF with $X_{\rm SVC}(n) = 0$ at $n \approx 3.7$ requires lower $R_{\rm tot}$ and $V_{\rm DC\_tot}$ for linear loads compensation, whereas the SVC-HAPF ($X_{\rm SVC}(n) = 0$ at $n \approx 5$) requires lower $R_{\rm tot}$ and $V_{\rm DC\_tot}$ for both linear and nonlinear loads compensation.

When the loads are linear, the SVC part is the only harmonic source, which can generate low-order harmonic currents when the switches/thyristors change their states. The two designs use different approaches to avoid harmonic injection by the SVC part. To avoid the harmonic currents injection by the SVC part, the conventional design $X_{\rm SVC}(n) = 0$ at $n \approx 3.7$ suggests tuning the zero impedance point away from the $6n \pm 1$th order and/or close to the 3nth order (e.g., $n \approx 3.7$). Thus, the SVC part does not generate a large harmonic current to the system, so the rating of the active inverter part can be reduced. Unlike the conventional method, the proposed SVC part with $X_{\rm SVC}(n) = 0$ at $n \approx 5$ may generate a fifth-order harmonic current. The SVC part also provides a zero impedance path for the generated fifth-order harmonic current flowing into the active part. Thus, the active inverter part can easily absorb the generated fifth-order harmonic current without affecting the compensation performance. Therefore, the required active inverter rating of the proposed design can be low for linear loads compensation.

When the loads are nonlinear, the required dc-link voltages for harmonic compensation are different for the two designs, which can be expressed as

$$V_{\rm DC\_toth} \approx \sqrt{6} \cdot V_{{\rm inv}xh} = \sqrt{6} \cdot \sqrt{\sum_{n=2}^{\infty} V_{{\rm inv}xn}^2} = \sqrt{6} \cdot \sqrt{\sum_{n=2}^{\infty} \left(X_{{\rm SVC}n} \cdot I_{Lxn}\right)^2} \quad (21)$$

where $V_{\rm DC\_toth}$ is the required dc-link voltage for harmonic current compensation, I_{Lxn} is the load harmonic current, and $X_{{\rm SVC}n}$ is the harmonic impedance of the SVC part. In (21), the difference between the conventional design and the proposed design is the $X_{{\rm SVC}n}$ values at each harmonic order. Based on

(6), (21), and Fig. 9, the proposed design with $X_{\mathrm{SVC}}(n) = 0$ at $n \approx 5$ has a lower required $V_{\mathrm{DC\_tot}h}$ than the conventional design with $X_{\mathrm{SVC}}(n) = 0$ at $n \approx 3.7$. Therefore, the proposed design $X_{\mathrm{SVC}}(n) = 0$ at $n \approx 5$ can obtain better THD and PF performance with the same dc-link voltage as in Figs. 4, 5, and 10.

IV. Comparisons Among the Conventional APF, HAPF, and the Proposed SVC-HAPF

In this section, comparisons are provided among the APF, HAPF, and the proposed SVC-HAPF. In Section IV-A, comparisons of dc-link voltages are given for APF, HAPF, and SVC-HAPF, and in Section IV-B, simulation comparisons are provided.

A. DC-Link Voltage Comparison

The dc-link voltage of the APF and HAPF can be deduced with the help of Fig. 3(a) and (b). Based on these, the equations for APF and HAPF can be obtained as

$$V_{\mathrm{invx1(APF)}} = |V_{x1} + X_{L1} \cdot I_{Lxq1}| = V_{x1} \cdot \left| \frac{V_{x1}^2 / X_{L1} - V_{x1} I_{Lxq1}}{V_{x1}^2 / X_{L1}} \right| = V_{x1} \cdot \left| \frac{Q_{cx\_L} + Q_{Lxf}}{Q_{cx\_L}} \right| \tag{22}$$

$$V_{\mathrm{invx1(HAPF)}} = |V_{x1} - (X_{Cc1} - X_{Lc1}) \cdot I_{Lxq1}| = V_{x1} \cdot \left| \frac{Q_{cx\_LC} - Q_{Lxf}}{Q_{cx\_LC}} \right| \tag{23}$$

$$V_{\mathrm{invxn(APF)}} = X_{Ln} \cdot I_{Lxn} \tag{24}$$

$$V_{\mathrm{invxn(HAPF)}} = (X_{Ccn} - X_{Lcn}) \cdot I_{Lxn} \tag{25}$$

where X_{L1}, X_{Ln}, X_{Cc1}, X_{Ccn}, X_{Lc1}, and X_{Lcn} are the fundamental and harmonic impedances of the coupling inductor (L) of APF, coupling capacitor (C_c), and inductor (L_c) of the HAPF, respectively. I_{Lxq1} is the reactive power component of the load current, and I_{Lxn} is the load harmonic current. In (22), the loading reactive power, the reactive power provided by the coupling L part of the APF, and the coupling LC part of the HAPF can be expressed as

$$Q_{Lx1} = V_{x1} \cdot I_{Lxq1} \tag{26}$$

$$Q_{cx1\_L} = V_{x1}^2 / X_{L1} \tag{27}$$

$$Q_{cx1\_LC} = V_{x1}^2 / (X_{L1} - X_{C1}). \tag{28}$$

Based on (6), (22)–(28), the required dc-link voltages of the APF and HAPF can be plotted as in Fig. 11.

By comparing Figs. 11 with 9(b), the following brief conclusions can be drawn.

1) For APF, as shown in Fig. 11(a), the required $V_{\mathrm{invx(APF)}}$ is close to V_x due to the small coupling impedance X_L.
2) The HAPF has a low dc-link voltage characteristic only within a narrow inductive load range. When the load reactive power is outside its designed range, the HAPF requires a high dc-link operating voltage (>10 kV) due to its large coupling capacitor impedance, and, thus, it easily loses its low-inverter rating advantage.
3) The SVC-HAPF has the desirable characteristic of a wide compensation range (from capacitive to inductive reactive power) with a low dc-link voltage.

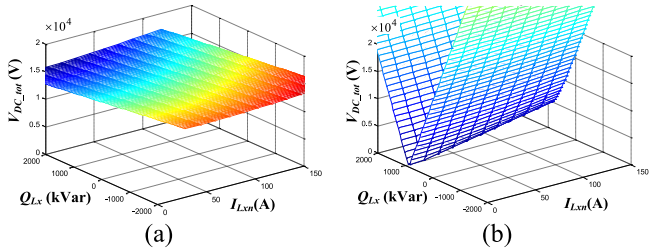

Fig. 11. $V_{\mathrm{DC\_tot}}$ with varying Q_{Lx} and I_{Lxn}. (a) APF. (b) HAPF.

TABLE III
Simulation System Parameters for APF, HAPF, and SVC-HAPF

	Parameters	Physical values
System parameters	V_{LL}, f, L_s	10 kV, 50 Hz, 0.1 mH
APF	L	5 mH
HAPF	L_c, C_c	5 mH, 80 μF
SVC-HAPF	L_c, L_{PF}, C_{PF}	5 mH, 30 mH, 80 μF
Case *A*: 1st inductive loads	L_{L1}, R_{L1}, Q_{Lx}	30 mH, 14 Ω, 1095 kvar (0.38 p.u.)
Case *B*: 2nd inductive loads	L_{L2}, R_{L2}, Q_{Lx}	30 mH, 9 Ω, 1840 kvar (0.64 p.u.)
Case *C*: Capacitive loads	C_{L3}, R_{L3}, Q_{Lx}	200 μF, 20 Ω, -813 kvar (-0.28 p.u.)

B. Simulated Comparison Between the HAPF and the Proposed SVC-HAPF

The tracking performance of APF, HAPF, and SVC-HAPF are compared and discussed in this section by simulation case studies. In the below simulations, the system parameters of the APF, HAPF, and SVC-HAPF are from Table III. In this study, the base values of the voltage, current, and power are $V_{\mathrm{base}} = 5.77$ kV ($V_{L-L} = 10$ kV), $I_{\mathrm{base}} = 500$ A, and $S_{\mathrm{base}} = 2887$ VA. The reactive powers of different loads in per unit (p.u.) values are provided in Table III. The power capacity of the active inverter parts of the APF, HAPF, and SVC-HAPF can be expressed as [26]

$$S_{\mathrm{inv}} = \sqrt{6} \cdot \frac{V_{\mathrm{DC\_tot}}}{\sqrt{2}} \cdot I_{cx} \tag{29}$$

where $V_{\mathrm{DC\_tot}}$ is the dc-link voltage and I_{cx} is the RMS value of the phase compensating current. The required power capacities of the active inverter part for different compensators are shown in Table IV.

Based on Fig. 12(a) and Table IV, the APF can provide a wide compensation range with high dc-link voltage $V_{\mathrm{DC\_tot}} = 15$ kV. For the different loads compensations, the APF can provide a satisfactory PF and source current THD_{isx} performance. After APF compensation, the PF is improved to ≥0.99 and THD_{isx} ≤4.2%.

From Fig. 12(b) and Table IV, the HAPF can only compensate for a narrow range of reactive power (matches only with the first inductive loads case). However, the HAPF cannot provide satisfactory source-side PF and current compensation results

TABLE IV
SIMULATION RESULTS BY USING APF, HAPF, AND SVC-HAPF

Load Type	Before/after Comp.	I_{sx}(A)	I_{cx}(A)	*PF*	$THDi_{sx}$(%)	V_{DC}(V)	S_{inv}(VA)
Case *A:* 1st inductive loads	Before Comp.	340	--	0.83	0.1	--	--
	APF	308	178	0.99	2.9	15.0k	4.62M
	HAPF	282	180	0.99	3.0	4.0k	1.25M.
	SVC-HAPF	290	184	1.00	2.4	2.5k	0.8M
Case *B:* 2nd inductive loads	Before Comp.	440	--	0.69	0.1	--	--
	APF	320	300	0.99	5.0	15.0k	7.80M
	HAPF	315	180	0.86	22.0	4.0k	1.25M
	SVC-HAPF	300	303	1.00	1.9	2.5k	1.31M
Case *C:* Capacitive loads	Before Comp.	225	--	0.78	0.1	--	--
	APF	192	132	1.00	4.2	15.0k	3.43M
	HAPF	372	180	0.62	26.5	4.0k	1.27M
	SVC-HAPF	181	132	1.00	4.0	2.5k	0.57M

**Shaded areas indicate undesirable results.*

when the reactive power is capacitive or outside its inductive compensation range. Specifically, the PF and THD$_{isx}$ are 0.86 and 22.0% for the second inductive loads compensation, and the PF and THD$_{isx}$ are 0.62 and 26.6% respectively, for the capacitive loads compensation.

From Fig. 12(c) and Table IV, the SVC-HAPF can provide a wide reactive power compensation range (from inductive to capacitive). After the proposed SVC-HAPF compensation, the source reactive power is reduced to around zero in different loads cases. The PF and THD$_{isx}$ are compensated to unity and $\leq$4.0%, respectively, for the different loads.

V. EXPERIMENTAL RESULTS

The experimental results should verify the dc-link voltage characteristics, tracking performances, and compensation performances of the APF, HAPF, and SVC-HAPF. The three-phase three-wire APF, HAPF, and SVC-HAPF experimental prototypes are constructed in the laboratory. The experimental conditions of the phase voltage and current in the laboratory are 110 V to 10 A. The base values of the voltage, current, and power are $V_{\text{base}} = 110$ V ($V_{L-L} = 191$ V), $I_{\text{base}} = 10$ A, and $S_{\text{base}} = V_{\text{base}} \cdot I_{\text{base}} = 1100$ VA (a total rating of 3.3 kVA for three phases). The constructed SVC-HAPF experimental prototype and the testing environment are shown in Fig. 13. The digital control system of the SVC-HAPF consists of two paralleled digital signal processors (DSPs) TMS320F2812s, and the basic settings of both DSPs are the same. The sampling frequency of the control system is 25 kHz in both simulation and experiment (for both DSPs). For every 1/25 kHz(s) period, the timer will provide a signal to process analog-to-digital (A/D) conversion and the corresponding interrupt. The SanRex PK110FG160 thyristors are used for the SVC part, while the Mitsubishi IGBT intelligent power modules PM300DSA60 are used as the switching devices of the inverter. Two sets of loads are built. The first loading is the six-pulse rectifier nonlinear loads, while the second is the inductive linear loads. The parameters of APF, HAPF, SVC-HAPF, and loads are given in Table V. The experimental results are summarized in Table VI.

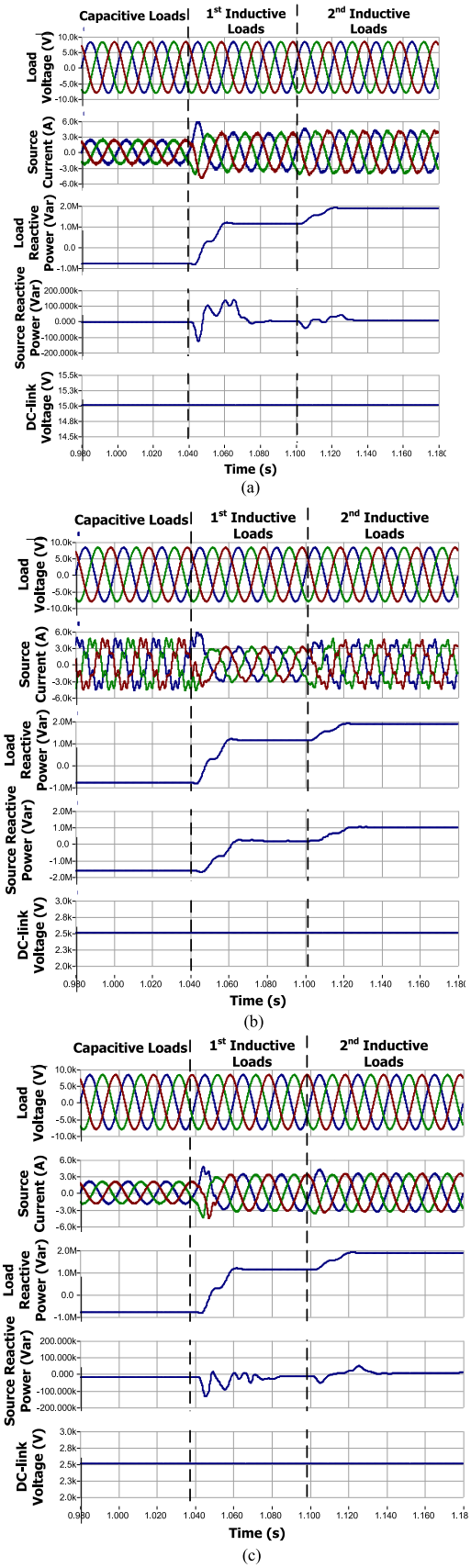

Fig. 12. Dynamic compensation waveforms of load voltage, dc-link voltage, source current, and load and source reactive powers by applying (a) APF, (b) HAPF, and (c) SVC-HAPF in different loadings cases.

Fig. 13. 110 V-5 kVA SVC-HAPF experimental prototype and its testing environment.

TABLE V
EXPERIMENTAL PARAMETERS FOR POWER QUALITY COMPENSATION OF APF, HAPF, AND SVC-HAPF

Systems	Parameters	Physical values
APF	L	5 mH(Q=18, ESR=0.09 Ω)
HAPF	L, C	5 mH(Q=18, ESR=0.09 Ω), 80 μF(Q=170, ESR=0.11 Ω)
SVC-HAPF	L_c, L_{PF}, C_{PF}	5 mH(Q=18, ESR=0.09 Ω), 30 mH(Q=23, ESR=0.41 Ω) 160 μF(Q=310, ESR=0.06 Ω)
1st loading	L_1, R_1, Q_1	25 mH, 50 Ω, 50 var (0.045 p.u.)
2nd loading	L_2, R_2, Q_2	70 mH, 15 Ω, 480 var (0.44 p.u.)

Notes: Q stands for the quality factor and ESR stands for equivalent series resistance

TABLE VI
EXPERIMENTAL RESULTS FROM USING APF, HAPF, AND SVC-HAPF

Load Type	Before/after Comp. for worst phase	I_{sx}(A)	I_{cx}(A)	PF	$THDi_{sx}$(%)	V_{DC}(V)
1st nonlinear load	Before Comp.	6.6	--	0.96	24.5	--
	APF	6.8	2.7	0.98	9.5	340
	HAPF	7.1	2.6	0.85	12.5	105
	SVC-HAPF	6.5	2.3	0.99	6.3	60
1st and 2nd nonlinear loads	Before Comp.	10.1	--	0.90	20.1	--
	APF	9.4	4.8	0.99	8.7	340
	HAPF	9.4	4.3	0.99	7.5	105
	SVC-HAPF	8.4	4.3	0.99	5.5	60

**Shaded areas indicate undesirable results.*

A. Experimental Results of APF

From Fig. 14 and Table VI, it can be seen that after APF compensation, the experimental PF and THD$_{isx}$ can be improved to 0.98 and 9.5%, respectively, for the worst phase for the first loading compensation, and 0.99 and 8.7, respectively, for the first and second loading compensation. The required dc-link voltage for APF is about 340 V.

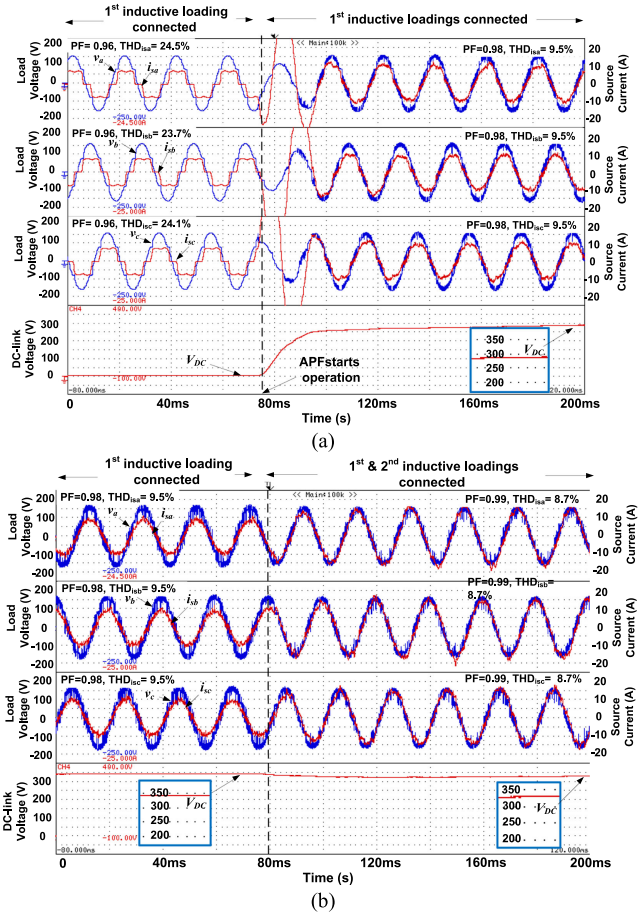

Fig. 14. Waveforms of source voltage, current, natural current, and dc-link voltage: Before and after APF starts operation (a) during the first load and (b) when the second load is connected.

For the transient performance, as shown in Fig. 14(b), when the load suddenly changes, the response time of the conventional APF is much less than one fundamental period.

B. Experimental Results of HAPF

From Fig. 15(a) and Table VI, it can be seen that the experimental PF and THD$_{isx}$ are compensated to 0.85 and 12.5%, respectively, for the worst phase after the HAPF compensation. Due to the loading falling outside of its operational range, the PF becomes even worse after compensation. During the start-up process, the HAPF requires about five fundamental periods to charge the dc-link voltage to its reference value. The dc-link charging period mainly depends on the design (such as P or PI gain) of the controller.

From Fig. 15(b) and Table VI, the experimental PF and THD$_{isx}$ are improved to 0.99 and 7.5%, respectively, for the worst phase during the first and second loads compensation. The required dc-link voltage for the HAPF is about 105 V. For the transient performance, as shown in Fig. 15(b), when the load suddenly changes the response time of the conventional HAPF is about 7 ms, which is less than one fundamental period.

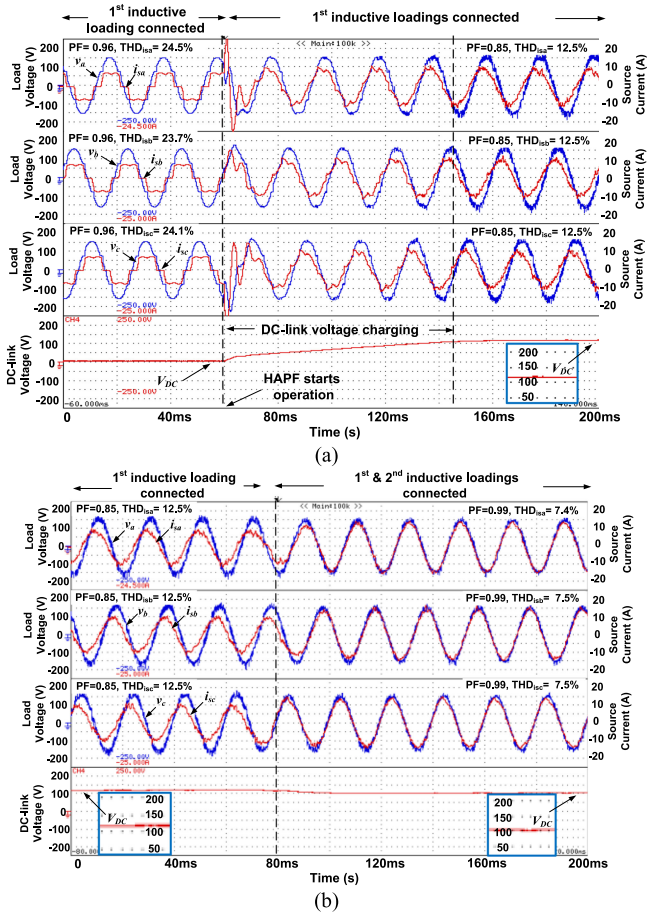

Fig. 15. Waveforms of source voltage, source current, and dc-link voltage: Before and after HAPF starts operation (a) during the first load case and (b) when the second load is disconnected.

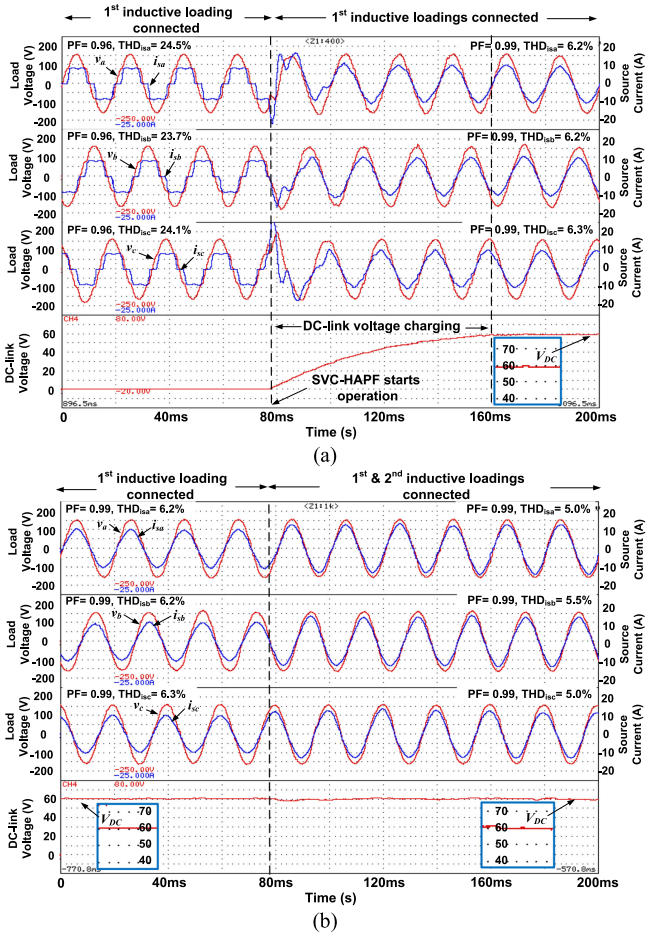

Fig. 16. Waveforms of source voltage, source current, and dc-link voltage: Before and after SVC-HAPF starts operation (a) during the first load case and (b) when the second load is connected.

Based on Fig. 15 and Table VI, the HAPF can be confirmed to have a narrow compensation range, thus causing overcompensation for the first loading compensation. The PF and THD$_{isx}$ compensation performance is also relatively poor for the first inductive loading case.

C. Experimental Results of SVC-HAPF

From Fig. 16(a) and Table VI, the experimental PF and THD$_{isx}$ can be improved to 0.99 and 6.3%, respectively, for the worst phase after SVC-HAPF compensation. During the start-up process, the SVC-HAPF also requires about five fundamental periods to charge the dc-link voltage to its reference value.

Based on Fig. 16(b) and Table VI, the experimental PF and THD$_{isx}$ are improved to 0.99 and 5.5%, respectively, for the worst phase during the first and second loads case. To compensate both loads, the required dc-link voltage for the SVC-HAPF is about 60 V, which is lower than that of the HAPF. The SVC-HAPF obtains a smooth transient performance, in which the response time is much less than one fundamental period. Comparing Figs. 15 with 16, the compensation results of the SVC-HAPF are better than the HAPF even with a lower dc-link voltage.

D. Power Loss and Efficiency Studies

The 1) switching loss, 2) component conduction loss, and 3) coupling transformer loss (SVC-HAPF only) contribute to the main power loss of the different compensators, which are discussed in Sections V-D1—V-D3, respectively. The total efficiency of APF, HAPF, and SVC-HAPF is provided in Section V-D4.

1) Switching Loss (Analysis and Measurement Results): The switching loss of the APF and HAPF are from the switching components (IGBTs) of the active inverter part. In contrast, the switching loss of the SVC-HAPF consists of two parts: 1) from the IGBTs of the active inverter part and 2) from the thyristors of the SVC part.

For the IGBTs in the active inverter part, the switching loss is obtained by measuring the collector–emitter voltage and the current of each IGBT, and the total inverter switching loss can

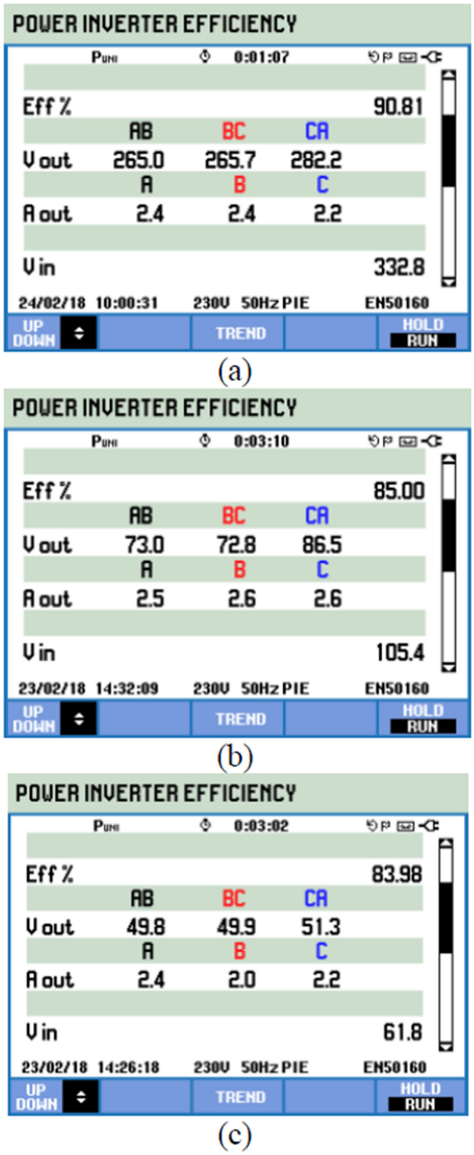

Fig. 17. Efficiency measurements for the first load compensation using (a) APF, (b) HAPF, and (c) SVC-HAPF.

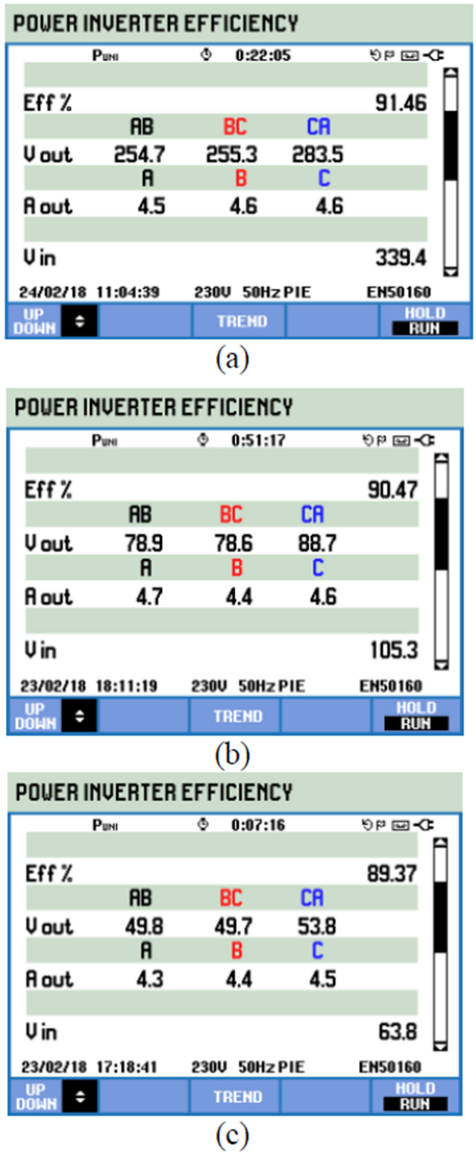

Fig. 18. Efficiency measurements for the first and second loads compensation using (a) APF, (b) HAPF, and (c) SVC-HAPF.

be found through the following equation [21]:

$$P_{\mathrm{sw(IGBT)}} = \sum_{n=0}^{n=6} P_{\mathrm{sw(IGBt),}n} = \sum_{n=0}^{n=6} \frac{1}{t_f} \int_0^{T_f} v_{ce,n}(t) \cdot i_{ce,n}(t) dt \quad (30)$$

where $v_{ce,n}(t)$ and $i_{ce,n}(t)$ are the collector–emitter voltage and current of IGBT, respectively. T_f is a fundamental period, and n is the number of IGBTs.

Each thyristor of the SVC part only turns on one time in a fundamental period, unlike the IGBTs of the active inverter part. In SVC-HAPF applications, the on-state switching loss is the dominant part for the thyristor, which can be easily calculated as [32]

$$P_{\mathrm{sw(thyristor)}} = \sum_{n=0}^{n=6} P_{\mathrm{thy},n} = \sum_{n=0}^{n=6} \left(U_{TO,n} \times I_{T\mathrm{AV},n} + r_T \times I^2_{T\mathrm{RMS},n} \right) \quad (31)$$

where $I_{T\mathrm{RMS},n}$ is the RMS value of the current passing through the thyristor, $I_{T\mathrm{AV},n}$ is the average value of the same current, U_{TO} is the thyristor threshold voltage, and r_T is the thyristor slope resistance. According to the datasheet of thyristor modules (PK110FG160), $r_t = \sim 0.44$ mΩ and $U_{TO} = 0.25$ V. Table VII shows the switching losses of APF, HAPF, and SVC-HAPF.

TABLE VII
SWITCHING LOSSES OF APF, HAPF, AND SVC-HAPF BY ANALYSIS

	DC-link voltage	Switching Loss (W) (1st loads)	Switching Loss (W) (1st and 2nd loads)
APF	340	138	162
HAPF	105	41	59
SVC-HAPF	60	37.5 ($30_{(IGBT)}$+$7.5_{(Thy)}$)	52.1($40_{(IGBT)}$+$12.1_{(Thy)}$)

TABLE VIII
INVERTER CAPACITY, LOSS, AND EFFICIENCY OF APF, HAPF, AND SVC-HAPF

		1st load (0.4 p.u)			1st and 2nd loads (0.495 p.u)		
		APF	HAPF	SVC-HAPF	APF	HAPF	SVC-HAPF
Measured inverter capacity (W)		1093	353	191	2092	644	389
Inverter/Sw loss (W)	Analysis results	138	41	30	162	59	40
	Measured results	100	53	31	179	61	41
Inverter efficiency (%)	Analysis results (Error in %)	87.4 (3.8%)	88.4 (4.0%)	84.3 (0.4%)	92.3 (0.9%)	90.8 (0.4%)	89.7 (0.4%)
	Measured results	90.8	85.0	84.0	91.5	90.5	89.4

The above switching loss analyses are based on experimental waveforms, equations, and calculations. To confirm the proposed loss analysis, direct loss/efficiency measurements are required by the FLUKE 435 POWER QUALITY ANALYZER measurement instrument, which has a "power inverter efficiency" function. The direct measurement results are provided in Figs. 17 and 18. Comparisons of the loss/efficiency analysis and the direct measurement results are provided in Table VIII.

In Table VIII, the analysis results of inverter/switching loss are derived from Table VII. The analysis results of efficiency are obtained from (32). The measured results of efficiency are obtained from Figs. 17 and 18, and the measured results of inverter/switching loss are calculated from (33) by using the efficiency from Figs. 17 and 18

$$E_{\text{ff\_inv}}(\%) = \left(\frac{S_{\text{comp\_inv}} - P_{\text{loss\_inv}}}{S_{\text{comp\_inv}}}\right) \cdot 100\% \tag{32}$$

$$P_{\text{loss\_inv}} = (1 - E_{\text{ff\_inv}}(\%)) \cdot S_{\text{comp\_inv}} \tag{33}$$

where $P_{\text{loss\_inv}}$ is the inverter power loss, $E_{\text{ff\_inv}}$ is the inverter efficiency, and $S_{\text{Comp\_inv}}$ is the inverter capacity, which can be obtained from Figs. 17 and 18 by multiplying the inverter voltage by the current. Table VIII shows that the analysis results and measured results are close to each other and that the error of efficiency is less than 5%.

2) Component Conduction Loss: According to the measurement results, the quality factor (Q) and equivalent series resistance (ESR) of APF, HAPF, and SVC-HAPF are given in Table V. The conduction loss is mainly caused by ESR in the inductor and capacitor.

TABLE IX
COMPONENT CONDUCTION LOSS OF APF, HAPF, AND SVC-HAPF

	Component conduction loss (W) (1st loads)	Component conduction loss (W) (1st and 2nd loads)
APF	1.2	1.6
HAPF	3.2	3.7
SVC-HAPF	5.7	7.7

TABLE X
IMPACT OF THE COUPLING TRANSFORMER ON THE LOSS/EFFICIENCY OF THE SVC-HAPF

	SVC-HAPF capacity	Transformer capacity (VA)	Transformer loss (W)	Total loss (W)	Efficiency (%)
1st load	759	191	3.8	48.0 (8.6%↑)	93.7 (0.5%↓)
1st and 2nd loads	1419	389	7.8	56.8 (13.7%↑)	96.0 (0.5%↓)

For APF and HAPF, the conduction loss of coupling inductor and/or coupling capacitor can be expressed as

$$P_{\text{loss}(L)} = 3 \cdot \text{ESR}_L \cdot I_{cx}^2 \tag{34}$$

$$P_{\text{loss}(C)} = 3 \cdot \text{ESR}_C \cdot I_{cx}^2 \tag{35}$$

where ESR_L and ESR_C are equivalent series resistances of coupling inductor L and coupling capacitor C of the APF and HAPF. I_{cx} is the RMS value of compensating current. For SVC-HAPF, the power loss of the L_c, L_{PF}, and CPF can be calculated as

$$P_{\text{loss}(L_c)} = 3 \cdot \text{ESR}_{L_c} \cdot I_{cx}^2 \tag{36}$$

$$P_{\text{loss}(C_{\text{PF}})} = 3 \cdot \text{ESR}_{C_{\text{PF}}} \cdot I_{C_{\text{PF}x}}^2 \tag{37}$$

$$P_{\text{loss}(L_{\text{PF}})} = 3 \cdot \text{ESR}_{L_{\text{PF}}} \cdot I_{L_{\text{PF}x}}^2 \tag{38}$$

where ESR_{Lc}, ESR_{CPF}, and ESR_{LPF} are the equivalent series resistance of L_c, C_{PF}, and L_{PF}. I_{cx}, $I_{C\text{PF}x}$, and $I_{L\text{PF}x}$ are the RMS values of the compensating current passing through C_{PF} and L_{PF}. Table IX shows the component conduction losses of APF, HAPF, and SVC-HAPF.

3) Coupling Transformer Loss: According to the datasheet of the coupling transformer, the efficiency of the transformer is ≥98%, and the capacity of the coupling transformer is small. Therefore, compared with the switching loss, the power loss of the coupling transformer constitutes a small proportion of the total power loss. Details of the impact of the coupling transformer on the loss/efficiency are provided in Table X.

In Table X, the coupling transformer is connected to the active inverter part, and the capacity of the coupling transformer can be calculated from Figs. 17 and 18. The transformer loss increases the total power loss by 8.6% for the first load compensation and 13.7% for the first and second loads compensation. The transformer loss is only reduced by about 0.5% for the SVC-HAPF efficiency for both cases.

4) Efficiency of APF, HAPF, and SVC-HAPF: The efficiency of the different compensators can be calculated as

$$E_{\text{ff}}(\%) = \frac{S_{\text{Comp}} - P_{\text{loss\_tot}}}{S_{\text{Comp}}} \times 100\% \tag{39}$$

TABLE XI
TOTAL POWER LOSSES AND EFFICIENCY OF APF, HAPF, AND SVC-HAPF

Compensator	1st loads		1st and 2nd loads	
	Total power loss (W)	Efficiency (%)	Total power loss (W)	Efficiency (%)
APF	101.2	86.7	180.3	87.3
HAPF	56.2	92.6	65.1	95.4
SVC-HAPF	48.0	93.7	56.8	96.0

where $P_{\text{loss\_tot}}$ is the total power loss, which can be derived from Table XI. S_{Comp} is the capacity flow in the compensator which can be expressed as

$$S_{\text{Comp}} = 3 \cdot V_x \cdot I_{cx} \tag{40}$$

where V_x is the load voltage and I_{cx} is the phase compensating current. The V_x is 110 V and I_{cx} can be derived from Table V.

Table XI shows that the proposed SVC-HAPF has the lowest total power loss and highest efficiency among the conventional APF, HAPF, and SVC-HAPF.

The experimental setup is scaled down from the simulation setup (voltage ratio 191 V:10 kV or 1:52). Unlike the experimental results, the simulation results are carried out under a relatively ideal situation, so the performance will be similar under different voltages (191 V or 10 kV). Therefore, the effects of the experimental setup scale down on the performance can be considered experimental factors that can affect performance.

Many factors can affect the performance of compensators in experiments. They can slightly affect the performances of the compensators, including but not limited to the ESRs in component parameters, the resolution of the transducers, the digital computation error, the response time of drivers for IGBTs and thyristors, and the noise in A/D signals and the controller.

However, the experimental results of the proposed SVC-HAPF can still obtain satisfactory PF and THD results according to the IEEE 519-2014 standard [33] when taking these factors into consideration.

VI. CONCLUSION

In this study, a minimizing inverter capacity design, characteristics, and performance analysis of the SVC-HAPF is proposed for medium-voltage level application. The conventional SVC-HAPFs, APF, HAPF, and the proposed SVC-HAPF are compared in terms of dc-link voltage and system performance through simulation and experimental results. The proposed SVC-HAPF requires a lower dc-link voltage than the conventional design of SVC-HAPFs and also of APF and HAPF. The proposed SVC-HAPF demonstrates better performance than APF and HAPF, and a wider compensation range than HAPF.

APPENDIX
SWITCHING MODELING (PWM TECHNIQUES) WITH TRADEOFF DISCUSSIONS

After obtaining the reference current i_{cx}^*, the PWM control is used to generate the switching signals for the active inverter part of APF, HAPF, and SVC-HAPF. The different PWM controls can generate 1) a regular switching frequency (e.g., proportional gain PWM control) or 2) an irregular frequency (e.g., hysteresis PWM control). The tradeoff between proportional gain PWM control with regular switching frequency [20], [34] and hysteresis PWM control with irregular switching frequency [21] are provided below.

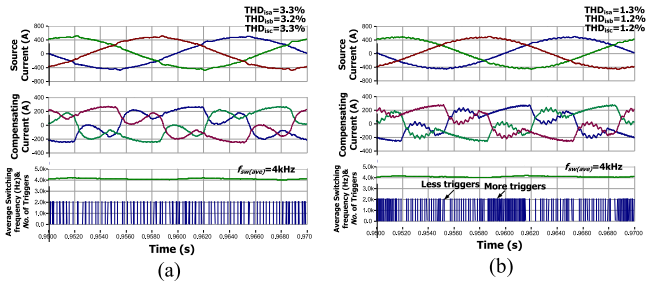

Fig. 19. Waveforms of source current, compensating current, average switching frequency, and number of triggers by using (a) proportional gain PWM control and (b) hysteresis PWM control.

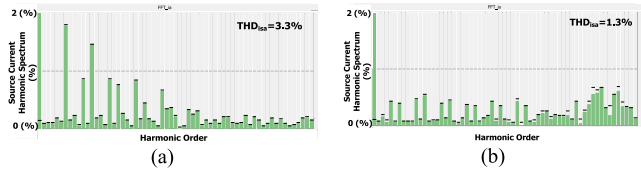

Fig. 20. Source current harmonic spectrum by using (a) proportional gain PWM control and (b) hysteresis PWM control.

The proportional gain control is an indirect current control (multiplying the reference current i_{cx}^* by a gain) to calculate the voltage reference. The voltage reference is then compared with a triangular waveform to produce PWM gate signals for the IGBTs. In contrast, the hysteresis band of the hysteresis PWM control defines the allowable current error to control the turning on or off of the IGBTs accordingly. The average switching frequency depends on the value of the hysteresis band. During the period when the compensating current stays within the hysteresis band, unnecessary switching can be avoided. The hysteresis current PWM can spread the energy concentrated around the harmonics of the switching frequency to a wider frequency range, to reduce the EMI peak value.

The simulation comparisons of proportional gain PWM control and hysteresis PWM control are provided in Figs. 19–21. Figs. 19 and 20 show a case study of the waveforms and source current harmonic (THD_{isx}) spectrum by using the above two PWM controls. Fig. 21 gives a more general THD_{isx} compensation comparison.

Figs. 19 and 20 show that proportional gain PWM control can compensate the worst phase source current THD_{isx} to 3.3%, while the hysteresis PWM control can compensate THD_{isx} to 1.3% performance under the same average switching frequency $f_{\text{sw(ave)}} = 4$ kHz.

Fig. 21 shows that the hysteresis PWM control method can obtain better THD_{isx} performance than the proportional gain control for loads with different THD_{iLx}.

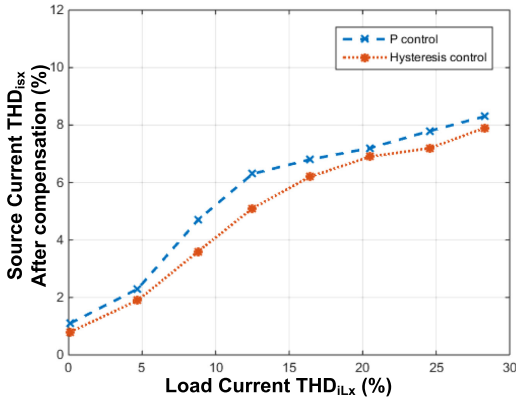

Fig. 21. Source current THD$_{isx}$ comparison between proportional gain PWM control and hysteresis PWM control for different load current THD$_{iLx}$ compensation.

The above analysis and Figs. 19–21 indicate that the hysteresis PWM control method (with irregular switching frequency) can obtain better performance than proportional gain control (with relative regular switching frequency) under the same average switching frequency. Therefore, the hysteresis PWM control is selected in this study.

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Lei Wang (M'18) received the B.Sc. degree in electrical and electronics engineering from the University of Macau (UM), Macao, China, in 2011, the M.Sc. degree in electronics engineering from Hong Kong University of Science and Technology, Hong Kong, in 2012, and the Ph.D. degree in electrical and computer engineering from UM in 2017.

He is currently a Postdoctoral Fellow with the Power Electronics Laboratory, UM. His research interests include power electronics, power quality and distribution flexible ac transmission system, power quality compensation, and renewable energy.

Dr. Wang received the champion award in the Schneider Electric Energy Efficiency Cup, Hong Kong, in 2011.

Chi-Seng Lam (S'04–M'12–SM'16) received the B.Sc., M.Sc., and Ph.D. degrees in electrical and electronics engineering from the University of Macau (UM), Macao, China, in 2003, 2006, and 2012, respectively.

From 2006 to 2009, he was an E&M Engineer with UM. In 2009, he simultaneously worked as a Laboratory Technician and started to work toward the Ph.D. degree, and completed his Ph.D. within three years. In 2013, he was a Postdoctoral Fellow with The Hong Kong Polytechnic University, Hong Kong. He is currently an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, UM. He has coauthored/coedited three books: *Design and Control of Hybrid Active Power Filters* (Springer, 2014), *Parallel Power Electronics Filters in Three-phase Four-wire Systems—Principle, Control and Design* (Springer, 2016), and *Tutorials in Circuits and Systems Selected Topics in Power, RF, and Mixed-Signal ICs* (River Publishers, 2017), two U.S. patent, two Chinese patents, and more than 70 technical journals and conference papers. His research interests include integrated power electronics controllers, power management integrated circuits, power quality compensators, smart grid technology, renewable energy, etc.

Dr. Lam received the IEEE PES Chapter Outstanding Engineer Award in 2016, and the Macao Science and Technology Invention Award (Third-Class) and the R&D Award for Postgraduates (Ph.D.) in 2014 and 2012, respectively. He also received the Macao Government Ph.D. Research Scholarship in 2009–2012, the Macao Foundation Postgraduate Research Scholarship in 2003–2005, and the third RIUPEEEC Merit Paper Award in 2005.

In 2007, 2008, and 2015, he was the GOLD Officer, Student Branch Officer, and Secretary of IEEE Macau Section. He is currently the Vice-Chair of IEEE Macau Section, the Chair of IEEE Macau CAS/COM Joint Chapter, and the Secretary of IEEE Macau PES/PELS Joint Chapter. He served as a member of Organizing Committee or Technical Program Committee of several international conferences.

Man-Chung Wong (SM'06) received the B.Sc. and M.Sc. degrees in electrical and electronics engineering from the University of Macau (UM), Macao, China, in 1993 and 1997, respectively, and the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, China, in 2003.

He was a Visiting Fellow at Cambridge University, U.K., in 2014. He is currently an Associate Professor with the Department of Electrical and Computer Engineering, UM. His research interests include power electronics converters, pulse with modulation, active power filters, hybrid active power filters, and hybrid power quality compensator for high-speed railway power supply system. He has coauthored two Springer books, more than 100 journal and conference papers, and eight patents (China and USA). Recently, an industrial power filter platform was developed and installed in a practical power system based on his research results.

Prof. Wong received the Macao Young Scientific Award from Macau International Research Institute in 2000, the Young Scholar Award of UM in 2001, the second prize for Tsinghua University Excellent Ph.D. Thesis Award in 2003, and the Macao Science and Technology Invention Award (Third-Class) in 2012 and 2014, respectively. He supervised several students to receive merit paper awards in conferences and champions in student project competitions. He was several conference committee members and the General Chair of IEEE TENCON 2015 Macau. He is with IEEE Macau Section and IEEE Macau Power Joint Chapter for many years. In 2014–2015, he was the Chair of IEEE Macau Section. Currently, he is the North Representative of IEEE Region 10 Power and Energy Society and the Chair of IEEE Macau PES/PELS Joint Chapter.