Gate Control Optimization of Si/SiC Hybrid Switch for Junction Temperature Balance and Power Loss Reduction

Jun Wang, *Senior Member, IEEE*, Zongjian Li, *Student Member, IEEE*, Xi Jiang, Cheng Zeng, and Z. John Shen, *Fellow, IEEE*

***Abstract*—The hybrid switch concept of paralleling a higher-current main Si IGBT and a lower-current auxiliary SiC MOSFET offers an improved cost/performance tradeoff in power converters. Currently, the gate control strategy of these two internal devices emphasizes on minimizing the total power loss, and is referred to as the efficiency control mode in this paper. However, there is a serious risk of overheating and reliability degradation of the SiC MOSFET if solely relying on this control strategy. In this paper, we propose a new method of gate control optimization, referred to as the thermal balance control mode, to keep the junction temperature of both devices within the specified temperature range, and to minimize the total power loss simultaneously. We first investigate the dependency of the hybrid switch switching losses on the gate control pattern both theoretically and experimentally. We then extensively study control optimization in these two distinct control modes in a dc–dc boost converter. It is found that the thermal balance control mode can achieve almost the same total power loss as the efficiency control mode, but much lower and more balanced junction temperatures of the two internal devices. Experimental results demonstrate that the Si/SiC hybrid switch in an optimal thermal balance control mode can achieve a 163% higher power handling capability in the 20-kHz boost converter or four times higher switching frequency in the 4-kW boost converter than a single IGBT solution with hard switching condition, and yet a considerably lower component cost than a single SiC MOSFET solution in the boost converter.**

***Index Terms*—Gate control, hybrid switch, IGBT, junction temperature, MOSFET , power loss, SiC.**

I. Introduction

POWER MOSFETs have advantage of fast switching speed, while high-voltage bipolar devices have advantage of low forward voltage drop, especially at high current density due to the strong conductivity modulation. In order to combine the advantages of power MOSFET and bipolar devices, the hybrid MOS-Bipolar concept was proposed and led to the invention of

Manuscript received December 3, 2017; revised February 9, 2018; accepted April 8, 2018. Date of publication April 23, 2018; date of current version December 7, 2018. This work was supported by Chinese National Natural Science Foundation (Project No. 51577054). Recommended for publication by Associate Editor J. Wang. *(Corresponding authors: Zongjian Li and Jun Wang.)*

The authors are with the College of Electrical and Information Engineering, Hunan University, Changsha 410082, China (e-mail:

inside the hybrid switch and reduce the IGBT's switching losses in most of these studies [11]–[21].

Under the inductive load switching condition, the auxiliary SiC MOSFET turns ON shortly before and turns OFF shortly after the main IGBT, conducting 100% of the load current during these short time delays [17], [18], [20]. Even with its inherently high switching speed, the auxiliary SiC MOSFET incurs a large switching loss under the high current and high voltage hard switching transient, resulting in a junction temperature considerably higher than that of the main IGBT due to its small chip size and high thermal resistance. Both high junction temperature and extreme temperature cycling will accelerate aging and/or induce failure of SiC MOSFETs [23]–[26]. One particular concern is the gate oxide reliability of the SiC MOSFETs at high temperatures due to the trapping and detrapping of high-density interface defects at the SiC/SiO_2 interface [27], [28]. Therefore, there is a serious risk of overheating and reliability degradation of the SiC MOSFET inside the cost-effective Si/SiC hybrid switch. However, most studies of the Si/SiC hybrid switch mainly focused on optimal gate control strategy to minimize the total power loss of the hybrid switch in a double pulse test circuit (referred to as the efficiency control mode in this paper), largely neglecting the thermal imbalance challenge in actual power converters.

The purpose of this paper is to investigate a new gate control optimization method, referred to as the thermal balance control mode, to keep the junction temperature of both the SiC MOSFET and Si IGBT within their specified temperature ranges, and to minimize the total power loss simultaneously. It helps prevent these two devices from operating with an excessive junction temperature, and improve the maximum power handling capability of the hybrid switch. The operation principal and characteristics of the hybrid switch is briefly explained in Section II. In Section III, both the conventional efficiency control mode and the proposed thermal balance control mode of the hybrid switch in a dc–dc boost converter are extensively investigated both theoretically and experimentally. The electrical and thermal performance of the hybrid switch in a dc–dc boost converter with the optimum thermal balance control mode is demonstrated in Section IV. Section V concludes the paper.

II. Operation Principle and Characteristics of Si/SiC Hybrid Switch

A. Forward Conduction Characteristics

The schematic of a hybrid switch consisting of a high-current Si IGBT as the main switch and a low-current SiC MOSFET as the auxiliary switch is shown in Fig. 1. The hybrid switch combines the advantages of Si IGBT and SiC MOSFET because most of the load current flows through the SiC MOSFET at a low current level and the Si IGBT at a high current level, thus offering a lower conduction loss.

Since the conduction and switching losses of the SiC MOSFET are relatively small under the nominal operation conditions, the implementation of a low power SiC MOSFET into the hybrid switch becomes possible, which makes it much cheaper than the single SiC MOSFET solutions. A 1200–V 40–A Si IGBT (IGW40T120) and a 1200–V 12.5–A SiC MOSFET

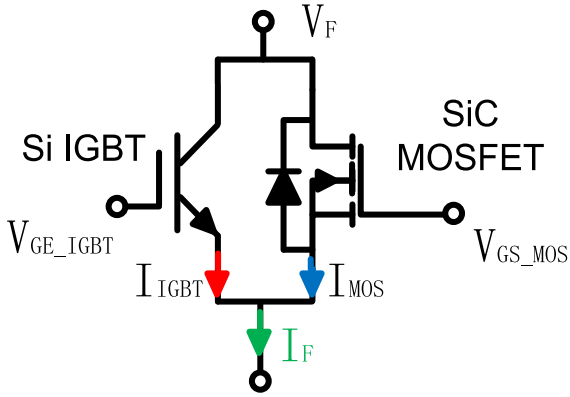


Fig. 1. Schematic of hybrid switch.

(C2M0160120D) [29] are parallel connected to constitute the hybrid device. Because the power losses and the junction temperatures of the IGBT and the SiC MOSFET may be different in various load conditions, the optimization of device design is complicated and not fully considered in this study. The manufacture cost per Ampere of the SiC MOSFET is approximately five times as much as that of the IGBT [22], so the manufacture cost of the hybrid switch is approximately 256% of a 40-A Si IGBT or 51% of a 40-A SiC MOSFET (C2M0040120D).

When the hybrid switch is in the steady-state condition, the current may flow through the auxiliary SiC MOSFET and/or the IGBT. The current ratio between the main IGBT and the auxiliary SiC MOSFET inside the hybrid switch is defined as

$$\gamma = \frac{I_{\mathrm{IGBT}}}{I_{\mathrm{MOS}}}. \tag{1}$$

Fig. 2 shows the forward *I–V* characteristics of the hybrid switch and the current ratio between its internal IGBT and SiC MOSFET at room temperature and 150 °C. The output characteristics of the hybrid switch show a positive temperature coefficient due to the positive temperature coefficients of the IGBT at a high current level and the SiC MOSFET at all current levels. When the forward conduction current of the hybrid switch is below 5 A, its forward voltage drop is below the turn-ON knee voltage of the IGBT, and 100% of the forward conduction current flows through the auxiliary SiC MOSFET. When the hybrid switch operates at 16 A, the forward conduction current is evenly distributed between the auxiliary SiC MOSFET and the main IGBT, resulting in their equal conduction losses. When the forward conduction current of the hybrid switch is larger than 16 A, the current flowing through the main IGBT is larger than that of the auxiliary SiC MOSFET. When the hybrid switch operates at 40 A and 150 °C, the SiC MOSFET conducts 11 A and the IGBT conducts 29 A. When the operating temperature of the hybrid switch increases, the current ratio between its internal IGBT and SiC MOSFET slightly increases. The reason is because the SiC MOSFET has a larger positive temperature coefficient than the IGBT.

B. Switching Characteristics

The unipolar SiC MOSFET has much lower switching losses than the bipolar Si IGBT. And the turn-OFF switching loss caused

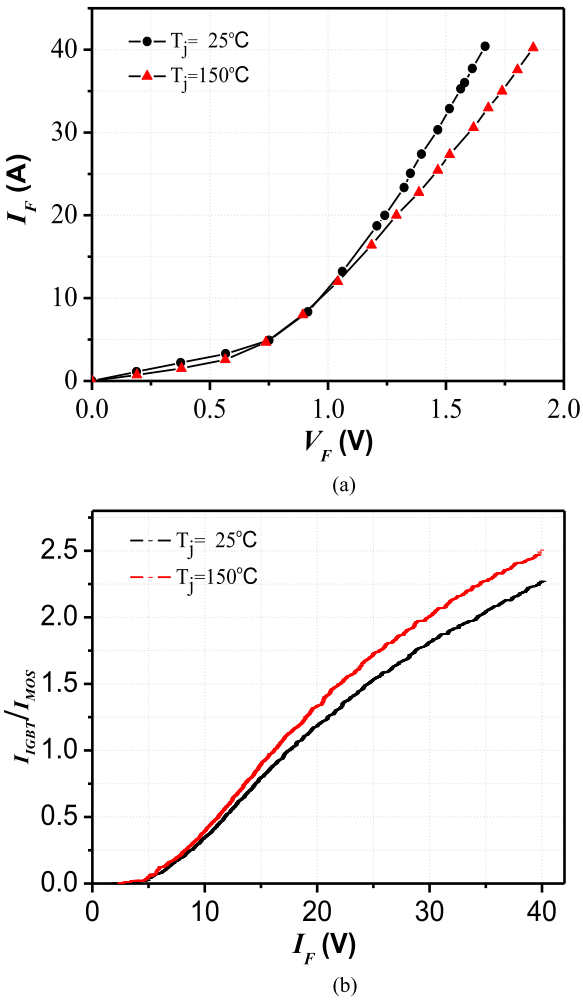


Fig. 2. Forward *I–V* curve and current distribution of hybrid switch. (a) Forward *I–V* curve. (b) Current distribution of hybrid switch's two internal devices.

by the IGBT's tail current is huge, which can be significantly reduced with the appropriate gate control pattern of the hybrid switch. As shown in Fig. 3, there are four gate control patterns for the hybrid switches. In the gate control pattern I, the auxiliary SiC MOSFET turns ON shortly before and turns OFF shortly after the main IGBT. During the switching transient, the auxiliary SiC MOSFET undertakes the hard switching actions and conducts 100% of the load current for a short commuting time, and the IGBT undertakes ZVS switching actions. In the gate control pattern II, both the turning ON and turning OFF of the SiC MOSFET are prior to those of the IGBT. The IGBT is ZVS turned ON, and the SiC MOSFET is ZVS turned OFF. In the gate control pattern III, both the turning ON and turning OFF of the IGBT are prior to those of the SiC MOSFET. The SiC MOSFET is ZVS turned ON and IGBT is ZVS turned OFF. In the gate control pattern IV, the main IGBT turns ON shortly before and turns OFF shortly after the auxiliary SiC MOSFET. The SiC MOSFET undertakes the ZVS switching actions.

The turn-ON and turn-OFF gate signals' delay time between the IGBT and the SiC MOSFET inside the hybrid switch are defined as $T_{\text{on\_delay}}$ and $T_{\text{off\_delay}}$, respectively. The switching losses of the IGBT and the auxiliary SiC MOSFET are mainly influenced by the polarity and magnitude of their turn-ON and turn-OFF gate

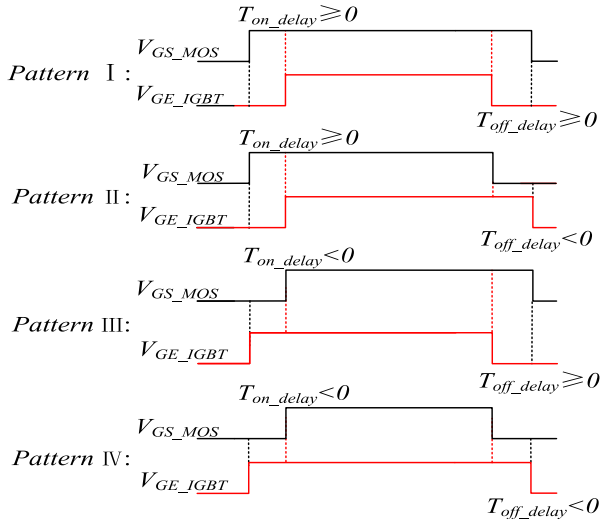


Fig. 3. Gate control patterns of hybrid switch.

signals' delay time. In order to investigate their correlation, a double pulse clamped inductive load circuit is built and tested. A 1200-V/14-A SiC JBS diode (C4D10120A) and an inductor of 150 μH are used.

The turn-ON process of the hybrid switch with $T_{\text{on_delay}} = 0.2\,\mu$s and $T_{\text{on_delay}} = -0.2\,\mu$s turn-ON gate signals' delay time under a load current of 40 A and a dc-link voltage of 600 V at room temperature is illustrated in Fig. 4. It shows the hybrid switch's drain voltage waveforms, its two internal devices' current waveforms, and the IGBT's gate voltage. The total turn-ON switching loss of the hybrid switch is expressed as

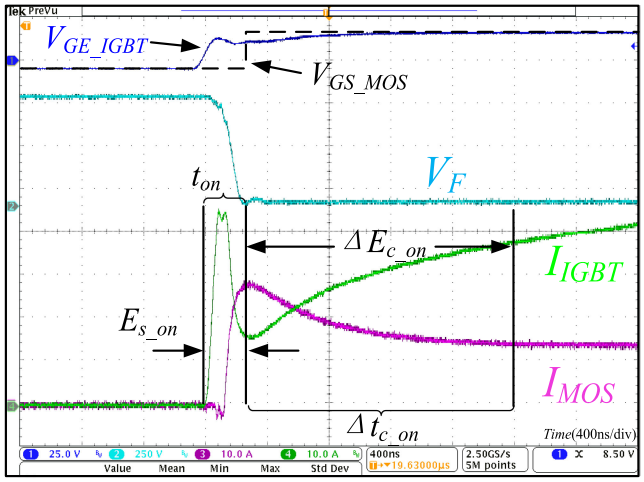
$$E_{\text{on}}(T_{\text{on\_delay}}) = E_{s\_\text{on}}(T_{\text{on\_delay}}) + \Delta E_{c\_\text{on}}(T_{\text{on\_delay}}) \quad (2)$$

where E_{s_on} is the total switching on loss of the IGBT and the SiC MOSFET, ΔE_{c_on} is the additional conduction loss of the SiC MOSFET when the forward conduction current commutates from the auxiliary SiC MOSFET to the IGBT during a commuting time of Δt_{c_on}. The Δt_{c_on} is defined as the time interval that begins when the forward voltage drop is 10% of the dc voltage and ends when the SiC MOSFET's forward conduction current reaches the steady-state value. The ΔE_{c_on} can be expressed as

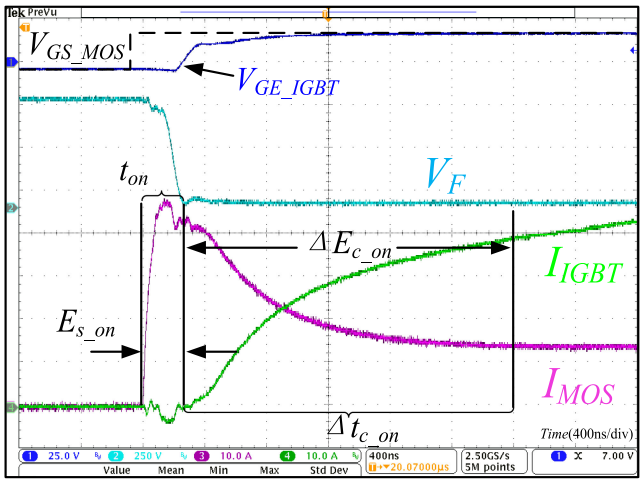
$$\triangle E_{c\_\text{on}} = \begin{cases} \int_{-t_{\text{on\_IGBT}}}^{\Delta t_{c\_\text{on}}} \left(i_{\text{MOS}} - \frac{i_F}{1+\gamma}\right) \cdot V_F\, dt, & T_{\text{on\_delay}} < -t_{\text{on\_IGBT}} \\ \int_{T_{\text{on\_delay}}}^{\Delta t_{c\_\text{on}}} \left(i_{\text{MOS}} - \frac{i_F}{1+\gamma}\right) \cdot V_F\, dt, & T_{\text{on\_delay}} \in [-t_{\text{on\_IGBT}}, t_{\text{on\_MOS}}] \\ \int_{t_{\text{on\_MOS}}}^{\Delta t_{c\_\text{on}}} \left(i_{\text{MOS}} - \frac{i_F}{1+\gamma}\right) \cdot V_F\, dt, & T_{\text{on\_delay}} > t_{\text{on\_MOS}} \end{cases} \quad (3)$$

where the $t_{\text{on\_IGBT}}$ and $t_{\text{on\_MOS}}$ are the turn-ON times of the IGBT and SiC MOSFET, respectively. V_F is the forward voltage drop of the hybrid switch, and i_{MOS} is the current flowing through the SiC MOSFET. The i_F is the total forward conduction current of the auxiliary SiC MOSFET and IGBT in the hybrid switch.

When the IGBT is turned ON, its forward voltage drop during the turn-ON transient is substantially larger than its forward



(a)



(b)

Fig. 4. Turn-ON process of hybrid switch. (a) $T_{\text{on_delay}} = -0.2\,\mu$s. (b) $T_{\text{on_delay}} = 0.2\,\mu$s.

voltage drop under steady-state condition because of the time taken to modulate the conductivity of its N-drift region. During the commuting time, most of the forward conduction current flows through the auxiliary SiC MOSFET because of its low on-state resistance, inducing the additional conduction loss of the hybrid switch.

Fig. 5 shows the measured additional conduction loss and the commutating time of the hybrid switch at various turn-ON gate signals' delay time between the IGBT and the SiC MOSFET in a double pulse clamped inductive load circuit with a dc-link voltage of 600 V and a load current of 40 A at room temperature. When the turn-ON gate signal's delay time is smaller than $-0.35\,\mu$s for the selected hybrid switch, the additional conduction loss and the commutating time are zero because the IGBT is fully turned ON before the turning ON of the SiC MOSFET. When the turn-ON gate signal's delay time increases, the additional conduction loss and the commutating time increase because the auxiliary SiC MOSFET entails more conduction loss.

When the absolute magnitude of the turn-ON gate signal's delay time is very large, the switch-on loss of the hybrid switch

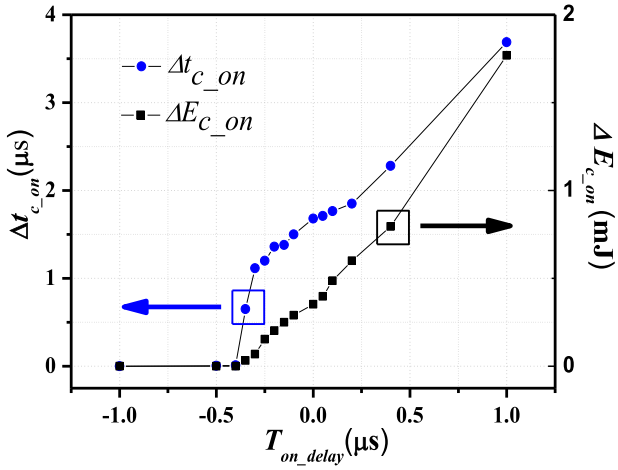


Fig. 5. Dependency of the hybrid switch's additional conduction loss and commutation time on its gate signal's turn-ON delay time.

is approximately equal to that of the IGBT or the SiC MOSFET because one of these two devices undertakes the ZVS turning ON actions. When the absolute magnitude of the turn-ON gate signal's delay time is small, the turn-ON switching loss distribution between the IGBT and the SiC MOSFET varies with the turn-ON gate signal's delay time because their transient load current varies. Therefore, the switch-on losses of IGBT and SiC MOSFET are approximately expressed as

$$E_{s\_on}(T_{\text{on\_delay}}) = \begin{cases} E_{s\_on\_IGBT}, & T_{\text{on\_delay}} < -t_{\text{on\_IGBT}} \\ \int_{-t_{\text{on\_IGBT}}}^{T_{\text{on\_delay}}} (i_{\text{IGBT}} + i_{\text{MOS}}) \cdot V_F\, dt, & T_{\text{on\_delay}} \in [-t_{\text{on\_IGBT}}, t_{\text{on\_MOS}}] \\ E_{s\_on\_MOS}, & T_{\text{on\_delay}} > t_{\text{on\_MOS}} \end{cases} \tag{4}$$

$$E_{s\_on\_MOS} = \int_{t_{\text{on\_MOS}}}^{T_{\text{on\_delay}}} i_{\text{MOS}} \cdot V_F\, dt, \quad T_{\text{on\_delay}} > t_{\text{on\_MOS}} \tag{5}$$

$$E_{s\_on\_IGBT} = \int_{-T_{\text{on\_delay}}}^{-t_{\text{on\_IGBT}}} i_{\text{IGBT}} \cdot V_F\, dt, \quad T_{\text{on\_delay}} < -t_{\text{on\_IGBT}} \tag{6}$$

where the i_{MOS} and i_{IGBT} are the current flowing through the SiC MOSFET and the IGBT, respectively. The $E_{s\_on\_IGBT}$ and $E_{s\_on\_MOS}$ are the switch-on losses of the IGBT and the SiC MOSFET, respectively.

Fig. 6 shows the measured switch-on losses of the IGBT, SiC MOSFET, and the hybrid switch at various turn-ON gate signals' delay time between the IGBT and the SiC MOSFET in a double pulse clamped inductive load circuit with a dc-link voltage of 600 V and a load current of 40 A at room temperature.

When the absolute magnitude of the turn-ON gate signal's delay time is small, the current rise (di/dt) of the IGBT and the SiC MOSFET has overlap, leading to a higher *di/dt* of the hybrid switch than other two cases. Therefore, the E_{s_on} of the

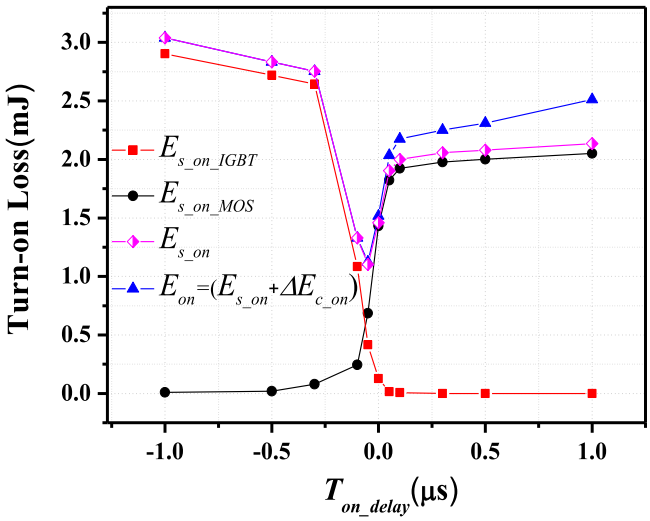


Fig. 6. Dependency of the hybrid switch's turn-ON switching loss on its gate signal's turn-ON delay time.

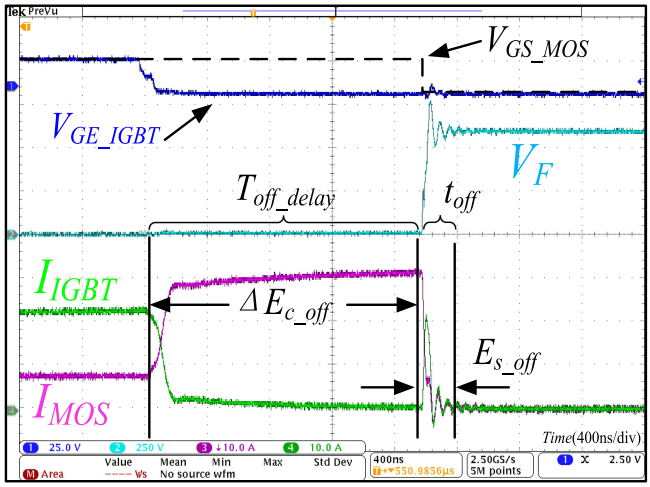


Fig. 7. Turn-OFF process of hybrid switch with $T_{\text{off_delay}} = 1.8\,\mu$s.

hybrid switch at a small absolute magnitude of the turn-ON gate signal's delay time is smaller than that at a large absolute magnitude of the turn-ON gate signal's delay time. Because the IGBT's turn-ON speed is lower than that of SiC MOSFET, a small negative turn-ON gate signal's delay time can achieve a large *di/dt* of the hybrid switch, leading to a local minimal value. The minimum switch-on loss and the total turn-ON switching loss of the hybrid switch occur at the turn-ON gate signal's delay time of approximately $-0.03\,\mu$s.

During the turn-OFF process of the hybrid switch, the IGBT's tail current can cause a large turn-OFF switching loss under a hard switching condition. The gate control pattern I and pattern III of the hybrid switch can enable the IGBT's ZVS turning OFF, so a positive turn-OFF gate signal's delay time is preferred to greatly reduce the turn-OFF switching loss of the hybrid switch. Fig. 7 shows measured turn-OFF waveforms of the hybrid switch at a positive turn-OFF gate signal's delay time $T_{\text{off_delay}} = 1.8\,\mu$s in a double pulse clamped inductive load circuit with a dc-link voltage of 600 V and a load current of 40 A at room temperature.

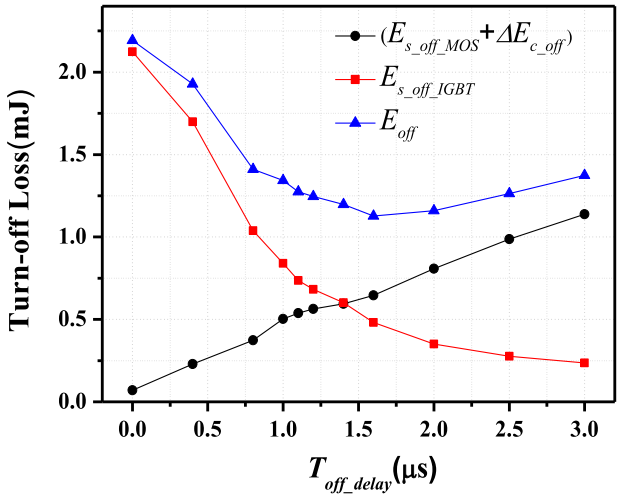


Fig. 8. Dependency of the hybrid switch's turn-OFF energy loss on its gate signal's turn-OFF delay time.

When the IGBT undertakes the ZVS turning-off action, the current initially flowing through the IGBT commutes to the auxiliary SiC MOSFET during the short gate turn-OFF delay time, inducing the additional conduction loss of the auxiliary SiC MOSFET.

The total turn-OFF switching loss of the hybrid switch consists of the turn-OFF switching loss of IGBT and SiC MOSFET, and the additional conduction loss of the SiC MOSFET. The dependency of its total turn-OFF switching loss on the turn-OFF gate signal's delay time between the IGBT and the SiC MOSFET is expressed as

$$\begin{aligned} E_{\text{off}}(T_{\text{off\_delay}}) &= \Delta E_{c\_\text{off}}(T_{\text{off\_delay}}) + E_{s\_\text{off}}(T_{\text{off\_delay}}) \\ &= \int_0^{T_{\text{off\_delay}}} i_{\text{IGBT}} \cdot V_F\, dt \\ &\quad + \int_{T_{\text{off\_delay}}}^{T_{\text{off\_delay}}+t_{\text{off\_MOS}}} (i_{\text{IGBT}} + i_{\text{MOS}}) \cdot V_F\, dt \end{aligned} \tag{7}$$

where E_{s_off} is the total turn-OFF switching loss of IGBT and SiC MOSFET, ΔE_{c_off} is the additional conduction loss of the SiC MOSFET, and $t_{\text{off\_MOS}}$ is the turn-OFF time of the SiC MOSFET.

Fig. 8 shows the measured turn-OFF energy loss of the hybrid switch at various turn-OFF gate signals' delay time between the IGBT and the SiC MOSFET in a double pulse clamped inductive load circuit with a dc-link voltage of 600 V and a load current of 40 A at room temperature. When the turn-OFF gate signal's delay time between the IGBT and the SiC MOSFET is too small, the total turn-OFF switching loss of the hybrid switch is mainly determined by that of IGBT. When the turn-OFF gate signal's delay time is too large, the total turn-OFF switching loss of the hybrid switch is mainly determined by that of the SiC MOSFET due to its large additional conduction loss. The minimum total turn-OFF switching loss of the hybrid switch occurs at a turn-OFF gate signal's delay time of approximately $1.6\,\mu$s.

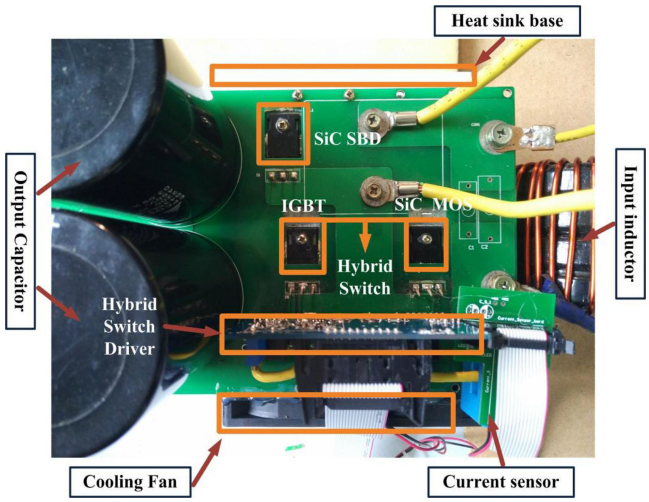


Fig. 9. Prototype of the hybrid switch boost converter.

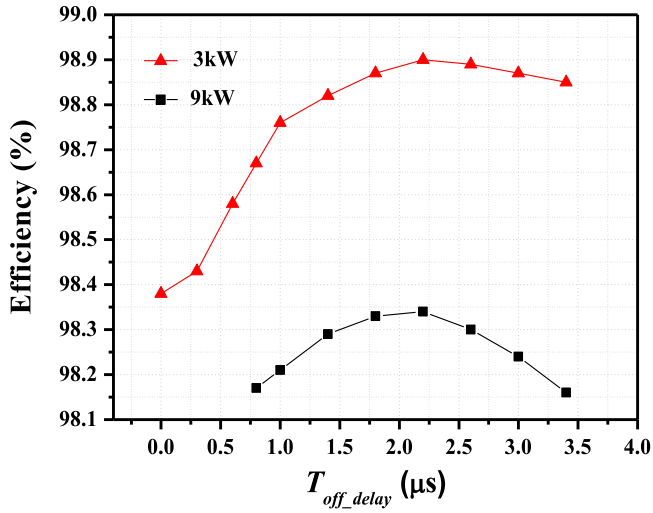


Fig. 10. Dependency of boost converter's efficiency on the turn-OFF gate signal's delay time of hybrid switch.

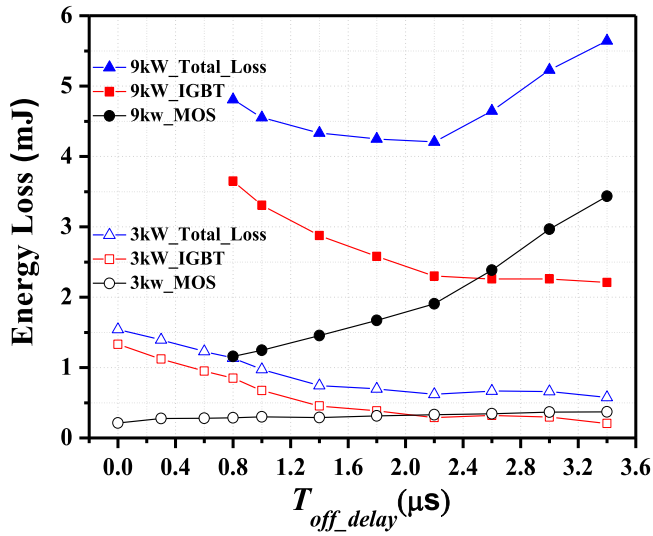


Fig. 11. Dependency of the hybrid switch's switching losses on the turn-OFF gate signal's delay time of hybrid switch.

III. Optimal Gate Control Strategies

A hybrid switch based dc–dc Boost converter prototype is built and tested in order to investigate the impact of the gate control strategies on the converter's conversion efficiency and its thermal characteristics, as shown in Fig. 9. The SiC MOSFET C2M0160120D and Si IGBT IGW40T120 are selected to constitute the hybrid device. It is assembled on a heat sink, and a designed integrated gate driver is used to achieve the special control patterns of the hybrid switch. The switching frequency of the dc–dc boost converter is 20 kHz. Its input and output voltages are chosen as 300 and 600 V, respectively. A 1-mH boost inductor is selected to meet the 30% current ripple specification of the converter. A 2200-μF output filter capacitor is selected to achieve the output voltage ripple of smaller than 2%.

A. *Efficiency Control Mode of Hybrid Switch*

Because the power losses of the IGBT and the auxiliary SiC MOSFET inside the hybrid switch are strongly influenced by the gate signal's delay time of the hybrid switch, the conversion efficiency of the boost converter is expressed as

$$\eta(T_{\text{on\_delay}}, T_{\text{off\_delay}}) = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss\_switch}}(T_{\text{on\_delay}}, T_{\text{off\_delay}}) + P_{\text{loss\_others}}} \tag{8}$$

where

$$P_{\text{loss\_switch}}(T_{\text{on\_delay}}, T_{\text{off\_delay}}) = P_{\text{loss\_MOS}}(T_{\text{on\_delay}}, T_{\text{off\_delay}}) + P_{\text{loss\_IGBT}}(T_{\text{on\_delay}}, T_{\text{off\_delay}}). \tag{9}$$

The P_{out} is the output power of the converter. $P_{\text{loss\_MOS}}$ and $P_{\text{loss\_IGBT}}$ are the power losses of the auxiliary SiC MOSFET and the IGBT, respectively. $P_{\text{loss\_others}}$ is the power loss of other components, such as the gate driver, inductor, and freewheeling diode.

The maximum efficiency of the hybrid switch based dc–dc boost converter can be achieved as shown in (8) by minimizing the total power loss of the hybrid switch. The minimum switching losses of the hybrid switch can be achieved with appropriate gate signal's delay time of the hybrid switch as shown in Figs. 6 and 8. Therefore, the maximum efficiency of the dc–dc boost converter is an indicator of optimal efficiency control of the hybrid switch.

Figs. 10 and 11 show the dependency of the measured efficiency of the dc–dc boost converter and the hybrid switch's switching loss on the turn-OFF gate signal's delay time between the IGBT and the SiC MOSFET at a zero turn-ON gate signal's delay time and various load conditions. The conversion efficiency of the boost converter in the steady state is measured by the power analyzer HIOKI PW3390. The energy loss of the hybrid switch is calculated by the integral of the measured voltage and current waveforms over the period of a duty cycle in the steady

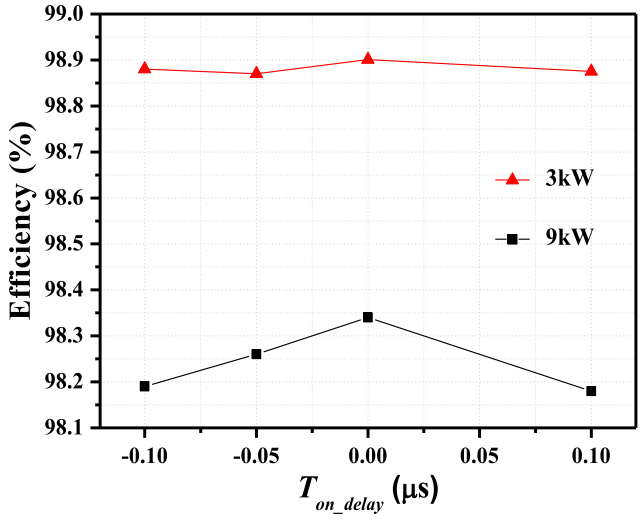


Fig. 12. Dependency of boost converter's efficiency on the gate signal's turn-ON delay time of hybrid switch.

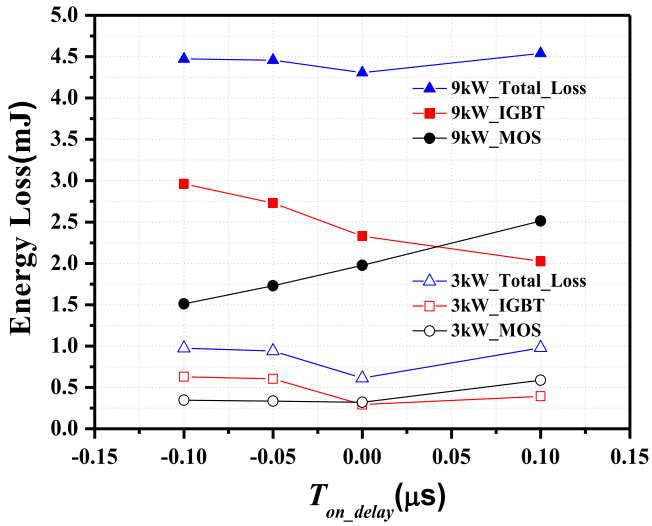


Fig. 13. Dependency of the hybrid switch's power losses on its gate signal's turn-ON delay time in the boost converter.

state. When the turn-OFF gate signal's delay time is very short, the efficiency of the dc–dc boost converter is low because of the large switching loss of the IGBT. When the turn-OFF gate signal's delay time is very long, the efficiency of the dc–dc boost converter is low because of the large additional conduction loss of the auxiliary SiC MOSFET. The turn-OFF switching loss of the IGBT is decreased and the turn-OFF switching loss of the auxiliary SiC MOSFET is increased with the increasing turn-OFF gate signal's delay time as shown in Fig. 8. A minimum total switching loss of the hybrid switch and a maximum efficiency of the dc–dc boost converter are achieved at a turn-OFF gate signal's delay time of approximately 2.2 μs, which is larger than the needed $T_{\text{off\_delay}}$ at its minimum total turn-OFF loss E_{off} as shown in Fig. 8. It is mainly induced by the difference of the junction temperature of the hybrid switch in the double pulse test circuit and the dc–dc boost converter, and the temperature dependent losses of the hybrid switch. As shown in Fig. 8, the optimum $T_{\text{off_delay}} = 1.6\,\mu$s and its minimum total turn-OFF loss E_{off} in the double pulse test circuit is achieved at room temperature. The junction temperature of the hybrid switch with optimum $T_{\text{off_delay}} = 1.6\,\mu$s and minimum energy loss in the steady state of the dc–dc boost converter is higher than 90 °C, as shown in Figs. 11 and 15. The conduction loss and the switching loss of the IGBT increase with the increasing temperature. Though the conduction loss of the SiC MOSFET increases with the increasing temperature, the SiC MOSFET's switching loss almost keeps constant in elevated temperatures. Therefore, the dependency of the hybrid switch's loss on its gate signal's switching delay time varies with its junction temperature, and the needed gate signal's turn-OFF delay time in its minimum energy loss in elevated temperatures is larger than that at room temperature.

Figs. 12 and 13 show the dependency of the measured efficiency of the dc–dc boost converter and the hybrid switch's switching loss on the turn-ON gate signal's delay time between the IGBT and the SiC MOSFET at a turn-OFF gate signal's delay time of 2.2 μs and various load conditions. When the turn-ON gate signal's delay time decreases from 0 to $-0.1\,\mu$s, the efficiency of the dc–dc boost converter slightly decreases because of the increase of the IGBT's turn-ON switching loss. When the turn-ON gate signal's delay time increases from 0 to 0.1 μs, the efficiency of the dc–dc boost converter slightly decreases because of the increase of the turn-ON loss of the SiC MOSFET. A maximum efficiency of the dc–dc boost converter is achieved at an approximately zero turn-ON gate signal's delay time. The turn-ON switching losses of the IGBT and the auxiliary SiC MOSFET in the hybrid switch dramatically increase with the increasing output power, so the impact of the turn-ON gate signal's delay time of the hybrid switch on the conversion efficiency of the boost converter at a high power rating is much stronger than that at a low power rating.

B. Thermal Balance Control Mode of Hybrid Switch

In order to analyze the thermal characteristics of the hybrid switch in the dc–dc boost converter, the relationship of its average junction temperature in the steady state and its power loss is expressed as

$$T_j = T_c + R_{\theta jc} \cdot P_{\text{loss}} \tag{10}$$

where the $R_{\theta jc}, P_{\text{loss}}, T_j$, and T_c are the thermal resistance at a fixed duty cycle, total power loss, junction temperature, and case temperature of the IGBT or the auxiliary SiC MOSFET inside the hybrid switch, respectively.

Because the switching losses of the main IGBT and the auxiliary SiC MOSFET are mainly influenced by the polarity and magnitude of their turn-ON and turn-OFF gate signals' delay time, their junction temperature can be controlled by adjusting the turn-ON and turn-OFF gate signals' delay time. The balanced junction temperature control of the main IGBT and the auxiliary SiC MOSFET inside the hybrid switch is proposed in order to prevent one of them from overheating and keep the junction temperature of both devices within the specified temperature range. The equation of the balanced junction temperature control of

the hybrid switch is expressed as

$$T_{j\_\mathrm{IGBT}} = T_{j\_\mathrm{MOS}} \tag{11}$$

where T_{j_MOS} and T_{j_IGBT} are the junction temperature of the auxiliary SiC MOSFET and the IGBT, respectively.

Substituting (10) into (11) yields

$$\frac{P_{\mathrm{loss\_IGBT}}}{P_{\mathrm{loss\_MOS}}} = \lambda_R + \frac{\Delta T_c}{R_{\theta jc\_\mathrm{IGBT}} \cdot P_{\mathrm{loss\_MOS}}}. \tag{12}$$

And the total power loss of the hybrid switch in the balanced junction temperature control mode can be expressed as

$$P_{\mathrm{loss\_switch}} = (1+\lambda_R)P_{\mathrm{loss\_MOS}} + \frac{\Delta T_c}{R_{\theta jc\_\mathrm{IGBT}}} \tag{13}$$

where

$$\Delta T_c = T_{c\_\mathrm{MOS}} - T_{c\_\mathrm{IGBT}} \tag{14}$$

$$\lambda_R = \frac{R_{\theta jc\_\mathrm{MOS}}}{R_{\theta jc\_\mathrm{IGBT}}}. \tag{15}$$

The T_{c_MOS} and T_{c_IGBT} are the case temperature of the auxiliary SiC MOSFET and the IGBT, respectively. ΔT_c is the case temperature deviation between the auxiliary SiC MOSFET and the IGBT. $R_{\theta jc\_\mathrm{MOS}}$ and $R_{\theta jc\_\mathrm{IGBT}}$ are the junction to case thermal resistance of the auxiliary SiC MOSFET and the IGBT, respectively. λ_R is the ratio of the auxiliary SiC MOSFET's and the IGBT's junction to case thermal resistances. The ratio of the auxiliary SiC MOSFET's and the IGBT's junction to case thermal resistances is selected to be 2 due to the difference of their chip areas and packaging techniques in the experiment.

Equations (12) and (13) mean that the balanced junction temperature of both devices inside the hybrid switch can be achieved when their power losses have an optimum ratio. The ratio is correlated with their case temperature deviation and the junction-to-case thermal resistances.

Under an ideal cooling condition or in the case of a hybrid switch power module with the SiC MOSFET die and the IGBT die on the same DBC substrate, the case temperature of the IGBT is assumed to be equal to that of the auxiliary SiC MOSFET. Equation (11) is simplified as

$$\frac{P_{\mathrm{loss\_IGBT}}}{P_{\mathrm{loss\_MOS}}} = \frac{R_{\theta jc\_\mathrm{MOS}}}{R_{\theta jc\_\mathrm{IGBT}}}. \tag{16}$$

Equation (16) means that both the junction temperature and the case temperature of two devices inside the hybrid switch can be balanced if the ratio of the IGBT's and the auxiliary SiC MOSFET's power losses is inversely proportional to the ratio of their junction to case thermal resistances.

The case temperatures of the auxiliary SiC MOSFET, the main IGBT, and the SiC Schottky diode are measured using an infrared imager of FLIR A655sc as shown in Fig. 14. Their junction temperatures are calculated using (10). The 1200-V/33-A SiC Schottky diode (C4D20120D) is selected as the freewheeling diode in this paper. Its maximum operating junction temperature (175 °C) is higher than the maximum operating junction temperature of the IGBT and the SiC MOSFET (150 °C), and its thermal resistance is smaller. Although its measured case temperature is higher than those of the IGBT and the SiC MOSFET at 9 kW power rating, its estimated junction temperature is 132 °C, which is still below the its junction temperature limit and slightly higher than the junction temperature of the IGBT and the SiC MOSFET.

Fig. 14. Infrared images of the hybrid switch at 9 kW.

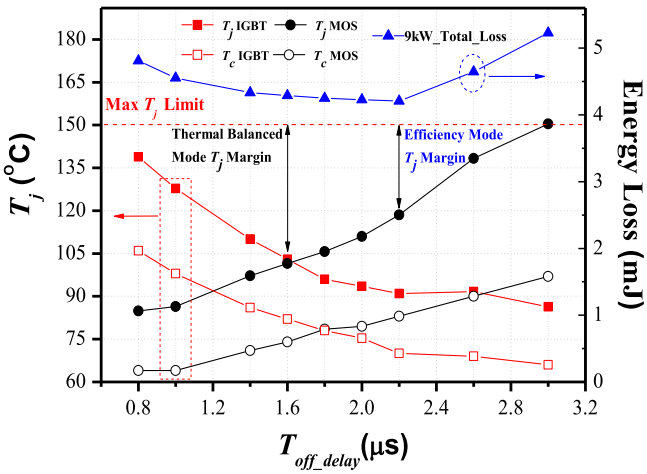


Fig. 15. Dependency of hybrid device's temperature and energy loss on its gate signal's turn-OFF delay time.

When the output power of the dc–dc boost converter is 9 kW, the hybrid switch's switching loss, measured case temperature, and calculated junction temperature of the auxiliary SiC MOSFET and the IGBT inside the hybrid switch at various gate signal's turn-OFF delay time and a zero turn-ON delay time are shown in Fig. 15. When the gate signal's turn-OFF delay time increases, the case temperature and the junction temperature of the IGBT decrease, while those of the auxiliary SiC MOSFET increase. It is explained by the decreasing switch-off loss of the IGBT and the increasing turn-OFF loss of the auxiliary SiC MOSFET with the increasing gate signal's turn-OFF delay time, as shown in Fig. 8. The balanced junction temperature between the auxiliary SiC MOSFET and the IGBT is achieved at the gate signal's turn-OFF delay time of 1.6 μs, and the corresponding case temperature deviation is approximately –8 °C. The ratio of the IGBT's and

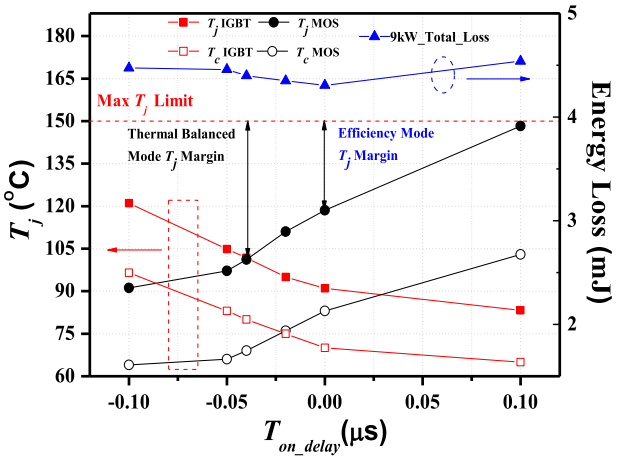


Fig. 16. Dependency of hybrid device's temperature and energy loss on its gate signal's turn-ON delay time.

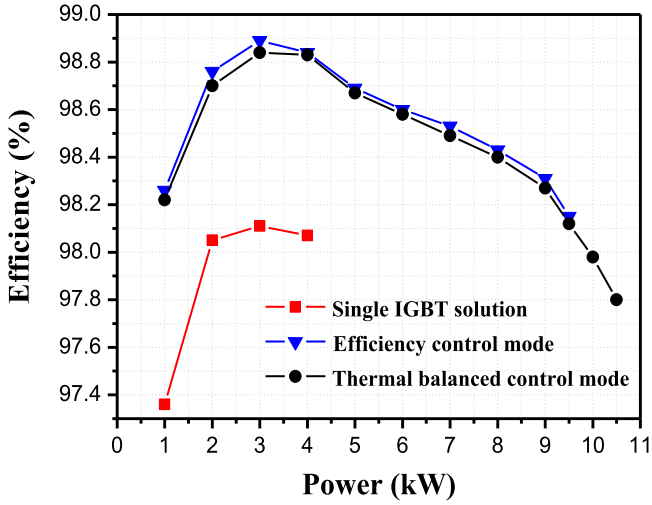


Fig. 17. Efficiency of hybrid switch and 40-A IGBT-based boost converter.

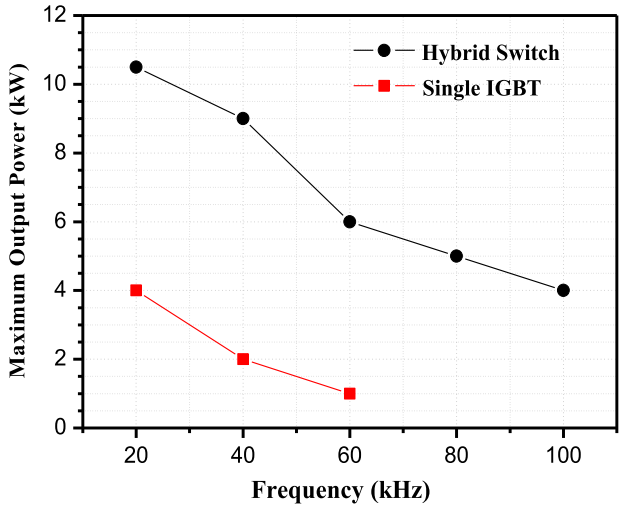


Fig. 18. Power rating of hybrid switch and 40 A IGBT.

the auxiliary SiC MOSFET's power losses is approximately 1.66 at the gate signal's turn-OFF delay time of 1.6 μs. The measured power loss and temperature are consistent with (12). And the total energy loss of the hybrid switch at the balanced junction temperature is 1.65% larger than its minimum total energy loss. The hybrid switch's junction temperature is 49 °C below the junction temperature limit in the balanced junction temperature control mode, while it is only 31 °C below the junction temperature limit in the efficiency control mode. Therefore, the balanced junction temperature control mode is helpful to reduce the failure rate of the hybrid switch or increase its lifetime. Also, the balanced junction temperature control mode can make full use of the hybrid switch's power handling capability, which is useful to greatly increase the converter's power rating.

When the output power of the dc–dc boost converter is 9 kW, the measured case temperature, the hybrid switch's switching loss, and the calculated junction temperature of the auxiliary SiC MOSFET and the IGBT inside the hybrid switch at a gate signal's turn-OFF delay time of 2.2 μs and various gate signal's turn-ON delay time is shown in Fig. 16. When the gate signal's turn-ON delay time increases, the case temperature and the junction temperature of the IGBT decrease, while those of the auxiliary SiC MOSFET increase. It is explained by the decreasing switch-on loss of the IGBT and increasing turn-ON loss of the SiC MOSFET, as shown in Figs. 5 and 6. The balanced junction temperature between the auxiliary SiC MOSFET and the IGBT is achieved with a gate signal's turn-ON delay time of -0.04 μs, and the corresponding case temperature deviation is approximately –11 °C, and the ratio of the IGBT's and the auxiliary SiC MOSFET's power losses is approximately 1.48 at the gate signal's turn-ON delay time of -0.04 μs. The measured power loss and temperature are consistent with (12). The total energy loss of the hybrid switch with the optimal balanced junction temperature control mode is 2.3% larger than its minimum total energy loss with the optimal efficiency control mode. The hybrid switch's junction temperature is 46 °C below the junction temperature limit in the balanced junction temperature control mode, while it is 31 °C below the junction temperature limit in the efficiency control mode.

C. Experimental Demonstration of Hybrid Switch

In order to demonstrate the superior performance of the hybrid switch to the single IGBT solution, the boost converters based on the 40-A single IGBT solution and the hybrid switch with two optimal control methods are tested and compared, respectively. Fig. 17 shows the measured efficiency of the boost converter based on the single IGBT solution and the hybrid switch at a switching frequency of 20 kHz and various load conditions. The efficiency of the boost converter based on the hybrid switch is approximately 0.8% higher than that based on the single IGBT solution at the same output power. The maximum output power of the boost converter based on the single IGBT solution is approximately 4 kW when the IGBT's junction temperature reaches its temperature limit. The maximum output power of the boost converter based on the hybrid switch with the thermal balance control mode and the efficiency control mode are approximately 10.5 and 9.5 kW, respectively. The maximum output power of the hybrid switch based boost converter with the thermal balance control model is 10% larger than that of the

efficiency control mode although its efficiency with the thermal balance control mode is approximately 0.05% smaller.

The maximum output power of the hybrid switch and the 40-A IGBT based dc–dc boost converter at various switching frequencies is shown in Fig. 18. When the switching frequency of the boost converter is 20 kHz, the maximum output power of the hybrid switch based dc–dc boost converter with the thermal balance control mode is 163% higher than that of the single IGBT solution with hard switching condition. When the output power of the boost converter is kept to be 4 kW, the switching frequency of the hybrid switch based dc–dc boost converter with the thermal balance control mode is four times higher than that of a single IGBT solution with hard switching condition.

IV. Conclusion

In order to achieve low power loss, large power handling capability, and reliable operation of the hybrid switch in power conversion applications, the theoretical analysis and experimental study of its loss and operation temperature at various gate control patterns in the double pulse test circuit and the dc–dc boost converter have been carried out. The theoretical principal and experimental comparison of the conventional efficiency control mode and the novel thermal balance control mode of the hybrid switch in the dc–dc boost converter is extensively investigated and analyzed. The target of the conventional efficiency control mode is to achieve the minimum total power losses of the hybrid switch and the maximum efficiency of the converter. However, the auxiliary SiC MOSFET has much higher junction temperature than the main IGBT in the steady state of the dc–dc boost converter with the efficiency control mode. It results in severe concern of the SiC MOSFET's degradation or thermal runaway, and induces the reduction of the converter's maximum output power.

In this paper, we propose a new method of gate control optimization, referred to as the thermal balance control mode, to keep the junction temperature of both devices within the specified temperature range, and to minimize the total power loss simultaneously. Theoretical analysis and experimental study show that the optimum ratio of the power losses between the auxiliary SiC MOSFET and the main IGBT is needed to achieve the thermal balanced control mode, which is correlated with their thermal resistance. Compared to the efficiency control mode, the implementation of the thermal balance control mode in the hybrid switch can achieve much low operation temperature of switching devices and much larger output power of the dc–dc converter with almost the same conversion efficiency. Using the optimum thermal balanced control method, the Si/SiC hybrid switch shows significant improvement in the maximum power handling capability and maximum frequency capability compared to the single IGBT solutions.

References

[1] B. J. Baliga, "Enhancement and depletion-mode vertical-channel m.o.s. gated thyristors," *Electron. Lett.*, vol. 15, no. 20, pp. 645–647, Sep. 27, 1979.

[2] B. W. Scharf and J. D. Plummer, "Insulated-gate planar thyristors: II—Quantitative modeling," *IEEE Trans. Electron Devices*, vol. ED-27, no. 2, pp. 387–394, Feb. 1980.

[3] Y. M. Jian, G. C. Hua, F. X. Yang, and F. C. Lee, "Soft-switching of IGBT's with the help of MOSFET's," in *Proc. VPEC Power Electron. Seminar*, Blacksburg, VA, USA, Sep. 1992, pp. 77–84.

[4] J. W. Kimball and P. L. Chapman, "Evaluating conduction loss of a parallel IGBT–MOSFET combination," in *Proc. Conf. Rec. 39th IEEE IAS Annu. Meeting*, Oct. 2004, pp. 1233–1237.

[5] K. F. Hoffmann and J. P. Kaerst, "High frequency power switch-Improved performance by MOSFETS and IGBTs connected in parallel," in *Proc. Eur. Power Electron. Appl.*, Dresden, Germany, Sep. 2005, pp. 1–11.

[6] J. Lai *et al.*, "A hybrid-switch-based soft-switching inverter for ultrahigh-efficiency traction motor drives," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1966–1973, May/Jun. 2014.

[7] G. Ortiz, C. Gammeter, J. W. Kolar, and O. Apeldoorn, "Mixed MOSFET-IGBT bridge for high-efficient medium-frequency dual-active-bridge converter in solid state transformers," in *Proc. IEEE 14th Workshop Control Model. Power Electron.*, Salt Lake City, UT, USA, 2013, pp. 1–8.

[8] J. W. Palmour, "Silicon carbide power device development for industrial markets," in *Proc. IEEE Int. Electron. Devices Meeting*, San Francisco, CA, USA, 2014, pp. 1.1.1–1.1.8.

[9] T. Wu, J. Chen, S. Mao, and M. J. Schutten, "1200 V SiC MOSFETS for high voltage power conversion," in *Proc. IEEE Energy Convers. Congr. Expo.*, Raleigh, NC, USA, 2012, pp. 2921–2926.

[10] J. Racsbkowski, D. Peftitsis, and H. P. Nee, "Silicon carbide power transistors: A new era in power electronics is initiated," *IEEE Ind. Electron. Mag.*, vol. 6, no. 2, pp. 17–26, Jun. 2012.

[11] A. Q. Huang, X. Song, and L. Zhang, "6.5 kV Si/SiC hybrid power module: An ideal next step?" in *Proc. IEEE Int. Workshop Integr. Power Packag.*, Chicago, IL, USA, 2015, pp. 64–67.

[12] X. Song and A. Q. Huang, "6.5kV FREEDM-Pair: Ideal high power switch capitalizing on Si and SiC," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, Geneva, Switzerland, 2015, pp. 1–9.

[13] R. A. Minamisawa, U. Vemulapati, A. Mihaila, C. Papadopoulos, and M. Rahimo, "Current sharing behavior in Si IGBT and SiC MOSFET cross-switch hybrid," *IEEE Electron. Device Lett.*, vol. 37, no. 9, pp. 1178–1180, Sep. 2016.

[14] U. R. Vemulapati, A. Mihaila, R. A. Minamisawa, F. Canales, M. Rahimo, and C. Papadopoulos, "Simulation and experimental results of 3.3 kV cross switch "Si-IGBT and SiC-MOSFET" hybrid," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, Prague, Czech Republic, 2016, pp. 163–166.

[15] A. Deshpande and F. Luo, "Design of a silicon-WBG hybrid switch," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl.*, Blacksburg, VA, USA, 2015, pp. 296–299.

[16] M. Rahimo, F. Canales, R. A. Minamisawa, C. Papadopoulos, U. Vemulapati, and A. Mihaila, "Characterization of a silicon IGBT and silicon carbide MOSFET cross-switch hybrid," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4638–4642, Sep. 2015.

[17] W. Zhang, S. Anwar, D. J. Costinett, and F. Wang, "Investigation of cost-effective SiC based hybrid switch and improved inductor design procedure for boost converter in electrical vehicles application," in *Proc. World Congr. Exhib. SAE Tech. Papers*, 2015, vol. 2, pp. 209–214.

[18] J. He, R. Katebi, and N. Weise, "A current-dependent switching strategy for Si/SiC hybrid switch based power converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8344–8352, Oct. 2017.

[19] T. Zhao and J. He, "An optimal switching pattern for "SiC+Si" hybrid device based voltage source converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Charlotte, NC, USA, 2015, pp. 1276–1281.

[20] S. Ozdemir, F. Acar, and U. S. Selamogullari, "Comparing different switching techniques for silicon carbide MOSFET assisted silicon IGBT based hybrid switch," in *Proc. Int. Conf. Electr. Eng. Inf.*, Denpasar, Indonesia, 2015, pp. 558–561.

[21] Y. Wang, N. Zhu, C. Yan, and D. Xu, "Efficiency improvement of 2- and 3-level inverters for distributed photovoltaic application using hybrid devices," in *Proc. IEEE 2nd Int. Future Energy Electron. Conf.*, Taipei, Taiwan, 2015, pp. 1–7.

[22] A. Agarwal, W. J. Sung, L. Marlino, P. Gradzki, J. Muth, and R. Ivester, "Wide band gap semiconductor technology for energy efficiency," *Mater. Sci. Forum*, vol. 858, pp. 797–802, 2016.

[23] M. Schulz, "Thermal management details and their influence on the aging of power semiconductors," in *Proc. IEEE Eur. Conf. Power Electron. Appl.*, 2014 pp. 1–6.

[24] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg, and M. Liserre, "Junction temperature control for more reliable power electronics," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 765–776, Jan. 2018.

[25] C. Busca, R. Teodorescu, F. Blaabjerg, S. Munk-Nielsen, L. Helle, and T. Abeyasekera, "An overview of the reliability prediction related aspects of high power IGBTs in wind power applications," *Microelectron. Reliab.*, vol. 51, nos. 9–11, pp. 1903–1907, 2011.
[26] F. Blaabjerg, K. Ma, and D. Zhou, "Power electronics and reliability in renewable energy systems," in *Proc. IEEE Int. Symp. Ind. Electron.*, Hangzhou, China, 2012, pp. 19–30.
[27] T. T. Nguyen, A. Ahmed, T. V. Thang, and J. H. Park, "Gate oxide reliability issues of SiC MOSFETs under short-circuit operation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2445–2455, May 2015.
[28] S. Liu, C. Gu, J. Wei, Q. Qian, W. Sun, and A. Q. Huang, "Repetitive unclamped-inductive-switching-induced electrical parameters degradations and simulation optimizations for 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4331–4338, Nov. 2016.
[29] Cree, C2M0160120D-silicon carbide power MOSFET datasheet, 2014, [Online]. Available: http://www.cree.com/

Jun Wang (S'06–M'10–SM'15) received the Ph.D. degree in electrical engineering from North Carolina State University, Raleigh, NC, USA, in 2010.

He was a Device Design Engineer with Texas Instruments, Inc., Bethlehem, PA, USA, between 2010 and 2013. He became a Professor with the College of Electrical and Information Engineering, Hunan University in 2014. His research interests include power semiconductor devices and their applications in power electronics systems.

Dr. Wang has been an Associate Editor of the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS since 2017.

Zongjian Li (S'17) received the B.S. degree in electronic information engineering from the College of Engineering, Hunan Normal University, Changsha, China, in 2012. He is currently working toward the Ph.D. degree in electric engineering with the College of Electrical and Information Engineering, Hunan University, Changsha, China.

His research interests include silicon carbide power electronic devices and their applications.

Xi Jiang received the B.S. degree in electric engineering from the School of Electrical and Automation Engineering, East China Jiaotong University, Nanchang, China, in 2014. He is currently working toward the Ph.D. degree with the College of Electrical and Information Engineering, Hunan University, Changsha, China.

His research interest includes power electronics devices, reliability of power devices, and their applications in power electronics systems.

Cheng Zeng received the B.S. degree in electrical engineering from Hunan University of Technology, Zhuzhou, China, in 2015. He is currently working toward the M.S. degree in electrical engineering with the School of Hunan University, Changsha, China.

His research interests include power electronic devices, gate drivers, and high power density converters.

Z. John Shen (S'89–M'94–SM'01–F'11) received the B.S. degree from Tsinghua University, Beijing, China, in 1987, and the M.S. and Ph.D. degrees from Rensselaer Polytechnic Institute, Troy, NY, USA, in 1991 and 1994, respectively, all in electrical engineering.

Between 1994 and 1999, he held a variety of positions including Senior Principal Staff Scientist with Motorola. He was with the faculty of the University of Michigan-Dearborn between 1999 and 2004, and the University of Central Florida between 2004 and 2012. He joined the Illinois Institute of Technology in 2013 as the Grainger Chair Professor in electrical and power engineering. He has also held a courtesy professorship with Hunan University, Changsha, China since 2007; and with Zhejiang University, Hangzhou, China, since 2013. His research interests include power electronics, power semiconductor devices and ICs, automotive electronics, renewable and alternative energy systems, and electronics manufacturing.

Dr. Shen is a recipient of the 2012 IEEE Region 3 Outstanding Engineer Award, the 2003 NSF CAREER Award, the 2006 IEEE Transaction Paper Award from IEEE Society of Power Electronics, the 2003 IEEE Best Automotive Electronics Paper Award from IEEE Society of Vehicular Technology, and the 1996 Motorola Science and Technology Award. He has served as VP of Products 2009–2012, Associate Editor and Guest Editor in Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS, Technical Program Chair, and General Chair of several major IEEE conferences.