Diode Reverse Recovery Process and Reduction of a Half-Wave Series Cockcroft–Walton Voltage Multiplier for High-Frequency High-Voltage Generator Applications

Saijun Mao, *Member, IEEE*, Jelena Popović, *Member, IEEE*, and Jan Abraham Ferreira, *Fellow, IEEE*

***Abstract*—This paper investigates the diode reverse recovery process and reduction of a half-wave (HW) series Cockcroft–Walton (CW) voltage multiplier based on the steady-state analysis for high-frequency high-voltage (HV) generator applications. The diode reverse recovery process for a multistage voltage multiplier is analyzed after the introduction of steady-state operation. The diode reverse recovery problem is the bottleneck to further increase the circuit operation switching frequency for achieving high power density and short HV pulse rise and decay times. The diode reverse recovery problem is mainly caused by the diodes in the first-stage voltage multiplier. It is suggested that the most effective and economic way to alleviate the diode reverse recovery problem is by employing diodes without reverse recovery such as silicon carbide Schottky diodes in the first stage only. The silicon carbide Schottky diode without reverse recovery needs to be used only in the first stage of the voltage multiplier to effectively mitigate the reverse recovery problems at high frequency. The 300 kHz switching frequency three-stage voltage multiplier circuit hardware prototype experimental results finally validate the analysis. A technology demonstrator of a 300 kHz 8 kW 160 kV HV generator based on the proposed hybrid silicon carbide and silicon diode solution for the HW series CW voltage multiplier is provided finally.**

***Index Terms*—Cockcroft–Walton (CW) voltage multiplier, half-wave (HW), high frequency, high-voltage (HV) generator, hybrid silicon carbide and silicon diode solution, reverse recovery, steady state.**

I. Introduction

IN THE past few decades, high-voltage (HV) generators had been widely used in various industrial applications such as X-ray generation, electrostatic precipitation, HV capacitor charger, plasma generator, as well as many other pulsed power areas [1]–[6]. Among these applications, the voltage multipliers, and especially, the half-wave (HW) series Cockcroft–Walton (CW) voltage multiplier are employed as one of the key power building blocks for the HV generator system since the voltage multiplier circuit offers an easy and economic way of generating low current high output dc voltage shown in Fig. 1. The high turn ratio of the HV transformer and the voltage rating of the rectifier diodes can be significantly reduced by using a multistage voltage multiplier circuit. The transformer nonidealities owing to a large turn ratio can be alleviated with the voltage multiplier [7], [8].

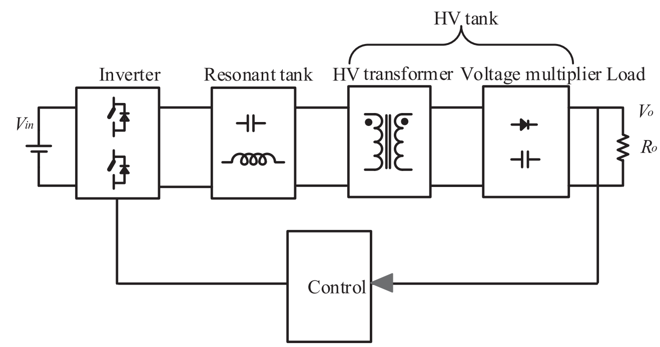

Fig. 1. Circuit diagram of HV generators.

Though the multistage HW series CW voltage multiplier circuit has been widely used for HV generator applications, however, the detailed steady-state analysis and reverse recovery problems of the multistage HW series CW voltage multiplier circuit at high switching frequency have not yet been investigated in the state-of-the-art works [9], [10]. The existing analysis for the multistage HW series CW voltage multiplier circuit is based on the ideal diode model [7]–[10]. However, if the actual diode model is taken into consideration, the reverse recovery process of the diodes should not be neglected at high frequency. Because of the different circuit conditions, the switching process of the diodes in the first stage and the diodes in the other stages are different. So, the diodes in the first stage and the diodes in the other multistage HW series CW voltage multiplier stages will be analyzed separately. The multiplier diode reverse recovery problem is the bottleneck of further increasing the circuit operation switching frequency to achieve high power density, HV pulse with short rise, and decay times [11].

The silicon carbide Schottky diode without reverse recovery is used to replace the conventional ultrafast silicon diode

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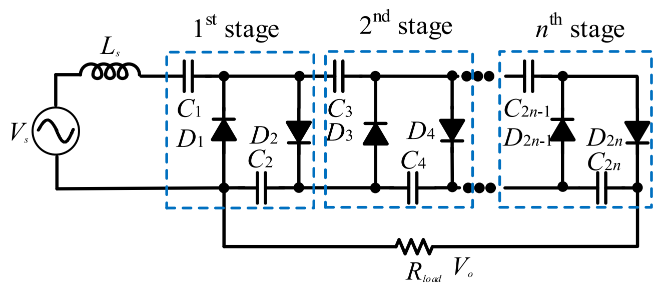

Fig. 2. Circuit diagram of the n-stage HW series CW voltage multiplier circuit.

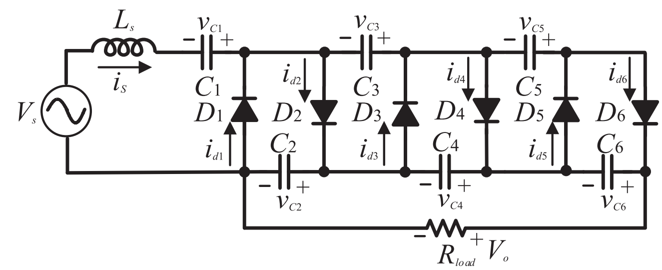

Fig. 3. Circuit diagram of the three-stage HW series CW voltage multiplier circuit.

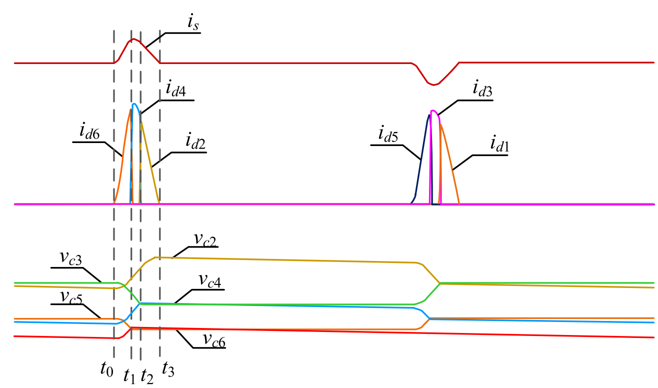

Fig. 4. Key waveforms for the HW series CW voltage multiplier.

in all voltage multiplier stages to mitigate the reverse recovery problems in high-frequency operations [11]–[14]. However, replacing the silicon diodes in all voltage multiplier stages with silicon carbide Schottky diode will significantly increase the cost of the voltage multiplier for the HV generator.

The diode reverse recovery process of the high-frequency voltage multiplier circuit has not been addressed in the literature yet. It is important to investigate the diode reverse recovery process at a high switching frequency and to study the diode reverse recovery reduction method to achieve optimal performance for a voltage multiplier based HV pulse converter. Furthermore, the cost-effective method to alleviate the diode reverse recovery problem for the multistage HW series CW voltage multiplier at high frequency is the research needs at a high switching frequency [15]–[18].

The sections of this paper are organized as follows. Section II introduces steady-state circuit analysis of the HW series CW voltage multiplier circuit. Section III provides the analysis of a diode reverse recovery process for the multistage HW series CW voltage multiplier. In Section IV, the hardware prototype experimental results validate the diode reverse recovery analysis. The technology demonstrator of a 300 kHz 8 kW 160 kV HV generator based on the proposed hybrid silicon carbide and silicon diode solution for the HW series CW voltage multiplier is given. Section V concludes this paper.

The main contributions and novelties of this paper are as follows.

1) The diode reverse recovery process is investigated for the high-frequency multistage HW series CW voltage multiplier based on the steady-state analysis. The diode reverse recovery problem is mainly caused by the diodes in the first-stage voltage multiplier.
2) The most effective and economic way to alleviate the diode reverse recovery problem for the multistage HW series CW voltage multiplier is proposed with the silicon carbide and silicon hybrid diode device solution.

II. Steady-State Circuit Analysis of the Voltage Multiplier

The HW series CW voltage multiplier in Fig. 2 is a popular voltage multiplier because of its HV boosting features, compact size, low voltage stress on diodes and capacitors, as well as its cost effectiveness [1]–[3]. A three-stage HW series CW voltage multiplier is shown as a case study in Fig. 3. V_s is a sinusoidal voltage source. L_s represents the circuit parasitic inductor, which can be the transformer leakage inductor or a real inductor introduced into the voltage multiplier circuit.

The positive half cycle of the three-stage HW series CW voltage multiplier circuit is analyzed as an example. There are four operation modes, as shown in Fig. 4, and the characteristics in each operation mode are depicted as follows.

Mode 1 (before t_0): In this mode, as shown in Fig. 5(a), i_s is zero and all diodes are blocked. Capacitors C_2, C_4, and C_6 charge the load, while C_1, C_3, and C_5 are floating. At t_0, the voltage of even diodes is lower than that of odd diodes in the same stage. So, $v_{c2} < v_{c1} + v_S$, $v_{c4} < v_{c3}$, and $v_{c6} < v_{c5}$.

Mode 2 (t_0–t_1): The equivalent circuit of this mode is shown in Fig. 5(b). i_s is positive. As $v_{c6} < v_{c5}$ and $v_{c4} < v_{c3}$, D_2 and D_4 are still blocked and D_6 is conducted first. Odd capacitors C_1, C_3, and C_5 are discharged by i_s and even capacitors C_2, C_4, and C_6 are charged. Simultaneously, even capacitors supply the load current.

Mode 3 (t_1–t_2): The equivalent circuit of this mode is shown in Fig. 5(c). At t_1, v_{c6} is equal to v_{c5} and D_6 is blocked. D_4 begins to be conducted. C_2 and C_4 are charged by i_s, while C_1 and C_3 are discharged. Simultaneously, even capacitors supply the load current, while C_5 is floating.

Mode 4 (t_2–t_3): The equivalent circuit of this mode is shown in Fig. 5(d). At t_2, v_{c4} is equal to v_{c3} and D_4 is blocked, while D_2 begins to conduct. C_2 is charged by i_s, while C_1 is discharged. Simultaneously, even capacitors supply the load current, while C_3 and C_5 are floating.

The circuit operation principle in the negative half cycle is similar to the positive half cycle.

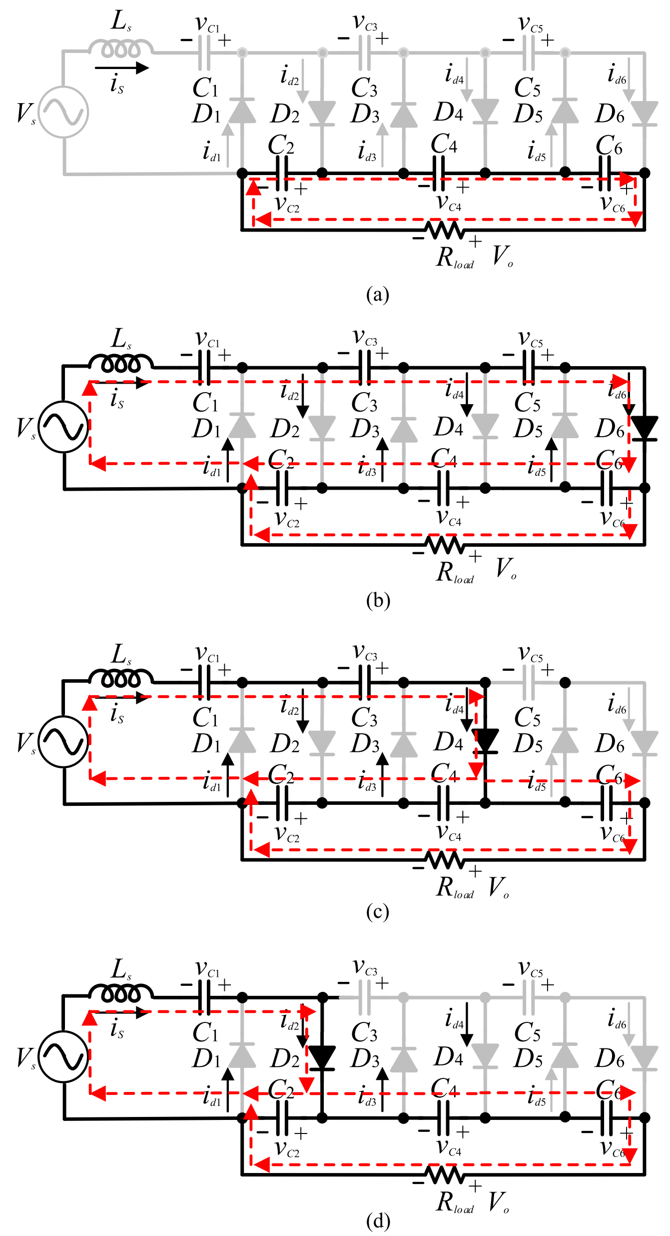

Fig. 5. Equivalent circuits of modes for the HW series CW voltage multiplier. (a) Before t_0. (b) t_0–t_1. (c) t_1–t_2. (d) t_2–t_3.

According to Fig. 5, in the positive half cycle of the sinusoidal voltage, only one of the even diodes conducts with the sequence D_6, D_4, and D_2. Similar behavior occurs during the negative half cycle. The odd diodes conduct in the sequence D_5, D_3, and D_1.

According to the above-mentioned analysis, the following conclusions can be obtained.

1) Only one of the diodes will conduct in a specific time frame when $i_s \neq 0$.
2) The conducting sequence is from right to left for even diodes in a positive half cycle and odd diodes in a negative half cycle.
3) The maximum value of v_{C2k} is equal to the minimum value of v_{C2k-1}. Similarly, the maximum value of v_{C2k-1} is equal to the minimum of v_{C2k-2}, where k represents the kth stage in the HW series CW voltage multiplier circuit.

At the no-load condition, the output voltage of the multistage HW series CW voltage multiplier is given by

$$V_o = 2nV_s \tag{1}$$

where V_S is the peak value of the transformer secondary winding output voltage or input voltage to the voltage multiplier and n represents the total number of stages of the voltage multiplier. However, when the voltage multiplier circuit supplies the current to the loads, the voltage multiplier suffers from voltage drop and the voltage ripple appears at its output voltage.

The voltage fluctuation of the kth-stage capacitors is

$$\delta V_{c2k-1} = \delta V_{c2k} = (n-k+1)\frac{I_o}{fC}. \tag{2}$$

The output voltage fluctuation is equal to the sum of the even capacitors voltage fluctuation

$$\delta V_o = \sum_{k=1}^{n} \delta V_{2k} = \frac{n(n+1)}{2}\frac{I_o}{fC}. \tag{3}$$

Based on the third conclusion in the operation principle section, the voltage drop of the kth-stage even (odd) capacitor is equal to the sum of the voltage fluctuation of even (odd) capacitors in stages that are before the kth stage

$$\Delta V_{2k-1} = \sum_{i=1}^{k-1} \delta V_{2i-1} = \frac{(n+k+1)(n-k)}{2}\frac{I_o}{fC} \tag{4}$$

$$\Delta V_{2k} = \sum_{i=1}^{k-1} \delta V_{2i} = \frac{(n+k+1)(n-k)}{2}\frac{I_o}{fC}. \tag{5}$$

The output voltage drop is equal to the sum of the voltage drop of even capacitors. The output voltage drop is related to the switching frequency, the capacitance and stage number of the HW series CW voltage multiplier, and output current

$$\Delta V_o = \frac{(4n^3+3n^2-n)}{6}\frac{I_o}{fC}. \tag{6}$$

The output voltage of the multistage HW series CW voltage multiplier with load is given by

$$V_o = 2nV_S - \frac{(4n^3+3n^2-n)}{6}\frac{I_o}{fC}. \tag{7}$$

The increase of the number of the voltage multiplier stages n increases the no-load gain proportionally but also increases the rate of voltage drop cubically.

If the capacitors throughout all the voltage multiplier stages are equal, the peak-to-peak HV pulse ripple of the multistage HW series CW voltage multiplier is approximated as

$$\delta V_{\text{pp}} = \frac{n\,(n+1)\,P_o}{2fCV_o} \tag{8}$$

where P_o is the output power, V_o is the output voltage, and C is the capacitance for the voltage multiplier [4], [5].

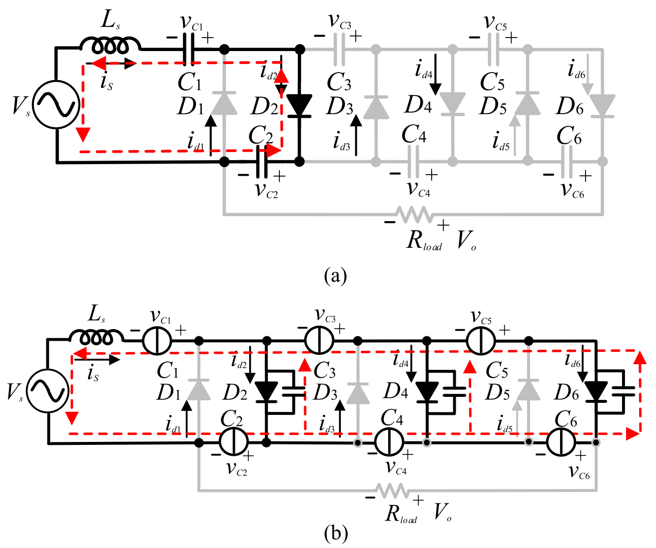

Fig. 6. Equivalent circuit for voltage multiplier stages 1 and 2. (a) Stage 1. (b) Stage 2.

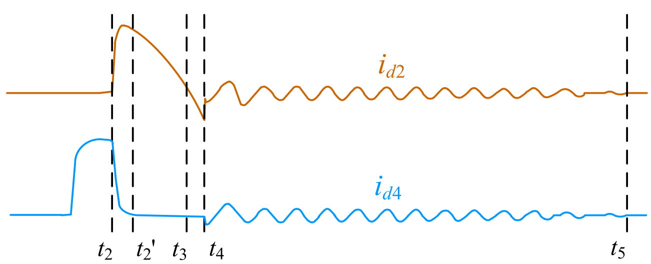

Fig. 7. Actual waveforms of i_{d2} and i_{d4}.

III. Diode Reverse Recovery Analysis for the Voltage Multiplier

A. *Reverse Recovery Procedure of Diodes in the First-Stage Multiplier Circuit*

D_2 is taken as an example for the analysis in the positive half cycle. The current flowing through D_2, which is equal to i_s, decreases to zero at t_3 in mode 3, and then D_2 is blocked. The equivalent circuits for stages 1 and 2 are illustrated in Fig. 6. The waveform of i_{d2} with the actual diode model is shown in Fig. 7. Before t_3, the working process is the same. Beyond t_3, the working process is analyzed in two stages.

Stage 1 (t_3–t_4): In this stage, the equivalent circuit is as shown in Fig. 6(a). To eliminate the minor carrier stored in D_2, i_{d2} continues to increase reversely after t_3. The slope of i_{d2} in this stage is determined by the voltage across the inductor L_s. The voltage across i_{d2} is zero in this stage. At t_4, this stage is completed when all minor carriers are eliminated.

Stage 2 (t_4–t_5): Beyond t_4, the inductor L_s, with the initial current value i_{s1}, begins to resonate with the parasitic capacitors of the diodes. The equivalent resonant circuit is as shown in Fig. 6(b). Compared to diodes parasitic capacitors, capacitors C_1–C_6 are very large and the voltage can be regarded as constant during the resonant period. They are modeled as constant voltage

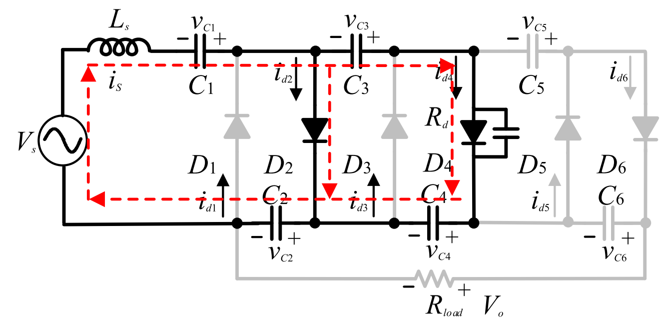

Fig. 8. Equivalent circuit for diodes in other voltage multiplier stages.

sources. The resonance will not complete until t_5, when D_5 conducts [16].

B. *Reverse Recovery Procedure of Diodes in the Other Stages*

In mode 3, when v_{C3} equals v_{C4} at t_3, D_4 is blocked and D_2 begins to conduct. However, with the actual diode model, the waveform of i_{d4} is as shown in Fig. 7. The equivalent circuit for diodes in other voltage multiplier stages is as shown in Fig. 8.

At t_2', i_{d4} decreases to zero. According to the model, the voltage across D_4 is equal to V_d as v_{C4} (v_{C3}) stops to increase (decrease) after t_2'. D_4 is not blocked although i_{d4} is zero.

Beyond t_3, the diode parasitic capacitor begins to resonate with L_s, and D_4 begins to be blocked. However, as i_{d4} was zero, zero current turn-OFF is realized for D_4 and there is no reverse recovery loss. Similarly, ZCS is also realized for D_6.

The power loss for the voltage multiplier can be calculated based on the following analysis. The power loss of capacitors in the voltage multiplier circuit

$$P_{\text{cap\_vm}} = \frac{\tan\delta I^2_{\text{cvm}-\text{rms}}}{2\pi f C_{\text{vm}}} \tag{9}$$

where C_{vm} is the capacitor of the voltage multiplier, $I_{\text{cvm-rms}}$ is the rms value of the ac current flowing through the capacitor of the voltage multiplier, and tanδ is the dissipation factor of the capacitor.

The power loss of the diode in the voltage multiplier circuit mainly consists of two parts: conduction loss and reverse recovery loss. The conduction loss can be calculated with the following expression:

$$P_{\text{diode\_vm\_con}} = V_{F0} I_{d\_F\text{av}} + I_{d\_\text{rms}} R_d^2 \tag{10}$$

where $I_{d\_F\text{av}}$ is the average current flowing through the diode, and $I_{d\_F\text{av}}$ is the rms current. The conduction losses of the antiparallel diode can be estimated using a diode approximation with a series connection of dc voltage source (V_{F0}) representing diode ON-state zero-current voltage and a diode ON-state resistance (R_d).

The switching loss can be approximated as follows:

$$P_{\text{diode\_rec\_rr}} = f Q_{\text{rr}} V_r \tag{11}$$

where Q_{rr} is the diode reverse recovery charge, and V_r is the reverse voltage of the diode.

Based on the analysis of the diode reverse recovery in the voltage multiplier circuit, only the diodes in the first stage of the

TABLE I
KEY PARAMETERS FOR THE VOLTAGE MULTIPLIER CIRCUIT PROTOTYPE

Key parameters	Values
Input voltage	50VAC
Output voltage	Around 2kVDC
Output power	30W
Switching frequency	300kHz
Multiplier diode	Silicon diode: BYV26E (1kV, 1A), 2 in series for each multiplier stage diode unit Silicon carbide diode: GB01SLT12(1.2kV, 1A), 2 in series for each multiplier stage diode unit
Multiplier capacitance	0.47nF, 3kV ceramic capacitor

voltage multiplier circuit suffer the reverse recovery loss. The silicon carbide Schottky diode without reverse recovery can be employed to effectively eliminate the diode reverse recovery loss in the multistage voltage multiplier circuit.

For the voltage multiplier circuit with *n* stages and *m* diodes connected in series for each stage, the total power loss of the diode in the voltage multiplier can be expressed as

$$P_{\mathrm{diode\_vm}} = 2mn(V_{F0} I_{d\_F\mathrm{av}} + I_{d\_\mathrm{rms}} R_d^2 + f Q_{\mathrm{rr}} V_r). \quad (12)$$

The total power loss of the voltage multiplier with silicon diode can be calculated with the following expression:

$$P_{\mathrm{vm\_Si-diode}} = 2mn \left(\frac{\tan\delta I_{\mathrm{cvm-rms}}^2}{2\pi f C_{\mathrm{vm}}} + V_{F0} I_{d\_F\mathrm{av}} + I_{d\_\mathrm{rms}} R_d^2 + f Q_{\mathrm{rr}} V_r \right) \quad (13)$$

The total power loss of the voltage multiplier with a silicon carbide Schottky diode can be expressed as

$$P_{\mathrm{vm\_SiC-diode}} = 2mn \left(\frac{\tan\delta I_{\mathrm{cvm-rms}}^2}{2\pi f C_{\mathrm{vm}}} + V_{F0} I_{d\_F\mathrm{av}} + I_{d\_\mathrm{rms}} R_d^2 \right). \quad (14)$$

According to the analysis, some conclusions can be obtained as follows.

1) The reverse recovery in the HW series CW voltage multiplier circuit is contributed by the diodes in the first stage. There is no reverse recovery for diodes in the other stages.
2) The resonant process is mainly influenced by the reverse recovery of the diodes in the first stage. So, the reverse recovery problem in the HW series CW voltage multiplier circuit depends on the performance of the diodes in the first stage.

IV. EXPERIMENTAL RESULTS

A. Experimental Validation

Based on the above-mentioned analysis, the hardware prototype of a three-stage HW series CW voltage multiplier circuit with the positive-side voltage multiplier circuit is built in the laboratory to validate the concept. The key parameters for the voltage multiplier circuit prototype are presented in Table I.

The input voltage of the voltage multiplier circuit prototype is 50 VAC with 300 kHz frequency. The output voltage is 2 kVDC and the output power is around 30 W. The silicon diode BYV26E and silicon carbide diodes are adopted in the first-stage diodes D_2, D_4, and D_6 for the three stages voltage multiplier circuit. The second- and third-stage diodes D_4 and D_6 are all silicon diodes. Two diodes are connected in series for each multiplier stage diode unit.

The key experimental waveforms of the first-, second-, and third-stage diodes D_2, D_4, and D_6 for the three stages CW voltage multiplier circuit with all silicon rectifiers BYV26E are shown in Fig. 9(a)–(c), respectively. The reverse recovery current can only be found from the first-stage silicon diode D_2. There are no reverse recovery currents for the second- and third-stage diodes D_4 and D_6. The experimental results validate the analysis.

The key waveforms of the first-stage diode D_2 with a silicon carbide Schottky diode GB01SLT12 for a three-stage CW voltage multiplier circuit are shown in Fig. 9(d). The second- and third-stage diodes D_4 and D_6 are silicon diodes. According to the experimental waveforms, there is no reverse recovery current for the first-stage silicon carbide diode D_2. The reverse current for the first-stage silicon carbide diode D_2 is due to the resonance of diode junction capacitance with the circuit parasitical inductance for the voltage multiplier circuit. The reverse current for the first-stage silicon carbide diode D_2 can be reduced with lower circuit parasitical inductance and smaller diode junction capacitance. The silicon carbide Schottky diode without reverse recovery used only in the first stage of voltage multiplier circuit can effectively mitigate the reverse recovery problems in a high switching frequency HW series CW voltage multiplier circuit with good circuit performance.

B. Technology Demonstrator With Hybrid Devices Solution

A 300 kHz 8 kW 160 kV HV generator technology demonstrator with the proposed hybrid silicon carbide and silicon diodes solution for the HW series CW voltage multiplier is built in the laboratory. With a higher output current and out power for a high-frequency HV generator, the power loss of a multistage voltage multiplier will be increased. The stage number of a voltage multiplier is set to 2 for the power loss reduction at 8 kW output power. The circuit diagram of a 300 kHz 8 kW 160 kV HV generator prototype based on the modular HV architecture with modular HV transformers and a two-stage voltage multiplier is shown in Fig. 10. The circuit diagram of the two-stage HW series CW voltage multiplier for 300 kHz frequency 8 kW 160 kV HV generator prototype is illustrated in Fig. 11. The key parameters for the 300 kHz 8 kW 160 kV HV generator prototypes are listed in Table II. The elementary two-stage HW series CW voltage multiplier prototype photo for a 300 kHz 8 kW 160 kV HV generator prototype is shown in Fig. 12. The size is 4.6 cm*1.7 cm*0.7 cm. The volume of the voltage multiplier circuit can be reduced greatly by high-frequency operation.

The prototype photo and key experimental waveforms of the 300 kHz 8 kW 160 kV HV generator with 3.3 kW/L high power density are shown in Figs. 13 and 14, respectively. The tested efficiency of the HV generator prototype with the proposed hybrid silicon carbide and silicon diodes solution for the HW series

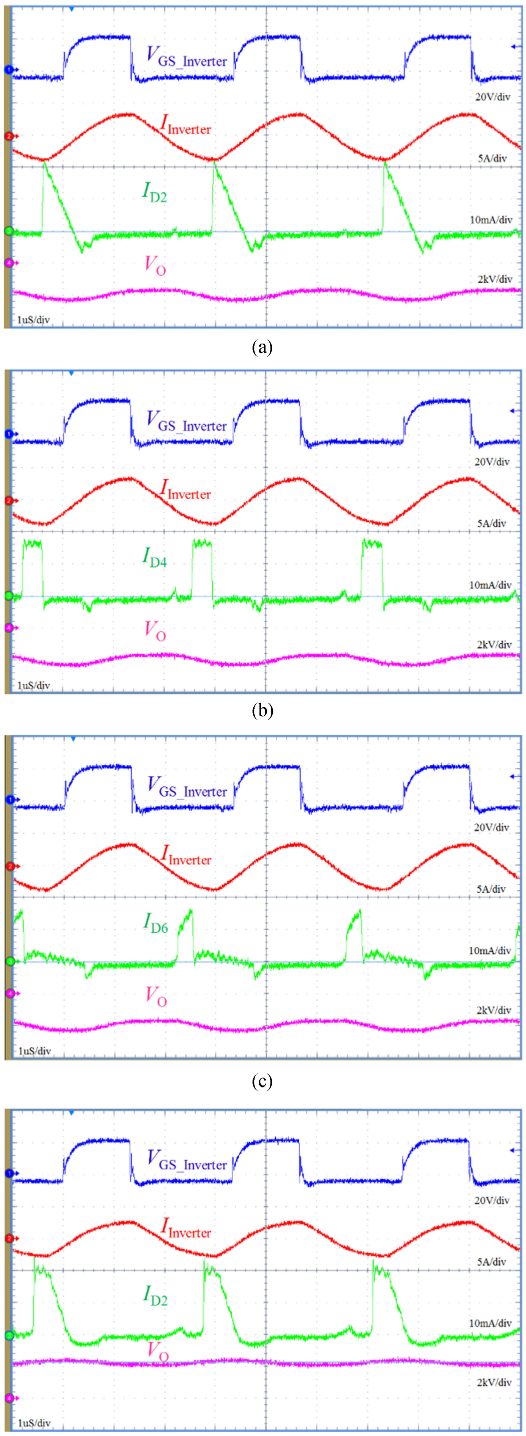

Fig. 9. Experimental waveforms for the three-stage voltage multiplier circuit. (a) Experimental waveforms of D_2. (b) Experimental waveforms of D_4. (c) Experimental waveforms of D_6. (d) Experimental waveforms of the SiC diode D_2.

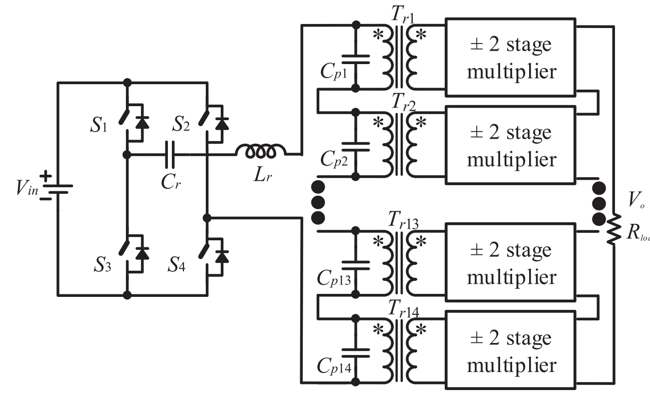

Fig. 10. Circuit diagram for the 300 kHz 8 kW 160 kV HV generator prototype.

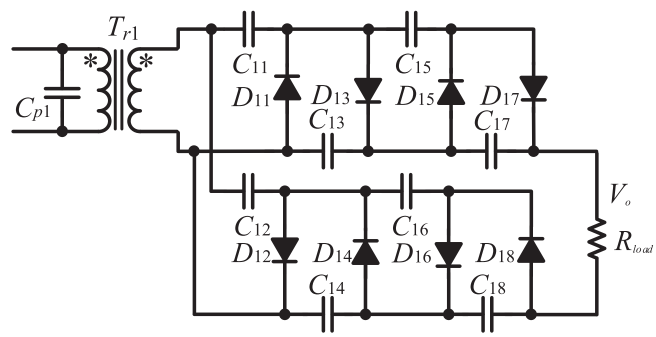

Fig. 11. Circuit diagram of the two-stage HW series CW voltage multiplier for the 300 kHz 8 kW 160 kV HV generator prototype.

TABLE II
KEY PARAMETERS FOR THE 300 KHZ 8 KW 160 KV HV GENERATOR PROTOTYPE

Key parameters	Values
Input voltage	600VDC
Output voltage	160kVDC
Output power	8kW
Switching frequency	300kHz
Architecture	Single inverter, twelve HV transformers, twelve 2 stage voltage multipliers
HV transformer	Turn ratio 3:72; Lp=22.89uH, Lp(lk)=0.55uH; Ls=13.36mH, Cp=1.7nF
Multiplier diode	-first stage: Silicon carbide GB01SLT12,1.2kV, SMB, 7 pcs in
	series -other stage: Silicon BYG23T, 1.3kV, SMA, 7 pcs in series
Multiplier capacitance	1nF/3kV, 1825 MLCC package, 2 pcs in series

CW voltage multiplier can achieve around 82.0% efficiency at 300 kHz switching frequency. The efficiency with the proposed hybrid device solution is 0.9% higher than the efficiency of the HV generator with all silicon diodes for the HW series CW voltage multiplier due to the reverse recovery loss saving. Based on the power loss calculation of the voltage multiplier with silicon diodes and silicon carbide diodes in (13) and (14), there is around 108 W total power loss saving due to the reverse recovery loss elimination with silicon carbide diodes for the first stage of the voltage multiplier for the 300 kHz 8 kW 160 kV HV generator prototype. The power loss estimation matches

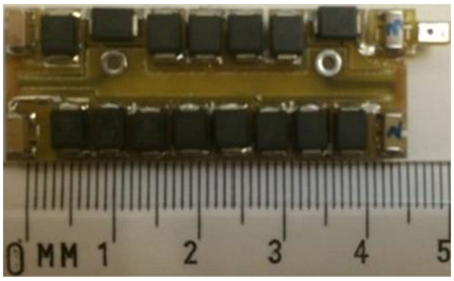

Fig. 12. Photo of the elementary voltage multiplier prototype.

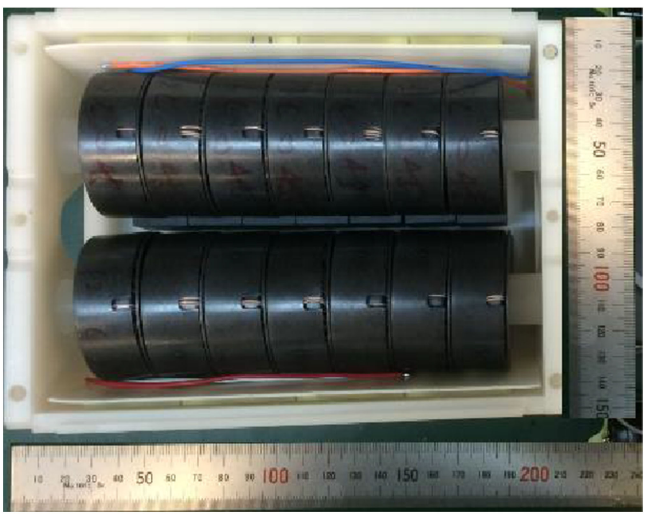

Fig. 13. Photo of the 300 kHz 8 kW 160 kV HV tank prototype.

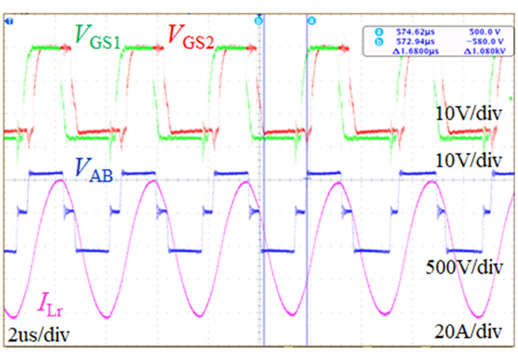

Fig. 14. Key experimental waveforms of the 300 kHz 8 kW 160 kV HV generator.

with the prototype efficiency test results. The proposed hybrid silicon carbide and silicon diodes solution is a cost-effective solution for the multistage HW series CW voltage multiplier for high-frequency operations with optimal performance on efficiency and power density.

V. Conclusion

The diode reverse recovery process and reduction solution of the multistage HW series CW voltage multiplier circuit are investigated for the HV generator applications. The diode reverse recovery problem is the bottleneck to further increase the circuit operation switching frequency for achieving high power density and short HV pulse rise and decay times. The diode reverse recovery problem is mainly caused by the diodes in the first-stage voltage multiplier based on the steady-state and reverse recovery process analysis. It is suggested that the most effective and economic way to alleviate the diode reverse recovery problem is by employing diodes without reverse recovery such as silicon carbide Schottky diodes in the first-stage voltage multiplier only. The silicon carbide Schottky diode without reverse recovery needs to be used in the first stage of the voltage multiplier to effectively mitigate the reverse recovery problems at high frequency. The 300 kHz switching frequency three-stage voltage multiplier circuit hardware prototype experimental results finally validate the analysis. The proposed hybrid silicon carbide and silicon diodes solution is a cost-effective solution for the multistage HW series CW voltage multiplier with optimal performance on efficiency and power density for high-frequency operations. At a high-temperature operation environment, the proposed hybrid silicon carbide and silicon diodes solution will enable further benefits to achieve optimal performance for multistage HW series CW voltage multiplier circuits.

References

[1] S. R. Jang, H. J. Ryoo, S. H. Ahn, J. Kim, and G. H. Rim, "Development and optimization of high-voltage power supply system for industrial magnetron," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1453–1461, Mar. 2012.

[2] J. A. Martin-Ramos, A. M. Pernia, J. Diaz, F. Nuno, and J. A. Martinez, "Power supply for a high-voltage application," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1608–1619, Jul. 2008.

[3] H. Hino, T. Hatakeyama, and M. Nakaoka, "Resonant PWM inverter linked dc-dc convertor using parasitic impedances of high-voltage transformer and its applications to X-ray generator," in *Proc. IEEE Power Electron. Spec. Conf.*, 1988, vol. 2, pp. 1212–1219.

[4] E. Bowles, S. Chapelle, G. Ferguson, and D. Furuno, "A high power density, high voltage power supply for a pulsed radar system," in *Proc. IEEE Power Modulator Symp.*, Jun. 1994, pp. 170–173.

[5] M. Khalifa, *High-Voltage Engineering: Theory and Practice*. New York, NY, USA: Marcel Dekker, Mar. 1990.

[6] L. Katzir and D. Shmilovitz, "A matrix-like topology for high-voltage generation," *IEEE Trans. Plasma Sci.*, vol. 43, no. 10, pp. 3681–3687, Oct. 2015.

[7] S. Mao, "A high frequency high voltage power supply," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–5.

[8] J. S. Brugler, "Theoretical performance of voltage multiplier circuits," *IEEE J. Solid-State Circuits*, vol. SSC-6, no. 3, pp. 132–135, Jun. 1971.

[9] A. Shenkman, Y. Berkovich, and B. Axelrod, "Novel ac–dc and dc–dc converters with a diode-capacitor multiplier," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 40, no. 4, pp. 1286–1293, Oct. 2004.

[10] J. Sun, X. Ding, M. Nakaoka, and H. Takano, "Series resonant ZCS-PFM dc-dc converter with multistage rectified voltage multiplier and dual-mode PFM control scheme for medical-use high-voltage X-ray power generator," *IEE Proc., Electr. Power Appl.*, vol. 147, no. 6, pp. 527–534, Nov. 2000.

[11] S. Iqbal, G. K. Singh, and R. Besar, "A dual-mode input voltage modulation control scheme for voltage multiplier based X-ray power supply," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 1003–1008, Mar. 2008.

[12] S. Mao, T. Wu, X. Lu, J. Popovic, and J. A. Ferreira, "High frequency high voltage power conversion with silicon carbide power semiconductor devices," in *Proc. IEEE Electron. Syst., Integr. Technol. Conf.*, 2016, pp. 1–5.

[13] P. Lürkens, P. Guimaraes, P. Godignon, and J. Millán, "High voltage SiC Schottky diodes in rectifiers for X-ray generators," *Mater. Sci. Forum*, vols. 717–720, pp. 1245–1248, 2012.

[14] L. Katzir and D. Shmilovitz, “A 1-MHz 5-kV power supply applying SiC diodes and GaN HEMT cascode MOSFETs in soft switching,” *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1474–1482, Dec. 2016.

[15] Y. Du, J. Wang, G. Wang, and A. Q. Huang, “Modeling of the high frequency rectifier with 10-kV SiC JBS diode in high-voltage series resonant type dc-dc converters,” *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4288–4300, Aug. 2014.

[16] S. Mao, P. Zhang, J. Popovic, and J. A. Ferreira, “Diode reverse recovery analysis of Cockcroft-Walton voltage multiplier for high voltage generation,” in *Proc. IEEE 3rd Int. Future Energy Electron. Conf. ECCE Asia*, 2017, pp. 1765–1770.

[17] I. H. Kang, S. C. Kim, W. Bahng, S. J. Joo, and N. K. Kim, “Accurate extraction method of reverse recovery time and stored charge for ultrafast diodes,” *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 619–622, Feb. 2012.

[18] Z. Yao and L. Xiao, “Push-pull forward three-level converter with reduced rectifier voltage stress,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 10, pp. 2815–2821, Oct. 2010.

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