Analysis and Experimental Characterization of a Large-Bandwidth Triple-Loop Controller for Grid-Tied Inverters

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***Abstract*—This paper analyzes a large-bandwidth, triple-loop controller designed for single-phase, grid-tied, and voltage–source inverters with *LCL* output filter. The inner control loops regulate the inverter output current and the filter capacitor voltage, respectively, while the third, outer one regulates the current injected into the grid. The inner loops are given deadbeat type regulators, whose minimum response delay allows the third loop to achieve a relatively large regulation bandwidth. This organization provides several benefits, including a regulated local ac voltage, a large-bandwidth control of the power flowing to the grid, and a good robustness against different types of commonly encountered grid perturbations. In particular, grid voltage harmonic pollution, amplitude, and frequency fluctuations or connection impedance parameter variations can be tolerated without incurring into instability or unacceptable performance degradation. Besides, the proposed controller is inherently able to guarantee seamless transitions between grid-tied and islanded operation, showing good potential for application to nano- and microgrid utility interface converters.**

***Index Terms*—Deadbeat (DB) control, digital control, grid-tied inverter.**

I. Introduction

GRID-TIED inverters represent the interface with the utility grid of a wide variety of power systems, ranging from single renewable energy sources to entire microgrids [1], [2]. The basic function of grid interface converters is to regulate the active and reactive powers exchanged between the subsystem and the grid. Different ancillary functions are often required, like the capability to operate in islanded mode [3] or to ride through different kinds of faults [4]. Control strategies for grid-connected, *LCL*-filtered inverters have been the object of intensive research efforts. The numerous solutions documented in the literature can

Manuscript received January 23, 2018; revised April 20, 2018; accepted May 1, 2018. Date of publication May 9, 2018; date of current version December 7, 2018. The work of Q. Liu was supported by the Chinese Scholarship Council grant #201606290045. Recommended for publication by Associate Editor Y. W. Li. (*Corresponding author: Tommaso Caldognetto.*)

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double-loop controllers that turn the voltage–source inverter (VSI) into a controlled voltage source [13], [22]–[24]. Droop control is based on the *a priori* knowledge, or estimation, of the grid connection impedance, and operates essentially at line frequency. In general, its performance can be negatively affected by grid voltage perturbations. To tackle these problems, He *et al.* [13] have proposed to replace the conventional droop control with a frequency adaptive approach that improves the accuracy of power control when the grid frequency fluctuates.

Compared with single-loop solutions, double-loop control strategies offer superior overall performance. However, they still show evident limitations in achieving the simultaneous realization of harmonic rejection, proper resonance damping, seamless operation-mode transitions, and low-voltage ride through (LVRT) capability, that are all equally important requirements, typically addressed in the National Grid Regulation Standards.

From this standpoint, triple-loop control is a promising solution, especially for the implementation of so called multifunctional converters. In [3], the grid current, output voltage, and capacitor current are fed back, respectively, from outer to inner, forming a triple-loop control structure. It makes the converter capable of providing continuous power to critical local loads and transferring seamlessly between grid-connected and islanded operation modes. However, the dynamic performance of the grid current loop and the harmonic rejection ability of the converter are expected to be negatively affected by the long response delay of inner loops, as these are regulated by PI controllers with relatively low bandwidth. Beside that, as the converter current is not directly controlled, serious overloading can be expected if an LVRT is attempted. That is an important reason why, in [20], the control target of the innermost loop is replaced by converter current, forming another possible triple-loop organization. However, as both grid current and output voltage loops are regulated by proportional-resonant (PR) controllers, the system is potentially sensitive to weak grids where voltage sags and frequency perturbations can be frequently encountered. Additionally, the harmonic attenuation and power control performance does not seem to be competitive, again because of the long settling times associated to resonant controllers.

In conclusion, large bandwidth grid current control is the key to improve the overall performance of grid-tied inverters, especially when the microgrid interfacing is concerned. A triple-loop control strategy is, therefore, introduced in this paper, whose purpose is exactly to enable the implementation of a large-bandwidth controller for the grid current. The converter current is regulated, in the inner loop, by a DB controller achieving ideal system damping and fast inverter over-current protection. The intermediate, output voltage loop is also introduced and regulated by a predictive, DB-type controller, to guarantee seamless mode transitions as well as to provide uninterrupted high-quality voltage for critical local loads. Compared to other solutions [25], the DB controller is indeed an almost ideal choice for inner loops, offering an excellent reference tracking ability and minimum response delay. At the same time, its known sensitivity to parametric mismatches does not represent a serious problem, as the variation of system parameters is, in practice, much smaller than it takes to cause significant performance degradation [11].

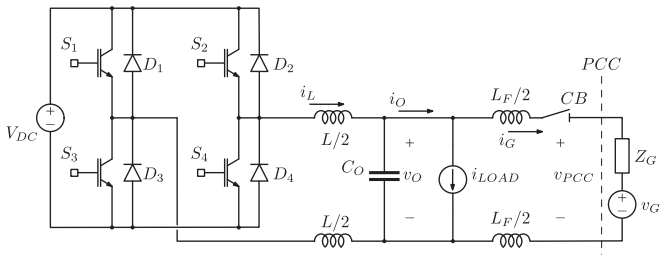

Fig. 1. Simplified schematic of the considered grid-tied power converter.

TABLE I
FULL BRIDGE VSI PARAMETERS

Parameter	Symbol	Value	
Nominal DC link voltage	V_{DC}	450	V
Switching frequency	f_{sw}	20	kHz
Filter inductance	L	1.4	mH
Equivalent series resistance	ESR_L	60	mΩ
Output capacitance	C_o	30	μF
Line inductance	L_F	0.55	mH
Equivalent series resistance	ESR_{L_F}	75	mΩ
Nominal power	S_o	3	kVA
Nominal grid voltage (RMS)	V_G	230	V

Thanks to the adoption of two nested DB type controllers, sufficient flexibility is gained to design a relatively fast PI controller (1 kHz bandwidth, equal to $1/20$ of the switching frequency) for the outer, grid current control loop. In discussing this control strategy, this paper gives the following three main contributions.

1) The analytical expression and experimental measurement of the inverter output impedance under different controllers.
2) The analysis of the inverter-grid connection stability.
3) The experimental test of the controller proposed herein on a 3kVA, grid-tied, single-phase inverter in typical operating conditions of a microgrid utility interface converter.

II. ANALYSIS OF CONVERTER/GRID CONNECTION

The stability of the connection between a grid-tied VSI and the utility grid can be discussed deriving some simple relations between the inverter output impedance and the series impedance of the grid source, $Z_G(\omega) = R_G + j\omega L_G$. The latter is, in general, only partially known and can vary significantly, which complicates the discussion to some extent. Nevertheless, stability conditions of general validity can be determined, that can be used to steer the design of the VSI control system. To this purpose, in the following, we will derive different output impedance expressions referring to the topology shown in Fig. 1, whose main parameters are listed in Table I.

Let us consider, in the first place, the case where the VSI is controlled as a voltage source. In this case, it is possible to model its small-signal behavior, as seen from the output terminals where the voltage v_O can be measured, with the series

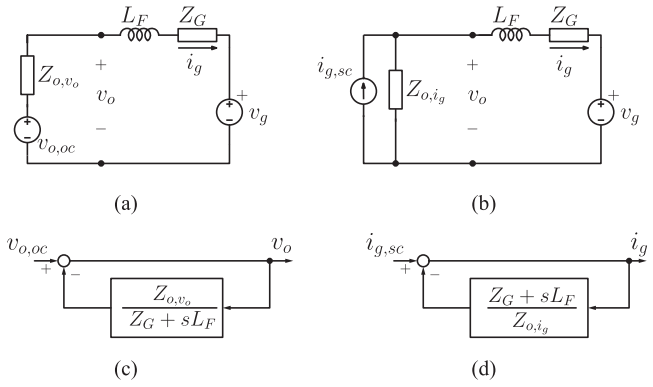

Fig. 2. Small-signal modeling of the inverter/grid connection. (a) Equivalent circuit for voltage mode control. (b) Equivalent circuit for grid current mode control. (c) Block diagram representation of (a). (d) Block diagram representation of (b).

connection of an equivalent voltage source $v_{o,\mathrm{oc}}$, generating the inverter open circuit voltage, and an equivalent output impedance Z_{o,v_o}. This is the situation described by Fig. 2(a).

The transfer function between the actual output voltage v_o and the open circuit voltage $v_{o,\mathrm{oc}}$ can be easily determined and is given by

$$\frac{v_o(s)}{v_{o,\mathrm{oc}}(s)} = \left[1 + \frac{Z_{o,v_o}}{Z_G + sL_F}\right]^{-1}. \tag{1}$$

This expression can be interpreted as the input–output, closed loop transfer function of a feedback system, as shown in Fig. 2(c). From this standpoint, according to Middlebrook's stability criterion [26], [27], the connection of the inverter with the grid is unconditionally stable if

$$|Z_{o,v_o}| < |Z_G + sL_F|. \tag{2}$$

Similarly, when the VSI is controlled as a current source, its small-signal behavior can be modeled by the parallel connection of an equivalent current source $i_{s,\mathrm{sc}}$, generating the inverter short-circuit current, and an equivalent output impedance Z_{o,i_g}. The transfer function between the grid current i_g and the short-circuit current $i_{s,\mathrm{sc}}$ is

$$\frac{i_g(s)}{i_{s,\mathrm{sc}}(s)} = \left[1 + \frac{Z_G + sL_F}{Z_{o,i_g}}\right]^{-1}. \tag{3}$$

The corresponding feedback system representation is displayed in Fig. 2(d). In this case, the connection is unconditionally stable if

$$|Z_{o,i_g}| > |Z_G + sL_F|. \tag{4}$$

In practice, (2) and (4) are often too conservative to be matched unconditionally and in a wide frequency range. Particularly critical cases are represented by possible resonances (or antiresonances) between L_F and Z_G. At resonant frequencies, to satisfy the stability conditions can be very difficult and, as a result, undesired, lightly damped modes can manifest themselves during transients or even in the steady state. Nevertheless, (2) and (4) clearly show that the design of a grid-tied inverter control system should always aim at properly shaping the converter output impedance. Indeed, the inverter/grid connection is expected to be robustly stable, even in the presence of uncertainty in Z_G, if the magnitude of the inverter output impedance is minimized, in case of voltage-controlled VSIs, or maximized, in case of current-controlled VSIs. In the following, these criteria will be applied in designing each controller of the proposed triple-loop organization. The resulting converter output impedance will be analytically derived in the frequency domain and experimentally measured. The impedance spectroscopy will allow to; first, quantify the controller's performance in a relatively simple and repeatable manner; second, quantitatively compare different control options, allowing to choose the highest performing regulator for each loop.

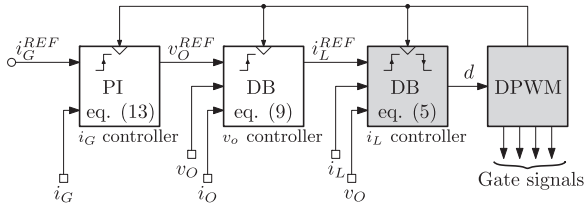

Fig. 3. Proposed triple-loop controller architecture. A symmetrical DPWM triggers signal sampling and computation of the indicated control equations. The FPGA implementation allows concurrent calculation of the three controllers.

III. Converter Control Strategy

The organization of the proposed controller is shown in Fig. 3. This architecture has the following advantages.

1) It guarantees high voltage quality to local loads, thanks to the v_O voltage control loop.
2) It employs a simple *LCL* output filter, commonly adopted in grid-tied converters [28].
3) It enables the seamless transition between grid-tied and islanded operations, thanks to the grid current i_G controller.

The down side is represented by the need for three current sensors and a voltage sensor. However, only the sensor of inductor current i_L needs to be of high quality, in terms of bandwidth and accuracy. The output current i_O and grid current i_G sensors, instead, operate on naturally filtered signals, which makes their bandwidth requirements much less demanding (a few kHz can perfectly do). As a consequence, they are not expected to significantly increase the overall cost of the system. The use of estimation techniques, especially for the load or the grid current [29], can also be considered, but will not be discussed in this paper.

In principle, a variety of regulators can be adopted for each control loop. Choosing among the various options is often a matter of designer's experience and preference. To make the design process somewhat less arbitrary, the above discussed impedance optimization criterion will be used in this paper, aimed at deriving a solidly built, robustly performing solution.

A. Inductor Current Controller

The inductor current controller and modulator organizations considered here (indicated by the shaded boxes in Fig. 3) replicate those presented in [11], as they offer excellent dynamic

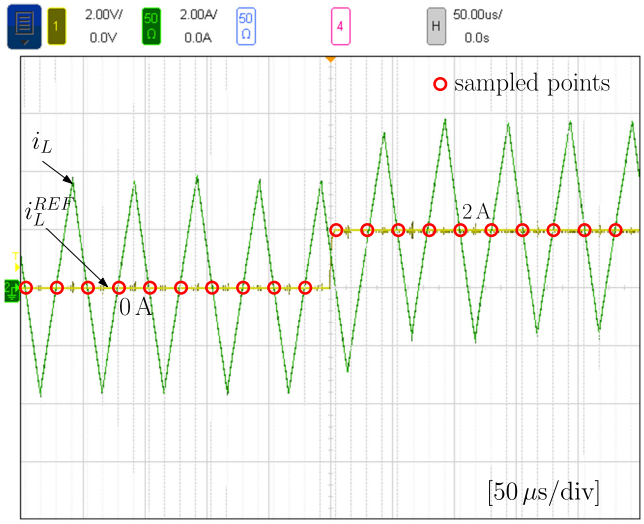

Fig. 4. Small-signal step response of the inductor current controller. The sampling instants are indicated to show that the error correction takes only one sampling period ($T = T_{sw}/2$), measured from the first sample after the step.

performance, in both small-signal and large-signal terms. As we will show in Section IV, they also guarantee the converter output impedance is maximized in a wide frequency range. The controller is designed to be realized in a hardware form, on an FPGA chip, so that the computation time is reduced to a negligible fraction of the switching period (34 ns, in our specific implementation), and the duty-cycle can be adjusted *twice per modulation period*. As is explained in [11], at each control iteration, the following *duty-cycle update* equation is computed:

$$d(k) = \frac{L f_{sw}}{V_{\rm dc}} \cdot \left[i_L^{\rm REF}(k) - i_L(k) \right] + \frac{v_O(k)}{2V_{\rm dc}} + \frac{1}{2}. \qquad (5)$$

The discrete-time, closed-loop transfer function W_{i_L} between the current reference $i_L^{\rm REF}$ and the inductor current i_L can be determined from (5) and the zero-order-hold (ZOH) discretization of inductor L dynamic equation, yielding

$$W_{i_L}(z) = \frac{I_L(z)}{I_L^{\rm REF}(z)} = z^{-1}. \qquad (6)$$

The result is exactly equal to a one-sampling-period delay, where the sampling period equals *one half of the modulation period* [i.e., $T_{sw}/2 = 1/(2f_{sw})$]. Therefore, this current controller guarantees a DB type dynamics with the minimum response delay ($T = T_{sw}/2$). For clarity, the experimental measurement of the inductor current loop step response is shown in Fig. 4.

B. Output Voltage Controller

A DB type controller is adopted to regulate v_O as well, aiming at achieving a large regulation bandwidth and a limited response delay. For the current controller, the synchronization between the symmetrical modulation carrier and the sampling process allows the average inductor current value to be exactly acquired at the beginning and at the middle of each modulation period, independently from the particular duty-cycle value or load condition, as is shown in Fig. 5.

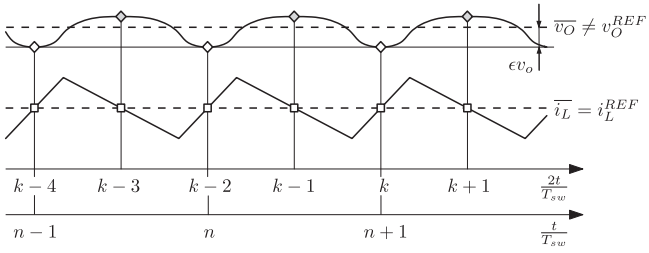

Fig. 5. Voltage and current sampling processes. White squares indicate the ideal sampling instants of i_L. Diamonds indicate the v_O samples.

Unfortunately, the exact value of the average output voltage cannot be acquired as easily, since there is not a fixed position within the sampling period where this can be found at all times and in any condition. Because it is not practical to track its ideal sampling instant, the output voltage is sampled synchronously with the converter current, even if that generates a (small) error, indicated as ϵv_O in Fig. 5. It is worth recalling that the output voltage ripple at the switching frequency is typically very small (0.55 V in the considered setup), so that ϵv_O is almost undetectable.

More importantly, the iteration period of the voltage controller cannot be equal to that of the current controller. Indeed, if two equally spaced voltage samples were taken in each modulation period, as is done for the current signal, the regulation error would unavoidably turn into a sequence of alternating positive and negative values, even in the steady state. Even if the inner loop maintained a stable operation, this would result in continuous adjustments of the current reference $i_L^{\rm REF}$ and a persistent limit cycle oscillation would be generated. To prevent that, only a single sample per period can be taken. In the implementation considered in this paper, only those samples indicated by white diamonds in Fig. 5 are actually acquired.

The voltage controller equation is now derived, assuming the inner current loop to be accurately described by (6) and neglecting again the calculation delay. That is possible because the voltage controller is realized on the same FPGA chip that executes the current control algorithm, which allows their concurrent calculation. Let us consider the discrete-time, ZOH approximation of the output voltage dynamic equation, calculated along two consecutive sampling periods of $T_{sw}/2$ duration

$$\begin{aligned} v_O(k+1) = \; & v_O(k-1) + \frac{1}{2C_O f_{sw}} \cdot \left[\overline{i_L(k)} + \overline{i_L(k-1)} \right] \\ & - \frac{1}{2C_O f_{sw}} \cdot \left[i_O(k) + i_O(k-1) \right]. \end{aligned} \qquad (7)$$

Being the average inductor current equal to its one-step-delayed reference, as per (6), and assuming the output current i_O not to vary significantly in, at least, two consecutive sampling periods, (7) can be simplified and rewritten, yielding

$$v_O(n+1) = v_O(n) + \frac{1}{C_O f_{sw}} \cdot \left[i_L^{\rm REF}(n) - i_O(n) \right] \qquad (8)$$

where the index n is updated *just once* per modulation period. Thus written, (8) represents the down-sampled (by a factor 2)

dynamic equation of the inverter output voltage, from which the following control equation can be derived:

$$i_L^{\mathrm{REF}}(n) = C_O f_{sw} \cdot \left[v_O^{\mathrm{REF}}(n) - v_O(n)\right] + i_O(n) \qquad (9)$$

where we assumed $v_O(n+1) = v_O^{\mathrm{REF}}(n)$. The down-sampling applied to (7) means that, from the standpoint of the inner current control algorithm, i_L^{REF} is invariant in two consecutive sampling periods of $T_{sw}/2$ duration, resulting in the following identity:

$$\overline{i_L(k)} = \overline{i_L(k-1)} = i_L^{\mathrm{REF}}(k-2) \qquad (10)$$

which was implicitly used in the derivation of (8). Please note that (8) is obtained integrating the output capacitor current during any two consecutive time intervals when the *average inductor current is stationary*.

Based on (7), it is possible to determine the closed loop transfer function between the output voltage and its reference. As can be inferred from the above derivation, the procedure requires some tricky rearrangement of the control equations, due to different sampling rates of the inner current loop and the outer voltage loop. An approximate solution can be found resampling (9) and integrating the output capacitor current during any two successive sampling periods, where the *current reference* i_L^{REF} *is stationary*. The dynamic equation for the output voltage then becomes

$$\begin{aligned} v_O(k+2) = v_O(k) &+ \frac{1}{2}\left[v_O^{\mathrm{REF}}(k) + v_O^{\mathrm{REF}}(k-1)\right] \\ &- \frac{1}{2}\left[v_O(k) + v_O(k-1)\right] \\ &+ \frac{1}{2C_O f_{sw}}\left[i_O(k-1) - i_O(k+1)\right]. \end{aligned} \qquad (11)$$

By $\mathcal{Z}$-transforming (11), after few mathematical manipulations, the small-signal transfer function is found to be equal to

$$W_{v_O}(z) = \frac{V_O(z)}{V_O^{\mathrm{REF}}(z)} = \frac{1}{2z^2 - 2z + 1}. \qquad (12)$$

It is worth noting that, differently from (6), the function $W_{v_O}(z)$ is not the pure z^{-2} delay one would expect. This is due to the dynamic interaction between the inner current control loop and the outer voltage control loop operating at different sampling rates. Because of that, the prediction of the output voltage trajectory that is used to derive the control law (9) is only approximated and the closed loop transfer function cannot be exactly a DB. Nevertheless, the practical consequence is very limited, as it is possible to see in Fig. 6. The figure shows the controller's response to a step reference variation from 50 to 10 V (peak), when the converter is operating with just the two inner control loops closed and with a distorting load applied at the output. As can be seen in Fig. 6(a), voltage v_O tracks the reference almost ideally, reaching the new set-point very rapidly and with no undesired transients. The steady-state tracking delay is shown in detail in Fig. 6(b), where it is possible to verify that it matches the expected single period duration ($T = T_{sw}$). This result is important because a small response delay allows the maximization of the third loop bandwidth and, as will be shown in Section IV, a significant output impedance reduction in a wide frequency range.

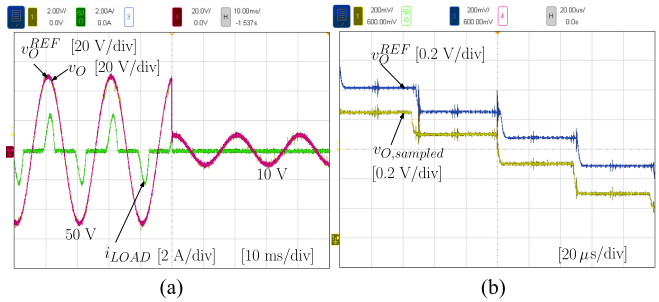

Fig. 6. (a) Step response of the output voltage loop from 50 to 10 V peak amplitude, when a distorting load is applied. (b) Comparison of sampled reference and output voltage signals, showing the expected one-sampling-period delay. One of the available DACs of the control hardware is used to output the data read from memory.

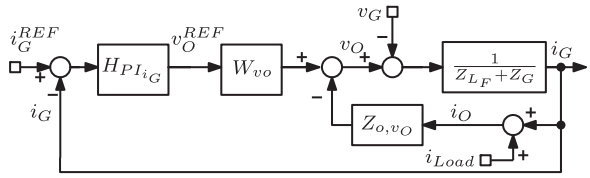

Fig. 7. Small-signal block-diagram of the proposed triple-loop controller.

C. Sensitivity to Parameter Mismatches

Predictive controllers can be negatively affected by *parameter mismatches*, that is, by differences between the physical system's and the control model's parameters. However, as is discussed in several past papers, beginning with [29], we statements conclude the following conditions.

1) When the converter output voltage v_O is measured, the DB control of the inverter inductor current i_L is actually very robust. Closed loop eigenvalues move outside the unity circle only when the model inductor is twice as large as the physical inductor. It is also shown that the opposite mismatch (where the physical inductor is larger) is a less critical condition.
2) In the case of voltage loop controllers, when the converter output current i_O is measured, a similar robustness is achieved, this time with respect to the output capacitor value.

It is important to underline those minor mismatches, in any case, just cause the loss of the ideal DB response, not the loss of stability. Because the considered organization satisfies the above conditions, the stability of the current and voltage controllers is expected to be quite robust. In Section V, such robustness will be experimentally verified in a case of great practical relevance.

D. Grid Current Loop

The grid current i_G is sampled once per switching period, synchronized with the output voltage v_O. Considering the expected uncertainty in the grid impedance parameters, a simple PI controller is adopted for the grid current loop. Indeed, the PI structure ensures a reasonably robust stability, once the loop phase margin is adequately oversized. The complete small-signal block-diagram of the controller is shown in Fig. 7.

Based on that, the control equation can be written as

$$V_O^{\text{REF}}(z) = H_{PI_{i_G}}(z)(I_G^{\text{REF}}(z) - I_G(z)) \tag{13}$$

where $H_{\text{PI}_{i_G}}(z) = Kp_{i_G} + Ki_{i_G} \cdot \dfrac{z}{z-1}$ is the PI controller's discrete-time transfer function. Accordingly, the open loop gain is given by

$$T_{i_G}(z) = H_{\text{PI}_{i_G}}(z) W_{v_O}(z) \frac{1}{Z_{o,v_O}(z) + Z_G(z) + Z_{L_F}(z)} \tag{14}$$

where Z_{o,v_O} is the inverter output impedance when inductor current and output voltage loops are both closed, while Z_{L_F} and Z_G are the grid interfacing inductor impedance and the grid impedance, respectively. All impedances are specified in the discrete time domain, as will be explained in Section IV. In particular, the analytical derivation of Z_{o,v_O} will be presented in Section IV-B. Based on that and on the knowledge of the grid interfacing inductor L_F, the PI controller can be designed to meet specified bandwidth and phase margin values. The grid impedance Z_G is considered negligible in this design, assuming the converter is connected to an ideal grid. As will be shown in Section IV-C, a satisfactory robustness against Z_G parameters variations can be achieved by the PI controller, making the ideal grid assumption not critical.

IV. Output Impedance Analysis

As discussed in Sections II and III, the optimal shaping of the converter's output impedance in the frequency domain is the criterion adopted to steer the whole control system design. In this section, we derive the analytical expressions of the converter output impedance as determined by the proposed control system in Fig. 3. We also verify the results by numerical simulations and direct measurements. Both simulations and measurements are performed as is illustrated in Fig. 8, namely, by injecting a perturbation signal and measuring the appropriate voltage and current signals at different frequencies. The frequency of the injected perturbation signal spans the range [0.1, 10] kHz. At low frequencies, an ac power supply is used, while the power operational amplifier PA107DP is employed above 1 kHz. It is worth noting that, in the literature, the converter output impedance is most often analyzed in the $\mathcal{S}$-domain, that is, using Laplace transform [30]–[34]. This approach is not applicable to digital controllers that have no continuous-time counterpart, like DB controllers. As known, these can only be approximately described in the continuous time domain, yielding inaccurate results, especially close to Nyquist frequency. On the contrary, the discrete-time analysis here performed perfectly matches the discrete-time controller nature and, as a consequence, provides more accurate results.

A. Inductor Current Loop

Even if the converter shown in Fig. 1 is not going to be controlled just by the single inductor current loop, the study of its output impedance is now presented, both for completeness and to further validate the analysis of the controller's dynamic response. Based on (5), the output impedance expression for the current DB controller, Z_{o,i_L}, is easily derived as

$$Z_{o,i_L}(z) = -\frac{V_O(z)}{I_L(z)} = \frac{4 f_{sw} L}{1 - z^{-1}}. \tag{15}$$

The form of (15), that corresponds to a discrete-time integral function, reveals that the output impedance is capacitive in nature, at least up to Nyquist frequency. It is easy to determine the equivalent capacitor corresponding to the same impedance. That turns to be very small, being equal to $C_{i_{L\,\text{eq}}} = 1/(8 f_{sw}^2 L) \cong 224$ nF in our setup. Fig. 9 compares the results given by (15), the results from an accurate simulation model, and the measurements from the experimental implementation of the system in Fig. 1, performed as shown in Fig. 8(a).

It is worth noting that, according to (15), Z_{o,i_L} is extremely high, which makes its measurement very sensitive to the effects of all possible nonidealities in the final implementation. For this reason, the validity of (15) is here proven by showing both the results marked as "simulation ideal," that refer to a simulation model, where the controller is fed with the *exact* values of i_L and v_O, and the results marked as "simulation with delays," that refer to a slightly more complex model, where the delays due to the analog denoising filters of i_L and v_O are included, as detailed in Table II. Notably, these small delays have a significant effect on the measured output impedance.

Even if lower than in the ideal case, the measured output impedance is still very high. In magnitude, it is higher than the converter physical impedance, ωL, even at the maximum test

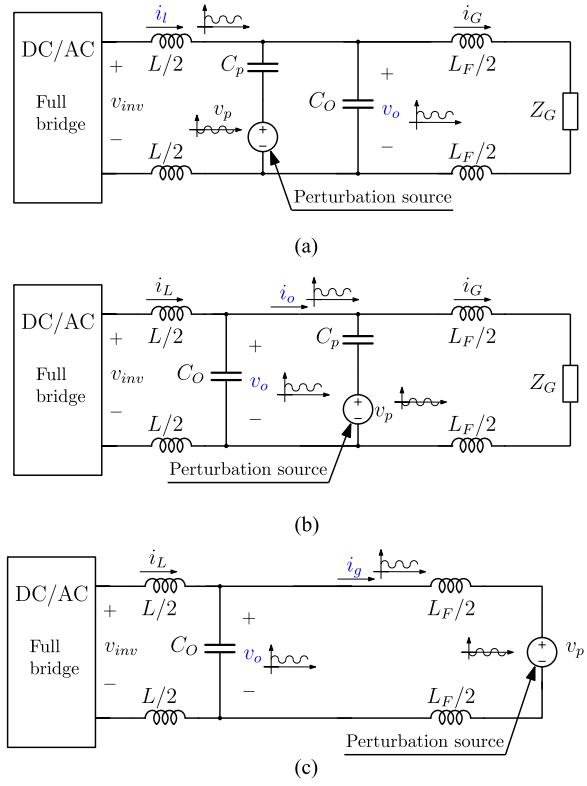

Fig. 8. Measurement of the converter output impedance with different controllers. The highlighted small-signal quantities are the ones considered to derive the output impedance spectrum. (a) Inductor current (i_L) loop is closed. (b) Output voltage (v_O) loop is closed. (c) Grid current (i_G) loop is closed.

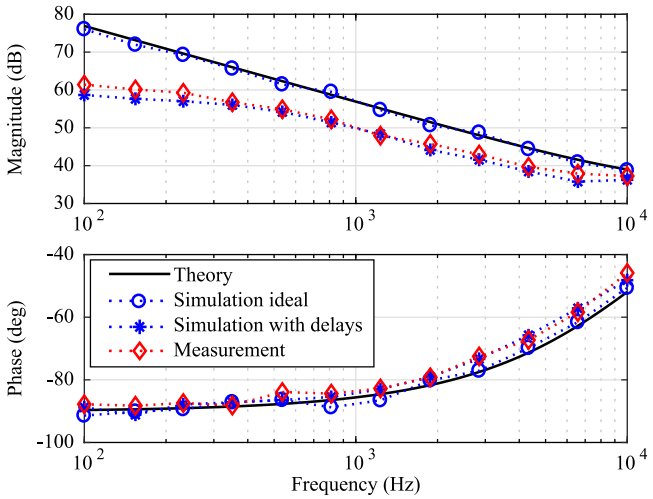

Fig. 9. Converter output impedance, in magnitude and phase, when only inductor current loop is closed.

TABLE II
SIGNAL SENSING BANDWIDTHS

Signals	Filter cutoff frequency	Unit
Inductor current, i_L	50	kHz
Output current, i_O	10	kHz
Grid current, i_G	10	kHz
Output voltage, v_O	8	kHz

frequency. This is due to the extremely large bandwidth of the current controller.

B. Output Voltage Loop

When also the voltage control loop is closed, the converter can be modeled as in Fig. 2(a). The resulting control structure, featuring two nested DB type controllers, is denoted here as DB–DB. The output impedance resulting from this control structure is now analyzed. It can be determined by $\mathcal{Z}$-transforming (11) and extracting the small-signal dynamic relation between the output voltage and the output current. After a few mathematical manipulations, we find

$$Z_{o,v_O}(z) = -\frac{V_O(z)}{I_O(z)} = \frac{1}{C_O f_{sw}} \cdot \frac{z-1}{2z^2-2z+1}. \tag{16}$$

It is interesting to determine the low frequency and high frequency asymptotic approximations of Z_{o,v_o} in the *continuous time domain.* As far as the former is concerned, we find that

$$Z^{\text{LF}}_{o,v_O} \approx \frac{C_O^{-1} f_{sw}^{-1}\left(1+\frac{T_{sw}}{2}s-1\right)}{2(1+T_{sw}s)-2(1+\frac{T_{sw}}{2}s)+1} \approx \frac{s}{2C_O f_{sw}^2} \tag{17}$$

where a first-order Taylor series approximation is used, while the latter is found to be

$$Z^{\text{HF}}_{o,v_O} \approx \frac{1}{C_O f_{sw}} \cdot \frac{1}{2(z-1)} \approx \frac{1}{C_O s} \tag{18}$$

using the backward Euler approximation of the integral function. It is therefore proven that, at low frequencies, the converter output impedance presents an approximately inductive behavior, with equivalent inductance value $L_{v_{o\text{eq}}} = 1/(2C_O f_{sw}^2)$. At high frequencies, instead, the converter output impedance is capacitive, with equivalent value $C_{v_{o\text{eq}}} = C_O$, as it could be expected. The intersection frequency f^* of the two asymptotes is

$$f^* = \frac{1}{2\pi \cdot \sqrt{L_{\text{eq}} \cdot C_{\text{eq}}}} = \frac{f_{sw}}{\sqrt{2}\pi} \tag{19}$$

which is equal to 4.50 kHz in the considered setup. To better highlight the advantages of the DB–DB controller, this is now compared to a DB–PI controller, that is, a controller that employs the same DB regulator (5) for i_L, but a standard PI regulator to control v_O. It is possible to calculate the converter output impedance Z'_{o,v_O} and closed loop transfer function W'_{v_O} determined by the DB–PI controller. These are given by

$$Z'_{o,v_O}(z) = -\frac{V_O(z)}{I_O(z)} = \frac{\frac{1}{2C_O \cdot f_{sw}} \cdot \frac{z}{z-1}}{1+\frac{H_{\text{PI}v_o}(z)}{2C_O \cdot f_{sw}} \cdot \frac{1}{z-1}} \tag{20}$$

$$W'_{v_O}(z) = \frac{V_O(z)}{V_O^{\text{REF}}(z)} = \frac{\frac{H_{\text{PI}v_o}(z)}{2C_O \cdot f_{sw}} \cdot \frac{1}{z-1}}{1+\frac{H_{\text{PI}v_O}(z)}{2C_O \cdot f_{sw}} \cdot \frac{1}{z-1}} \tag{21}$$

where $H_{\text{PI}v_O}(z) = Kp_{v_O} + Ki_{v_O} \cdot \frac{z}{z-1}$ is the discrete-time transfer function of the output voltage PI controller. For a fair comparison, the PI gains are chosen to achieve a relatively large crossover frequency, equal to 1.5 kHz, and a 60° phase margin. Actually, with the parameters of Table I and the considered phase margin, 1.5 kHz represents the largest possible bandwidth. The asymptotes of the converter output impedance are derived in this case too: at low frequency, the output impedance shows again an inductive behavior, corresponding to an equivalent inductance $L'_{v_{o\text{eq}}} = 1/Ki_{v_O}$; at high frequency, the output impedance shows the expected capacitive behavior, corresponding to capacitance C_O. The corresponding intersection frequency is now $f'^* = \sqrt{Ki_{v_O} f_{sw}/C_O}/2\pi$, which is equal to 0.82 kHz with the considered parameter values.

Fig. 10 displays the converter output impedance in DB–DB and DB–PI cases. First, the figure shows a close match between the obtained analytical, simulation, and experimental results, which validates the expressions (16) and (20). Moreover, comparing Fig. 10(a) and (b), one sees that the DB–DB controller allows to significantly decrease the converter output impedance with respect to the DB–PI one in a wide frequency range. As an example, at 1 kHz, the DB–PI impedance magnitude is more than 20 dB larger than the DB–DB's. This result proves that a DB controller in the voltage loop is, by far, a better choice with respect to a PI controller. This holds also for other types of widely adopted linear voltage controllers, like the PR ones. Indeed, replacing the integrator with a bank of resonant filters boosts the loop gain, reducing the output impedance, only at the resonance frequencies, but everywhere else worsens the gain

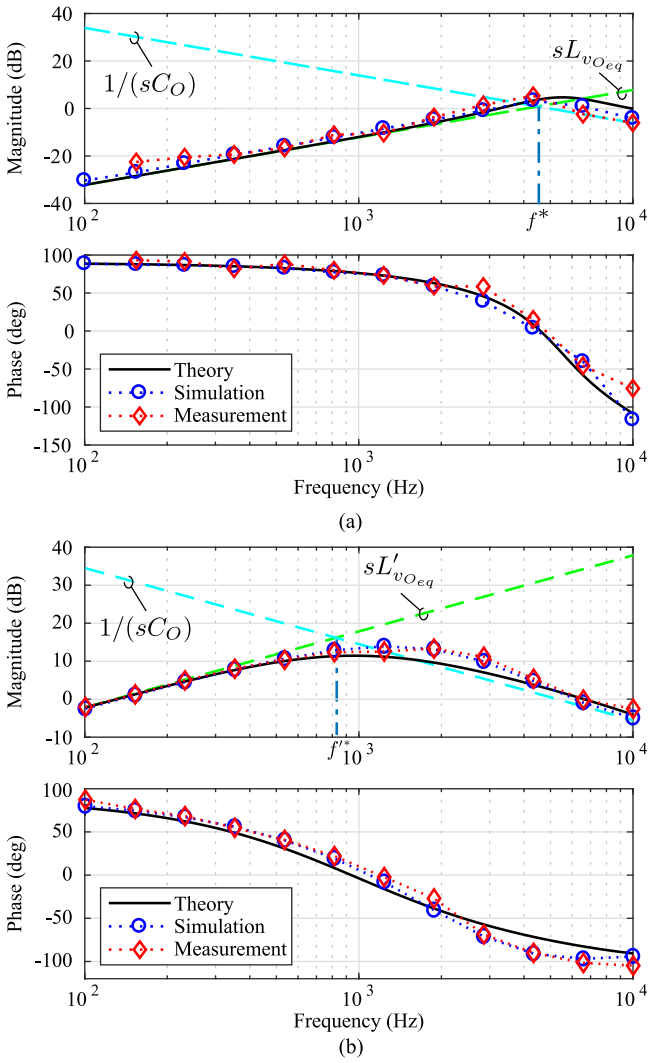

Fig. 10. Converter output impedance when inductor current i_L and capacitor voltage v_O loops are both closed. The low and high frequency asymptotes, $sL_{v_{O\,\mathrm{eq}}}$, $sL'_{v_{O\,\mathrm{eq}}}$, and $1/(sC_O)$ are indicated by dashed lines. (a) DB–DB control system. (b) DB–PI control system.

of the controller. Furthermore, the settling time of the resonant filters is unavoidably tradedoff against their selectivity, which makes it impossible to simultaneously achieve high gain and fast response. The proposed solution instead guarantees a minimum delay response and high gain in the whole low frequency region.

As a further assessment, the bandwidth of the closed loop transfer function W_{v_O} has been determined for the two controllers, finding it equal to 1.5 kHz for the DB–PI and to 7.9 kHz for the DB–DB. Clearly, the wider small-signal bandwidth of the DB–DB solution ensures an easier design of the third control loop (i.e., the i_G control loop), as is discussed in the following section.

C. Grid Current Loop

As explained in Section III-D, a PI controller is adopted for the outer, grid current i_G control loop. Differently from the inner loops, the external controller's design needs to cope with significant uncertainties in the grid impedance, Z_G. As known, a PI controller is, in principle, capable of ensuring robust stability, provided that the loop phase margin is adequately oversized. The final triple-loop controller is denoted as DB–DB–PI or DB–PI–PI, based on whether the DB or the PI controller is adopted for output voltage control, the latter being considered only as the benchmark of a high performance conventional design. The third control loop turns the converter again into a controlled current source, that can be represented by the equivalent circuit of Fig. 2(b).

According to (4), the equivalent converter output impedance should be as large as possible. The impedance has been derived both for the DB–DB–PI and the DB–PI–PI case, yielding respectively

$$\begin{aligned} Z_{o,i_G}(z) &= -\frac{V_O(z)}{I_G(z)} = W_{v_O}(z)\cdot H_{\mathrm{PI}_{i_G}}(z) + Z_{o,v_O}(z) \\ &= \frac{1}{C_O f_{sw}}\cdot\frac{C_O f_{sw}\cdot H_{\mathrm{PI}_{i_G}}(z) + z - 1}{2z^2 - 2z + 1} \end{aligned} \tag{22}$$

$$\begin{aligned} Z'_{o,i_G}(z) &= -\frac{V_O(z)}{I_G(z)} = W'_{v_O}(z)\cdot H_{\mathrm{PI}_{i_G}}(z) + Z'_{o,v_O}(z) \\ &= \frac{\dfrac{1}{2C_O\cdot f_{sw}}\left[H_{\mathrm{PI}v_O}(z)\cdot\dfrac{H_{\mathrm{PI}_{i_G}}(z)}{z-1} + \dfrac{z}{z-1}\right]}{1 + \dfrac{1}{2C_O\cdot f_{sw}}\cdot H_{\mathrm{PI}v_O}(z)\cdot\dfrac{1}{z-1}}. \end{aligned} \tag{23}$$

Fig. 11 shows the simulation and experimental results for both cases. The maximum achievable bandwidth of the third loop, given a target 60° phase margin, is 1.5 and 260 Hz in the DB–DB–PI and in the DB–PI–PI case, respectively. Please note that the design assumed $R_G = 0\,\mathrm{m\Omega}$, $L_G = 0\,\mathrm{mH}$, that is, an ideal connection to the grid. The obtained theoretical, simulation, and experimental results are consistent among each other. By comparing Fig. 11(a) and (b), it is possible to remark that the output impedance with the DB–DB–PI case is significantly higher than that of the DB–PI–PI case. As a consequence of (4), the former is expected to be capable of higher robustness and performance for any given operating condition.

To verify that, a simple robustness analysis of the third loop PI controller for different values of the grid impedance is illustrated in Fig. 12. The plots show how the controller phase margin degrades as R_G and L_G increase. For a fair comparison, the PI controller has been designed for the same 260 Hz bandwidth, both in the DB–DB–PI and in the DB–PI–PI case. As can be seen, the 30° phase margin, assumed as a lower limit for an acceptable dynamic response, is crossed by the DB–DB–PI controller at significantly higher values of both R_G and L_G, showing the following main expected features: first, better robustness to line impedance parameter variations, and second, capability to offer stable operation and limited performance penalization in the presence of weak grids [35]. Two examples of the controller's time domain behavior are given in Fig. 13, where the measured step response of current i_G are shown. In both cases, the values of R_G and L_G are 0.5 Ω and 6 mH,

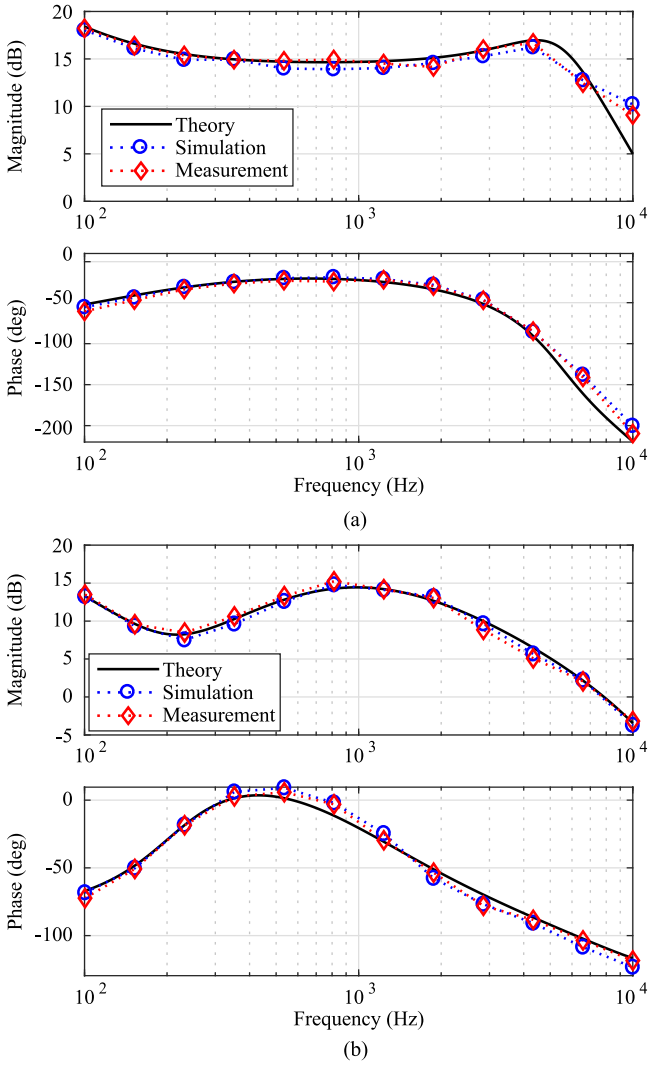

Fig. 11. Converter output impedance when grid current loop is closed. (a) DB–DB–PI control system. (b) DB–PI–PI control system.

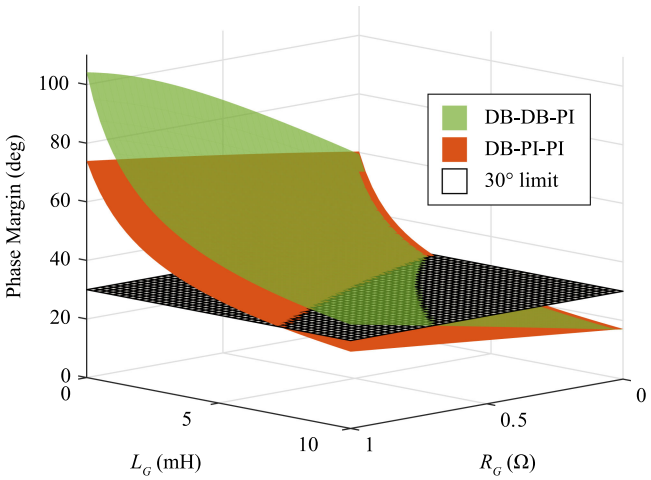

Fig. 12. Phase margin of the grid current control loop as a function of the grid connection parameters for a constant 260 Hz bandwidth.

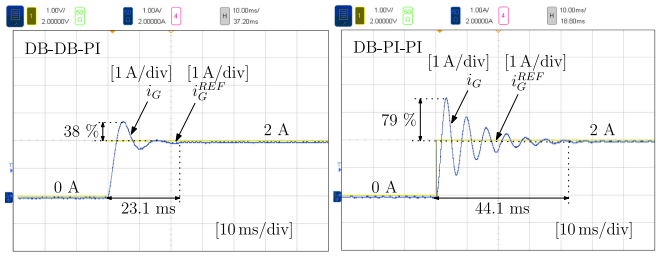

Fig. 13. Step response test for the grid current i_G when values of R_G and L_G are 0.5 Ω and 6 mH, respectively. PI target bandwidth and phase margin are 260 Hz and 60°, respectively.

respectively, representing a relatively large parameter deviation from the design values (both equal to 0). As can be seen, the DB–DB–PI solution shows a significantly better performance, in terms of overshoot and settling time, as compared to the DB–PI–PI case.

V. Experimental Validation

The results presented in Section IV show that the DB–DB–PI control structure allows to achieve a large-bandwidth control of the grid current i_G and a high impedance seen at the point of connection (i.e., PCC) with the grid. These features bring forth the following benefits.

1) Excellent dynamic performance in controlling the grid current.
2) Enhanced robustness of the inverter/grid connection.
3) Good rejection of grid voltage distortions and, consequently, harmonic current circulation.
4) Improved performance under perturbed grid conditions (e.g., amplitude fluctuations and frequency variations).

In addition, the presence of a large-bandwidth v_O voltage controller in the second loop, allows seamless transitions between grid-tied and islanded operation modes.

These characteristics are now verified experimentally on a 3-kVA, grid-tied inverter, whose setup exactly matches Fig. 1, with the parameters listed in Table I. The control system is implemented in a NI cRIO-9068, which is based on a Xilinx Zynq 7020 all programmable system on chip (AP-SoC) and equipped with suitable NI C Series Modules to allow analog and digital input/output. Inductance current i_L, output voltage v_O, output current i_O, and grid current i_G are sensed by a custom interfacing board, equipped with LEM current and voltage sensors and proper conditioning circuits, and then provided to the AP-SoC through an NI 9223 module. The control algorithm is implemented in the FPGA of the AP-SoC, while parameter setting and monitoring functions are performed by a human machine interface executed on the general purpose processor of the AP-SoC. The control system is programmed and managed by means of NI LabVIEW™. The tests reported in the following refer to the control system configured as in Table III.

A. Dynamic Response of Grid Current Loop

To illustrate the dynamic tracking performance of the injected grid current i_G, the response of the system to step changes of

TABLE III
CONTROLLER PARAMETERS

Loop	Type	Parameter	Symbol	Value
i_L	DB	i_L error gain	$L\,f_{sw}/V_{DC}$	0.0622
		v_O gain	$V_{DC}/2$	0.0011
		closed loop gain	W_{i_L}	z^{-1}
v_O	DB	v_O error gain	$C_O \cdot f_{sw}$	0.6
		bandwidth (kHz)	BW_{v_O}	7.94
i_G	PI	proportional gain	Kp_{i_G}	5
		integral gain	Ki_{i_G}	0.43
		bandwidth (kHz)	BW_{i_G}	1
		phase margin (°)	PM_{i_G}	60

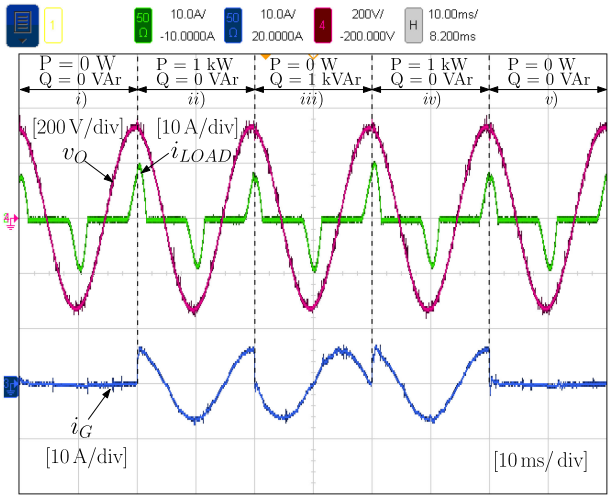

Fig. 14. Dynamic response. i) Zero power exchange. ii) 1 kW pure active power injection. iii) 1 kVAr pure reactive power injection. iv) 1 kW pure active power injection. v) Zero power exchange.

the current reference i_G^{REF} is considered in Fig. 14. In this test, a nonlinear load (NLL), represented by a diode rectifier with a large capacitive filter (the measured current crest factor is 2.6), is connected in parallel with capacitor C_O.

The current reference is set to apply, at grid voltage peaks, step changes of the power injected into the grid. Specifically, the following sequence of power references is considered: i) zero power exchange, ii) 1 kW pure active power injection, iii) 1 kvar pure reactive power injection, and iv) zero power exchange. The current quality under the working condition of pure active or reactive power injection is also evaluated by extending the testing time of phases ii) and iii), respectively. With the NLL connected ($\text{THD}_{i_{\text{Load}}} = 96.4\%$, RMS current is 2.8 A), the proposed triple-loop controller still achieves low-distortion current injection as well as a firm supply to the local loads. In case ii), the total harmonic distortion (THD) values of the output voltage and the grid current are 0.47% and 1.33%, respectively; in case iii), THD_{v_O} equals 0.48% and THD_{i_G} equals 1.25%.

Zoomed-in views of the transitions are shown in Fig. 15. As can be seen, grid current i_G reaches its new reference within 450 μs with no significant overshoot. At the same time, the local

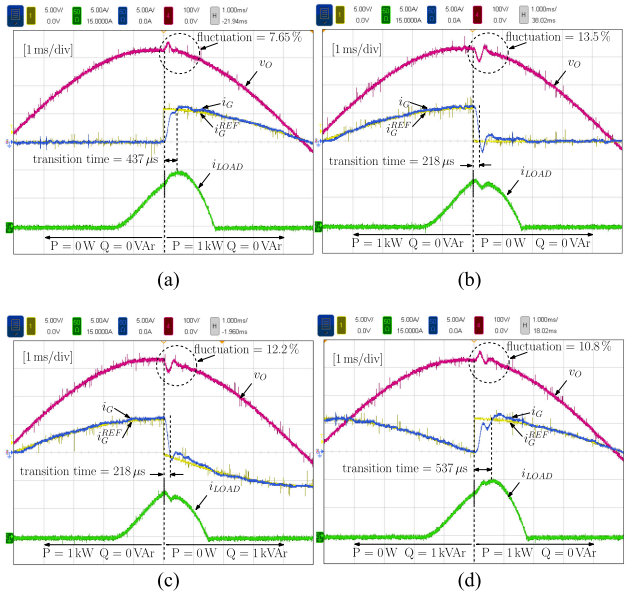

Fig. 15. Zoomed-in views of the transients in Fig. 14. (a) Step up. (b) Step down. (c) From active to reactive power. (d) From reactive to active power.

voltage v_O is almost unaffected by the current step changes; we measured a maximum voltage fluctuation equal to 13.5% of peak voltage, that is rapidly dampened. In all cases, i_G shows very little sensitivity to the NLL current and so does voltage v_O. The latter is a particularly interesting result considering that, when the diode bridge is conducting, a large mismatch is created between the modeled capacitance C_O and the total load capacitance, that becomes more than 50 times larger. Despite that, the voltage does not show any particular deviation from the desired sinusoidal trajectory. As mentioned above, the result is made possible by the decoupling action of current i_O measurement. That, together with the controller's very small response delay, makes the voltage loop practically insensitive to external disturbances and yields the observed robustness with respect to parameter variations.

B. *Distortions Attenuation Ability*

The proposed triple-loop control strategy is capable of significantly attenuating grid current harmonics, either injected by the local NNLs connected at the converter-side or due to grid voltage distortions. This feature is tested by considering two distinct situations, namely, a *stiff grid* connection and a *weak grid* connection.

In the former situation, the grid voltage presents very low distortion and is quite insensitive to the injected current. Nevertheless, in order to minimize the grid current RMS and prevent harmonic pollution, it is recommendable that the possible harmonic currents generated by local distorting loads are filtered by the converter. This feature is tested by connecting an NLL (same as in the test of Section V-A). The experiment is performed in two different cases: first, no power injection at the PCC and second, $P = 1.5$ kW active power injection at the PCC.

Fig. 16 shows the obtained results. In Fig. 16(a) it is possible to see, in particular, that the grid current i_G stays almost equal

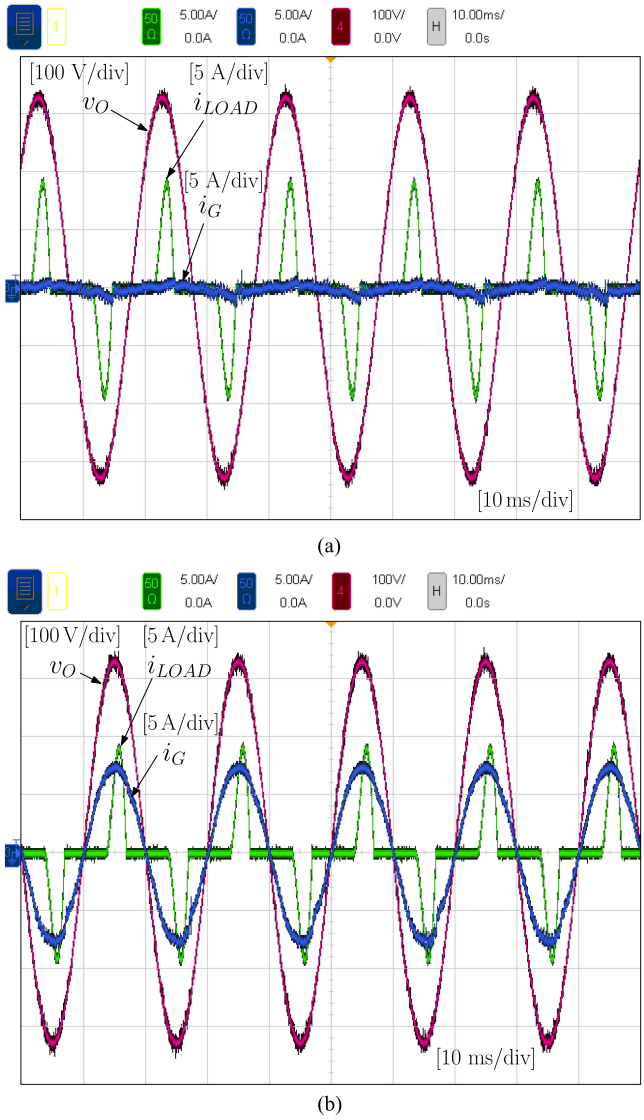

Fig. 16. Converter performance when connected to a stiff grid and supplying a local NLL. (a) $P = 0\,\text{W}$, $Q = 0\,\text{var}$. (b) $P = 1.5\,\text{kW}$, $Q = 0\,\text{var}$.

TABLE IV
HARMONIC COMPENSATION PERFORMANCE UNDER STIFF GRID

THD(%)	v_{PCC}	i_G	v_O	i_{LOAD}
no local load	0.94	-	1.04	-
$P = 0\,\text{W}$, $Q = 0\,\text{VAr}$	0.95	-	1.07	107
$P = 1.5\,\text{kW}$, $Q = 0\,\text{VAr}$	0.95	1.79	1.10	107

to zero, with a small effect of the NLL. The local load voltage v_O is accordingly almost unaffected. The same can be said for Fig. 16(b), where, in addition, an almost sinusoidal grid current i_G is visible. Table IV displays the measured THD values for all waveforms of Fig. 16 and v_{PCC}.

First of all, the THD for v_{PCC} and v_O is measured in no-load conditions, and turns out to be equal to 0.94 % and 1.04 %, respectively. When the NLL is connected, the THD of i_{LOAD} is equal to 107 % both in case i) and in case ii). The corresponding measured output voltage THD are 1.07 % and 1.10 %, showing

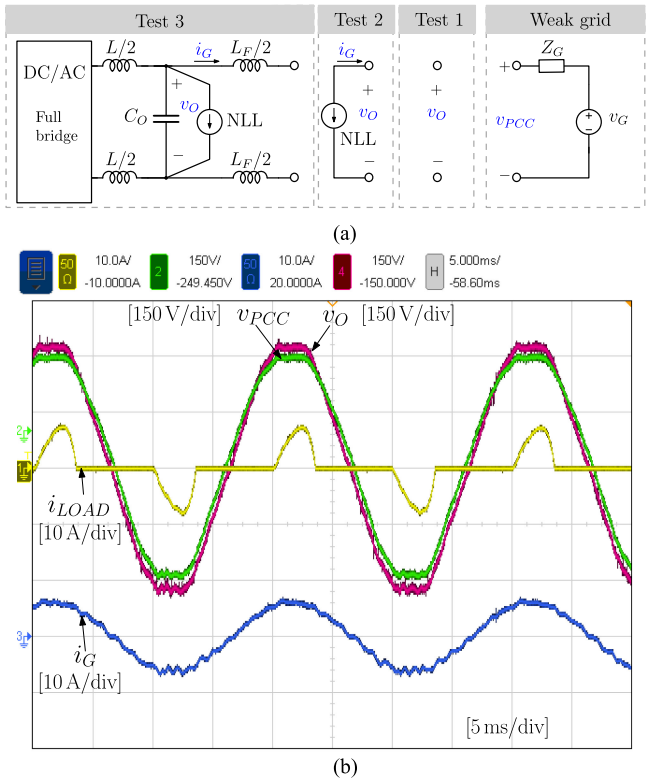

Fig. 17. (a) Experimental setup of harmonic attenuation tests under weak grid. (b) Measured waveforms for test 3.

just a small degradation with respect to the no-load case, as a consequence of the stiffness of the grid source. At the same time, in case ii), the grid current THD is found equal to 1.79 %. This result is due to the large bandwidth controls performed on v_O and i_G, that allow the converter to operate quite effectively as an active filter for the local distorting loads.

As a second test case, the converter is connected to a much *weaker* grid, whose series impedance parameters are found equal to $R_G = 0.16\,\Omega$ and $L_G = 0.43$ mH. In addition, the grid voltage itself is significantly distorted. In this case, if no provision is taken, harmonic currents are injected into the inverter output filter, even if local loads are perfectly linear. It is obviously recommendable that the converter limits such grid-injected, circulating harmonic currents. As shown in Fig. 17(a), the following three tests are performed.

1) In test 1, the grid is open-circuited, so as to determine its inherent distortion.
2) In test 2, an NLL is tied to the grid, so as to evaluate the impact of the relatively large series impedance on voltage and current distortions.
3) In test 3, the converter is connected to the grid and commanded to deliver 1.5 kW active power, while the same NLL is connected to its voltage output port.

The measured THD values are listed in Table V. The grid voltage v_G is inherently distorted with a THD equal to 4.58%. When an NLL is connected with this grid, the corresponding THD values of load voltage v_O (in this case, $v_O = v_{\text{PCC}}$) and grid current i_G are 5.87% and 80.9%, respectively. When the inverter is tied to the grid, the harmonics of load voltage v_O

TABLE V
HARMONIC ATTENUATION RESULTS UNDER WEAK GRID

THD (%)	v_{PCC}	i_G	v_O
Test 1	4.58	-	-
Test 2	5.87	80.9	5.87
Test 3	6.37	1.92	3.81

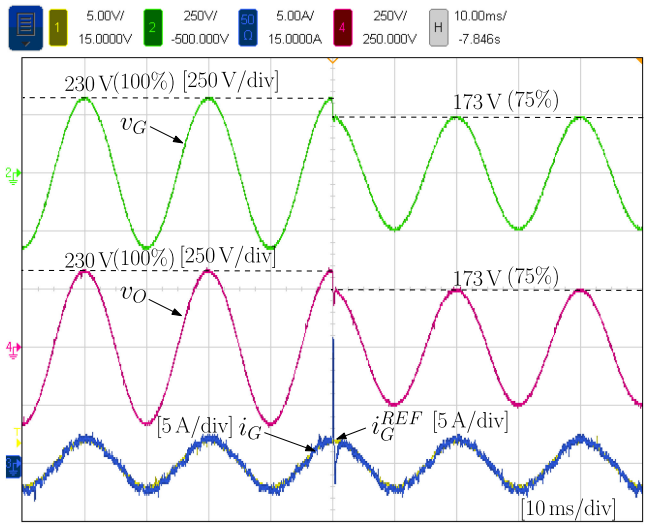

Fig. 18. Response to a step variation of grid voltage amplitude from 230 V_{RMS} (nominal) to 173 V_{RMS} (75%).

and grid current i_G are decreased, respectively, to 3.81% and 1.92%. Again, the active filtering capability of the converter is evident from the reduction of the grid current and local voltage THD values. The waveforms corresponding to test 3 are shown in Fig. 17(b).

C. System Performance Under Grid Voltage Perturbations

Amplitude perturbations and frequency variations are commonly encountered abnormal conditions, especially in weak grids [36]. A grid interface converter should operate reliably even in those cases. Therefore, we tested the performance of the proposed control system in such conditions, obtaining the results discussed in the following.

Fig. 18 shows the system behavior when a step change (from 100% to 75% of the nominal voltage) occurs in the amplitude of the grid voltage. As can be seen, despite the severity of the transient, the system remains stable, and recovers normal operation immediately after the step, without measurable performance degradation. Fig. 19, instead, shows the converter's response to frequency steps (from 50 to 51 Hz and *vice versa*) of the grid voltage. Notably, the system keeps a stable operation, without causing any visible fluctuation in output voltage v_O or grid current i_G. Only the injected power is slightly affected (less than 5%) during the transients, with negligible practical consequences.

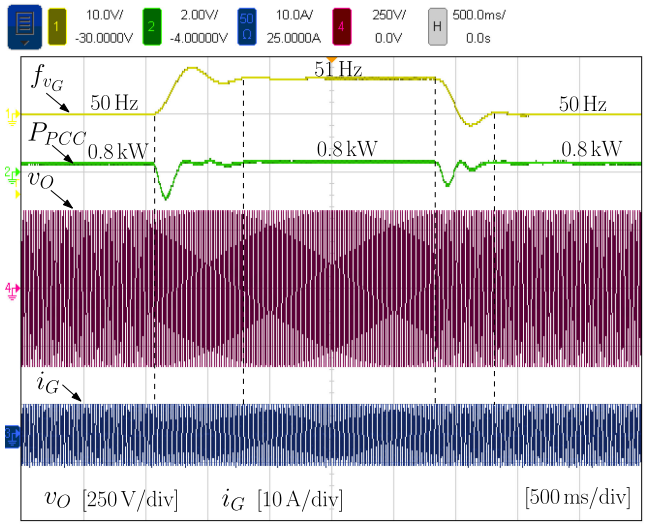

Fig. 19. Response to a step variation of the grid voltage frequency from 50 to 51 Hz and *vice versa*. The upper (yellow) trace is the instantaneous frequency estimation calculated by PLL, the green trace is the average power injected into the PCC. DC biases are added to f_{v_G} and P_{PCC} to ease visualization.

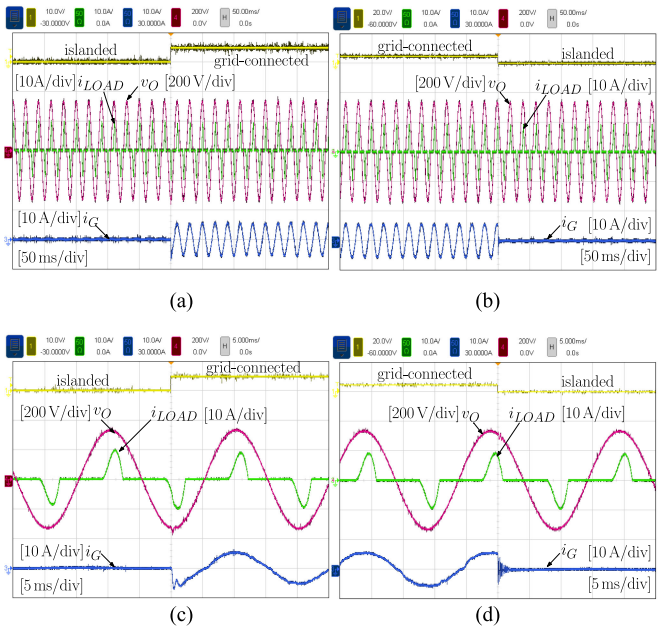

Fig. 20. Transitions between grid-connected (G) and islanded (I) operations. (a) I–G transition. (b) G–I transition. (c) Zoomed-in view of (a). (d) Zoomed-in view of (b).

D. Transition Between Grid-Connected and Islanded Operations

The proposed triple-loop control system enables seamless transitions between grid-connected and islanded operation modes. The experimental results related to these transitions are displayed in Fig. 20. In particular, Fig. 20(a) and (c) illustrates the islanded to grid-connected (I–G) transition. The inverter initially operates islanded (i.e., CB in Fig. 1 is switched OFF), feeding an NLL (same as previous tests). Then, the CB breaker is switched ON at the peak of grid voltage and the system is

transferred to grid-connected operation mode, injecting 1 kW of active power into the grid. Similarly, Fig. 20(b) and (d) shows how the system is transferred from grid-connected back to islanded (G–I) operation mode. Again, the circuit breaker CB opens at the peak of the grid voltage, which brings current i_G to zero.

It is worth remarking that, during the transitions, the output voltage waveform v_O is almost unaffected, with a measured instantaneous voltage perturbation equal to 7.1% of its peak value. Moreover, the output voltage distortion due to the NLL is nearly the same in both grid-connected and islanded operations, thanks to the decoupling ability of the grid current controller. The capability of maintaining a well regulated output voltage across grid-connected and islanded transitions, even in presence of heavily distorted load currents, is an extremely valuable feature to guarantee continuity of supply to critical loads in nano- and microgrids.

VI. Conclusion

This paper presents a large-bandwidth, triple-loop control strategy for grid-tied single-phase VSIs. The control system is designed hierarchically from inner inductor current, to output voltage and, finally, outer grid current loop. Output impedance optimization criteria are considered to steer the regulators' design, resulting in the adoption of DB type controllers for the two inner loops. A PI controller is chosen for the outer loop as it offers a good tradeoff between performance and robustness with respect to grid impedance parameter variations. Thanks to the large-bandwidth control of the injected grid current, the converter achieves the following.

1) An excellent reference tracking performance.
2) A strong attenuation of grid current harmonics.
3) Seamless transitions between grid-connected and islanded operations.
4) Robust stability in the presence of grid perturbations and impedance variations.

The proposed control strategy, therefore, shows good potential for application to nano- and microgrid utility interface converters.

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