Letters

A Sinusoidal Pulsewidth Modulation (SPWM) Technique for Capacitor Voltage Balancing of a Nested T-Type Four-Level Inverter

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***Abstract*—In this letter, a new control method based on the sinusoidal pulsewidth modulation scheme is proposed to control capacitor voltages of a T-type four-level nested neutral-point-clamped (NNPC) inverter. The T-type four-level NNPC inverter has a lower number of switches and components compared with other four-level classic and advanced inverters, which make this topology attractive for high-power medium-voltage applications. This topology has been proposed and studied with the assumption of constant dc sources instead of flying capacitors. In this letter, a simple single-phase modulator is developed to balance flying capacitor voltages. The performance and the feasibility of the proposed control technique are evaluated experimentally under a steady-state and transient conditions and for different modulation indexes and loads. The experimental results demonstrate the effectiveness of the developed control method to control the capacitors' voltages.**

***Index Terms*—Capacitor voltage balancing, multilevel converters, sinusoidal pulsewidth modulation (SPWM), T-type structure.**

I. Introduction

MULTILEVEL inverters are very attractive and commonly used for high-power medium-voltage applications [1], [2]. The neutral-point-clamped (NPC) converter, flying capacitors (FC) converter, and the cascaded H-bridge (CHB) converter are classical multilevel converters [3]. However, these classic topologies have some disadvantages that limit their applications. For NPC topologies, voltage balancing of the dc-link capacitors is a challenge, especially for a higher number of levels. The number of clamping diodes also increases significantly with the higher number of levels. For the FC topology, a higher switching frequency is needed in order to keep the capacitor voltages balanced. Also, the FC topology in a higher number of levels has a higher number of capacitors, which reduce the reliability and lifetime of the converter. A CHB has a modular structure that can get higher voltages and number of levels with an increase in the number of cells. However, the CHB topology needs several isolated dc sources provided by a bulky and expensive phase-shifting transformer. The number of switches in

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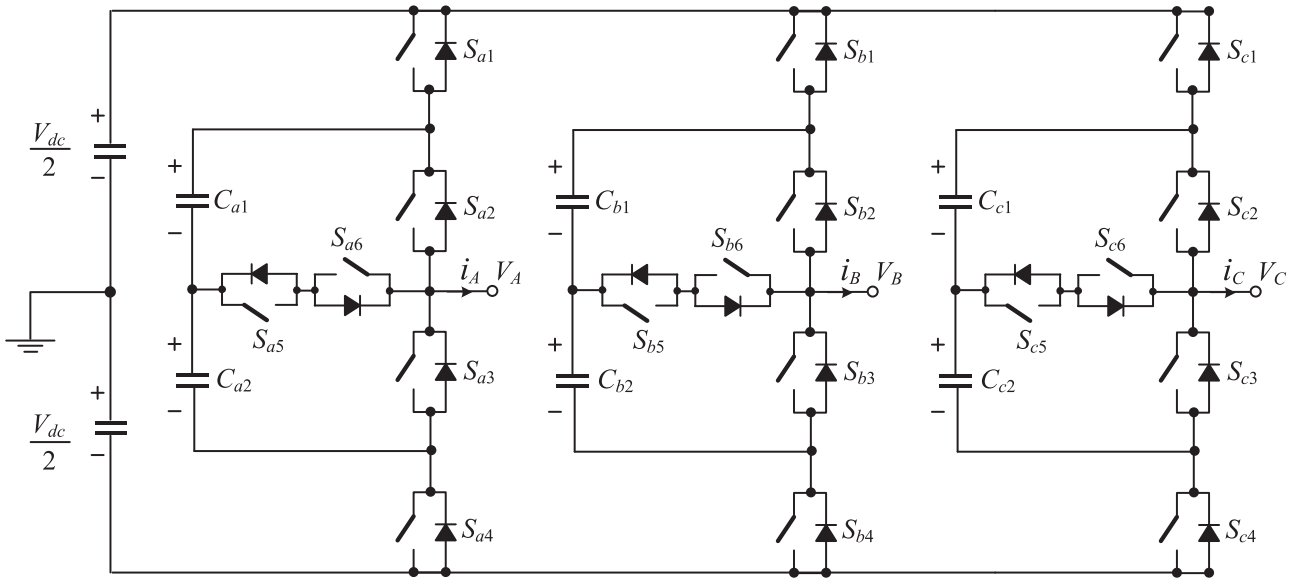

Fig. 1. Nested T-type 4L-NNPC inverter [17].

TABLE I
COMPARISON NUMBER OF DEVICES AMONG DIFFERENT TOPOLOGIES

Topology	Number of switches	Number of clamping diodes	Number of flying capacitors
NPC	18	18	-
FC	18	-	9
NNPC	18	6	6
T-Type NNPC	**18**	**-**	**6**

method is required to regulate the FC voltages. In this letter, a new control method based on the sinusoidal pulsewidth modulation (SPWM) is developed to control and balance the voltages of FCs at the desired voltage level, and thus, the T-type NNPC can operate properly under different operation conditions.

The performance of the developed control strategy is studied in the MATLAB/Simulink environment and verified experimentally under steady-state and transient conditions and for different modulation indexes.

In Section II, the T-type NNPC operation is explained briefly, and then, the SPWM will be used to control FC voltages. In Section III, the proposed control technique is developed. In Section IV, the feasibility and performance of the proposed controller are verified experimentally.

II. OPERATION OF THE NESTED T-TYPE NPC INVERTER

A T-type 4L-NNPC topology is a combination of an FC topology and a T-type inverter [17]. The capacitor C_{x1} and C_{x2}, $x = a, b, c$ are charged to one-third of the total dc-link voltage. Six switching states can generate four output voltage levels as given in Table II. A controllable current path is provided by the bidirectional switches to control the direction of the output current. As given in Table II, levels 2 and 3 have two redundant switching states that generate medium voltage level $1/6V_{\rm dc}$ and $-1/6V_{\rm dc}$ with respect to the midpoint of the dc source.

Each of these redundant switching states has a specific charging and discharging effect for each FC. The method for controlling the capacitors' voltages is based on choosing the best redundant switching state that makes the capacitor charge or discharge to the desired voltage, which is one-third of the total dc-link voltage.

III. SINUSOIDAL PULSEWIDTH MODULATION FOR A T-TYPE NNPC CONVERTER

The capacitor voltage balancing of a T-type NNPC converter is a technical challenge to make sure that the converter can operate properly under different operating conditions. If there is no control, the FCs will be charged or discharged during the converter operation and the capacitors' voltages will deviate from the desired values, and thus, the converter cannot generate a four-level output voltage. In this section, a new control technique based on the SPWM scheme is explained.

The deviation of the capacitor voltages from the desired value ($V_{\rm dc}/3$) can be written as

$$\Delta V_{Cxi} = V_{Cxi} - V_{\rm dc}/3$$
$$x = a,\, b,\, c; \quad i = 1,\, 2.$$

In order to balance the capacitor voltages, ΔV_{CXi} ($x = a, b, c;\ i = 1, 2$) should be zero or close to zero under all operating conditions. If the voltage deviation is positive, a switching state should be selected to discharge the capacitor and if the deviation is negative, the switching state should be selected to charge the capacitor.

However, as it can be seen from Table II, for some switching states, capacitors of a phase are jointly charged and discharged, which is a challenge for controlling the capacitor voltages. For example, assuming the voltage level is 1, if the deviation for C_1

TABLE II
SWITCHING STATES OF THE T-TYPE FOUR-LEVEL INVERTER AND CONTRIBUTION OF THE AC-SIDE CURRENTS TO THE FC VOLTAGES

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	V_{Cx1}	V_{Cx2}	V_{xn}	Output Level	State
1	**1**	**0**	**0**	**1**	**0**	No Impact	No Impact	$\frac{V_{dc}}{2}$	3	3
1	**0**	**0**	**0**	**1**	**1**	Charging (ix>0) Discharging (ix < 0)	No Impact	$\frac{V_{dc}}{6}$	2	2B
0	**1**	**0**	**1**	**1**	**0**	Discharging (ix > 0) Charging (ix < 0)	Discharging (ix > 0) Charging (ix< 0)			2A
1	**0**	**1**	**0**	**0**	**1**	Charging (ix >0) Discharging (ix < 0)	Charging (ix > 0) Discharging (ix < 0)	$-\frac{V_{dc}}{6}$	1	1B
0	**0**	**0**	**1**	**1**	**1**	No Impact	Discharging (ix > 0) Charging (ix< 0)			1A
0	**0**	**1**	**1**	**0**	**1**	No Impact	No Impact	$-\frac{V_{dc}}{2}$	0	0

TABLE III
PROPOSED VOLTAGE CONTROL METHOD

Output Level	i_x	ΔV_{CX1}	ΔV_{CX2}	Condition	State
1	≥ 0	≥ 0	≥ 0	-	1A
			< 0	-	1B
		< 0	≥ 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	1A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	1B
			< 0	-	1B
	< 0	≥ 0	≥ 0	-	1B
			< 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	1A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	1B
		< 0	≥ 0	-	1B
			< 0	-	1A
2	≥ 0	≥ 0	≥ 0	-	2A
			< 0	-	2A
		< 0	≥ 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	2A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	2B
			< 0	-	2B
	< 0	≥ 0	≥ 0	-	2B
			< 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	2A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	2B
		< 0	≥ 0	-	2A
			< 0	-	2A

is positive and the deviation of C_2 is negative, and the output current is larger than zero, choosing 1A will not only charge C_2 toward the desired value but also charges C_1 more, and the deviation for C_1 will increase, which is not desirable.

To solve this problem, Table III gives the procedure of selecting the best switching state to balance the capacitors' voltages at the desired values. For levels 0 and 3, there is no redundant switching state and these two levels do not affect the capacitor voltages. However, for levels 1 and 2, there are redundant switching states and based on the current direction and voltage deviation of the capacitors, the best switching states will be selected from Table III.

For instance, when the output voltage level is 1, and $i_x \geq 0$, $\Delta V_{Cx1} \leq 0$, $\Delta V_{Cx2} \leq 0$, both capacitors need to be charged and, thus, switching state 1B should be selected.

The flowchart in Fig. 2 shows the procedure to control the voltage of FCs in each phase.

1) First, by comparing carriers (three carriers for a four-level converter) and the modulation signal, the desired output voltage level is determined.
2) The direction of the phase currents and capacitor voltages should be measured.
3) Based on the output voltage level, current direction, and capacitor voltage deviations, the proper switching state will be selected from Table III.
4) Finally, the gate signals are generated and applied to the switching devices.

IV. EXPERIMENTAL RESULTS

The feasibility of the proposed control technique based on the SPWM scheme is evaluated experimentally. The parameters given in Table IV are used to obtain the experimental results from a scaled-down prototype.

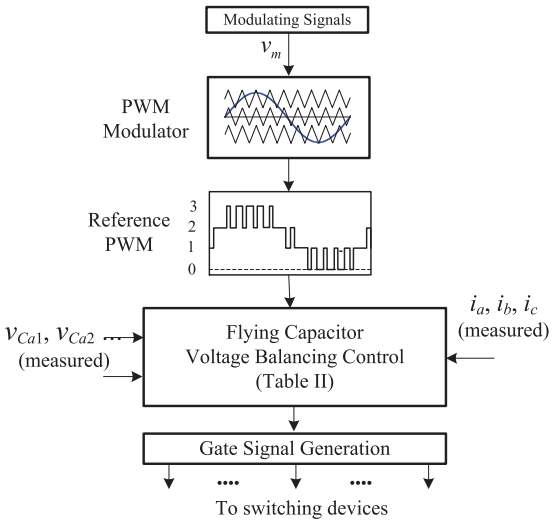

Fig. 2. Block diagram of capacitor voltage balancing control.

TABLE IV
PARAMETERS OF THE STUDY SYSTEM

Converter parameters	Values
Converter rating (kVA)	5
Capacitor Value (μF)	2200
Input dc voltage (V)	320
Output frequency (Hz)	60
Output inductance (mH)	5
Output load (Ω)	12

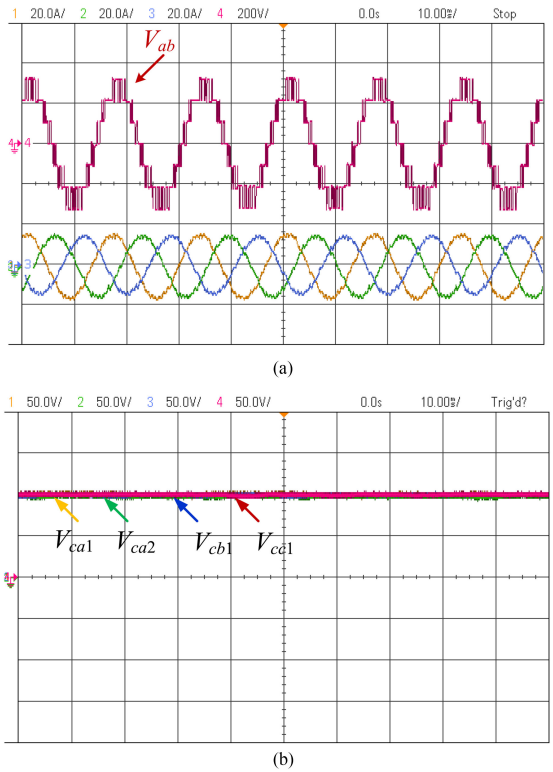

Fig. 3. Experimental results, $m = 0.9$ and PF $= 0.9$. (a) Inverter output line voltage and output currents (200 V/div, 10 A/div, 10 ms/div). (b) Voltages of FCs (50 V/div, 10 ms/div).

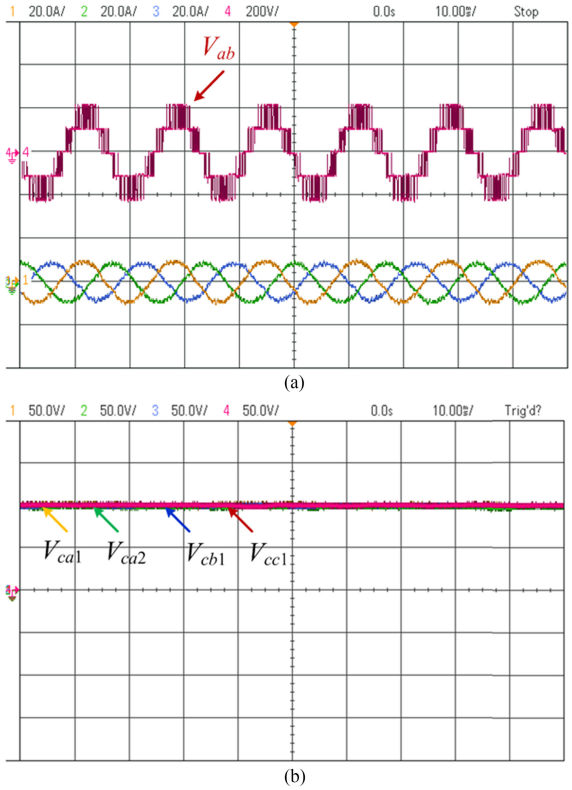

Fig. 4. Experimental results, $m = 0.55$ and PF $= 0.9$. (a) Inverter output line voltage and output currents (200 V/div, 10 A/div, 10 ms/div). (b) Voltages of FCs (50 V/div, 10 ms/div).

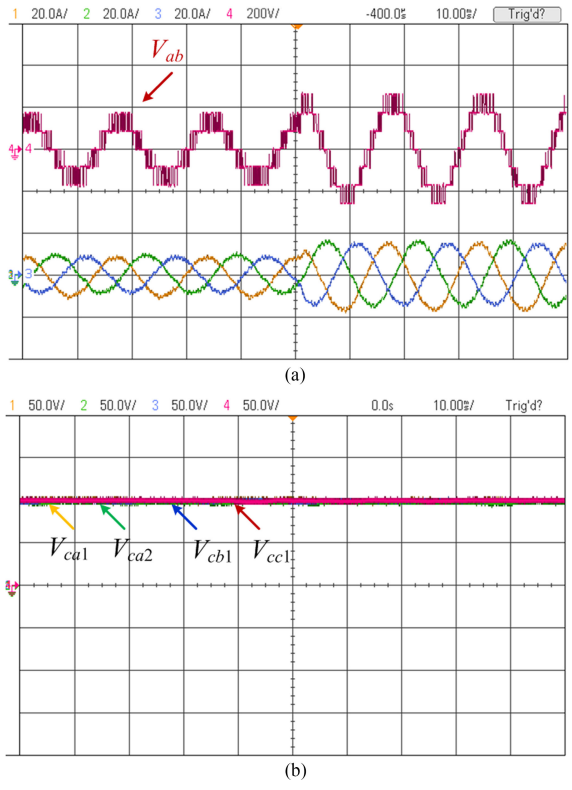

Fig. 5. Experimental results, modulation change from $m = 0.9$ to 0.55. (a) Inverter output line voltage and output currents (200 V/div, 10 A/div, 10 ms/div). (b) Voltages of FCs (50 V/div, 10 ms/div).

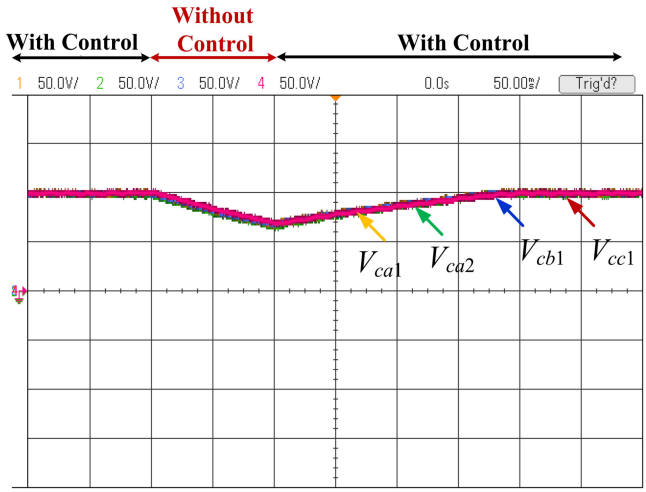

Fig. 6. Voltage of FC when the controller is deactivated and activated.

Figs. 3–6 show the performance of the proposed control technique under steady-state and transient conditions. Fig. 3 shows the inverter output voltage, output currents, and FC voltages where modulation index $m = 0.9$ and load PF $= 0.9$. The inverter output voltage THD is 24.7%. Fig. 4 also shows the inverter output voltage, output currents, and FC voltages where modulation index $m = 0.55$ and load PF $= 0.9$. The inverter output voltage THD is 40.7%.

Fig. 5 shows the performance of the converter when the modulation index m changes from 0.55 to 0.9.

Fig. 6 shows the performance of the controller when the controller is deactivated and activated. Without the controller, capacitors start to diverge and when the controller is activated, the capacitor will be converged. Figs. 3–6 show the effectiveness of the proposed controller and demonstrate that all capacitor voltages are well balanced under different operating conditions.

V. Conclusion

A new method to control the FC voltages of a T-type 4L-NNPC inverter based on the SPWM is proposed in this letter. This topology is very attractive for medium-voltage applications due to the lesser number of components as compared to that of the existing topologies. The proposed control method selects the best switching state among the redundant switching states to charge and discharge the FCs and minimize the voltage deviations of the capacitors from the desired values. As the proposed controller is based on the SPWM technique, it is very simple to implement. The feasibility of the proposed control technique is evaluated by simulation studies and experimentally. The results demonstrate the effectiveness of the proposed technique.

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