A Load Impedance Specification of DC Power Systems for Desired DC-Link Dynamics and Reduced Conservativeness

Syam Kumar Pidaparthy, *Student Member, IEEE*, Byungcho Choi, *Member, IEEE*, and Yeonjung Kim

***Abstract*—This paper proposes a new load impedance specification for multistage dc power conversion systems. The proposed specification avoids drawbacks of the existing specifications, such as the lack of explicit connections to the dc-link dynamics and the unnecessary conservativeness. The new specification offers a direct command/supervision of the frequency- and time-domain dynamics of the intermediate dc link, while being less conservative than the existing specifications. This paper also presents procedures for redesigning ill-conditioned load impedances to comply with the specification. The validity and utility of the proposed specification are demonstrated using an experimental two-stage dc power conversion system.**

***Index Terms*—DC power conversion systems, dynamic interaction, loading effects, load impedance specification, minor loop gain, stability and performance.**

I. Introduction

In PRACTICAL multistage dc power conversion systems, the upstream converter stage is first fabricated as a standalone unit and later integrated with an independently engineered load subsystem. For such cases, certain specifications for load impedance are often issued, in order to secure the stability and performance of the integrated system. Load impedance specifications are initially given in the form of a forbidden region for the polar plot trajectory of the minor loop gain [1], $T_{mn} = Z_{oC}/Z_L$, which is defined as the ratio of the output impedance of the upstream converter stage, Z_{oC}, to the input impedance of the load subsystem, namely, the load impedance Z_L. The forbidden region is an especially selected s-plane territory such that *not* allowing the minor loop gain trajectory to enter the forbidden territory ensures the stability and performance of the integrated system. The forbidden region is later converted into the specification for the load impedance Z_L, which is referred to as the load impedance specification [2], [3].

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The authors are with the School of Electronics Engineering, Kyungpook National University, Daegu 41566, South Korea (e-mail:

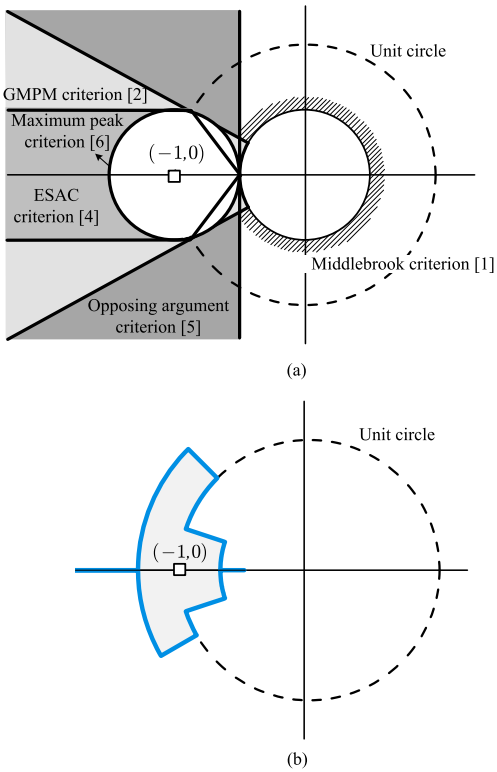


Fig. 1. Forbidden regions for $T_{mn} = Z_{oC}/Z_L$ trajectory. (a) Existing forbidden regions [1], [2], [4]–[6]. (b) New forbidden region.

Various forbidden regions have been proposed as shown in Fig. 1(a), including Middlebrook criterion [1], gain margin and phase margin criterion [2], energy source analysis consortium (ESAC) criterion [4], opposing argument criterion [5], and maximum peak criterion [6]. A comprehensive review of the previous forbidden regions was presented in [7].

While all the existing criteria ensure stability [7], the connections between the forbidden regions and other performance metrics are unclear. Further drawbacks of the aforementioned criteria include conservativeness and complexity. Some forbidden regions [1], [2], [5] occupy a larger s-plane territory than necessary, thus imposing undue constraints on the load subsystem. Other criteria [4], [6] require complex treatments of Z_{oC} to generate the load impedance specification.

This paper proposes a load impedance specification based on a new forbidden region, which is depicted in Fig. 1(b). The

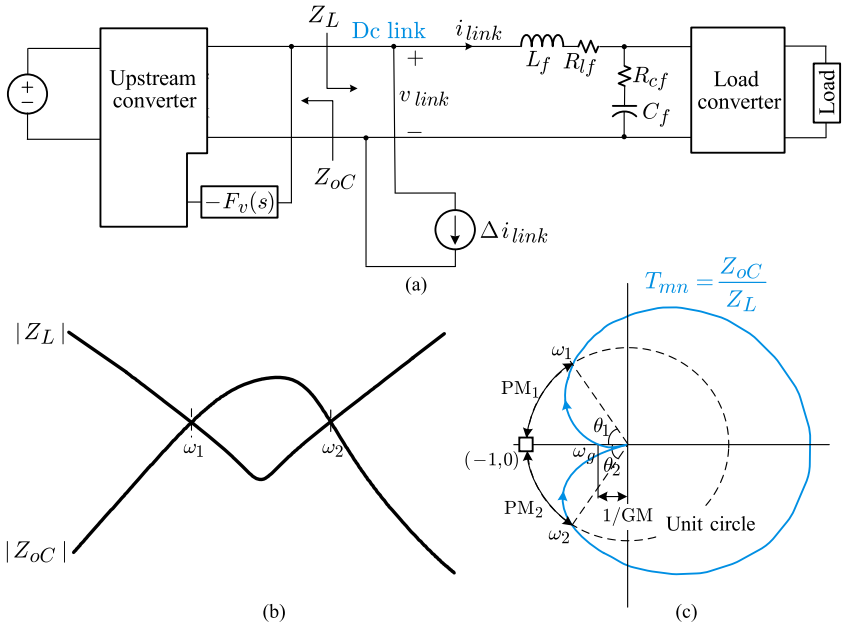


Fig. 2. Two-stage power conversion system and impedance ratio as minor loop gain. (a) Two-stage power conversion system. (b) Conceptual plots of $|Z_{oC}|$ and $|Z_L|$. (c) Polar plot of minor loop gain, $T_{mn} = Z_{oC}/Z_L$.

proposed forbidden region offers direct command/supervision of the frequency- and time-domain dynamics of the intermediate dc link. The new forbidden region takes a smaller territory than the existing ones. The proposed load impedance specification itself serves as an instrumental tool for redesigning ill-conditioned load impedances to meet the specification. This paper demonstrates the procedures and benefits of such load impedance shaping technique, using an experimental two-stage dc power conversion system.

Section II addresses the relation between the minor loop gain and the system performance, focusing on dc-link dynamics in multistage dc power conversion systems. Section III presents the formation of the new forbidden region. In Section IV, the forbidden region is converted into the load impedance specification. Moreover, an adoption of the proposed load impedance specification is also discussed. Section V demonstrates a load impedance shaping technique to comply with the given load impedance specification. Section VI provides experimental validations of the proposed work. Finally, Section VII concludes this paper.

II. Minor Loop Gain and System Performance

This section illustrates the relation between the minor loop gain and system performance using a two-stage dc power conversion system shown in Fig. 2. The system is configured with an upstream converter and the load subsystem consisting of a line filter and load converter. The current source Δi_{link} at the intermediate dc link represents a current disturbance to evaluate the transient performance of the dc-link voltage, v_{link}.

A. Impedance Overlap and Stability

The minor loop gain is closely related with the concept of the impedance overlap [2], [8], [9], which refers to the overlap between $|Z_{oC}|$ and $|Z_L|$. Fig. 2(b) shows the conceptual plot of an impedance overlap. If the impedance overlap is avoided, the system stands stable. Avoiding the overlap is the sufficient condition for the stability, but this requirement is overly conservative and restrictive [2]. On the other hand, an excessive impedance overlap could reduce the stability margins of the system and degrade the transient performance of the dc-link voltage, as will be clarified in Section II-C.

Fig. 2(c) shows the polar plot of the minor loop gain, $T_{mn} = Z_{oC}/Z_L$. Even though the impedance overlap exists, the system is stable because the polar plot does not pass or encircle the $(-1, 0)$ point. At frequencies ω_1 and ω_2, the $|Z_L|$ curve crosses the $|Z_{oC}|$ curve. As shown in Fig. 2(c), two different phase margins, $\mathrm{PM}_1 = 180^\circ - \angle T_{mn}(j\omega_1) = \theta_1$ and $\mathrm{PM}_2 = \angle T_{mn}(j\omega_2) - (-180^\circ) = \theta_2$, are defined at ω_1 and ω_2, where the polar plot crosses the unit circle.

A gain margin GM is defined at the frequency ω_g, where the polar plot crosses the negative real axis. The detailed description about the phase and gain margins can be found in [2] and [8]. The stability margins predict the dynamic performance of the dc power conversion system. Particularly, the phase margins, PM_1 and PM_2, play an important role in the dc-link dynamics, as will be shown in Section II-C.

B. Peak Factor

The impedance seen at the dc link, referred to as the dc-link impedance, is given by

$$Z_{\text{link}} = Z_{oC} \parallel Z_L = \frac{Z_{oC}\, Z_L}{Z_L + Z_{oC}} = Z_{oC} \frac{1}{1 + \frac{Z_{oC}}{Z_L}} = Z_{oC} \frac{1}{1 + T_{mn}}. \quad (1)$$

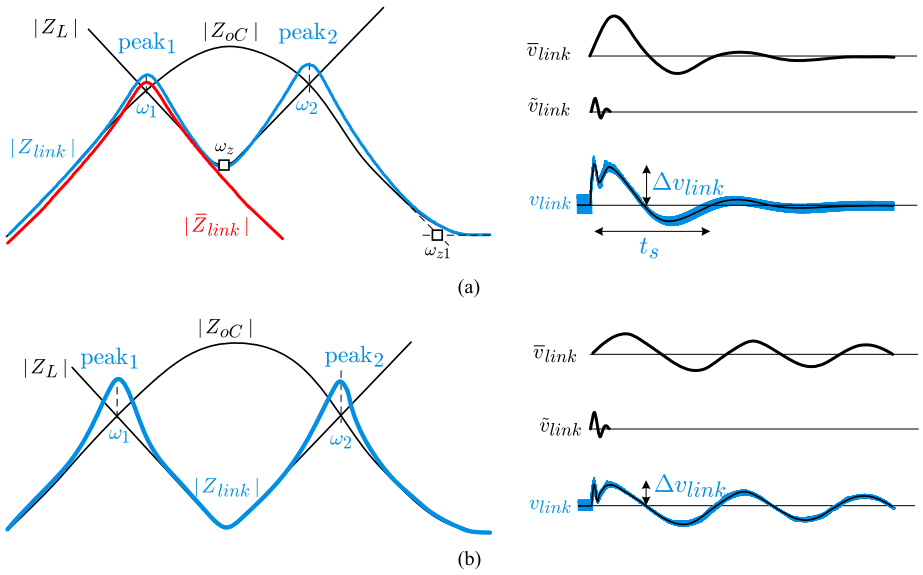


Fig. 3. DC-link dynamics. (a) Small magnitude peaks. (b) Large magnitude peaks.

The input-to-dc link noise transmission is determined as

$$A_{u\,\text{link}} = A_{uC}\frac{Z_L}{Z_L + Z_{oC}} = A_{uC}\frac{1}{1+\frac{Z_{oC}}{Z_L}} = A_{uC}\frac{1}{1+T_{mn}} \tag{2}$$

where A_{uC} is the input-to-output noise transmission of the upstream converter. The $|Z_{\text{link}}|$ and $|A_{u\,\text{link}}|$ are proportional to the common term, defined as the peak factor [6]

$$\text{peak factor} \equiv \frac{1}{|1+\vec{T}_{mn}|}. \tag{3}$$

As shown in Appendix A, the denominator of the peak factor is the distance from the $(-1, 0)$ point to the coordinate of $\vec{T}_{mn}$. When $\vec{T}_{mn}$ approaches the $(-1, 0)$ point, the peak factor rapidly increases and deteriorates the dc-link dynamics [6].

C. Impacts of Impedance Overlap on DC-Link Dynamics

Fig. 3 illustrates the impacts of impedance overlap on dc-link dynamics. Fig. 3(a) is a conceptual plot of $|Z_{\text{link}}|$. The $|Z_{\text{link}}|$ follows the smaller of $|Z_{oC}|$ and $|Z_L|$ for most frequencies. However, at the frequencies around ω_1 and ω_2, where $|Z_{oC}|$ and $|Z_L|$ intersect and the T_{mn} trajectory crosses the unit circle, $|Z_{\text{link}}|$ exhibits two isolated peaks, labeled $\mathbf{peak_1}$ and $\mathbf{peak_2}$. As shown in Appendix A, the magnitude of the peaks are given by

$$|\text{peak}_{1,2}| = 20\log\frac{1}{\sqrt{2-2\cos\theta_{1,2}}} \tag{4}$$

where the angles $\theta_{1,2}$ are the phase margins at ω_1 and ω_2. The two peaks in $|Z_{\text{link}}|$ transform into underdamped second-order terms in the s-domain expression [10], which trigger decaying oscillations in v_{link} in response to a step change in i_{link}. The peak_1 induces a low-frequency oscillation at ω_1, represented by $\bar{v}_{\text{link}}$ in Fig. 3(a), while the peak_2 produces a high-frequency oscillation at ω_2, $\tilde{v}_{\text{link}}$. The dc link voltage, v_{link}, is predicted by combining $\bar{v}_{\text{link}}$ and $\tilde{v}_{\text{link}}$, as depicted in Fig. 3(a). The frequencies of oscillations correspond to the frequencies of the peaks, ω_1 and ω_2.

The amplitude and persistence of the oscillations are both proportional to the magnitude of the peaks, which is inversely proportional to the phase margins $\text{PM}_1 = \theta_1$ and $\text{PM}_2 = \theta_2$. Fig. 3(a) illustrates an impedance overlap with sufficient phase margins, which produces small peaks in $|Z_{\text{link}}|$. As the impedance overlap increases, the margins, PM_1 and PM_2 decrease, which eventually increase the peaks in $|Z_{\text{link}}|$. Fig. 3(b) depicts such a case, where the smaller phase margins produce the larger peaks in $|Z_{\text{link}}|$. The dc-link voltage, v_{link}, becomes more oscillatory due to the larger peaks. Moreover, the increase in the impedance overlap decreases both the value of ω_1 and the magnitude of dc-link impedance. The decrease in the value of ω_1 slows down the transient response, while the decrease in dc-link impedance reduces the maximum overshoot, Δv_{link} [10].

Because $\omega_1 \ll \omega_2$, the high-frequency oscillation at ω_2 will decay so fast that only the low-frequency (slowly decaying) oscillation at ω_1 dominates the transient behavior of v_{link}. Hence, the transient dynamics of the dc-link voltage are closely related with the phase margin of the minor loop gain at ω_1, $\text{PM}_1 = \theta_1$.

Based on the shape of the dc-link impedance, Z_{link} can be formulated as a fourth-order function

$$Z_{\text{link}} \approx k_d s\frac{\left(1+\frac{s}{Q_z\omega_z}+\frac{s}{\omega_z^2}\right)\left(1+\frac{s}{\omega_{z1}}\right)}{\left(1+\frac{s}{Q_1\omega_1}+\frac{s}{\omega_1^2}\right)\left(1+\frac{s}{Q_2\omega_2}+\frac{s}{\omega_2^2}\right)} \tag{5}$$

with

$$k_d = \frac{|Z_{oC}|_{@\omega_1}}{\omega_1} \tag{6}$$

$$Q_1 = \frac{1}{\sqrt{2-2\cos\theta_1}} \tag{7}$$

$$Q_2 = \frac{1}{\sqrt{2-2\cos\theta_2}}. \tag{8}$$

The values of Q_z, ω_z, and ω_{z1} are estimated from the shape and value of the $|Z_{\text{link}}|$. The analysis of the dc-link dynamics using (5) will be impractically complex.

A practical method is proposed in order to predict the low-frequency dynamics of v_{link} using the standard second-order system analysis. As discussed earlier, the low-frequency oscillation at ω_1 usually dominates the transient response of v_{link}. Accordingly, the double pole at ω_1 can be used to predict the transient behavior of the v_{link}. The Z_{link} can be approximated as a second-order function

$$\bar{Z}_{\text{link}} = k_d s \frac{1}{1 + \frac{s}{Q_1 \omega_1} + \frac{s^2}{\omega_1^2}} \tag{9}$$

only considering the low-frequency dynamics of the dc-link impedance, while ignoring the high-frequency dynamics. Fig. 3(a) illustrates the low-frequency approximation, $\bar{Z}_{\text{link}}$.

When a step current change occurs at the dc link, $\bar{Z}_{\text{link}}$ induces a low-frequency oscillation at ω_1, represented by $\bar{v}_{\text{link}}$ in Fig. 3(a). The $\bar{v}_{\text{link}}$ expression in response to the step current change, Δi_{link}, is given by

$$\bar{v}_{\text{link}} = \mathcal{L}^{-1}\left(\bar{Z}_{\text{link}} \frac{\Delta i_{\text{link}}}{s}\right). \tag{10}$$

By evaluating (10) and analyzing the resulting expression [11], the maximum overshoot of v_{link} is found to be

$$\begin{aligned} \Delta v_{\text{link}} &\approx \Delta \bar{v}_{\text{link}} \\ &= \Delta i_{\text{link}}\, k_d\, \omega_1\, e^{-\frac{1}{\sqrt{4Q_1^2-1}} \tan^{-1} \sqrt{4Q_1^2-1}} \end{aligned} \tag{11}$$

and the 5%-boundary settling time, t_s, is evaluated as

$$t_s \approx \frac{6Q_1}{\omega_1}. \tag{12}$$

The expressions (11) and (12) provide estimates of the maximum overshoot and settling time of the actual dc-link voltage, v_{link} in Fig. 3. The accuracy of the second-order low-frequency approximation $\bar{Z}_{\text{link}}$ is given in Appendix B.

III. Formation of New Forbidden Region

The forbidden region is issued by the manufacturer of the upstream converter. The designer of the load subsystem is responsible to properly shape the load impedance Z_L so that the minor loop gain T_{mn} trajectory does not enter the forbidden region. This section discusses the elements, formation, and features of the new forbidden region.

A. Elements of the New Forbidden Region

The proposed forbidden region shown in Fig. 1(b) is defined using the five s-plane elements. The five s-plane elements are shown in Fig. 4. The five elements include real axis segment, three discrete points A–C, and a circle centered at the $(-1, 0)$ point. The five s-plane elements are all connected with dc-link dynamics, robustness, and the stability of the system.

The line segment stretching from the $(-k, 0)$ point toward negative infinity ensures stability, while excluding the chance of being conditionally stable. Points A and B in Fig. 4 are

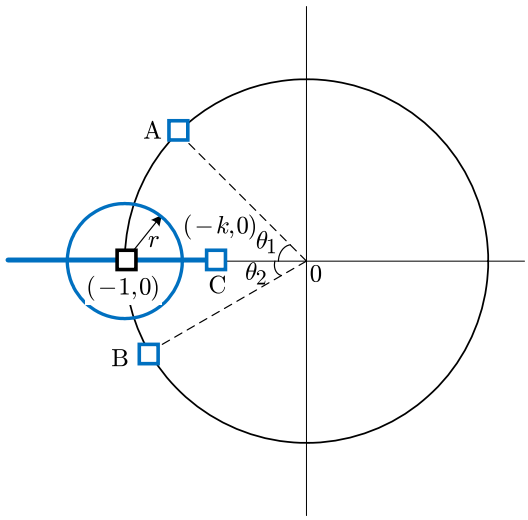


Fig. 4. Elements of the proposed forbidden region.

employed as a guard of the minimum allowable phase margins of the minor loop gain [2]. When the minor loop gain trajectory just passes Point A at ω_1 and Point B at ω_2, the first phase margin becomes $\text{PM}_1 = \theta_1$ and the second phase margin is $\text{PM}_2 = \theta_2$. Inclusion of Points A and B in the forbidden region sets the angles θ_1 and θ_2 as the lower limits of the phase margins.

Point C is employed to set the minimum value of the gain margin. Point C specifies the allowable increase in the dc-link current, while retaining stability. Point C at $(-k, 0)$ provides a $20\log(1/k)$-dB margin against a potential increase in the dc-link current, for example, Point C at the $(-0.5, 0)$ point permits about 6-dB increase in the dc-link current without destabilizing the system. A circle centered at the $(-1, 0)$ point specifies an upper bound of the peak factor. For example, if the circle of radius $r = 0.5$ is included, the peak factor is limited at $20\log(1/0.5) \approx 6$ dB.

B. Conservativeness and Convertibility of the Forbidden Region

The forbidden region should include the three squares A−C to bound the worst-case stability margins, the circle centered at the $(-1, 0)$ point to limit the peak factor, and the portion of the $-$ real axis for the system stability. Any region including these elements deserves as a potential forbidden region. Fig. 5 shows four different forbidden regions that are formulated from the five s-plane elements. In order to simplify the generation of load impedance specification, the forbidden regions are constructed with the curved boundaries and straight lines that are drawn with respect to the origin. The angle α employed in forbidden regions C and D is determined as $\alpha = \sin^{-1} r$, where r is the radius of the circle centered at the $(-1, 0)$ point. The forbidden regions all ensure the system stability, the stability margins greater than the specified minimum, the peak factor bounded by the selected maximum. However, the forbidden regions with a larger area would be more conservative and restrictive. Forbidden region A is most restrictive, while Forbidden region D is least conservative. Forbidden region D is selected as the final

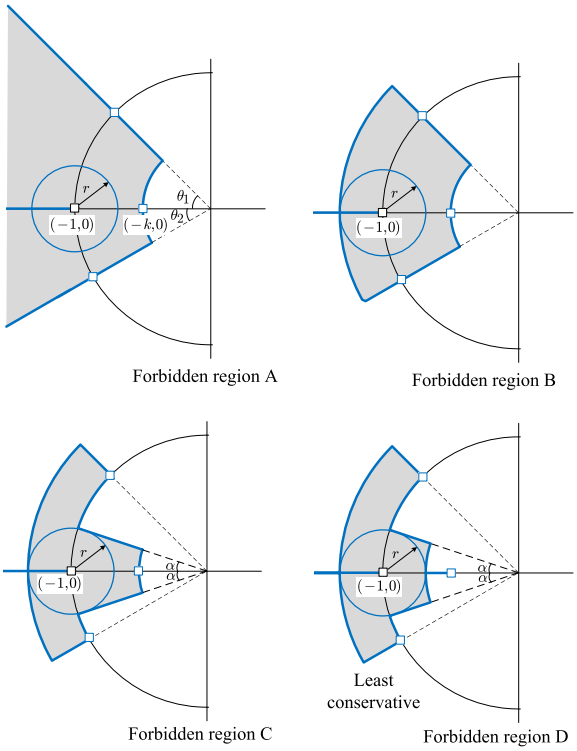


Fig. 5. Four forbidden regions.

territory, which is smaller and less conservative, compared with the existing criteria [1], [2], [4]–[6].

IV. Load Impedance Specification

For the given $|Z_{oC}|$ and $\angle Z_{oC}$ curves, the forbidden region for the minor loop gain trajectory can be transformed into the load impedance specification. Fig. 6 shows the formation and adoption of the load impedance specification. The forbidden region in Fig. 6(a) is converted into the load impedance specification in Fig. 6(b). The specification consists of three magnitude curves around $|Z_{oC}|$, denoted as the magnitude specification, and six phase curves above and below $\angle Z_{oC}$, referred to as the phase specification.

The construction of the magnitude and phase specifications is as follows.

1) Three magnitude curves are drawn in reference to $|Z_{oC}|$ plot. The top curve, elevated by $20\log(1/\mathrm{k})$ dB from $|Z_{oC}|$, is related with Point C at $(-\mathrm{k}, 0)$ in the forbidden region. The other two curves, separated by $20\log(1/(1-\mathrm{r}))$ dB and $20\log(1+\mathrm{r})$ dB from $|Z_{oC}|$, are associated with the horizontal distance between the $(-1, 0)$ point and the curved borderlines of the forbidden region.
2) Three phase plots are constructed below the $\angle Z_{oC}$ plot. The bottom curve, separated by 180° from $\angle Z_{oC}$, is affiliated with the $-$ real axis. The other two curves are linked with the two straight lines, pointing to the origin with the phase of θ_1 and α.
3) Three phase curves are drawn above the $\angle Z_{oC}$ plot. These curves are associated with the $-$ real axis and the straight lines with the phase of θ_2 and α.

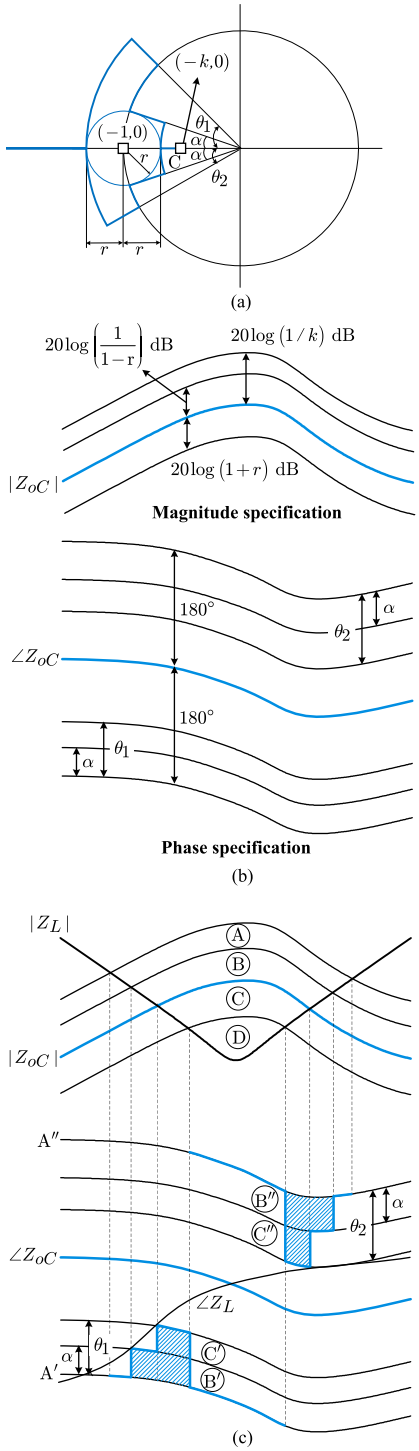


Fig. 6. Forbidden region and load impedance specification. (a) Forbidden region. (b) Formation of load impedance specification. (c) Adoption of load impedance of load impedance specification.

Fig. 6(c) displays illustrative $|Z_L|$ and $\angle Z_L$ plots over the magnitude and phase specifications. For the given $|Z_L|$ curve, the minor loop gain trajectory does not enter the forbidden region if $\angle Z_L$ curve simultaneously meet the following requirements.

1) For the frequencies where $|Z_L|$ plot passes Ⓐ band in the magnitude specification, $\angle Z_L$ does not touch A′ line or A″ line on the phase specification.

2) For the frequencies where $|Z_L|$ plot passes Ⓑ band, $\angle Z_L$ does not fall in Ⓑ′ band or Ⓑ″ band in the phase specification.
3) For the frequencies where $|Z_L|$ plot travels Ⓒ band, $\angle Z_L$ does not fall in Ⓑ′, Ⓒ′, Ⓑ″, or Ⓒ″ band.
4) For the frequencies where $|Z_L|$ plot travels Ⓓ region, $\angle Z_L$ does not touch A′ or A″ line.

An illustrative $\angle Z_L$ does not violate the phase specification and Z_L meets the load impedance specification.

The phase of the load subsystems terminated with a regulated converter starts with -180° at low frequencies and continuously increases toward the 90° high-frequency asymptote [8]. This simplifies the load impedance specification as follows. *The $\angle Z_L$ should not touch the shaded regions or thick line segments of the phase specification for the frequencies where $|Z_L|$ falls below the top curve of the magnitude specification, which is raised by* $20\log(1/\mathrm{k})$ dB *from* $|Z_{oC}|$. The aforementioned requirements exclude any chance of the intrusion into the forbidden region in the s-plane.

V. Load Impedance Shaping and Line Filter Redesign

If the polar plot of the minor loop gain breaks the forbidden region, the load impedance should be modified. This process is referred to as the load impedance shaping. The load impedance shaping only requires the redesign of the line filter, while using the same load converter, because the load impedance is dictated by the line filter impedance, as will be shown later.

A. Load Impedance Analysis

Referring to Fig. 2(a), the load impedance Z_L is a cascaded connection of the line filter impedance, Z_{iF}, and the input impedance of the regulated load converter, Z_{iC}. It has been shown [1], [12]–[17] that the input impedance of a regulated converter behaves as a negative resistance up to the loop gain crossover frequency of the converter regardless of the topology, control scheme, and load characteristics. Thus, the load converter is replaced with the negative resistance for the load impedance evaluation. Fig. 7(a) and (b) depicts this concept. The value of the negative resistance is given by $-R_{iC} = -V_{\text{link}}/I_{\text{link}}$, where V_{link} is the dc-link voltage and I_{link} is the dc-link current.

After replacing the load converter in Fig. 7(a) with $-R_{iC}$, the load impedance Z_L is evaluated as

$$Z_L = sL_f + R_{lf} + \left(R_{cf} + \frac{1}{sC_f}\right) \parallel -R_{iC} \tag{13}$$

$$= -R_{iC}\frac{1 + \frac{s}{Q_o\omega_o} + \frac{s^2}{\omega_o^2}}{1 + \frac{s}{\omega_p}} \tag{14}$$

where

$$\omega_o \approx \frac{1}{\sqrt{L_f C_f}} \tag{15}$$

$$Q \approx \frac{1}{R_{lf} + R_{cf}}\sqrt{\frac{L_f}{C_f}} \tag{16}$$

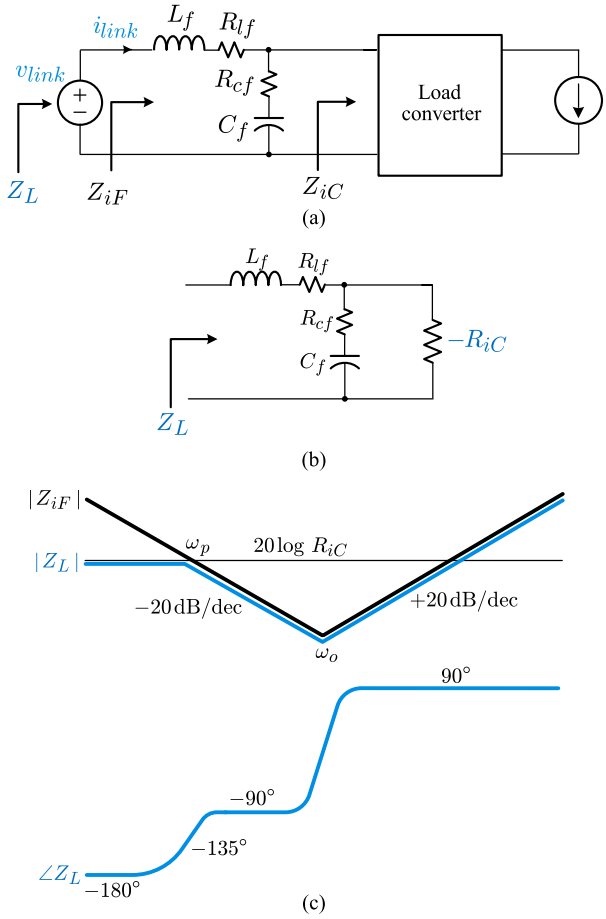


Fig. 7. Load impedance analysis. (a) Load subsystem. (b) Circuit model. (c) Asymptotic plots for Z_L, $|Z_{iF}|$, and $20\log R_{iC}$.

$$\omega_p \approx -\frac{1}{C_f R_{iC}} \tag{17}$$

with the assumptions of $R_{iC} \gg R_{cf}$, $R_{iC} \gg R_{lf}$, and $C_f(R_{lf} + R_{cf}) \gg L_f/R_{iC}$.

The ω_p in (17) is a right-half plane (RHP) pole, which boosts $\angle Z_L$ by 90° while bringing down the $|Z_L|$ slope by -20 dB/dec. Thus, $\angle Z_L$ starts with -180° at low frequencies and increases continuously toward the 90° high-frequency asymptote. Fig. 7(c) displays the asymptotic plots of $|Z_L|$ and $\angle Z_L$ of (14) along with the $|Z_{iF}|$, and $20\log R_{iC}$. As discussed in [8] and [9], the load impedance initially follows the $-R_{iC}$ at low frequencies. At mid and high frequencies, on the other hand, the load impedance tracks the Z_{iF}. Therefore, the Z_{iF} of the line filter determines the load impedance Z_L for the frequencies of practical importance.

The load impedance analysis has been done for the specific load subsystem consisting of a line filter and regulated load converter. Although the outcome of this analysis can be broadly extended, there are some cases that need special attentions and considerations, depending on the nature/feature of the downstream load converter or load subsystem.

1) *Narrow-bandwidth load converters with a line filter stage:* The line filter masks the mid- and high-frequency dynamics of input impedance of the regulated load converter,

regardless of the topology, control scheme, and bandwidth of the converter. The line filter governs the load impedance even for the cases of narrow-bandwidth load converters. The changes in bandwidth only affect the input impedance of the load converter at mid and high frequencies where the line filter dominates the load impedance.

2) *Regulated load converters without a line filter stage:* At the absence of a line filter, the load impedance Z_L becomes the input impedance of the load converter Z_{iC}. The $|Z_{iC}|$ is usually lager than the output impedance of the upstream converter $|Z_{oC}|$, thus creating an impedance gap. For this case, the polar plot of the impedance ratio, Z_{oC}/Z_{iC}, stays within the unit circle and ensures the system stability. However, there still exist possibilities that $|Z_{oC}|$ exceeds $|Z_{iC}|$ at the frequencies where Z_{iC} behaves as a negative resistance. This case would occur when $|Z_{iC}|$ is unusually small due to a very large input current of the load converter. For this instance, the system would become unstable and countermeasure should be employed. In order to shape the load impedance without using an intermediate line filter, the input impedance shaping techniques [18]–[21] can be applied to the load converter. Alternatively, the shunt active damping methods [22] and [23] can also be employed between cascaded converter stages.

3) *Unregulated converters with a line filter stage:* The impact of the input impedance of an unregulated converter, $Z_{iC\,\text{unreg}}$, on the load impedance depends on the magnitudes of $Z_{iC\,\text{unreg}}$ and input impedance of the line filter, Z_{iF}. When $|Z_{iC\,\text{unreg}}|$ is significantly larger than $|Z_{iF}|$, the line filter governs the load impedance characteristics. However, when $|Z_{iC\,\text{unreg}}|$ is smaller than or comparable with $|Z_{iF}|$, the load impedance will be affected by the $Z_{iC\,\text{unreg}}$. For this case, the load impedance should be tested against the load impedance specification. If the impedance specification is violated, the load impedance shaping technique can be applied to redesign the line filter, explained as follows.

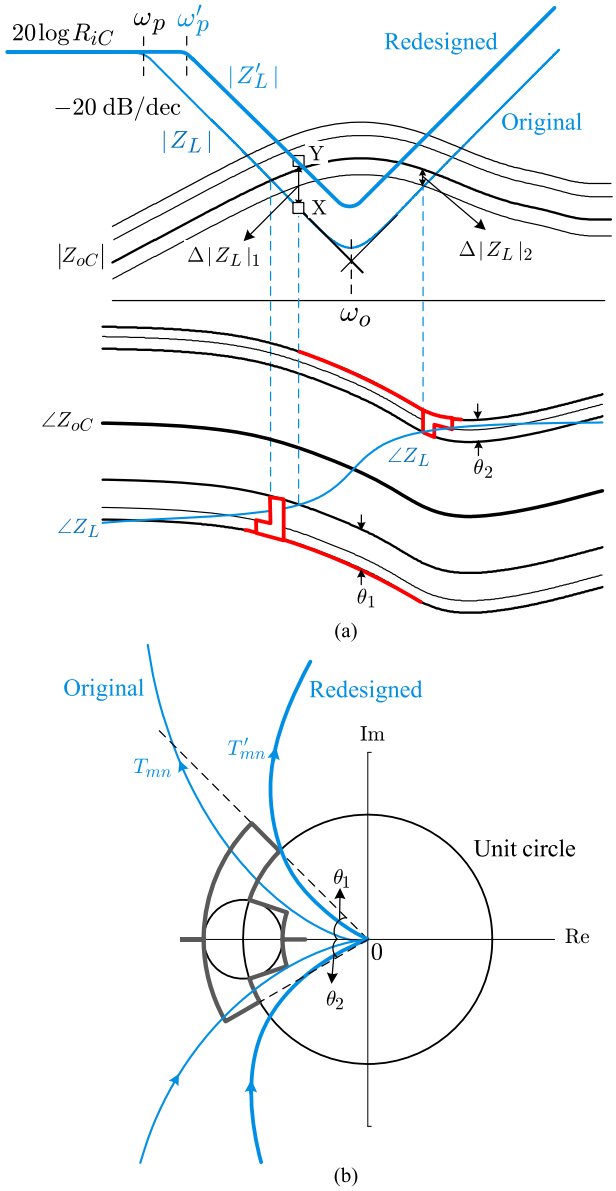


Fig. 8. Load impedance shaping. (a) Load impedance specification. (b) Minor loop gain.

B. Load Impedance Shaping

Fig. 8 describes the process of the load impedance shaping. Fig. 8(a) shows illustrative plots for $|Z_L|$ and $\angle Z_L$, while Fig. 8(b) displays the corresponding minor loop gain trajectories. The thin curves are the plots of the original load subsystem. The original load subsystem fails to meet the specification and requires redesigning. The plots of the redesigned load subsystem are shown with thick curves.

The original load subsystem violates the phase specification at the two different frequency ranges and the minor loop gain trajectory crosses the forbidden region twice. The two phase margins of the minor loop gain are determined at the frequencies where $|Z_L|$ intersects with $|Z_{oC}|$. The $\angle Z_L$ curve indicates that the two phase margins fall below the aimed values of θ_1 and θ_2.

Fig. 8(a) shows that the aimed phase margin θ_1 will be obtained if $|Z_L|$ is raised by $\Delta|Z_L|_1$, from the point **X** to point **Y**, while $\angle Z_L$ remains unchanged. Similarly, the second phase margin will be θ_2 when $|Z_L|$ is increased by $\Delta|Z_L|_2$. By noting that $\Delta|Z_L|_1 > \Delta|Z_L|_2$, the conceptual $|Z'_L|$ plot is shown with a thick line, which precisely meets the target value of the first phase margin θ_1, while satisfying the second phase margin θ_2 with some margin. The $|Z'_L|$ curve is obtained by shifting the frequency of the RHP pole from ω_p to ω'_p.

The minor loop gain trajectory with the modified load impedance, T'_{mn}, is shown in Fig. 8(b) with a thick line. The polar plot just passes the upper right edge of the forbidden region, thus yielding the first phase margin $\text{PM}_1 = \theta_1$.

From Fig. 8(a), the following relations are formulated:

$$20\log R_{iC} - 20\log\frac{\omega_1}{\omega'_p} = Y \tag{18}$$

$$20\log R_{iC} - 20\log\frac{\omega_1}{\omega_p} = X. \tag{19}$$

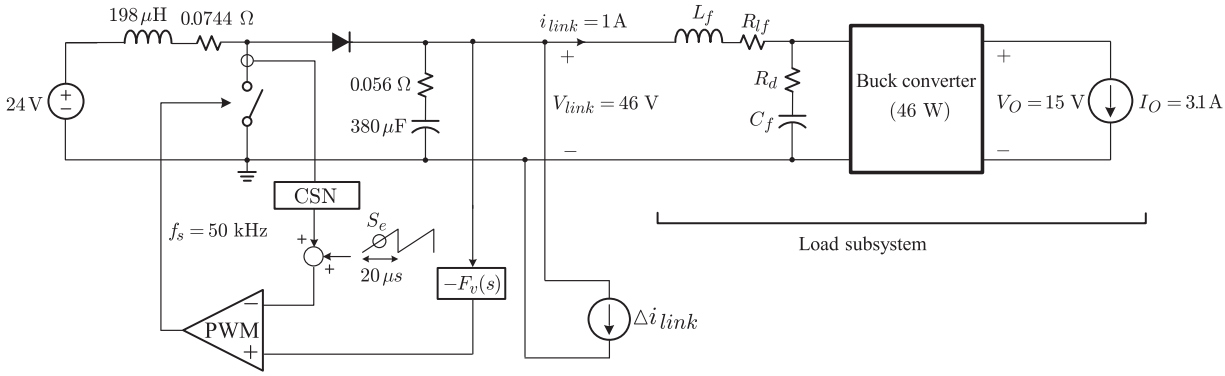


Fig. 9. Two-stage power conversion system. Peak current mode control is employed to the front-end boost converter. The CSN is the current sensing network with the dc gain of $R_i = 0.4$, $S_e = 6.26 \times 10^4$ V/s is the slope of the compensation ramp, PWM is the pulsewidth modulation block, and $F_v(s) = 2.77 \times 10^3 (1 + s/2\pi \cdot 242)/(s(1 + s/2\pi \cdot 4.98 \times 10^3))$ is the voltage feedback compensation.

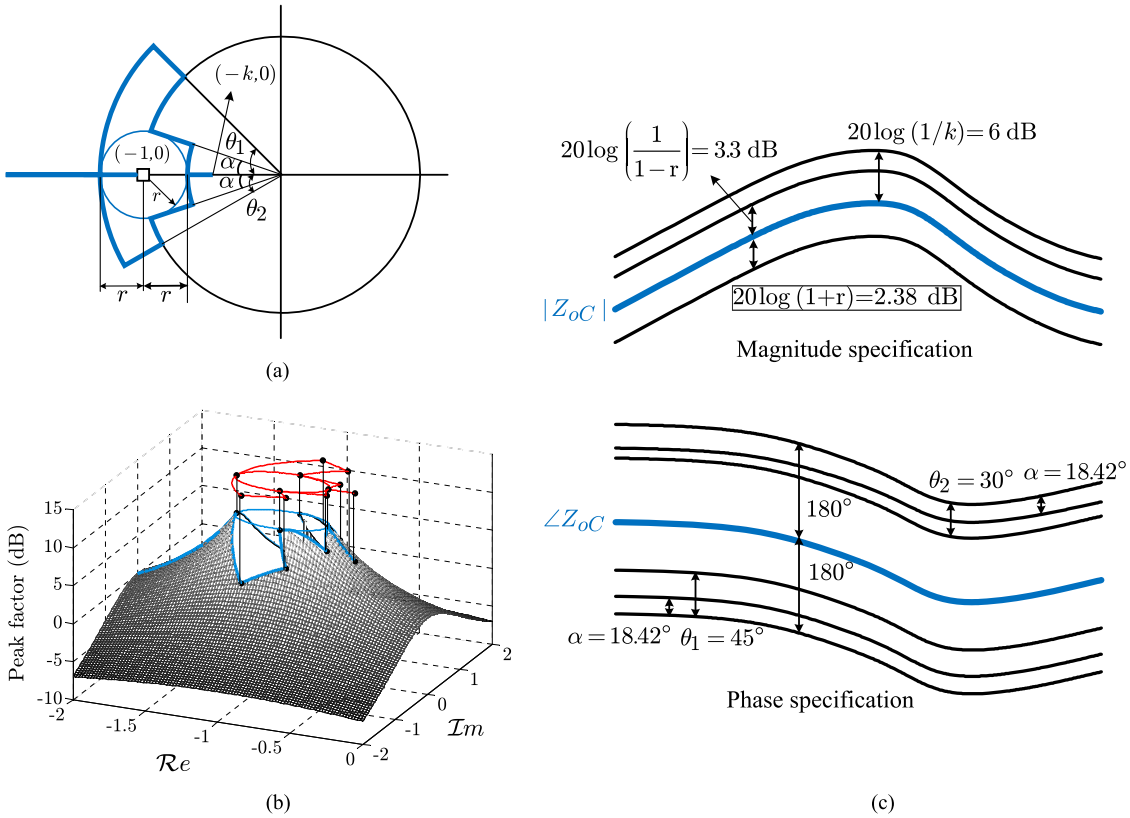


Fig. 10. Forbidden region, peak factor contour, and load impedance specification. (a) Forbidden region. (b) Peak factor contour. (c) Magnitude and phase specifications.

From these equations, it follows that

$$\Delta|Z_L|_1 = Y - X = 20\log\left(\frac{\omega_p'}{\omega_1}\frac{\omega_1}{\omega_p}\right) = 20\log\frac{\omega_p'}{\omega_p} \tag{20}$$

leading to the equation for the load impedance shaping

$$\frac{\omega_p'}{\omega_p} = 10^{\frac{\Delta|Z_L|_1}{20}}. \tag{21}$$

The load impedance shaping assumes that the phase characteristics of the load impedance, $\angle Z_L$, remain unchanged over the frequencies where $|Z_L|$ intersects with $|Z_{oC}|$. This assumption holds true when a sizable magnitude overlap exists between $|Z_L|$ and $|Z_{oC}|$. For such instances, the line filter pole ω_p appears at sufficiently low frequencies and the influence of moderate changes in ω_p is negligible when $\angle Z_L$ evaluated at mid frequencies.

C. Line Filter Redesign

The outcomes of the previous analyses are employed to redesign the line filter. From (17) and (21), the new value for the filter capacitor, C_f', is given by

$$C_f' = \frac{C_f}{10^{\frac{\Delta|Z_L|_1}{20}}} \tag{22}$$

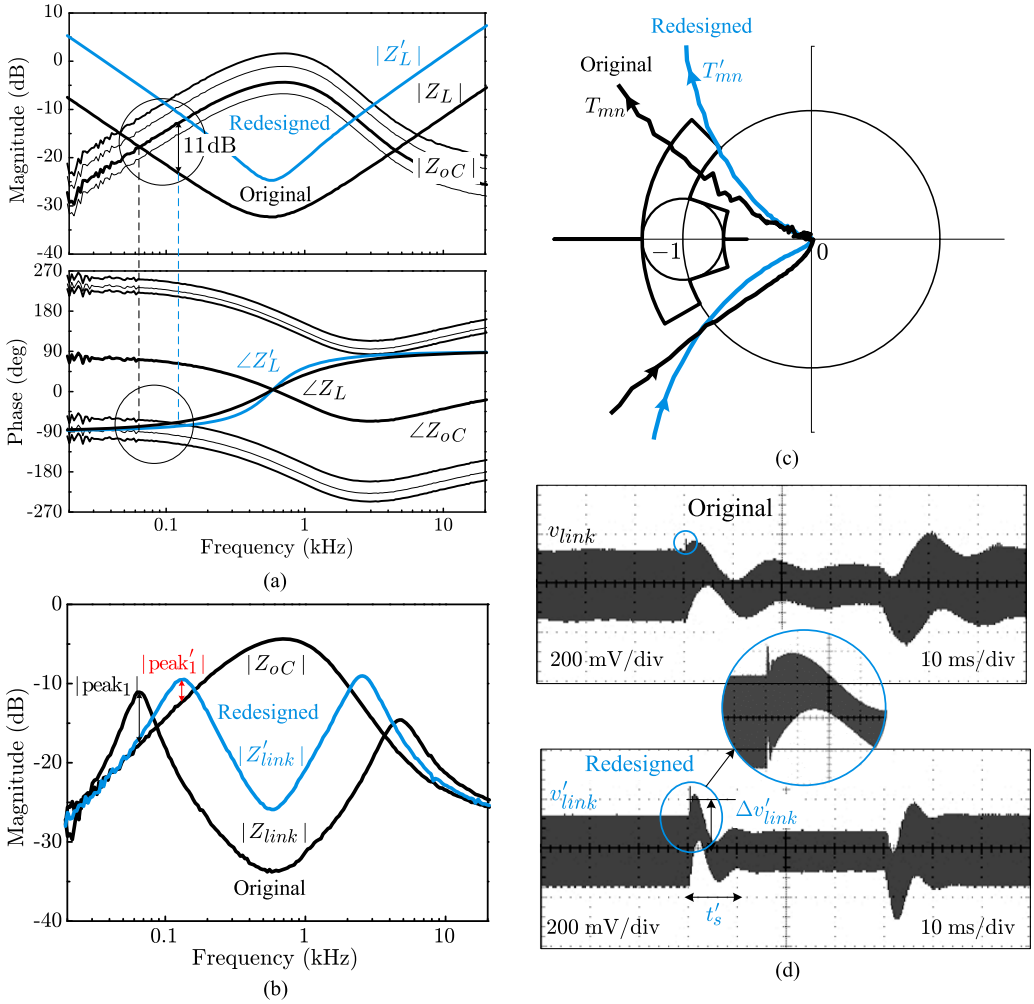


Fig. 11. Load Impedance specification, load impedance shaping, and dc-link dynamics. (a) Load impedance specification and load impedance shaping. (b) Measured trajectories of minor loop gains. (c) Measured dc-link impedances. The $|\text{peak}'_1|$ is predicted as 2.32 dB. (d) Measured dc-link voltage. Theoretical estimations of the overshoot and settling time are $\Delta v'_{\text{link}} = 0.1$ V and $t'_s = 12$ ms. The frequency-domain dynamics are measured with an impedance analyzer PSM1735-NumetriQ [24] using the measurement setups presented in [25].

where C_f is the original filter capacitor. Fig. 8(a) implies that the resonant frequency of the line filter remains the same during the load impedance shaping

$$\omega_o = \frac{1}{\sqrt{L_f C_f}} = \frac{1}{\sqrt{L'_f C'_f}}. \tag{23}$$

This equation leads to the new value of the filter inductor

$$L'_f = L_f \, 10^{\frac{\Delta |Z_L|_1}{20}}. \tag{24}$$

The quality factor is given by

$$Q' = \frac{1}{R'_{lf} + R'_{cf}} \sqrt{\frac{L'_f}{C'_f}}. \tag{25}$$

The quality factor can be selected between $0.5 < Q' < 1.5$ to avoid the resonant peaking in filter transfer functions. The parasitic resistance of the filter inductor, R'_{lf}, is minimized within practical limits to reduce the dc power loss. Once Q' and R'_{lf} are fixed, the damping resistor, R'_{cf}, is determined from (25) as

$$R'_{cf} = \frac{1}{Q'} \sqrt{\frac{L'_f}{C'_f}} - R'_{lf}. \tag{26}$$

VI. Experimental Validation

The two-stage power conversion system in Fig. 9 is built in order to test the load impedance shaping. Fig. 10(a) shows a forbidden region, which is constructed with $\theta_1 = 45°$, $\theta_2 = 30°$, $k = 0.5$, and $r = 0.316$. The angle α is determined as $\alpha = \sin^{-1} r = \sin^{-1} 0.316 = 18.42°$. Fig. 10(b) is the peak factor contour for the admissible trajectory of $T_{mn} = Z_{oC}/Z_L$. The upper limit of the peak factor is $20 \log(1/0.316) \approx 10$ dB. The forbidden region is converted into the load impedance specification in Fig. 10(c).

Fig. 11 shows the utility of the proposed load impedance specification. Fig. 11(a) is the load impedance specification, experimentally constructed using the upstream boost converter in Fig. 9. Two sets of the load impedance curves, $\{|Z_L|, \angle Z_L\}$

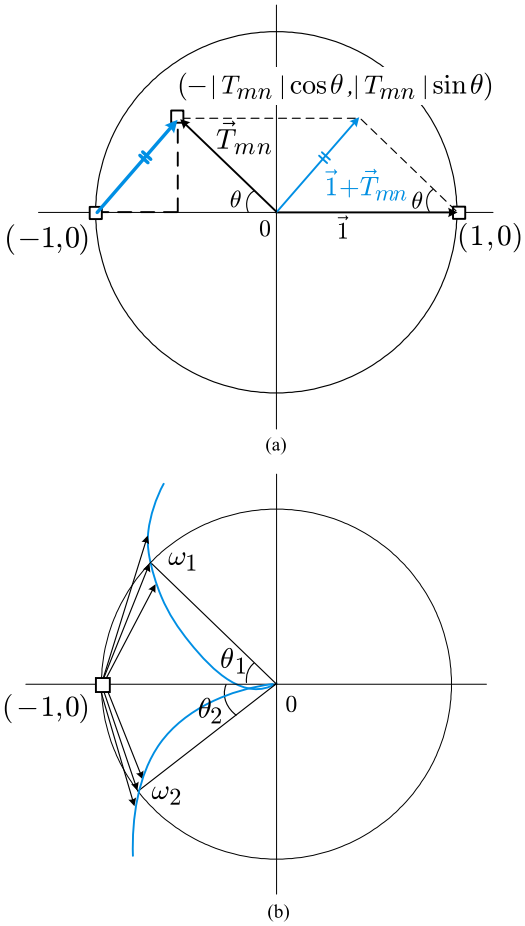


Fig. 12. Evaluation of vector length $|1+T_{mn}|$. (a) Vector length $|1+T_{mn}|$. (b) Evaluation of $|1+T_{mn}|$ near unit-circle crossover frequencies of T_{mn}.

and $\{|Z'_L|, \angle Z'_L\}$, are shown on the load impedance specification. The $|Z_L|$ and $\angle Z_L$ are measured with the original line filter of $L_f = 4.14\,\mu$H, $R_{lf} = 0.008\,\Omega$, $C_f = 19.9$ mF, and $R_{cf} = 0.02\,\Omega$. Fig. 11(a) indicates that the load impedance violates the specification at low frequencies. Fig. 11(b) confirms that $T_{mn} = Z_{oC}/Z_L$ trajectory trespasses the forbidden region at low frequencies.

Fig. 11(a) reveals that T_{mn} trajectory will bypass the forbidden territory, if $|Z_L|$ is raised by 11 dB, while $\angle Z_L$ stays approximately the same. Thus, the line filter is redesigned as $L'_f = 18\,\mu$H, $R'_{lf} = 0.021\,\Omega$, $C'_f = 4.38$ mF, and $R'_{cf} = 0.035\,\Omega$, based on the procedures discussed in Section V. The load impedance and minor loop gain with the redesigned line filter are represented by Z'_L and T'_{mn} in Fig. 11. The Z'_L meets the load impedance specification and T'_{mn} trajectory bypasses the forbidden region.

The dc-link impedance with the original line filter, $|Z_{\text{link}}|$, is compared with that of the redesigned line filter, $|Z'_{\text{link}}|$, in Fig. 11(c). The $|\text{peak}_1|$ in $|Z_{\text{link}}|$ is noticeably reduced to $|\text{peak}'_1|$ in $|Z'_{\text{link}}|$ due to the increased phase margin. The $|\text{peak}'_1|$ is close to the theoretical prediction of $20\log(1/(2-2\cos 45^\circ)) = 2.32$ dB.

The load impedance of the redesigned system has been elevated to meet the specification. This inevitably increases the dc-link impedance, as shown in Fig. 11(c), thereby producing a larger overshoot in the transient response of the dc-link voltage. The enlarged overshoot would propagate to the load converter. However, the line filter usually provides sufficient attenuation to the voltage spike and the input voltage of the load converter will not be notably affected by the overshoot. The audio susceptibility of the load converter would further reject the offshoots of the dc-link voltage overshoot. In fact, the impacts of the dc-link voltage overshoot will be nearly undetectable at the output voltage of the load converter.

The measured dc-link voltages, v_{link} and v'_{link}, in response to 1 A changes in i_{link} are shown in Fig. 11(d). The experimental results show good correlations with the analysis in Section II-C along with Fig. 3. The system with the original load subsystem makes the transient response oscillatory and sluggish. On the other hand, the redesigned load subsystem generates a larger overshoot due to an unavoidable increase in the dc-link impedance. The redesigned load subsystem meets the load impedance specification and yields a more stable and faster transient response. The overshoot and setting time of v'_{link} are close to the analytical predictions of $\Delta v'_{\text{link}} = 0.1$ V and $t'_s = 12$ ms, which are estimated from (11) and (12).

VII. Conclusion

This paper proposed a new load impedance specification for multistage dc power conversion systems. The proposed specification ensures aimed boundaries for the dc-link dynamics, robustness, and stability of the system. The new specification is less conservative and easier to implement, compared with the existing specifications. This paper also presented procedures of reshaping ill-conditioned load impedances to comply with the specification. While the load impedance shaping is presented using a specific filter structure, the procedure can be extended other filter topologies, including multistage filters and distributed filters for parallel load converters.

The procedures and benefits of the load impedance shaping are experimentally validated. The impacts of the phase margins of the minor loop gain, which are the most critical parameters of the load impedance specification, are demonstrated focusing on the intermediate dc-link dynamics.

Appendix

A. DC-Link Impedance Peaking

Referring to (1), the magnitude of the dc-link impedance is evaluated as

$$|Z_{\text{link}}| = |Z_{oC}|\frac{1}{|1+T_{mn}|} \tag{27}$$

Fig. 12(a) depicts the evaluation of $|1+T_{mn}|$. The vector length $|1+T_{mn}|$ corresponds to the distance between the $(-1,0)$ point and the $(-|T_{mn}|\cos\theta,\ |T_{mn}|\sin\theta)$ point

$$\begin{aligned}|1+T_{mn}| &= \sqrt{(1-|T_{mn}|\cos\theta)^2 + |T_{mn}|^2\sin^2\theta} \\ &= \sqrt{1+|T_{mn}|^2 - 2|T_{mn}|\cos\theta}.\end{aligned} \tag{28}$$

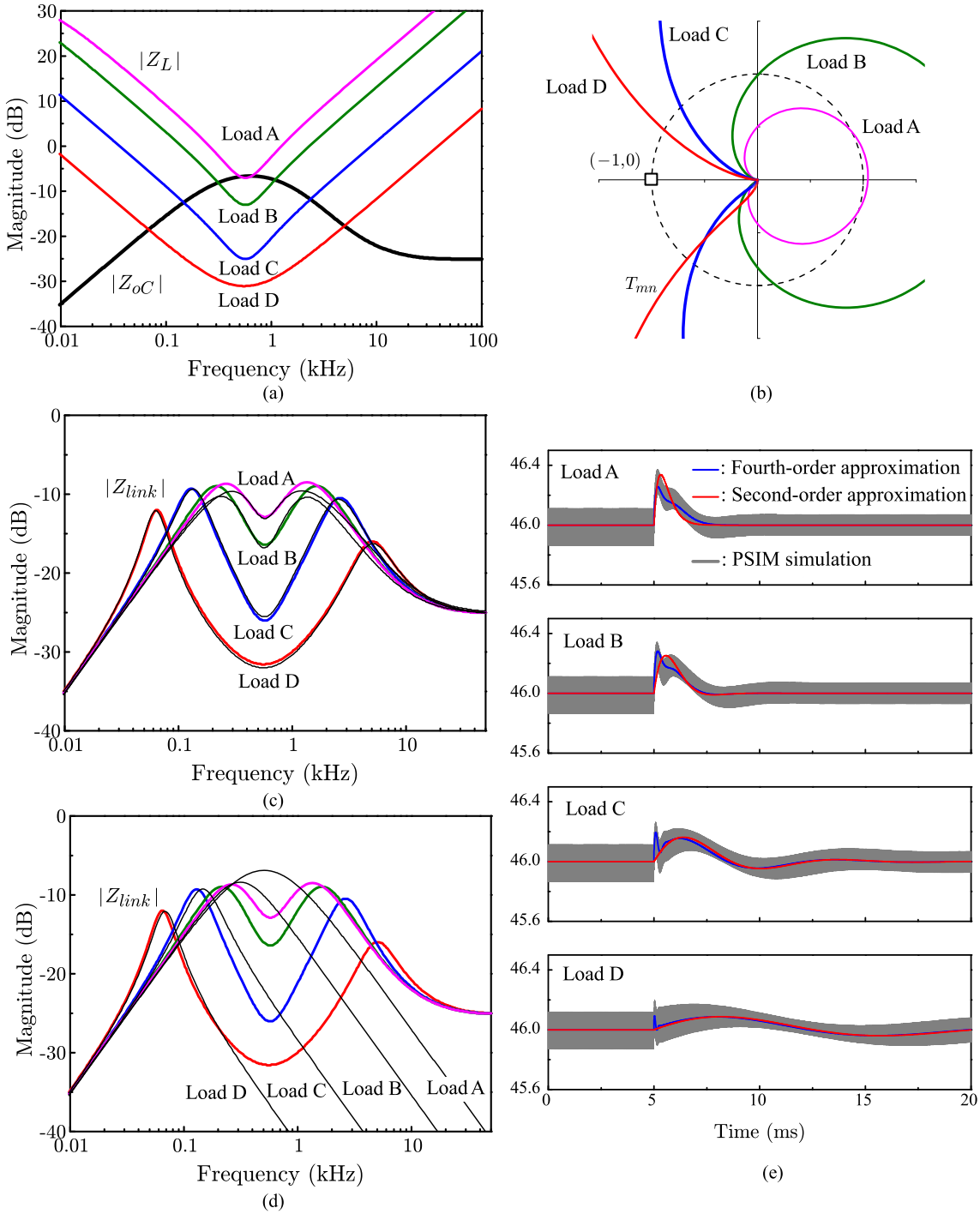


Fig. 13. DC-link dynamics with different load impedances. (a) Output impedance of the upstream converter and load impedances. (b) Polar plots of minor loop gains. (c) DC-link impedances and fourth-order approximations. (d) DC-link impedances and second-order approximations. (e) DC-link voltage in response to 1-A change in i_{link}.

The decibel scale $|Z_{\text{link}}|$ is given by

$$20\log|Z_{\text{link}}| = 20\log|Z_{oC}| + 20\log\frac{1}{\sqrt{1+|T_{mn}|^2-2|T_{mn}|\cos\theta}}. \tag{29}$$

This expression is approximated as

$$20\log|Z_{\text{link}}| \approx \begin{cases} 20\log|Z_{oC}| : \text{for frequencies where } |T_{mn}| \ll 1 \\ 20\log\frac{|Z_{oC}|}{|T_{mn}|} = 20\log|Z_L| : \text{for frequencies where } |T_{mn}| \gg 1 \end{cases} \tag{30}$$

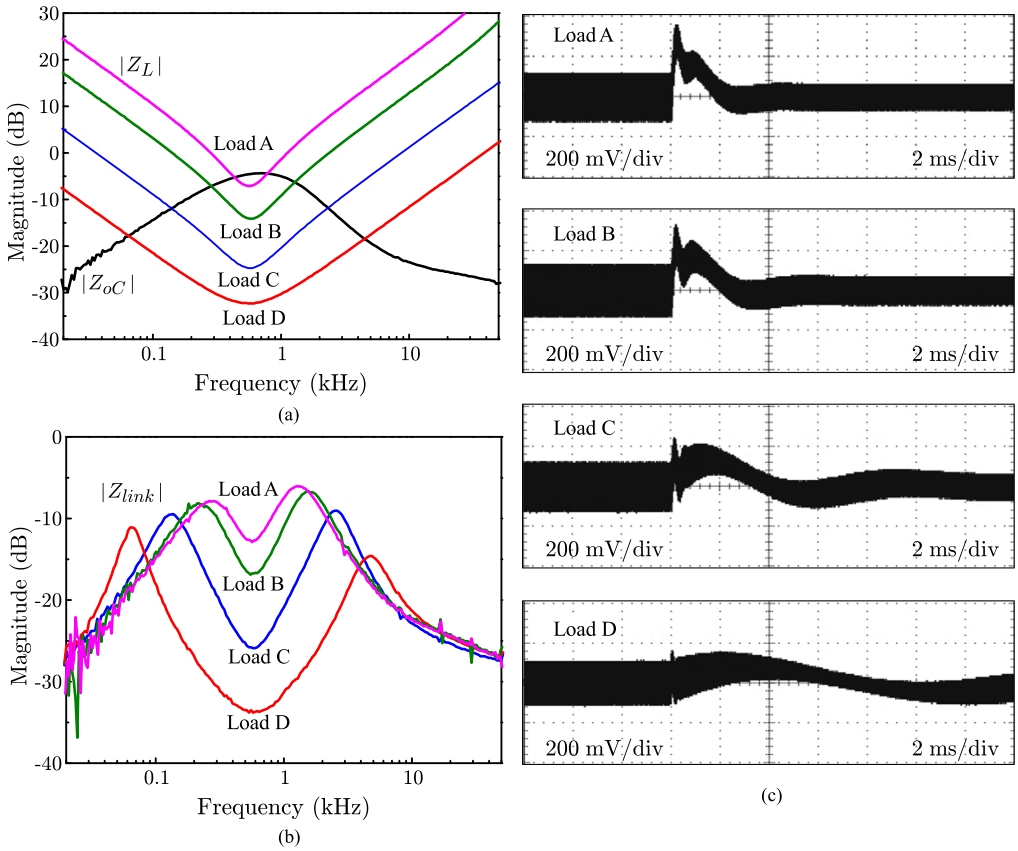


Fig. 14. Experimental verification of dc-link dynamics. (a) Output impedance of upstream converter and load impedances. (b) DC-link impedances. (c) DC-link voltages in response to 1-A change in i_{link}.

to provide the prediction of $|Z_{\text{link}}|$ at the frequencies where T_{mn} trajectory is remotely separated from the unit circle. However, around ω_1 and ω_2, where T_{mn} trajectory crosses the unit circle with $|T_{mn}| = 1$, the expression (29) is needed to predict the behavior of $|Z_{\text{link}}|$.

The second term in (29) becomes the magnitude of the peak in $|Z_{\text{link}}|$. Fig. 12(b) shows the vector length $|1 + T_{mn}|$ in the neighborhood of the unit-circle crossover frequencies. In the vicinity of ω_1 and ω_2, $|1 + T_{mn}|$ passes the minimum points and exhibits the peaks. The magnitude of the peak at ω_1 and ω_2, where $|T_{mn}| = 1$, is evaluated as

$$|\text{peak}_{1,2}| = 20 \log \frac{1}{\sqrt{2 - 2\cos\theta_{1,2}}}. \tag{31}$$

B. Second-Order Approximation of DC-Link Impedance

In Section II-C, the dc-link impedance was approximated as a second-order equation based on the low-frequency dynamics. The main assumption of this approximation is the condition $\omega_1 \ll \omega_2$. This section discusses the accuracy of the approximation when the assumption $\omega_1 \ll \omega_2$ is not fully met. It will be shown that the proposed approximation is reasonably accurate and useful in predicting the transient response of the dc-link voltage, when ω_1 and ω_2 are not remotely separated.

Fig. 13(a) shows $|Z_{oC}|$ of the upstream boost converter in comparison with the four different load impedances $|Z_L|$: Loads A–D. The load impedances originated from the buck load converter with four different line filter stages.

The polar plots of $T_{mn}(s)$ with the four different loads are shown in Fig. 13(b). As the impedance overlap intensifies, the phase margins successively decrease, as predicted from the phase characteristics of the impedances.

Fig. 13(c) compares the exact dc-link impedances $|Z_{\text{link}}|$ (thick colored lines) and the fourth-order approximations (thin lines). The fourth-order approximations are formulated based on the expression (5). The fourth-order approximation closely predicts both the low-frequency and high-frequency dynamics of $|Z_{\text{link}}|$.

Fig. 13(d) shows the second-order approximation of $|Z_{\text{link}}|$ based on (9). The approximated asymptotic plots match with the first peak of actual dc-link impedances for Loads C and D, where $\omega_1 \ll \omega_2$ condition is satisfied. As the impedance overlap lessens, this approximation becomes less accurate because the condition $\omega_1 \ll \omega_2$ is not fully met. Although there exist noticeable differences between the predictions and actual impedances, the second-order approximation provides relatively accurate and useful predictions of the transient response of the dc-link voltage.

The fourth-order and second-order approximations of the dc-link impedances are converted into the transient response of the dc-link voltage using MATLAB software and compared with the results of the exact time-domain PSIM simulations [26]. Fig. 13(e) displays the results of this analysis, where a 1-A change in i_{link} is assumed. The v_{link} waveforms produced

from the fourth-order approximations produce both the high-frequency and low-frequency behavior of the time-domain simulations. For Loads A and B, where the condition $\omega_1 \ll \omega_2$ is not fully met, some deviations can be observed. On the other hand, v_{link} waveforms of the second-order approximation only generate the low-frequency behavior of v_{link}. This analysis shows that the second-order approximation of Z_{link} provides reasonably accurate predictions for the low-frequency dc-link dynamics.

Fig. 14 provides the experimental verification of the dc-link dynamics with the four different load subsystems, Loads A–D in Fig. 13. Fig. 14(a) shows the measured load impedances, while Fig. 14(b) displays the dc-link impedances. The dc-link voltages in response to 1-A change in i_{link} are shown in Fig. 14(c). Close connections are found when Figs. 13 and 14 are compared.

REFERENCES

[1] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proc. IEEE Ind. Appl. Soc.*, Oct. 1976, pp. 366 –382.

[2] C. Wildrick, F. Lee, B. Cho, and B. Choi, "A method of defining the load impedance specification for a stable distributed power system," *IEEE Trans. Power Electron.*, vol. 10, no. 3, pp. 280–285, May 1995.

[3] Y. Kim, S. K. Pidaparthy, and B. Choi, "A load impedance specification of dc power systems for desired dc link dynamics and reduced conservativeness," in *Proc. IEEE 18th Workshop Control Model. Power Electron.*, Jul. 2017, pp. 1–6.

[4] S. Sudhoff, S. Glover, P. Lamm, D. Schmucker, and D. Delisle, "Admittance space stability analysis of power electronic systems," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 36, no. 3, pp. 965–973, Jul. 2000.

[5] X. Feng, J. Liu, and F. Lee, "Impedance specifications for stable dc distributed power systems," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 157–162, Mar. 2002.

[6] S. Vesti, T. Suntio, J. A. Oliver, R. Prieto, and J. A. Cobos, "Impedance-based stability and transient-performance assessment applying maximum peak criteria," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2099–2104, May 2013.

[7] A. Riccobono and E. Santi, "Comprehensive review of stability criteria for dc power distribution systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3525–3535, Sep. 2014.

[8] S. K. Pidaparthy and B. Choi, "Stability analysis of PWM converters connected to general load subsystems," in *Proc. IEEE 9th Int. Conf. Power Electron., ECCE Asia*, Jun. 2015, pp. 1033–1040.

[9] S. K. Pidaparthy, B. Choi, H. Kim, and Y. Kim, "Stabilizing effects of load subsystem in multistage dc-to-dc power conversion systems," *IEEE J. Emerg. Sel. Topics Power Electron*, vol. 5, no. 4, pp. 1589–1603, Dec. 2017.

[10] B. Choi, *Pulsewidth Modulated DC-to-DC Power Conversion: Circuits, Dynamics, and Control Designs*. New York, NY, USA: Wiley, 2013.

[11] K. Ogata, *Modern Control Engineering*, 4th ed. Upper Saddle River, NJ, USA: Prentice Hall, 2001.

[12] S. Erich and W. Polivka, "Input filter design criteria for current-programmed regulators," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 143–151, Jan. 1992.

[13] Y. Jang and R. Erickson, "Physical origins of input filter oscillations in current programmed converters," *IEEE Trans. Power Electron.*, vol. 7, no. 4, pp. 725–733, Oct. 1992.

[14] M. Kazimierczuk and I. Cravens, R., "Input impedance of closed-loop PWM buck-boost dc-dc converter for CCM," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 3, Apr. 1995, pp. 2047–2050.

[15] S. Kriventsov and J. Mayer, "An exact expression for the input impedance of the buck converter in continuous conduction mode," in *Proc. 32nd Annu. IEEE Power Electron. Spec. Conf.*, 2001, vol. 1, pp. 351–356.

[16] S. K. Pidaparthy and B. Choi, "Input impedances of PWM DC–DC converters: Unified analysis and application example," *J. Power Electron.*, vol. 16, no. 6, Nov. 2016.

[17] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. New York, NY, USA: Springer, 2001.

[18] X. Zhang, X. Ruan, and Q.-C. Zhong, "Improving the stability of cascaded DC/DC converter systems via shaping the input impedance of the load converter with a parallel or series virtual impedance," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7499–7512, Dec. 2015.

[19] X. Zhang, Q. C. Zhong, and W. L. Ming, "Stabilization of cascaded DC/DC converters via adaptive series-virtual-impedance control of the load converter," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6057–6063, Sep. 2016.

[20] X. Song, S. Zheng, B. Han, C. Peng, and X. Zhou, "Active damping stabilization for high-speed BLDCM drive system based on band-pass filter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5438–5449, Jul. 2017.

[21] Y. Gu, D. Zhang, X. Wu, and X. Zhang, "Research on stability improvement of the cascaded dc-dc converters based on AC signal sampling control method," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4547–4559, May 2018.

[22] X. Zhang, X. Ruan, H. Kim, and C. K. Tse, "Adaptive active capacitor converter for improving stability of cascaded dc power supply system," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1807–1816, Apr. 2013.

[23] H. J. Kim, S. W. Kang, G. S. Seo, P. Jang, and B. H. Cho, "Large-signal stability analysis of DC power system with shunt active damper," *IEEE Trans. Power Electron.*, vol. 63, no. 10, pp. 6270–6280, Oct. 2016.

[24] PSM1735-NumetriQ *Frequency Response Analyzer*, Newtons4th Ltd., Leicester, U.K., 2005.

[25] R. Ridley, *Frequency Response Measurements* (Power Supply Design). Bradenton, FL, USA: Ridley Engineering Inc., 2011. [Online]. Available: https://books.google.co.kr/books?id=Nc-itwAACAAJ

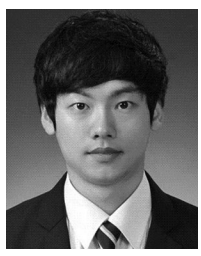
[26] *PSIM User's Guide*, version 9.0 ed., Powersim Inc., Mar. 2010.

Syam Kumar Pidaparthy (S'17) received the B.Tech. degree in electrical and electronics engineering from Acharya Nagarjuna University, Guntur, India, in 2010, and the M.S. and the Ph.D. degrees in circuits and embedded systems engineering from Kyungpook National University, Daegu, Korea, in 2013 and 2017, respectively.

He is currently working as a Postdoctoral Researcher with Kyungpook National University. His current research interests include the modeling, dynamic analysis, and control design of large-scale dc-to-dc power conversion systems.

Byungcho Choi (S'90–M'91) received the B.S. degree in electronics from Hanyang University, Seoul, Korea, in 1980, and the M.S. and the Ph.D. degrees in electrical engineering from Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, in 1988 and 1992, respectively.

In 1996, he joined the School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, Korea, where he is currently a Professor. His research interest includes modeling and design optimization of high-frequency power converters for portable electronics, computer power systems, and distributed power systems. He is the author of the book *Pulsewidth Modulated DC-to-DC Power Conversion* (Wiley, Hoboken, NJ, USA).



Yeonjung Kim received the B.S. degree in electronics and the M.S. degree in circuits and embedded systems engineering from Kyungpook National University, Daegu, Korea, in 2016 and 2018, respectively.

He is currently working on the advanced air conditioners, LG electronics, Changwon, Korea. His research interests include high-speed switching dc-to-dc power converters, electromagnetic compatibility optimization, and designing printed circuit board.