A Family of PWM Control Strategies for Single-Phase Quasi-Switched-Boost Inverter

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***Abstract*—This paper proposed a novel family of pulsewidth modulation (PWM) strategies for single-phase quasi-switched boost inverter (qSBI). By combining shoot-through (ST) mode in the inverter's switches and the turning-ON state of an additional switch, the qSBI produced a high voltage gain without adding any passive components. Compared to the conventional PWM strategy for the same input and output voltage gain, the introduced PWM strategies for qSBI could reduce voltage stress across semiconductors and capacitor with the following additional merits: having smaller high-frequency inductor current and capacitor voltage ripples, using high modulation index with low ST duty cycle, and having higher efficiency. Circuit analysis, operating theories, and simulation results of the single-phase qSBI with the introduced PWM5 strategy are shown. A 500-W laboratory prototype was constructed and the effectiveness of the introduced PWM strategy was validated. The qSBI with the proposed PWM strategies is suitable for applications where the required voltage gain lies between 2 and 3.**

***Index Terms*—Pulsewidth modulation (PWM) strategy, quasi-switched-boost inverter (qSBI), quasi-Z-source inverter (qZSI), voltage gain.**

I. Introduction

In THE design process of power inverter for renewable energy systems applications, the reliability, efficiency, and volume are major factors. The two-stage voltage source inverter (VSI) with a boost converter [1] is the conventional solution for renewable energy systems. To solve a shoot-through (ST) problem of VSIs where both upper and lower switches in the same branch of H-bridge circuit cannot switch ON simultaneously, Z-source/quasi-Z-source inverters (ZS/qZSIs) have been proposed in [2]–[7]. Because ZS/qZSIs present a high reliability with ST immunity and buck-boost voltage ability, they are suitable for applications of the renewable energy sources. However, voltage gain in ZS/qZSIs is not high. It depends on the modulation index of the H-bridge circuit. To get a desired boost voltage demand, a large ST duty cycle is utilized. As a result, the modulation index is small. When a low modulation index is used in ZS/qZSIs, total harmonic distortion (THD) value and voltage gain at the output are increased and decreased, respectively. The boost factor in the conventional qZSI is given as

$$B_1 = V_{\mathrm{PN}}/V_g = 1/(1 - 2D) \tag{1}$$

where D and V_{PN} are ST duty cycle and dc-bus voltage across the H-bridge, respectively.

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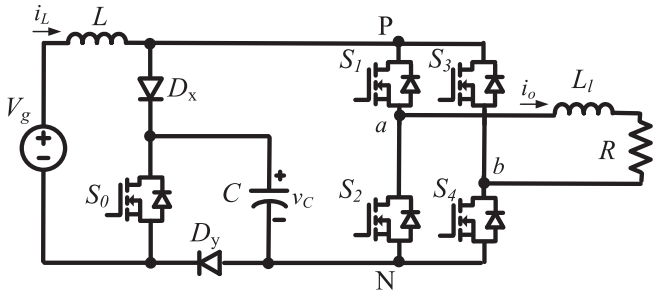

Fig. 1. Single-phase single-stage qSBI.

For applications where the high voltage gain is required, the capacitor, inductor, transformer, and diode have been inserted into the power circuit of qZSIs, resulting in switched-inductor qZSI [4], enhanced-boost ZSI [5], trans-ZSI [6], asymmetrical Γ-source inverter [7], and improved trans-ZSI [8]. Nevertheless, topologies of these qZSIs increase the cost, volume, and weight of the power circuit because a large number of passive elements are used [4]–[8]. To decrease the cost, weight, and volume of the power circuit, a family of quasi-switched-boost inverters (qSBIs) has been introduced [9]–[14]. These qSBIs use one less *LC* pair with the same characteristics as qZSI. However, qSBI has the following merits over qZSI [11]: lower passive elements, smaller current stress on semiconductor devices, lower power loss, and higher efficiency. Fig. 1 presents a single-phase qSBI [9] using five switches $(S_0 - S_4)$, two diodes (D_x and D_y), one capacitor (C), one inductor (L), and an inductive load (R and L_l). The boost factor in qSBI is the same as that in qZSI as expressed in (1). Similar to qZSI, passive elements are also added to qSBI to increase the boost factor. For instance, switched-inductor qSBI with increasing cost and volume has been proposed in [13]. Transformer-based qSBI with a spike on dc-bus voltage due to leakage inductance in the transformer has also been introduced in [14] and [15].

Recently, different pulsewidth modulation (PWM) techniques [16]–[27] have been applied to the qZS/qSBIs to improve the inverter's performance. Maximum boost (MB) control [16] and maximum constant boost (MCB) control [17] strategies have

been used to optimize the voltage gain of the three-phase ZS/qZSI. A third-harmonic injection PWM strategy [17] has been applied to the three-phase ZS/qZSI to extend the operation range of the modulation index. Nevertheless, capacitor voltage and inductor current ripples are very high when MB and MCB control strategies are used. A PWM strategy for the three-phase ZSIs with minimum inductor current ripple has been discussed [19]. It can rearrange ST time intervals according to active state and zero state time intervals. To maximize boost capability, an improved PWM method for the three-phase ZSI has been presented in [20] generating six-time-line-frequency ripple at the dc side. The space vector modulation (SVM) techniques for the three-phase qZSI have been also introduced in [21] based on inserting the ST state number of two, four, or six into the conventional SVM. To enhance the performance of the three-phase ZSIs, a simple-boost modified SVM method was proposed in [22] with a single switch commutation at a time. The SVM was extended to the single-phase ZSI as presented in [23]. To decrease power loss without increasing voltage gain, a hybrid PWM strategy for single-phase qZS grid-tie photovoltaic system has been presented [24]. To reduce the switching losses of the qZSI, a dual switching frequency modulation has been introduced in [25] with unchanged voltage gain. In [26], a maximum control boost method was used to improve qSBI by modifying the ST control signal. In addition, Nguyen and Choi [27] introduced a PWM strategy to get better modulation index of the qSBI.

In practice, the qZSI has a high performance than the traditional two-stage inverter with the boost converter when the voltage gain is in the range of 1–1.5 [28]. In the case of higher voltage gain, the qSBI is a better solution than the qZSI as presented in [11]. Because the qSBI has the same operating principle as the qZSI, all PWM strategies [16]–[27] for qZSI can be used for qSBI. For instance, a simple boost control method is usually applied to qSBI topologies [9]–[12] to control five switches where a constant ST control signal is used. Nevertheless, the ST state in conventional PWM control methods [9]–[12] was generated by turning ON all five switches at the same time. As a result, the operating frequency of the input inductor in the qSBI is the same as that of switch S_0. Moreover, the voltage gain of the qSBI under the conventional PWM strategies is unchanged when compared to that of the qZSI. In fact, the voltage gain of the qSBI can be improved by controlling the additional switch S_0 that is not used in the qZSI.

In this paper, a family of PWM strategies is introduced to reduce the high-frequency (HF) inductor current ripple of the single-phase qSBI without adding any passive components while improving voltage gain. In comparison with the conventional PWM strategy for the qSBI, the introduced PWM strategy uses a greater modulation index to generate the same voltage gain. Therefore, voltage stress on semiconductors and capacitor and THD value of the load current under the proposed PWM methods are decreased significantly. Section II reviews the conventional PWM control strategy for the single-phase qZSI and qSBI. The proposed PWM control strategies are presented in Sections III. Section IV presents a comprehensive comparison between the introduced PWM strategy and the traditional PWM strategy for the single-phase qSBI. In Section V, simulation and experimental verifications are presented to verify the analysis.

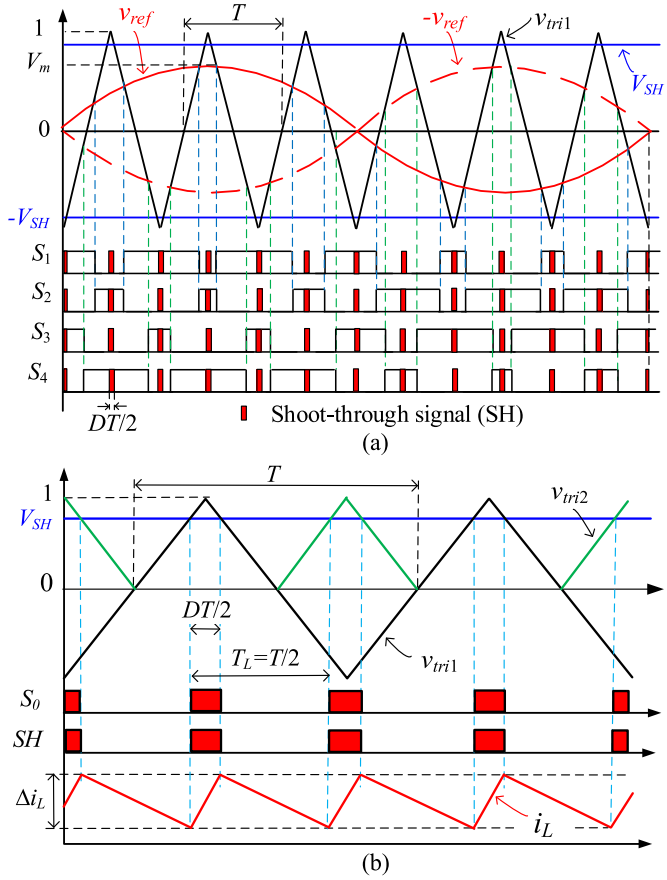

Fig. 2. Conventional PWM1 control method for the single-phase qZSI and qSBI. (a) H-bridge signal generation. (b) S_0 signal generation.

II. Conventional PWM Control Method for the qZSI/qSBI

Fig. 2 illustrates the conventional PWM strategy for the single-phase qZSI and qSBI [9]. As indicated in Fig. 2(a), two reference signals, v_{ref} and $-v_{\text{ref}}$, are used to compare to an HF carrier waveform, v_{tri1}, to create control signals for H-bridge switches $(S_1 - S_4)$. To produce an ST control signal, a fixed signal (V_{SH}) is used to compare to another carrier waveform (v_{tri2}) with a double frequency of v_{tri1} as shown in Fig. 2(b). This constant ST control signal is used to control both S_0 and H-bridge switches. As a result, the number of ST states per half of the switching period $(T/2)$ of v_{tri1} is 1, where T is the switching period of v_{tri1}. The number of storage/delivery time of the inductor current during $T/2$ is also 1. Therefore, the conventional control method is also called PWM1 method.

Because the modulation index (M) cannot be over $(1 - D)$, M is low when a large D is used to achieve a great boost voltage. Using a low M will enhance the THD value and decrease the overall inverter voltage gain. The boost factor in the PWM1 control strategy used for qZSI/qSBI is given in (1). In the conventional PWM1 method for the qZSI/qSBI, the HF inductor current ripple is fixed. It depends on the switching fre-

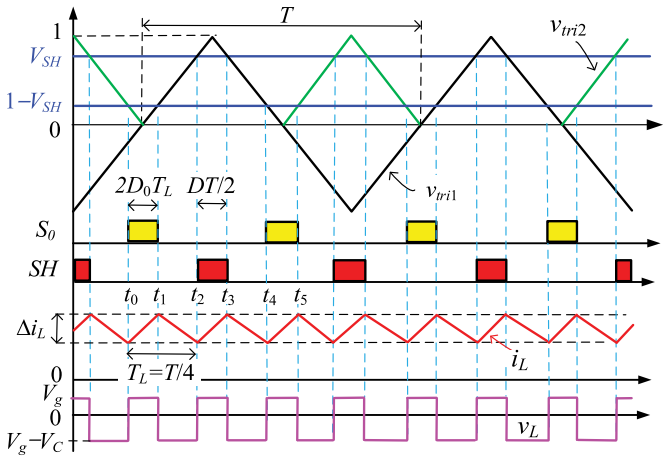

Fig. 3. Proposed PWM2 method for the single-phase qSBI.

quency. To limit the inductor current ripple to reduce the cost and volume of the inductor in the qZS/qSB network, the switching frequency of the H-bridge inverter should be increased. Using a high switching frequency will increase the switching loss in the H-bridge switches of qZSI/qSBI. Note that a low-frequency (LF) inductor current ripple of the impedance source network can be eliminated by using an active filter method as described previously [29].

Unlike the qZSI, the qSBI uses one more switch to reduce passive elements in the impedance-source network. In the conventional PWM1 control method for the qSBI, the switch S_0 is simultaneously turned ON with H-bridge switches in the ST state as shown in Fig. 2. Because all switches are switched ON simultaneously, the conduction loss in the ST state is high. In the qSBI, H-bridge switches are used to produce sinusoidal voltage at the output, while switch S_0 is used to boost the voltage at the dc-bus. Therefore, switch S_0 and H-bridge switches in the qSBI can be controlled individually. In addition, operating frequency of the inductor can be increased by controlling switch S_0.

III. Proposed PWM Control Methods for the qSBI

A. Proposed PWM2 Method

Fig. 3 shows the proposed PWM2 control strategy for the single-phase qSBI. A fixed signal, V_{SH}, is used to compare to v_{tri2} with a twofold frequency of v_{tri1} to produce ST control signal (SH) for H-bridge switches. Another fixed signal with a value of $(1 - V_{SH})$ is used to compare to v_{tri2} to produce the control signal for switch S_0. In comparison with the conventional PWM1 method, switch S_0 control signal in the proposed PWM2 method is shifted to the time interval of $T/4$, while control signals of H-bridge switches are unchanged as shown in Fig. 2(a). As a result, the number of storage/delivery time of the inductor current during $T/2$ is two. Therefore, the HF inductor current ripple in the introduced PWM2 strategy is half of that of the PWM1 strategy. In addition, the period of the input inductor current, T_L, is one fourth of the switching period, T, as shown in Fig. 3.

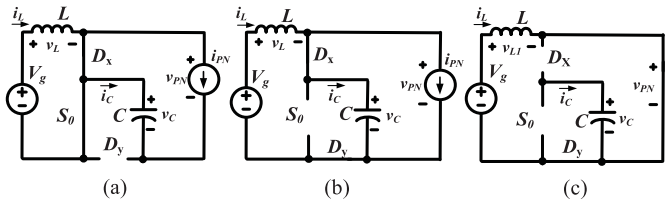

Fig. 4. Operating states of the qSBI with introduced PWM strategies. (a) NST state 1. (b) NST state 2. (c) ST state.

Fig. 4 illustrates operating states of the single-phase qSBI under the introduced PWM2 strategy. In comparison with the conventional PWM1 control strategy, the qSBI with the introduced PWM2 strategy has an additional state as indicated in Fig. 4(a). In the non-ST (NST) state 1 ($t_0 - t_1$ and $t_4 - t_5$; see Fig. 3), the switch S_0 is turned ON and operating states of the H-bridge circuit are active and zero as shown in Fig. 4(a). The diode D_x is conducting, while D_y is blocking. The capacitor C is discharged, while the inductor L stores energy from the input voltage source. Time interval in the NST state 1 is $2D_0 \cdot T_L$, where $2D_0$ is the duty cycle of switch S_0. The following is obtained:

$$L\frac{di_L}{dt} = V_g \quad \text{and} \quad C\frac{dv_C}{dt} = -I_{\text{PN}}. \tag{2}$$

In NST state 2 ($t_1 - t_2$ and $t_3 - t_4$; see Fig. 3), the switch S_0 is turned OFF, while both diodes D_x and D_y are conducting as shown in Fig. 4(b). The capacitor C is charged from V_g, while the inductor L delivers energy to the load. The inverter bridge circuit is tantamount to a current source, i_{PN}. In NST state 2, the time interval is $(1 - D_0 - D) \cdot T/2$, where D represents the ST duty cycle in the H-bridge circuit. The following is obtained:

$$L\frac{di_L}{dt} = V_g - V_C \quad \text{and} \quad C\frac{dv_C}{dt} = I_L - I_{\text{PN}}. \tag{3}$$

During the ST state ($t_2 - t_3$; see Fig. 3), all switches in the H-bridge circuit are switched ON, while S_0 is switched OFF as shown in Fig. 4(c). The diode D_x is blocking, while D_y is conducting. The capacitor C is disconnected to the circuit. In this state, the inductor L stores energy and the time interval is $D \cdot T/2$. The following is obtained:

$$L\frac{di_L}{dt} = V_g \quad \text{and} \quad C\frac{dv_C}{dt} = 0. \tag{4}$$

Using principles of capacitor amp-second balance and inductor volt-second balance, from (2) to (4), the following is obtained:

$$V_{\text{PN}} = V_C = \frac{V_g}{1 - D_0 - D} \quad \text{and} \quad I_L = \frac{1 - D}{1 - D_0 - D} I_{\text{PN}}. \tag{5}$$

The boost factor of the qSBI with the proposed PWM2 strategy can be expressed as (6)

$$B_2 = V_{\text{PN}}/V_g = 1/(1 - D_0 - D). \tag{6}$$

Comparing (6) to (1), the proposed PWM2 method has the same boost factor as the PWM1 method when $D_0 = D$.

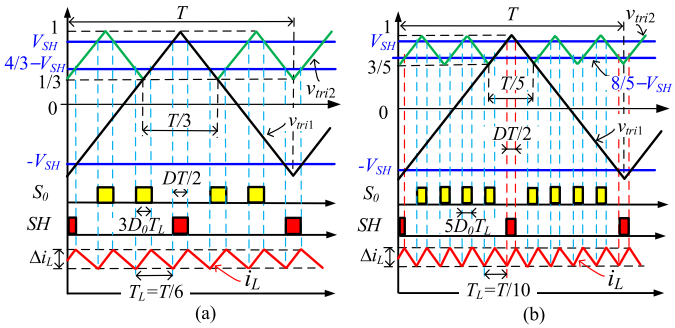

Fig. 5. Proposed PWM methods for the qSBI. (a) PWM3. (b) PWM5.

B. Proposed PWM3 Method

Fig. 5(a) shows the proposed PWM3 control strategy for the single-phase qSBI. Similar to PWM1 and PWM2 methods, two fixed signals, V_{SH} and $-V_{SH}$, are used to compare to v_{tri1} to generate the ST control signal for H-bridge switches. To produce control signal for switch S_0, two fixed voltages, V_{SH} and $(4/3 - V_{SH})$, are compared to v_{tri2}. Note that the frequency of v_{tri2} is three times of v_{tri1} and the peak-to-peak value of v_{tri2} is 2/3. The compared signal from v_{tri2} and the ST control signal (SH) are then integrated through XOR logic gate to control switch S_0. The number of storage/delivery time of the inductor current during $T/2$ with the proposed PWM3 method is three. Therefore, the HF inductor current ripple in the proposed PWM3 method is decreased three times compared to that of the PWM1 method. Similar to the proposed PWM2 control strategy, the qSBI under the proposed PWM3 control strategy also has three operating states as indicated in Fig. 4. In the half-switching period (T/2), the total time interval in NST state 1 is $2D_0 \cdot T/2$. The time interval in the NST state 2 is $(1 - 2D_0 - D) \cdot T/2$, while that in the ST state is $D \cdot T/2$. Using the inductor volt-second balance theory in steady state, the boost factor is obtained as

$$B_3 = 1/\left(1 - 2D_0 - D\right). \tag{7}$$

Comparing (7) to (1) and (6), the boost factor of the qSBI with the introduced PWM3 strategy is improved.

C. Extending to PWMn Control Method for qSBI

By changing the peak-to-peak value and frequency of v_{tri2}, various PWM control methods can be obtained. From Figs. 2, 3, and 5, the triangle waveform, v_{tri1} is

$$v_{\mathrm{tri1}}(t) = \begin{cases} 4t/T - 1, & 0 \le t < 0.5T \\ -4t/T + 3, & 0.5T \le t < T. \end{cases} \tag{8}$$

In the proposed PWMn $(n = 2, 3, 4, \ldots)$ method, the PWM generation depends on v_{tri2}. The peak-to-peak value of v_{tri2} is $2/n$, and the frequency of v_{tri2} is n-times that of v_{tri1}. The function of v_{tri2} is expressed as

$$v_{\mathrm{tri2}}(t) = \begin{cases} \begin{cases} \frac{-4}{nT_n}t + 1, & 0 \le t < \frac{T_n}{2} \\ \frac{4}{nT_n}t + \frac{n-4}{n}, & \frac{T_n}{2} \le t < T_n \end{cases}, \\ \qquad\qquad \text{when } n : \text{even} \\ \begin{cases} \frac{4}{nT_n}t + \frac{n-2}{n}, & 0 \le t < \frac{T_n}{2} \\ \frac{-4}{nT_n}t + \frac{n+2}{n}, & \frac{T_n}{2} \le t < T_n \end{cases}, \\ \qquad\qquad \text{when } n : \text{odd} \end{cases} \tag{9}$$

where T_n is the time period of v_{tri2} in the PWMn method.

In the half-switching period (T/2), the number of turning ON/OFF time of the switch S_0 is $(n - 1)$, while that of ST states in the H-bridge switches is always 1. Therefore, the HF ripple of the inductor current in the proposed PWMn method is reduced n-times to that in the conventional method. Moreover, the operating frequency of the input inductor is $2n$-times the operating frequency of H-bridge switches. The sum of time interval in NST state 1 is $(n-1) \cdot D_0 \cdot T/2$. In NST state 2, the time interval is $[1 - (n-1)D_0 - D] \cdot T/2$. In ST state, the time interval is $D \cdot T/2$. Using the inductor volt-second balance theory, the boost factor of the proposed PWMn method is

$$B_n = V_{\mathrm{PN}}/V_g = 1/(1 - (n\ -\ 1)\, D_0 - D) \tag{10}$$

where $n = 2, 3, 4, \ldots$.

As an example, the proposed PWM5 control method is used to prove the effectiveness of the introduced PWM strategies for the qSBI in this paper. Fig. 5(b) shows the proposed PWM5 control strategy for the single-phase qSBI. It can be seen from Fig. 5(b) that the peak-to-peak inductor current is remarkably decreased in comparison with that of the PWM1 strategy.

Similar to the proposed PWM2 and PWM3 control strategies, the qSBI with the proposed PWM5 strategy also has three operating states as presented in Fig. 4. The sum of time interval in NST state 1 is $4D_0 \cdot T/2$. The time interval in NST state 2 is $(1 - 4D_0 - D) \cdot T/2$. The time interval in ST state is $D \cdot T/2$. Applying balance principles to the capacitor and inductor in steady state, the following is obtained:

$$V_C = \frac{V_g}{1 - 4D_0 - D} \quad \text{and} \quad I_L = \frac{1\ -\ D}{1 - 4D_0 - D} I_{\mathrm{PN}}. \tag{11}$$

The dc-bus voltage equals either the capacitor voltage in NST states or zero in ST state. Thus, the peak voltage at the dc-bus of qSBI with the proposed PWM5 method is expressed as

$$V_{\mathrm{PN}} = V_C = V_g/\left(1 - 4D_0 - D\right). \tag{12}$$

The boost factor of the qSBI with the introduced PWM5 strategy is expressed as

$$B_5 = V_{\mathrm{PN}}/V_g = V_C/V_g = 1/\left(1 - 4D_0 - D\right). \tag{13}$$

To minimize the inductor current ripple as shown in Fig. 5(b), D_0 should be equal to D. Thus, the boost factor of qSBI with the introduced PWM5 strategy is $1/(1 - 5D)$.

The amplitude of the ac output voltage is expanded as

$$\hat{v}_{\,o} = M \cdot V_{\mathrm{PN}} = \frac{M \cdot V_g}{1\ -\ 5D}. \tag{14}$$

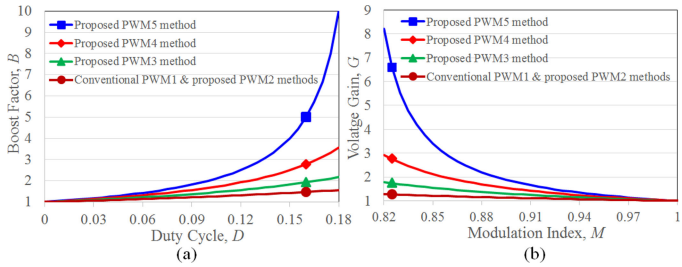

Fig. 6. (a) Boost ratio. (b) Voltage gain with different PWM methods.

The inverter voltage gain can be expressed as

$$G = M \cdot B = \hat{v}_o / V_g \tag{15}$$

where B represents the boost factor as shown in (1) or (10).

Similar to the conventional PWM1 strategy, ST interval must be inserted into the zero state to guarantee a high-quality output. Thus, the amplitude of v_{ref} must be less than V_{SH}. Therefore, the maximum value of D is $(1-M)$. The voltage gain $(M \cdot B)$ of the conventional PWM1 control strategy and the proposed PWMn control strategy are defined by G_1 and G_n, respectively

$$G_1 = M \cdot \frac{1}{1-2D} = \frac{M}{2M-1}$$
$$G_n = M \cdot \frac{1}{1-nD} = \frac{M}{n(M-1)+1}. \tag{16}$$

Fig. 6(a) shows the boost factor comparison of the qSBI with different PWM strategies. The boost factor of the qSBI with the introduced PWM2 strategy is the same as that of the conventional PWM1 method. For the similar ST duty ratio *D*, the proposed PWMn strategy (with $n = 3, 4, 5, \ldots$) achieved a higher voltage gain than the PWM1 control method.

Fig. 6(b) shows voltage gain comparison of qSBI with PWM1 strategy and the proposed PWM strategies. The PWM1 method has the lowest voltage gain at the same modulation index. Based on (16), in case of similar voltage gain, if the modulation index in the PWM1 strategy is guaranteed to be M_1, the corresponding modulation index (M_n) in the PWMn strategy is expressed as

$$M_n = \frac{(n-1)M_1}{(n-2)M_1 + 1} > M_1. \tag{17}$$

For the proposed PWM5 method, (17) is rewritten as

$$M_5 = \frac{4M_1}{3M_1 + 1} > M_1. \tag{18}$$

As shown in (18), the proposed PWMn strategy uses a large modulation index to get better output voltage quality.

Note that the proposed PWM methods cannot be applied to traditional ZS/qZSI because the ZS/qZSI does not use an additional switch S_0. The proposed PWM methods can be extended to three-phase qSBI. Similar to single-phase qSBI, the three-phase qSBI uses an extra switch S_0 to reduce passive components in the impedance-source network. In the introduced PWM methods for three-phase qSBI, the switch S_0 and H-bridge switches are controlled individually. By triggering switch S_0 control signal in the NST state, the operating frequency of the inductor is increased significantly. Because switches in the H-bridge circuit and switch S_0 are individually controlled, the proposed strategies require two carriers to generate control signals for H-bridge circuit switches and switch S_0. Consequently, the proposed PWM strategies are more complex than the conventional strategy.

IV. Comparison Analysis

For the same input and output case, a comprehensive comparison between the introduced PWM5 strategy and the traditional PWM1 strategy for single-phase qSBI is illustrated in this section. From Fig. 6(b), the modulation index with the introduced PWM5 strategy is larger than that with the PWM1 strategy. The single-stage qSBI with the proposed PWM5 strategy is also compared with a two-stage VSI with the boost converter. The two-stage VSI is created by shorting the diode D_x of the qSBI in Fig. 1. In the two-stage VSI with the boost converter, the modulation index at the inverter side can be set at the maximum value of 1. Thus, the voltage stress of the switch, capacitor, and diode in the two-stage VSI is lower than that in the single-stage qSBI. However, the two-stage VSI with the boost converter cannot immunize with ST phenomenon. Therefore, a deadtime between two switches in a phase leg must be required to keep away the two-stage VSI from short circuit. Consequently, the distortion of the output current in the two-stage VSI is increased even though the maximum modulation index is used [28].

A. Ripple Comparison

The HF peak-to-peak capacitor voltage and inductor current ripples in the conventional PWM1 strategy [11] are

$$\Delta I_{L\_\text{PWM1}} = \frac{V_g D_1 (1-D_1) T}{L(1-2D_1)} \quad \text{and}$$
$$\Delta V_{C\_\text{PWM1}} = \frac{I_L D_1 T}{2C}. \tag{19}$$

From (2), the HF capacitor voltage and inductor current ripples in the proposed PWM5 strategy in NST state 1 are

$$\Delta I_{L\_\text{PWM5}} = \frac{D V_g T}{2L} \quad \text{and}$$
$$DeltaV_{C\_\text{PWM5}} = \frac{D(1-5D) I_L T}{2(1-D) C}. \tag{20}$$

From (18), the relationship between ST duty ratio (D_1) in the conventional PWM1 method and the ST duty ratio (D) in the introduced PWM5 method for the same voltage gain is

$$D = D_1 / (4 - 3D_1). \tag{21}$$

Substituting D of (21) into (20), and comparing ΔI_{L_PWM1} and ΔV_{C_PWM1} to those in (19), the HF peak-to-peak capacitor voltage and inductor current ripples in the introduced PWM5 strategy are smaller than those in the PWM1 strategy.

Peak values of the LF capacitor voltage and the LF inductor current under the conventional PWM1 strategy indicated in [11]

are

$$\begin{cases} \hat{i}_{L\_\mathrm{PWM1}} = \dfrac{(1-2D)MI_m}{2\left[4LC\omega^2-(1-2D)^2\right]} \\ \hat{v}_{C\_\mathrm{PWM1}} = \dfrac{\omega LMI_m}{4LC\omega^2-(1-2D)^2}. \end{cases} \tag{22}$$

Applying the analysis method in [11], the LF capacitor voltage and the LF inductor current with the introduced PWM5 strategy are obtained with the following:

$$\begin{cases} \tilde{i}_{L\_\mathrm{PWM5}} = \dfrac{(D-1)(1-5D)\tilde{i}_{PN}}{4LC\omega^2-(1-5D)^2} = \dfrac{(1-5D)MI_m\cos(2\omega t-\varphi)}{2\left[4LC\omega^2-(1-5D)^2\right]} \\ \tilde{v}_{C\_\mathrm{PWM5}} = \dfrac{\omega LMI_m\sin(2\omega t-\varphi)}{4LC\omega^2-(1-5D)^2}. \end{cases} \tag{23}$$

Peak values of the LF capacitor voltage and the LF inductor current in the PWM5 strategy are calculated as

$$\begin{cases} \hat{i}_{L\_\mathrm{PWM5}} = \dfrac{(1-5D)MI_m}{2\left[4LC\omega^2-(1-5D)^2\right]} \\ \hat{v}_{C\_\mathrm{PWM5}} = \dfrac{\omega LMI_m}{4LC\omega^2-(1-5D)^2}. \end{cases} \tag{24}$$

Substituting (18) and (21) into (24), and comparing $\hat{i}_{L\_\mathrm{PWM1}}$ and $\hat{v}_{C\_\mathrm{PWM1}}$ to those in (22), peak values of the LF capacitor voltage and the LF inductor current in the introduced PWM5 strategy are larger than those in the PWM1 strategy. The LF oscillation of the capacitor voltage and the inductor current can be efficiently eliminated by using an active filter method as described previously [29]. Total peak-to-peak ripples on the inductor current and the capacitor voltage are defined as

$$i_{L_{P-P}} = 2\hat{i}_L + \Delta I_L \quad \text{and} \quad v_{C_{P-P}} = 2\hat{v}_C + \Delta V_C. \tag{25}$$

Here, $V_{Dx}, V_{Dy}, V_{DS0-4}, V_{\mathrm{PN}}, I_{\mathrm{PN}}, I_L$, and P_o are voltage stress on D_x and D_y, drain-source voltage stress on S_{0-4}, dc-bus voltage, average dc-bus current in the NST states, inductor current, and output power, respectively.

B. Comparison of Voltage and Current Stresses

Table I shows major equations of the single-phase qZSI/qSBI with the traditional PWM1 strategy and the introduced PWM5 strategy. In Table I, the sum of the individual device rating of all semiconductor devices is called total device rating (TDR). Substituting D of (21) into equations of the proposed PWM5 strategy and comparing stresses between these two PWM strategies, voltage stresses on the diodes, switches, capacitor, and dc-bus in the introduced PWM5 strategy are lower than those in the PWM1 method for the qZSI/qSBI. As a result, the TDR under the proposed PWM5 strategy is significantly limited. Fig. 7 shows the comparative curves of the introduced PWM5 and PWM1 methods in terms of component voltage stresses and TDR. It is worth noting that the voltage stress on diodes, capacitor, and switches of the qSBI is the same. As shown in Fig. 7(a), the voltage stress on capacitor, diodes, and switches of the qSBI under the proposed PWM5 strategy is lower than that under the traditional PWM1 strategy. Furthermore, from Fig. 7(b), the TDR of the qSBI under the introduced PWM5 strategy is also lower than that under the conventional PWM1 method.

TABLE I
VOLTAGE AND CURRENT STRESSES OF QSBI AND QZSI WITH DIFFERENT PWM CONTROL STRATEGIES

	qZSI	qSBI	
	Conventional PWM1	Conventional PWM1	Proposed PWM5
V_C/V_g	$1/(1-2D_1)$	$1/(1-2D_1)$	$1/(1-5D)$
G	$M_1/(2M_1-1)$	$M_1/(2M_1-1)$	$M/(5M-4)$
$V_{DS0\text{-}4}$, V_{Dx}, V_{Dy}	$\dfrac{V_g}{1-2D_1}$	$\dfrac{V_g}{1-2D_1}$	$\dfrac{V_g}{1-5D}$
V_{PN}	$V_g/(1-2D_1)$	$V_g/(1-2D_1)$	$V_g/(1-5D)$
I_L	P_o/V_g	P_o/V_g	P_o/V_g
I_{PN}	$\dfrac{1-2D_1}{1-D_1}\dfrac{P_o}{V_g}$	$\dfrac{1-2D_1}{1-D_1}\dfrac{P_o}{V_g}$	$\dfrac{1-5D}{1-D}\dfrac{P_o}{V_g}$
$\hat{i}_L$	$\dfrac{0.5(1-2D_1)M_1I_m}{4LC\omega^2-(1-2D_1)^2}$	$\dfrac{0.5(1-2D_1)M_1I_m}{4LC\omega^2-(1-2D_1)^2}$	$\dfrac{0.5(1-5D)MI_m}{4LC\omega^2-(1-5D)^2}$
$\hat{v}_C$	$\dfrac{\omega LM_1I_m}{4LC\omega^2-(1-2D_1)^2}$	$\dfrac{\omega LM_1I_m}{4LC\omega^2-(1-2D_1)^2}$	$\dfrac{\omega LMI_m}{4LC\omega^2-(1-5D)^2}$
ΔI_L	$\dfrac{V_gD_1(1-D_1)T}{2L(1-2D_1)}$	$\dfrac{V_gD_1(1-D_1)T}{L(1-2D_1)}$	$\dfrac{DV_gT}{2L}$
ΔV_C	$\dfrac{I_LD_1T}{C}$	$\dfrac{I_LD_1T}{2C}$	$\dfrac{D(1-5D)I_LT}{2(1-D)C}$
$i_{L_{P-P}}$	$\dfrac{(1-2D_1)M_1I_m}{4LC\omega^2-(1-2D_1)^2}+\dfrac{V_gD_1(1-D_1)T}{2L(1-2D_1)}$	$\dfrac{(1-2D_1)M_1I_m}{4LC\omega^2-(1-2D_1)^2}+\dfrac{V_gD_1(1-D_1)T}{L(1-2D_1)}$	$\dfrac{(1-5D)MI_m}{4LC\omega^2-(1-5D)^2}+\dfrac{DV_gT}{2L}$
$v_{C_{P-P}}$	$\dfrac{2\omega LM_1I_m}{4LC\omega^2-(1-2D_1)^2}+\dfrac{I_LD_1T}{C}$	$\dfrac{2\omega LM_1I_m}{4LC\omega^2-(1-2D_1)^2}+\dfrac{I_LD_1T}{2C}$	$\dfrac{2\omega LMI_m}{4LC\omega^2-(1-5D)^2}+\dfrac{D(1-5D)I_LT}{2(1-D)C}$
TDR	$\dfrac{(9-8D_1)V_gI_L}{(1-D_1)(1-2D_1)}$	$\dfrac{(6-5D_1)V_gI_L}{(1-D_1)(1-2D_1)}$	$\dfrac{(6-2D)V_gI_L}{(1-D)(1-5D)}$

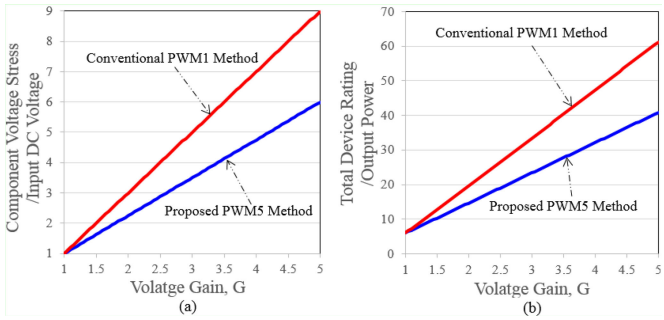

Fig. 7. Comparison curves of the proposed PWM5 and PWM1 in terms of (a) component voltage stresses/input dc voltage ($V_C/V_g, V_{Dx,Dy}/V_g$ and V_{DS0-4}/V_g) and (b) TDR/output power.

C. Power Loss Comparison

Using the PWM1 control method, if the switching frequency of H-bridge switches is f_{sw}, the switching frequency of switch S_0, f_{S0} is $2\cdot f_{\mathrm{sw}}$. When the proposed PWMn $(n=2,3,4\ldots)$ control method is applied to the qSBI, f_{S0} is $2\cdot(n-1)\cdot f_{\mathrm{sw}}$. Therefore, the switching frequency of switch S_0 in the PWMn method is increased by (n – 1) times.

The switching power loss of switch S_0 is determined based on the overlap area of the drain-source voltage and the drain

current as shown below

$$P_{\text{sw\_s0}} = V_C \cdot I_L \cdot f_{s0} \cdot (t_{ru} + t_{fi} + t_{ri} + t_{fu})/2 \quad (26)$$

where $V_c, I_L, t_{ri}, t_{fi}, t_{ru}$, and t_{fu} are capacitor voltage, average input current, current rising time, current falling time, voltage rising time, and voltage falling time, respectively.

The conduction power loss of switch S_0 is

$$P_{\text{cond\_s0}} = R_{\text{ds}} \cdot (I_{s0\_\text{rms}})^2 \quad (27)$$

where R_{ds} is the ON state drain-source resistance of switch S_0 and I_{s0_rms} is the rms current of switch S_0. It is calculated as

$$I_{s0\_\text{rms}} = \begin{cases} I_{L\_\text{rms}} \cdot \sqrt{D} & \text{for PWM1} \\ I_{L\_\text{rms}} \cdot \sqrt{(n-1)D} & \text{for PWMn.} \end{cases} \quad (28)$$

The power loss of H-bridge switches includes the switching and conduction power losses. The switching power loss of H-bridge switches is a sum of the switching power losses in the NST state ($P_{\text{sw\_NST}}$) and ST state ($P_{\text{sw\_ST}}$) as

$$P_{\text{sw\_}H} = P_{\text{sw\_ST}} + P_{\text{sw\_NST}}$$

$$\text{with} \begin{cases} P_{\text{sw\_ST}} = 4 \cdot V_C \cdot (I_L/2) \\ \qquad \cdot (2f_{\text{sw}}) \cdot (t_{ru} + t_{fi} + t_{ri} + t_{fu})/2 \\ P_{\text{sw\_NST}} = \frac{2}{\pi} \int_0^{\pi} [V_C \cdot i_o \cdot f_{\text{sw}} \\ \qquad \cdot (t_{ru} + t_{fi} + t_{ri} + t_{fu})/2] d\omega t \\ \qquad +2 \cdot Q_{rr} \cdot V_C \cdot f_{\text{sw}} \end{cases} \quad (29)$$

where Q_{rr} and i_o are the reverse recovery charge and the output current, respectively.

The conduction power loss of H-bridge switches includes conduction power losses in NST state ($P_{\text{cond\_NST}}$) and ST state ($P_{\text{cond\_ST}}$). Thus, the conduction power loss of H-bridge switches is calculated as

$$P_{\text{cond\_}H} = P_{\text{cond\_ST}} + P_{\text{cond\_NST}} \quad (30)$$

with

$$\begin{cases} P_{\text{cond\_ST}} = 4 \cdot R_{\text{ds}} \cdot (I_L/2)^2 \cdot D \\ P_{\text{cond\_NST}} = \frac{2}{\pi} \int_0^{\pi} [R_{\text{ds}} \cdot (i_o)^2 \cdot (1-D)] d\omega t \end{cases}$$

where R_{ds} is the ON state drain-source resistance of the switch.

The inductor copper loss is calculated based on the rms current through inductor as

$$P_{Cu} = r_L \cdot I_{L\_\text{rms}}^2 \quad (31)$$

where r_L is the inductor's resistance, and I_{L_rms} is the rms value of current through the inductor and calculated as [30]

$$I_{L\_\text{rms}} = \sqrt{I_L^2 + (\Delta I_L)^2/12} \quad (32)$$

where ΔI_L is the HF peak-to-peak inductor current.

The inductor core loss for an MPP of 125 μ [31] is expressed as

$$P_{fe} = 0.33 \cdot B^{1.98} \cdot {f_L}^{1.64} \cdot A_c \cdot l_m \quad (33)$$

where B is the peak ac flux density; $f_L = 1/T_L$ is the operating frequency of inductor; A_c is the core cross-sectional area; and l_m is the core mean magnetic path length. The peak ac flux density is given by the following equation:

$$B = \frac{V_{\text{pk}}}{2A_e \cdot N} D \cdot T_L \quad (34)$$

where V_{pk} and N are the peak voltage across the coil and the turn number, respectively.

The power loss of capacitor is calculated as

$$P_C = r_C \cdot I_{C\_\text{rms}}^2 \quad (35)$$

where r_c represents the equivalent series resistance (ESR) of the capacitor; and I_{c_rms} is the rms capacitor current and calculated for the proposed PWM5 method as

$$I_{C\_\text{rms}} = \sqrt{\frac{1}{\pi} \int_0^{\pi} i_o^2 \cdot (4D) \cdot d\omega t + \frac{1}{\pi} \int_0^{\pi} (i_L - i_o)^2 \cdot (1-5D) \cdot d\omega t}. \quad (36)$$

The power loss of diode contains the conduction loss and the reverse recovery loss. The conduction loss of D_x, D_y and the free-wheeling body diode under the PWM5 method is calculated as

$$\begin{aligned} P_{\text{con\_}D} = & \frac{1}{\pi} \int_0^{\pi} [U_D \cdot (i_L - i_o) + R_D \cdot (i_L - i_o)^2](1-D) d\omega t \\ & + \frac{1}{\pi} \int_0^{\pi} [U_D \cdot (i_L) + R_{Do} \cdot (i_L)^2].(1-4D) d\omega t \\ & + \frac{2}{\pi} \int_0^{\pi} [U_D \cdot (i_o) + R_{Do} \cdot (i_o)^2].(D/2) d\omega t. \end{aligned} \quad (37)$$

where U_D is the forward voltage drop of the diode, R_D is the equivalent resistance of the diode, and R_{Do} is the equivalent resistance of the body diode.

The reverse recovery loss of D_x and D_y is calculated as

$$\begin{aligned} \text{P}_{\text{rr\_}D} &= Q_{\text{rr}-d} \cdot V_C \cdot (2f_{\text{sw}}) + Q_{\text{rr}-d} \cdot V_C \cdot (8f_{\text{sw}}) \\ &= 10 \cdot Q_{\text{rr}-d} \cdot V_C \cdot f_{sw} \end{aligned} \quad (38)$$

where $Q_{\text{rr}-d}$ is the reverse recovery charge of the diodes D_x and D_y.

TABLE II
PARAMETERS FOR POWER LOSS CALCULATION

Parameters	Values
MOSFETs (IRFP460)	20 A, 500 V, r_s=0.27 Ω
Diodes (FF60UP30DN)	60A, 300 V, r_D = 15 mΩ
ESR of *C* capacitor at 450 VDC	50 mΩ (1360 μF)
Parasitic resistance of inductors	0.12 Ω
Inductor core	CM778125 (178 nH/N2)
Output voltage	110 V_{RMS}

Table II shows parameters for power loss calculation. Using (26)–(38), the power losses of the qSBI and the two-stage VSI with the boost converter are determined. Fig. 8 shows loss distribution of the two-stage VSI with the boost converter and the qSBI under the PWM1 method and the proposed PWM5 strategy

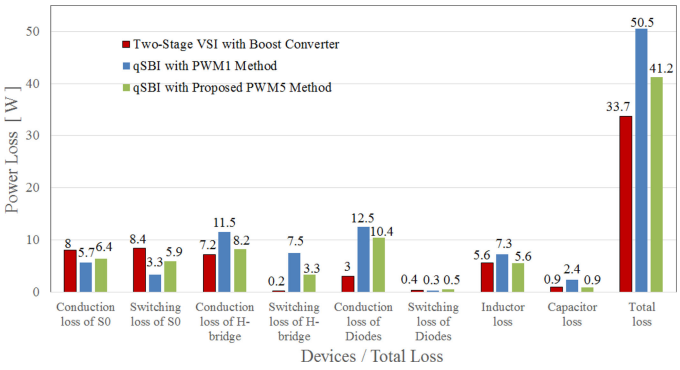

Fig. 8. Power loss comparison between the two-stage VSI and the single-stage qSBI with PWM1 and PWM5 methods at output power of 400 W.

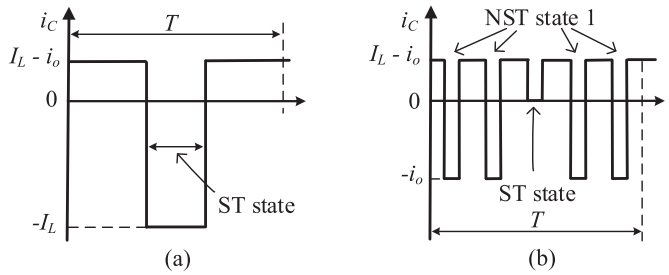

Fig. 9. Capacitor current waveform of the qSBI with (a) the traditional PWM1 strategy and (b) the proposed PWM5 strategy.

when V_g is at 60 V and P_o is at 400 W. Although the proposed PWM5 strategy increases the conduction and switching losses of S_0, total power loss of all switches in the qSBI under the proposed PWM5 method is still lower than that under the PWM1 method. This is because the voltage stress on switches and the ST time interval with the proposed PWM5 method are significantly reduced. Thus, the conduction and switching losses of switches on the H-bridge under the proposed strategy are lower than those under the PWM1 strategy. Fig. 9 shows the capacitor current waveform of the qSBI with the PWM1 strategy and the proposed PWM5 method. As shown in Fig. 9, the rms current of the capacitor under the proposed PWM5 method is lower than that under the PWM1 method. Thus, the capacitor loss of the qSBI under the introduced PWM5 strategy is dropped. Furthermore, because the HF peak-to-peak inductor current with the introduced PWM5 strategy is lower than that with the PWM1 strategy, the rms current of the inductor under the proposed PWM5 method is lower than that under the PWM1 method at the same average inductor current. Consequently, the inductor copper loss under the proposed method is lower than that under the PWM1 method. Because both peak inductor voltage and ST time interval with the proposed PWM5 are reduced, peak ac flux density with the proposed PWM5 is also decreased. Thus, the core loss with PWM5 method is reduced even though the operating frequency of the inductor is increased. Therefore, the efficiency of the qSBI under the introduced PWM5 strategy is higher than that under the PWM1 method under the same operating condition.

Fig. 8 also compares the power loss between qSBI with the proposed PWM5 strategy and the two-stage VSI with the

TABLE III
SIMULATION AND EXPERIMENT PARAMETERS

Parameters		Values
Power rating		500 W
Inverter output voltage		110 Vrms / 50 Hz
Input voltage		60 – 80 V
Inductor (L) and capacitor (C)		2 mH and 1360 μF/ 450 V
Switching frequency	S_0	80 kHz with PWM5 20 kHz with PWM1
	$S_{1\text{-}4}$	10 kHz

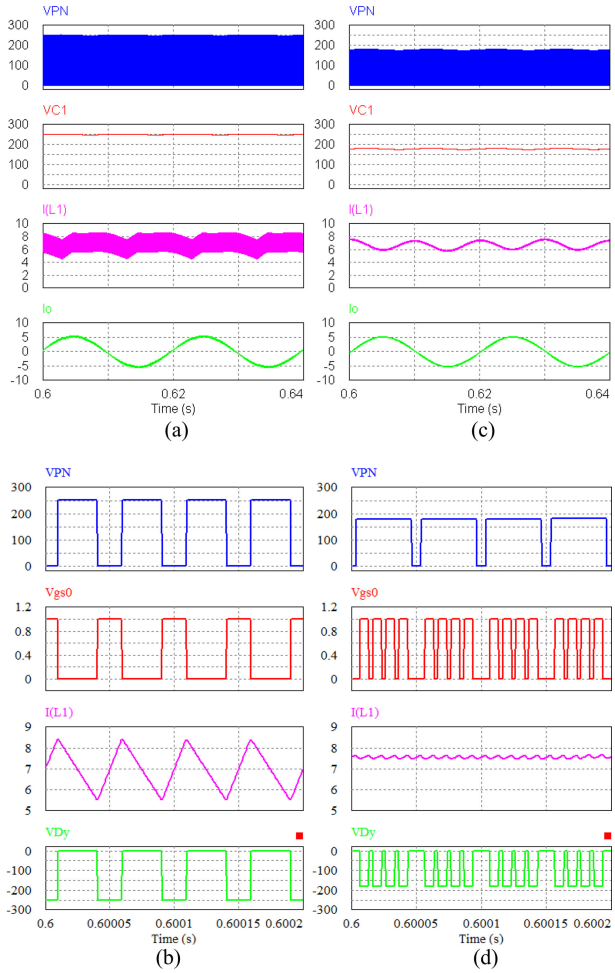

Fig. 10. Simulation results for the qSBI under (a), (b) PWM1 method and (c), (d) PWM5 method. From top to bottom: (a), (c) DC-bus voltage, capacitor voltage, inductor current, and load current. (b), (d) DC-bus voltage, control gate signal of S_0, input current, and diode D_y voltage.

boost converter. The same parameters as qSBI were used in the two-stage VSI. The switching frequency of boost converter is 100 kHz, while the switching frequency of the H-bridge inverter is 10 kHz. The duty cycles of the boost converter and the modulation index of inverter are 0.616 and 1, respectively. As shown in Fig. 8, the inductor and capacitor losses in the qSBI under the PWM5 strategy are the same as those in the two-stage VSI with

TABLE IV
VOLTAGE AND CURRENT STRESSES UNDER TWO PWM METHODS WITH $V_g = 60\,\text{V}$, $V_{o(\text{RMS})} = 110\,\text{V}$ AND $P_o = 400\,\text{W}$

	qZSI		qSBI					
	with PWM1		with PWM1		with PWM2		with PWM5	
	Sim.	Cal.	Sim.	Cal.	Sim.	Cal.	Sim.	Cal.
D	0.38	0.38	0.38	0.38	0.38	0.38	0.133	0.133
M	0.62	0.62	0.62	0.62	0.62	0.62	0.867	0.867
$V_{DS0\text{-}4}$, V_{Dx}, V_{Dy}	250 V	250 V	250 V	250 V	250 V	250 V	179 V	179 V
V_C	95 V for C_2 155V for C_1	95 V for C_2 155V for C_1	250V	250 V	250V	250 V	179 V	179 V
I_L	6.8 A	6.67 A	6.9 A	6.67 A	6.9 A	6.67 A	6.72 A	6.67 A
ΔI_L	2.9 A	2.95 A	2.8 A	2.95 A	0.55 A	0.57 A	0.18 A	0.2 A
ΔV_C	0.14 V	0.09 V	0.14 V	0.09 V	0.03 V	0.03 V	15 mV	13 mV
$\hat{i}_L$	0.37 A	0.4 A	0.35 A	0.4 A	0.35 A	0.4 A	0.77 A	0.78 A
$\hat{v}_C$	2.2 V	2 V	2 V	1.98 V	2 V	1.98 V	2.86 V	2.93 V
$i_{L_{p-p}}$	3.64 A	3.75 A	3.5 A	3.75 A	1.25	1.37	1.72 A	1.76 A
$v_{C_{p-p}}$	4.54 V	4.1 V	4.14 V	4.05 V	4.03	3.99	5.73 V	5.97
I_{PN}	2. 68 A	2.58 A	2.86 A	2.58 A	2.86 A	2.58 A	2.69 A	2.58 A
TDR		16 kVA		11 kVA		11 kVA		1.9 kVA

the boost converter. Because the qSBI uses an additional diode D_x, the total diode loss in qSBI with PWM5 strategy is higher than that in the two-stage VSI. Meanwhile, the conduction and switching losses of switch S_0 in qSBI with PWM5 strategy are lower than those in the two-stage VSI. The main reason is because the number of turning ON/OFF time of switch S_0 in the boost converter of the two-stage VSI in the half-switching period of H-bridge circuit is 5, while it is 4 in the qSBI with the PWM5 strategy. On the other hand, the conduction and switching losses of H-bridge switches in the qSBI with the PWM5 strategy are higher than those in the two-stage VSI because the ST state is inserted into the H-bridge circuit in the qSBI. It is worth noting that the deadtime effect in the H-bridge circuit of the two-stage VSI is ignored in the power loss calculation. In summary, the total power loss of qSBI with the PWM5 strategy is higher that of the two-stage VSI with the boost converter.

V. SIMULATION AND EXPERIMENT RESULTS

A. Simulation Results

In order to validate the operating principle of the single-phase qSBI with the proposed PWM strategy, PSIM simulation is performed. Table III lists simulation parameters for the single-phase qSBI. Fig. 10 shows simulation results with a passive load of 30 Ω and 6 mH for qSBI at $V_g = 60\,\text{V}$ and $P_o = 400\,\text{W}$. To generate the same output voltage of 110 V in RMS from input voltage of 60 V, ST duty cycle and modulation index in the proposed PWM5 strategy are 0.133 and 0.867, respectively. ST duty cycle and modulation index are 0.38 and 0.62, respectively, for the conventional PWM1 and proposed PWM2 methods.

Table IV shows calculated and simulation results of the current and voltage stresses of qSBI and qZSI with different PWM control methods. As shown in Table IV, the qSBI under the introduced PWM5 strategy has many merits over that under the conventional PWM1 method: lower voltage stress, improved modulation index, and lower HF peak-to-peak capacitor voltage and inductor current ripples. The demerit of the introduced PWM5 strategy is that the LF capacitor voltage and inductor current ripples are greater than those in the PWM1 method. However, total peak-to-peak inductor current ripple of the qSBI with the introduced PWM5 strategy is lower than that with the PWM1 method. With the proposed PWM5 method, the TDR is dramatically decreased as shown in Table IV.

Table IV also compares the proposed PWM2 method to the conventional PWM1 method. As shown in Table IV, the qSBI under both PWM1 and PWM2 methods has the same value of the voltage gain, voltage stress across the capacitor, switch and diodes, LF ripple on capacitor voltage and inductor current, and TDR. Furthermore, the proposed PWM2 method is easy to implement because it uses the two carrier waveforms as the conventional PWM1 strategy (see Figs. 2 and 3). Because the switching frequency of S_0 under both PWM1 and PWM2 methods is the same, the switching loss for S_0 under the proposed PWM2 method is also the same as that under the conventional PWM1 strategy. Because the operating frequency of the input inductor in the proposed PWM2 method is twice of that of the conventional PWM1 method, the HF inductor current ripple in the proposed PWM2 strategy is less than that of the conven-

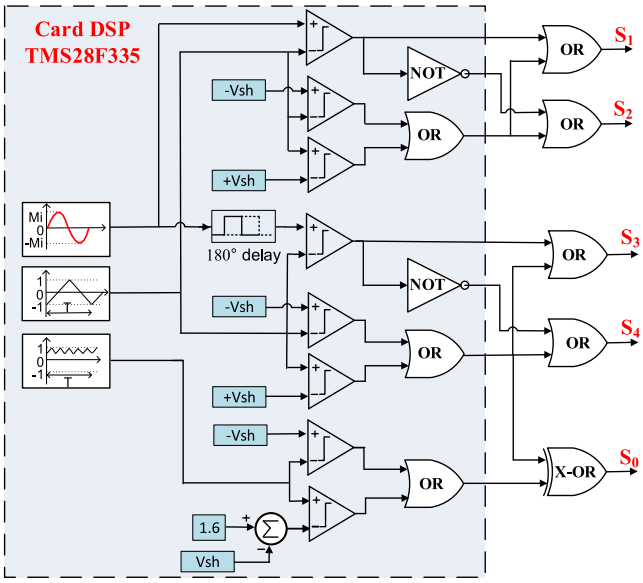

Fig. 11. Gating signal generation for the proposed PWM5 control method.

tional PWM1 strategy as shown Table IV. As a result, the size and cost of the inductor and capacitor are decreased when the proposed PWM2 method is used.

B. Experiment Results

A 500-W prototype was set up in the laboratory to verify the effectiveness of the introduced PWM5 technique. Insulated TLP250 amplifiers were used to control five IRFP460 MOSFETs. Two FF60UP30DN diodes were used in the single-phase qSBI. The inductance of L was 2 mH. Two $450-\mathrm{V}/680-\mu F$ capacitors were connected in parallel to get $1360-\mu$F capacitance of capacitor C. Note that the capacitor C with voltage rating of 200 V could be used to reduce the size of the qSBI under the proposed PWM5 method. The filter inductor was 6 mH and the resistor load was 30 Ω. Using the proposed PWM5 control method, the operating frequency of switches on H-bridge circuit was 10 kHz, while the switching frequency of the switch S_0 was 80 kHz. Fig. 11 illustrates the gating signal generation for the introduced PWM5 strategy.

Fig. 12 presents experimental results of the qSBI under the traditional PWM1 strategy and the proposed PWM5 strategy at $V_g = 60\,\mathrm{V}, V_o = 110\,\mathrm{V_{rms}}, P_o = 400\,\mathrm{W}, R = 30\,\Omega$, and $L_l = 6\,\mathrm{mH}$. In the same input/output voltage case, with the PWM1 strategy, the peak value of the dc-bus voltage and the capacitor voltage were stepped-up to 270 V as shown in Fig. 12(a). The measured RMS value of output current was 3.57 A, while the measured RMS value of output voltage was 110 V. As shown in Fig. 12, inductor current was continuous. The measured THD load current was 1.4%. As shown in Fig. 12(b), the HF peak-to-peak ripple value of inductor current was 3 A, while the total inductor ripple current was 5 A as shown in Fig. 12(a). The operating frequency of the input inductor was 20 kHz. With the proposed PWM5 strategy, capacitor voltage and the peak value of the dc-bus voltage were stepped-up to 190 V as shown in

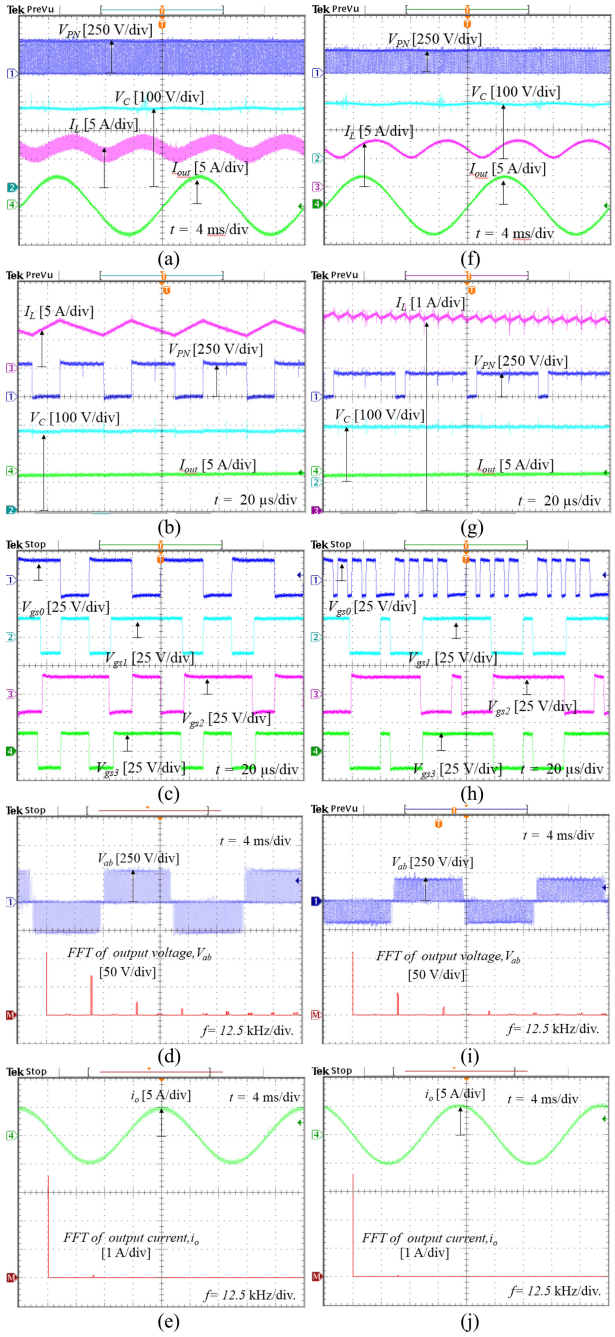

Fig. 12. Experimental results for the qSBI under (a)–(e) PWM1 method and (f)–(j) the proposed PWM5 method. From top to bottom: (a), (f) dc-bus voltage, capacitor C_1 voltage, source current, and output current; (b), (g) input current, dc-bus voltage, capacitor C_1 voltage, and load current; (c), (h) control gate signals of $S_0 - S_3$; (d), (i) output voltage and its harmonic spectrum; and (e), (j) output current and its harmonic spectrum.

Fig. 12(f). Measured RMS values of output current and output voltage were 3.55 A and 110 V, respectively. The input current was continuous. The measured THD value of the output current was 0.8%. The HF peak-to-peak ripple value of inductor current was 0.2 A as shown in Fig. 12(g), while the total inductor ripple current was 3 A as shown in Fig. 12(f). The operating frequency of the input inductor was 100 kHz. These experimental results of the inductor current ripple were higher than that of the

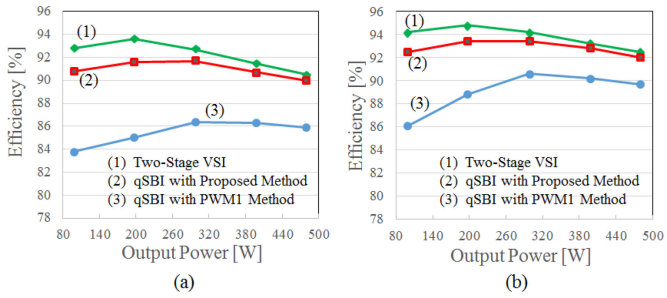

Fig. 13. Measured efficiency comparison between the two-stage VSI with the boost converter and the qSBI with PWM1 and PWM5 schemes. (a) $V_g = 60$ V. (b) $V_g = 80$ V.

calculation and simulation results (see Table IV). This is due to the appearance of parasitic components in the experimental setup.

Fig. 13 shows measured efficiency comparison at different power levels between the two-stage VSI with the boost converter and qSBI with the existing PWM1 and the proposed PWM5 strategies. Because qSBI uses an additional diode D_x, its efficiency is lower than that of the two-stage VSI with the boost converter. A sacrifice on the efficiency of 0.5% was found at load power of 480 W to gain ST immunity in qSBI with the introduced PWM5 strategy. The efficiency of qSBI with the introduced PWM5 strategy is greater than that of the qSBI with the PWM1 strategy. This is because the proposed PWM5 strategy uses a lower ST interval to produce the same voltage gain. Moreover, voltage stresses on semiconductor devices in the introduced PWM5 strategy are lower than those in the PWM1 strategy. Therefore, conduction loss in the proposed PWM5 strategy is significantly decreased.

VI. Conclusion

This paper proposed a new family of PWM strategies for qSBI. In comparison with the conventional PWM strategy, the proposed PWM strategies have higher efficiency. Under the same operating conditions, comparison results illustrated that voltage stress on semiconductor devices and capacitor of the single phase qSBI with the introduced PWM strategy was lower than that with the conventional PWM strategy. Furthermore, HF ripple of the current through the inductor was significantly reduced. Demerits of the proposed PWMn (n $= 3, 4, 5 \ldots$) strategies over the conventional PWM strategy are: 1) the LF ripple on capacitor voltage and inductor current is increased, 2) the switching loss of the switch S_0 is higher, and 3) PWM generation is more complex. When the proposed PWM2 method is compared to the existing PWM1 method, three obvious issues of the proposed PWM methods do not appear. Because the proposed PWM2 strategy has a low HF ripple on inductor current and capacitor voltage, it can be used to replace the conventional PWM1 method. Circuit analysis, operating principles, and simulation results for qSBI with the introduced PWM strategy are shown. A prototype was built and the effectiveness of the proposed PWM5 scheme was validated.

Because qSBI with the proposed PWM strategies has a high reliability, it can be used to replace the two-stage VSI with the boost converter for applications where the required voltage gain is in the range of 2 to 3. Therefore, qSBI should have a performance that lies between qZSI and two-stage VSI with the high boost converter.

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