Modified Dual Output Cuk Converter-Fed Switched Reluctance Motor Drive With Power Factor Correction

Aniket Anand, *Member, IEEE*, and Bhim Singh, *Fellow, IEEE*

***Abstract*—The control of a switched reluctance motor (SRM) drive is proposed with a front end power factor correction (PFC) converter. It uses a modified Cuk converter-fed SRM drive to improve power quality at ac mains. The converter configuration consists of two Cuk converters and each of them operates separately for two half-cycles of the supply voltage. The proposed converter generates two identical voltages across two output capacitors to feed a split capacitor converter of a four-phase SRM drive. The proposed pulsewidth modulated ac–dc converter operates in the discontinuous conduction mode to reduce its size and cost by eliminating couple of sensor requirements. The incorporated voltage control loop regulates the dc-link voltage with PFC at ac mains. The SRM is considered for the proposed drive because of its low cost and constructional ease. The motor speed is controlled over a wide range by regulating the PFC converter output dc voltage. The proposed SRM drive is tested for steady-state and dynamic state conditions on a developed prototype in the laboratory. The obtained test results demonstrate good drive performance and line drawn power quality. The input current total harmonic distortion is observed within a limit of a standard.**

***Index Terms*—Discontinuous conduction mode (DCM), midpoint converter, modified Cuk converter, power quality, switched reluctance motor (SRM), total harmonic distortion (THD).**

I. Introduction

POWER factor correction (PFC) converters are becoming popular due to their distinguished features of low input current total harmonic distortion (THD) with a high power factor. These PFC converters are basically the input current shapers as they reduce the harmonics current content, which are at the frequency other than the fundamental frequency. To reduce harmonics content from the input supply current, active as well as passive filters are incorporated in the circuit, which bring down the supply current THD under acceptable limits as per the standard IEC 61000-3-2 [1]. To meet the demand for energy efficient, low-cost variable speed drive is a fan type of load

Manuscript received June 25, 2017; revised October 16, 2017, January 15, 2018, and March 19, 2018; accepted April 4, 2018. Date of publication April 15, 2018; date of current version November 19, 2018. Recommended for publication by Associate Editor Y. Sozer. (*Corresponding author: Aniket Anand.*)

The authors are with the Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi 110016, India (e-mail:

SRM-based drives are proposed in the literature but SRM drive with improved power quality is not well addressed till now.

The low-cost switched reluctance motor drive fed by a unity power factor converter appears as a promising solution to the available drive structure. The midpoint converter, which utilizes single switch and single diode to excite individual phases, is selected here to build the proposed drive as a low-cost system. This converter is well suited for inexpensive application due to reduced count of switches and drivers requirement. However, switch voltage rating requirement is half because of its split dc-link configuration. The only drawback associated with midpoint converter topology, is the required voltage symmetry. This encourages the design of the PFC converter, which can take care of power quality issues at ac mains and generates two symmetrical voltages across the two capacitors. Therefore, a dual output Cuk converter-fed SRM drive is proposed here. The selection of modified dual output Cuk converter is made because of the following influential features.

1) It provides a fully regulated two equal output voltages utilizing single voltage loop.
2) It improves the power quality when the drive operates under steady state as well as dynamic conditions.
3) The selected operating mode for the proposed converter has reduced the size of an output side inductor, thus the cost and required board area are also reduced.

To control SR motor, two control methodologies are adopted as a constant dc-link voltage-based control and a variable dc-link voltage-based control. The constant dc-link voltage-based control is the conventionally adopted control algorithm, which is further divided into two operating modes on the basis of operating speed. If the low-speed operation is desired, then the chopping control mode is adopted, whereas a single pulse mode is selected at high-speed operation. During low speed, the turn-ON and turn-OFF angles are kept constant and the required torque is obtained by regulating the amplitude of the current. However, during high-speed operation, the current control is not possible due to comparable back electromotive force and dc-link voltage. Therefore, SR motor at high speed is controlled on the basis of turn-ON and turn-OFF angles which can be called as a single pulse mode control. In this conventional control method, full dc-link voltage is applied across the winding during low speed operation, which results in high current gradient and thus initializes the different vibration modes in the stator and produces increased acoustic noise. However, acoustic noise becomes prominent when the stator frequency of vibration coincides with the natural frequency of the stator. The high acoustic noise and radial vibrations in SRM can be reduced using single pulse control, which is selected here. In this proposed control algorithm, the dc-link voltage is considered as a function of speed. The PFC converter before the midpoint converter-fed SR motor provides required power quality improvement at supply side and at the same time it is capable of maintaining sufficient current to maintain the rated torque. Thus, low-speed operation of SR motor can be easily obtained without using any chopping control strategy. The reduced dc bus voltage at low-speed operation results in reduced current gradient and thus the acoustic noise as compared to the conventional control method.

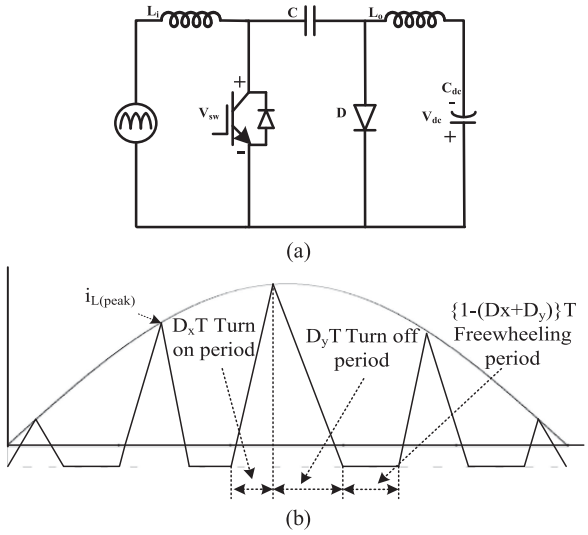

Fig. 1. (a) Conventional Cuk converter. (b) Output inductor current during DCM of operation.

II. Principle of PFC Technique

The switching control for PFC-based converters can be categorized as a variable frequency control and a constant frequency control [6], [7]. The variable frequency control is generally based on output voltage ripple with constant-on-time (COT) or constant-off-time. Moreover, the converter operates with fixed duty cycle, however, at variable frequency, the converter switch turns ON if the condition $V_{\text{ref}} > V_{\text{dc}}$ is true, where V_{dc} is the dc-link voltage and V_{ref} is the set reference voltage [8]. The pulse bursting phenomenon is the demerit associated with the COT control, i.e., the occurrence of very short OFF time pulse after COT pulse. Whereas, the constant frequency control is the pulsewidth modulation (PWM) based control, which are further categorized as a voltage-based control and a current-based control.

The voltage-based control with variable duty cycle is proposed here. The continuous and discontinuous natures of the inductor current decide the operating mode of the PFC converter. On the basis of the current nature through the inductor, three operating modes are reported in the literature, i.e., continuous conduction mode (CCM), critical conduction mode (CRM) and DCM [8], [9]. In CCM, the continuous inductor current results in low current ripple with reduced electromagnetic interference. However, the switch experiences hard switching as the current is continuous all the time. The CRM and DCM are preferred because the inductor current is discontinuous in every switching cycle, which allows the zero current switching [10]. The only difference in CRM and DCM modes is that in CRM one customizes the design for boundary condition to reduce peak current stress through the switch.

Fig. 1(a) and (b) represents the conventional Cuk converter configuration in DCM of operation. However, Fig. 1(b) presents the output inductor current behavior during the switch ON period D_xT as the inductor current increases and then it decreases to zero till the switch OFF period D_yT, while the remaining period $\{1-(D_x+D_y)\}T$ of the switching period is the freewheeling

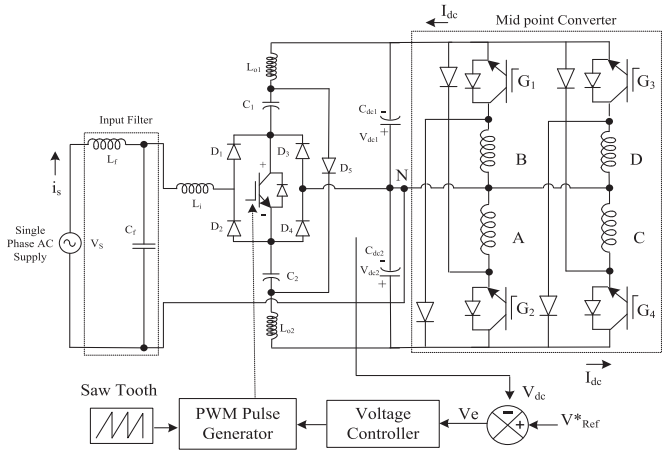

Fig. 2. Proposed modified Cuk converter-fed SRM drive.

period when the output inductor current freewheels through the circuit diode. To obtain inherent PFC, the duty cycle D_x is varied from zero to its maximum value for every half-cycle of the supply voltage.

III. Modified Dual Output Cuk Converter-Fed SRM Drive

The proposed PFC converter-fed SRM drive is shown in Fig. 2. The need for a dual output arises as a special split capacitor converter configuration is used, such that each phase is connected through a single switch and one diode to drive an SRM. The converter circuit comprises two Cuk converters with one common switch and featured with two output voltages equal in magnitude. This converter topology is derived from PFC-based three-phase rectifier topology first proposed in [11]. The proposed converter consists of single input inductor operating in CCM to reduce input current ripple. The other circuit components including intermediate capacitors, output side inductors, and output capacitors, which are separate for both the Cuk converters. The circuit configuration has added advantage of self-balanced output voltages without any required complex control for voltage balancing. The balanced output voltages have reduced the sensor cost, as while sensing the output voltage across one output capacitor gives the total dc-link voltage. The sensed dc-link voltage is compared with the reference dc voltage to generate switching pulses for the converter.

IV. Operation of Modified Cuk Converter

The converter operation is divided into two half-cycles, i.e., negative half and positive half of the input voltage waveforms. Two intermediate capacitors C_1 and C_2 and output inductors L_{o1} and L_{o2} are introduced in the circuit. The input side inductor L_i operates in continuous conduction mode (CCM) and output inductors L_{o1} and L_{o2} are allowed to enter DCM during each cycle of operation, which is shown in Fig. 3. The energy transfer between passive elements in the circuit can be explained under five different modes of operation.

1) *Mode I (During positive half-cycle switch ON period t_2–t_1):* During this time interval, positive half-cycle is shown in Fig. 4(a). This mode presents the energy flow from mains to inductor L_i through diodes D_1 and D_4. The switch ON state is described in this mode during positive half-cycle. The charging current for the inductor L_{o1} passes through the switch and the output side capacitor C_{dc1}. However, intermediate capacitor is discharged during this mode.
2) *Mode II (During positive half-switch OFF period t_3–t_2):* In the previous mode, capacitor C_1 is left discharged, which is charged from the inductor current i_{Li}. It finds its path through diodes D_1, D_4 and D_5 as shown in Fig. 4(b). The output side inductor L_{o1}, which is charged during *Mode-I,* is discharged through a capacitor C_{dc1} during this mode. This mode ends with fully charged output capacitor C_{dc1}.
3) *Mode III (DCM Mode t_4–t_3):* Fig. 4(c) shows the circuit operation during this time interval. The output inductor current decreases below zero during this operation mode. During this mode, the converter circuit appears as emulated resistance, which allows constant circuit current.
4) *Mode IV (During negative half-switch ON period t_2–t_1):* During this time interval, a negative half-cycle is associated with converter operation. This mode is shown in Fig. 4(d). This mode describes the switch ON period, inductor L_i stores energy, the switch ON state provides the path for input inductor current and the current is flowing through the intermediate capacitor C_2 and inductor L_{o2}. The output side capacitor C_{dc2} is charged during this mode. Moreover, the input inductor current finds its path through diodes D_1 and D_2.

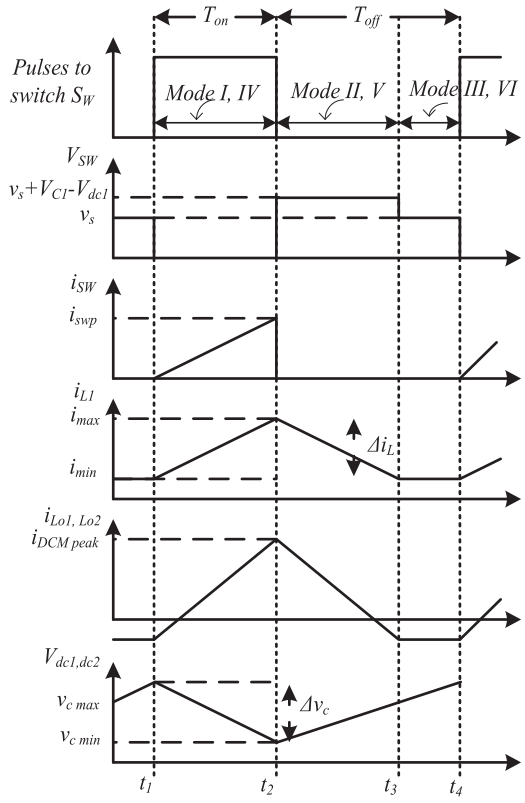

Fig. 3. Theoretical waveforms during different operating modes.

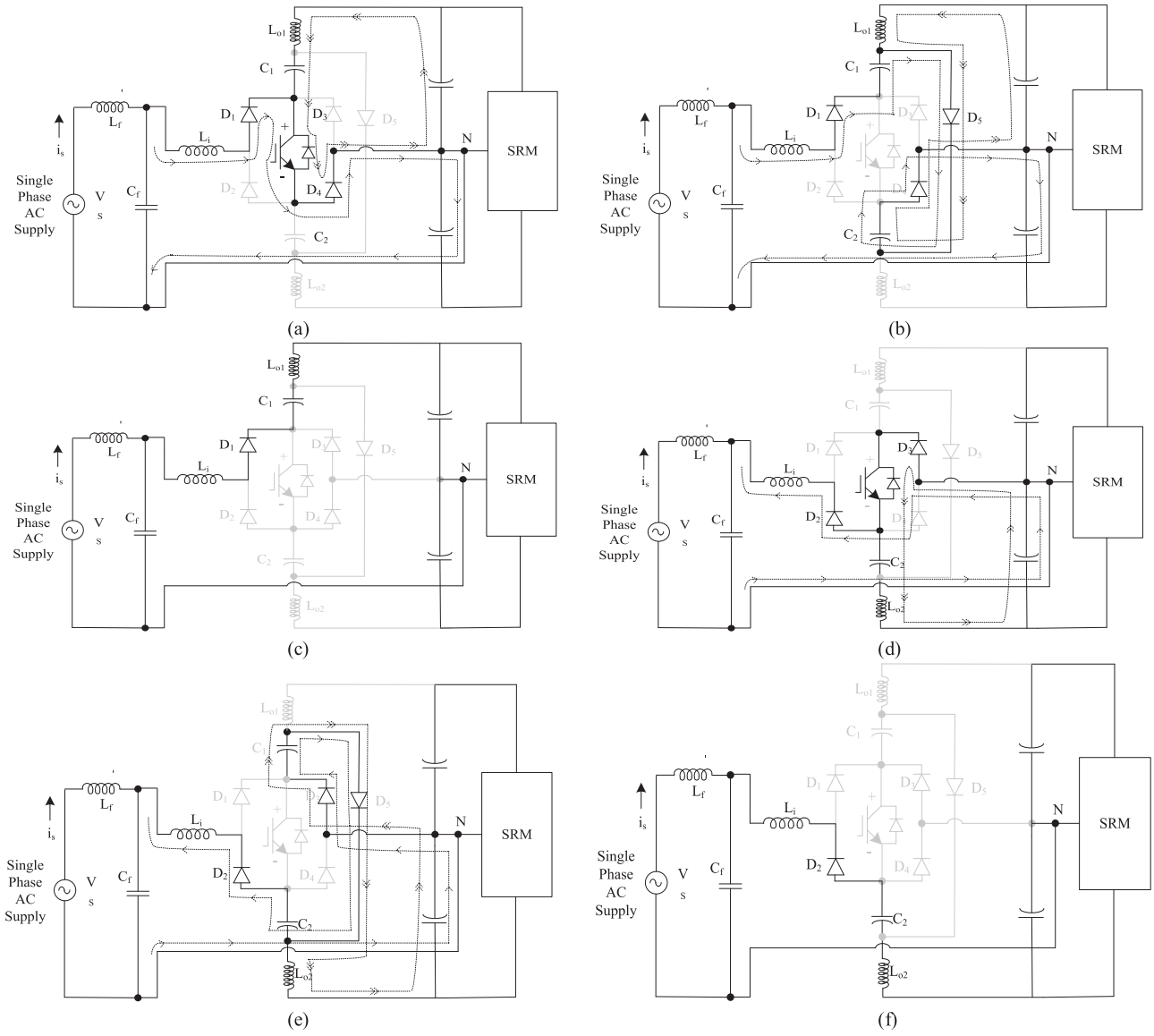

Fig. 4. Converter operating modes during positive half. (a) Mode I (t_2–t_1). (b) Mode II (t_3–t_2). (c) Mode III (t_4–t_3) and during negative half. (d) Mode I (t_2–t_1). (e) Mode II (t_3–t_2). (f) Mode III (t_4–t_3).

5) *Mode V (During negative half-switch OFF period t_3–t_2):* The stored energy in L_i during *Mode V* is transferred to intermediate capacitor C_2. Moreover, diodes D_2, D_3 and D_5 provide path for capacitor charging current. The inductor L_{o2} transfers its energy to output side capacitor C_{dc2} through diodes D_5 and D_3. The flow of current during this interval is displayed in Fig. 4(e).
6) *Mode VI (DCM mode t_4–t_3):* Fig. 4(f) shows the DCM with zero output inductor current during negative half-cycle.

V. Design of the Modified Cuk Converter

The proposed drive is designed for a power of 400 W for household applications. The design of circuit components for dual output converter comprises the design of input inductor L_i, intermediate capacitors (C_1 and C_2), output inductors (L_{o1} and L_{o2}), output capacitors (C_{dc1} and C_{dc2}) and high-pass input *LC* filter. The selected value for the circuit inductors and capacitors after calculation and all the related motor parameters are given in the Appendix. The output voltage for the modified Cuk converter is given as follows [12]:

$$V_{\text{dc}} = \frac{D}{1-D} V_{\text{in}} \sqrt{2}. \tag{1}$$

Such that instantaneous supply voltage is given as follows:

$$V_{\text{in}} = |V_m \text{Sin}(\omega t)| = \left| 220\sqrt{2}\text{Sin}(314t) \right| \text{ V}.$$

A. Input Inductor (L_i) Design for CCM

In CCM, the current ripple is small enough, such that ac core loss is not significant. Whereas in DCM, large flux swing and high core loss occur due to high current ripple. The input

inductor $L_{\rm i}$ for CCM of operation is given as follows [12]:

$$L_i = \frac{V_{\rm in}D(t)}{\eta I_{\rm in} f_s} = \frac{R_{\rm in}D}{\eta f_s} = \left(\frac{{V_s}^2}{P_i}\right)\frac{D}{\eta f_s} = \frac{1}{\eta f_s}\left(\frac{V_s^2}{P_{\rm max}}\right)\left(\frac{V_{\rm dc\ max}}{V_{\rm dc\ max}+V_{\rm in}}\right). \quad (2)$$

An equivalent input resistance is given as $R_{\rm in}$, input power as P_i, and f_s is taken as 20 kHz. With $V_{\rm dc}$ as 300 V and supply voltage dip as $v_{\rm ac} = 170$ V, the maximum ripple through the input inductor can be observed. Thus, the calculation of L_i is given as follows:

$$L_i = \frac{1}{0.4\times 20\,000}\left(\frac{170^2}{400}\right)\left(\frac{300}{300+170\sqrt{2}}\right) = 5.01\ \text{mH} \simeq 5\ \text{mH}.$$

Here, an inductor current ripple (η) is considered as 40%, therefore, an input inductor is selected as 5 mH.

B. Output Inductors (L_{o1} and L_{o2}) Design for DCM

The selected DCM of operation, provides good line drawn power quality, therefore, output inductors for Cuk converter are designed for discontinuous current. The calculation of output inductors is given as follows [13]–[15]:

$$L_o = \frac{V_{\rm dc}(1-D)}{2I_{Lo}f_s} = \frac{V_{\rm dc}D}{2I_{\rm in}f_s} = \frac{R_{\rm in}V_{\rm dc}D}{2V_{\rm in}f_s} = \left(\frac{V_s^2}{P_i}\right)\frac{V_{\rm dc}}{2V_{\rm in}f_s}\left(\frac{V_{\rm dc}}{V_{\rm in}+V_{\rm dc}}\right) \quad (3)$$

$$L_o = \left(\frac{V_s^2}{P_{\rm max}}\right)\frac{V_{\rm dc\ max}}{2\sqrt{2}V_s f_s}\left(\frac{V_{\rm dc\ max}}{V_{\rm dc\ max}+\sqrt{2}V_s}\right)$$

$$L_0 = \left(\frac{220^2}{400}\right)\frac{100}{2\sqrt{2}\times 220\times 20\,000}\left(\frac{100}{100+220\sqrt{2}}\right) = 236.48\ \mu\text{H}. \quad (4)$$

The value of the output inductor L_{o1} and L_{o2} is selected as 200 μH thus the required physical size of the inductor is reduced.

C. Design of Capacitors (C_1 and C_2) for Continuous Voltage

The capacitor voltages are kept in CCM as per the design. Therefore, the permitted ripple voltage (κ) is allowed for capacitors C_1 and C_2, thus its calculation is given as follows [15]–[17]:

$$C_1 = \frac{V_{\rm dc}D}{\Delta V_{c1} f_s R_L} = \frac{V_{\rm dc}D}{\Delta V_{c1} f_s R_L}. \quad (5)$$

For a rated dc-link voltage $V_{\rm dc}$ and input power P_i at this voltage, the value for load resistance R_L is given as $R_L = V_{\rm dc}^2/P_i$. To derive the expression for calculating the values of capacitor, the value of equivalent load resistance R_L and $V_{c(1,2)} = \{V_{\rm dc}+V_{\rm in}\}$ are substituted in (5) and the final expression after rearranging is obtained as follows:

$$C_1 = \frac{V_{\rm dc}}{\kappa\{V_{\rm dc}+V_{\rm in}\}f_s(V_{\rm dc}^2/P_i)}\left(\frac{V_{\rm dc}}{V_{\rm in}+V_{\rm dc}}\right) = \frac{P_{\rm max}}{\kappa\left(V_{\rm dc\ max}+\sqrt{2}V_{s\ \rm max}\right)^2 f_s}. \quad (6)$$

Therefore, at maximum power and rated $V_{\rm dc}$, i.e., $V_{\rm dc} = 300$ V with $V_{s\rm max} = 220$ V, the calculation for C_1 and C_2 is made for a ripple voltage (κ) as 10% as follows:

$$C_1 = C_2 = \frac{400}{0.1\times 20000\times\left(220\sqrt{2}+300\right)^2} = 535.50\ \text{nF}.$$

The above design ensures the continuous voltage across the two intermediate capacitors. Therefore, the capacitors are selected as 690 nF each.

D. Design of DC-Link Capacitor

The converter output appears across two midpoint capacitors $C_{\rm dc1}$ and $C_{\rm dc2}$, which are connected in series to generate midpoint *N*. The capacitor is determined to control $V_{\rm dc}$ with voltage ripple (δ) within 3%. However, the change in $V_{\rm dc}$ is considered from 100 to 300 V, therefore, the output capacitor is computed by the following [13]–[15]:

$$C_{\rm DC} = \frac{I_{\rm dc}}{2\omega\Delta V_{\rm dc}} = \frac{P_i/V_{\rm dc}}{2\omega\delta V_{\rm dc}}$$

$$C_{100} = \frac{P_{\rm min}}{2\omega\delta V_{\rm dc\ min}^2} = \frac{132}{2\times 314\times .03\times 100^2} = 700.63\ \mu\text{F}$$

$$C_{300} = \frac{P_{\rm max}}{2\omega\delta V_{\rm dc\ max}^2} = \frac{400}{2\times 314\times .03\times 300^2} = 235.90\ \mu\text{F}. \quad (7)$$

Therefore, two capacitors connected across dc link are chosen as $C_{\rm dc1} = C_{\rm dc2} = 1000\ \mu$F.

E. Design of Input Filter (L_f and C_f)

A passive *LC* filter is designed to eliminate switching harmonics. The peak values of input current and voltage are denoted by I_m and V_m and displacement angle by θ. The calculations for filter inductor L_f and filter capacitor C_f are given as follows [15]–[17]:

$$C_{\rm max} = \frac{I_m}{\omega_L V_m}\tan(\theta) = \frac{\left(P_o\sqrt{2}/V_s\right)}{\omega_L V_m}\tan(\theta) = \frac{\left(400\sqrt{2}/220\right)}{314\times 220\sqrt{2}}\tan(0.5^\circ) = 229.69\ \text{nF}. \quad (8)$$

Therefore, the value of C_f is taken as 220 nF. The design of the input filter is required to reduce the THD. A filter is a combination of inductor (L_f) and capacitor (C_f). The values of filter components are designed and tuned at less than one-tenth of the switching frequency. The high-frequency switching harmonics are absorbed by this filter, thus acting as an input current shaper. Considering the effect of source inductance L_s,

the calculation is given as follows:

$$L_f = L_{\text{req}} + L_s \Rightarrow \frac{1}{4\pi^2 {f_c}^2 C_f} = L_{\text{req}} + 0.04\left(\frac{1}{\omega_L}\right)\left(\frac{V_s^2}{P_i}\right)$$

$$L_{f\ \text{req}} = \frac{1}{4\pi^2 \times 2000^2 \times 220 \times 10^{-9}} - 0.04\left(\frac{1}{314}\right)\left(\frac{220^2}{400}\right) = 4.4\,\text{mH}. \quad (9)$$

Whereas a value of L_s is considered as 4% of base impedance, thus L_f is selected as 4.5 mH.

VI. Control Algorithm

The control of the proposed drive consists of control of PFC converter and SRM. The control is designed to operate the converter at high switching frequency to obtain inherent PFC and output voltage control. The switching frequency f_s is selected as 20 kHz to reduce the overall size of the system. To obtain PFC, two approaches are conventionally used, i.e., voltage follower approach and current follower approach. Considering the cost and size constraints, the voltage follower approach is adopted here. As the sensor requirement is reduced in this approach, the size of the inductor is also reduced while selecting this approach as the current through the inductor is allowed to enter the DCM.

A. Control of Front-End PFC Converter

The fully controlled two equal output voltages of the converter are varied up to 300 V to obtain motor speed control up to 1500 r/min. The proposed drive consists of a single voltage feedback loop control. This converter output dc voltage across one output capacitor (V_{dc1}) is compared with the reference voltage (v^*_{ref}). The output of the comparator is an error voltage (v_e) and this error voltage at any particular instant, is given as follows:

$$v_e(k) = v^*_{\text{ref}}(k) - V_{\text{dc1}}(k). \quad (10)$$

The controlled voltage signal is given as follows:

$$v_{c\text{dc}}(k) = v_{c\text{dc}}(k-1) + k_{pv}\{v_e(k) - v_e(k-1)\} + k_{iv}v_e(k). \quad (11)$$

The controlled voltage signal as shown in (11) is used to generate modulating signal to obtain controlled V_{dc}. Where the proportional gain is given as k_p and an integral gain is given as k_i. The output of the PI controller is finally compared with the high-frequency carrier signal at a frequency of 20 kHz. Therefore, the generated PWM pulses are at fixed frequency and a variable duty to obtain control of V_{dc} and PFC at ac mains.

B. Control of SRM

The control of SRM requires phase to phase commutation of current in accordance with rotor position (θ), which is achieved using position sensors. Here, the optical encoders-based sensors are used to determine the rotor position in the proposed drive. The motor control is based on switching sequence, which is given in Table I. The split dc converter is used to excite the motor phases with respect to switching sequence. In SRM, a discontinuous nature of the motor phase current results in high torque ripples when one motor phase is excited at a time, therefore, in the proposed SRM drive, the motor control is based on simultaneous excitation of two phases to get reduced torque ripples. Fig. 5 shows the path of current through motor phases during state I to state IV. However, phase A and phase B are excited during state I, which is then followed by a state II during this state, phase B and phase C are excited. Similarly, the excitation is realized for state III and state IV.

TABLE I
Switching States Based Upon Encoder Output

State	Encoder Output		SRM converter Pulses			
	P_1	P_2	G_1	G_2	G_3	G_4
State I	0	0	1	1	0	0
State II	0	1	0	1	1	0
State III	1	0	0	0	1	1
State IV	1	1	1	0	0	1

VII. Performance of SRM Drive

To study the performance of the proposed SRM drive, a prototype is developed of same motor and converter rating. The SRM is coupled to a dc generator (Benn make) feeding a resistive load bank. The voltage sensor is used to sense output capacitor voltage across one midpoint capacitor. The isolation to pulses is provided by using an opto-coupler (IC 6N136), however, for sensing dc-link voltage, a voltage sensor board is developed using a hall-effect voltage sensor (LV 25-P), with galvanic isolation between primary and secondary circuits. Pulse width modulated pulses for the midpoint converter and the proposed PFC converter are generated using DSP-dSPACE-1104. The obtained test results on a developed prototype are discussed as follows.

A. Performance of Drive During Steady-State Conditions

The SRM is operated while energizing two motor phases at a time. The sequence for exciting the motor phases is decided on the basis of rotor position information as shown in Table I. Here, optical encoders are used to achieve the rotor position. Fig. 6(a) shows test results obtained with two motor phases excited at the same instant as per the given switching sequence. The motor phase currents at any instant are recorded and demonstrated in Fig. 6(b). The proposed converter possesses self-balancing of two output capacitor voltages without any voltage balancing. During two half-cycles of the supply voltage, both the output capacitors are charged separately, thus maintaining V_{dc} as 300 V, with two output capacitors voltages as 150 V each, which is shown in Fig. 6(c). As per the proposed design, the speed control is obtained up to 1500 r/min with dc-link voltage variation up to 300 V. Fig. 6(d) shows the improved power quality operation at rated speed as 1500 r/min and rated V_{dc} of 300 V. The input current is in phase with supply voltage with reduced current THD. The motor performance is also evaluated at V_{dc} of 100 V as shown in Fig. 6(e), however, the motor speed is recorded as 490 r/min at this voltage.

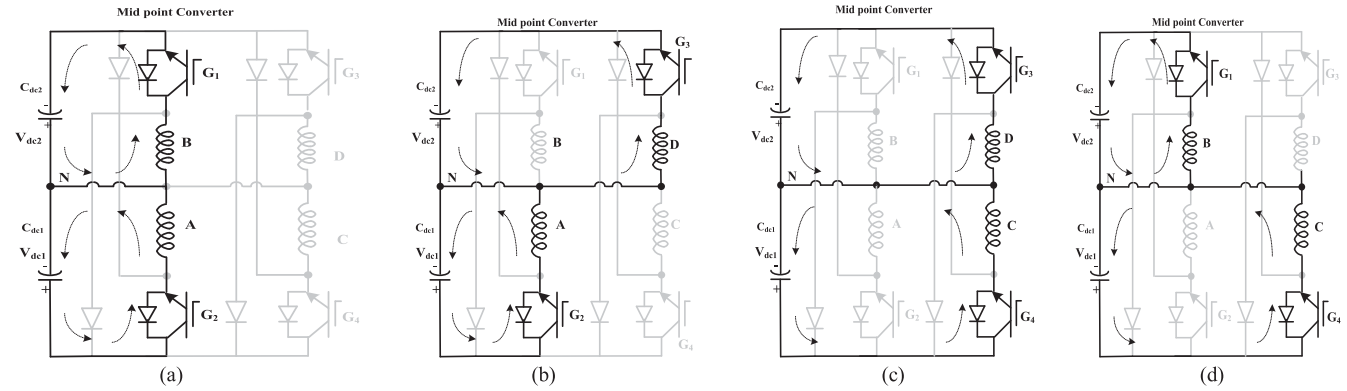

Fig. 5. Operation of SRM during four different switching states.

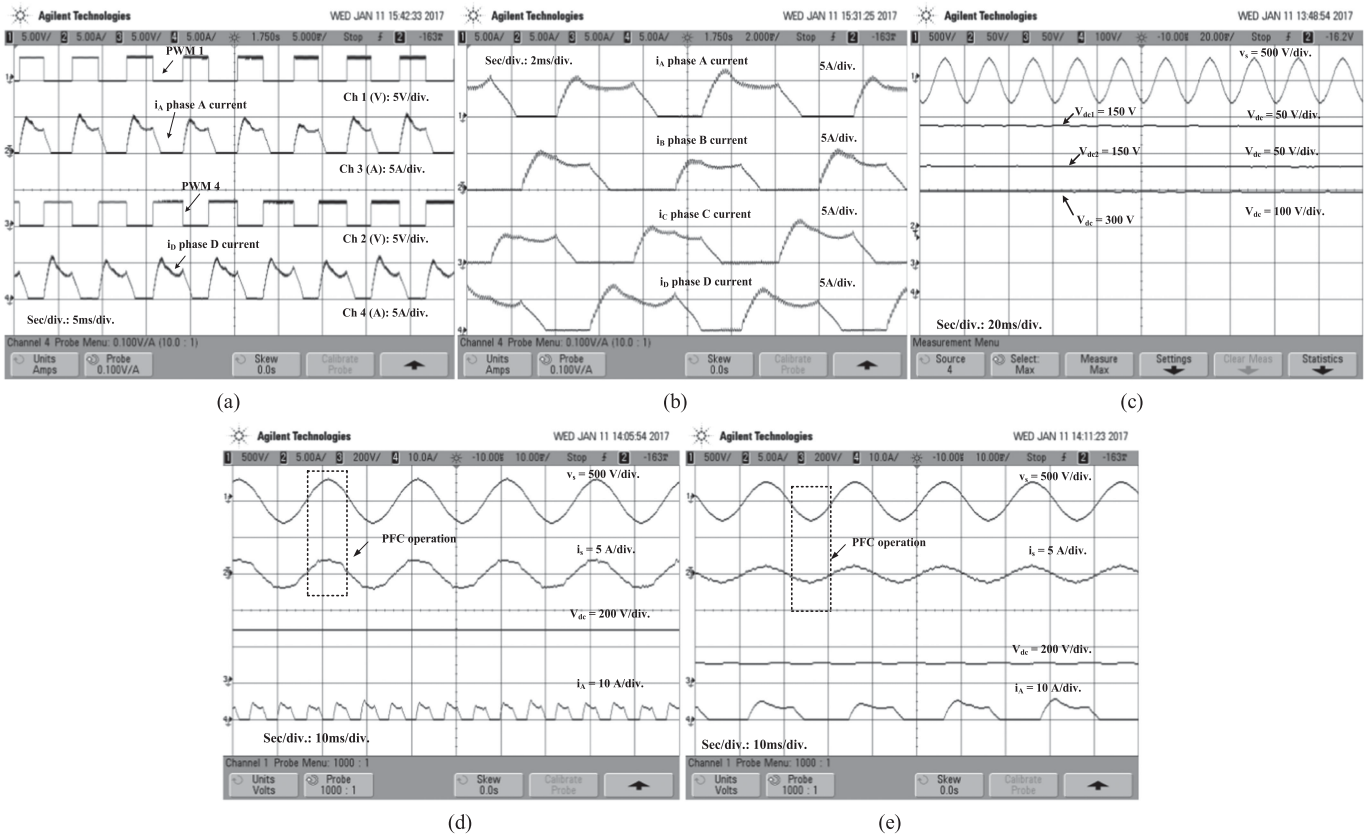

Fig. 6. Obtained results demonstrating. (a) Two motor phases excitation at any instant. (b) Motor current at rated speed. (c) Voltage across two output capacitors as $V_{dc1} = V_{dc2} = 150$ V. (d) Improve power quality operation with V_{dc} as 300 V. (e) PFC operation at $V_{dc} = 100$ V.

B. Performance of the Proposed Converter

The selection of magnetic component of the proposed converter is made such that the output side inductor of the Cuk converter operates in DCM and the input side inductor is common to both converters in CCM. Fig. 7(a) shows the voltages across both the intermediate capacitors. Moreover, these capacitors are operating in CCM as per the design. The enlarged view of Fig. 7(a) is shown in Fig. 7(b) to demonstrate the discontinuous current through output inductors. The large freewheeling current period through both the inductors depicts the DCM of operation of the proposed converter. An inductor L_i operates in CCM with permissible current ripple up to 40%. However, Fig. 7(d) shows currents through all three inductors, whereas current in high-resolution mode is also shown on the right corner of the figure to demonstrate the sinusoidal nature of input inductor current operating in CCM. The peak voltage across and current stress through switch are shown in Fig. 7(e). Moreover, the peak voltage stress across switch is recorded as 620 V. The peak current stress through switch is calculated as the summation of input inductor current and output inductor current, i.e., 14 A.

C. Drive Performance During Dynamic Conditions

The proposed drive is designed for the variable speeds. Therefore, the motor performance is evaluated at different dynamic conditions during the speed change. Fig. 8(a) shows the

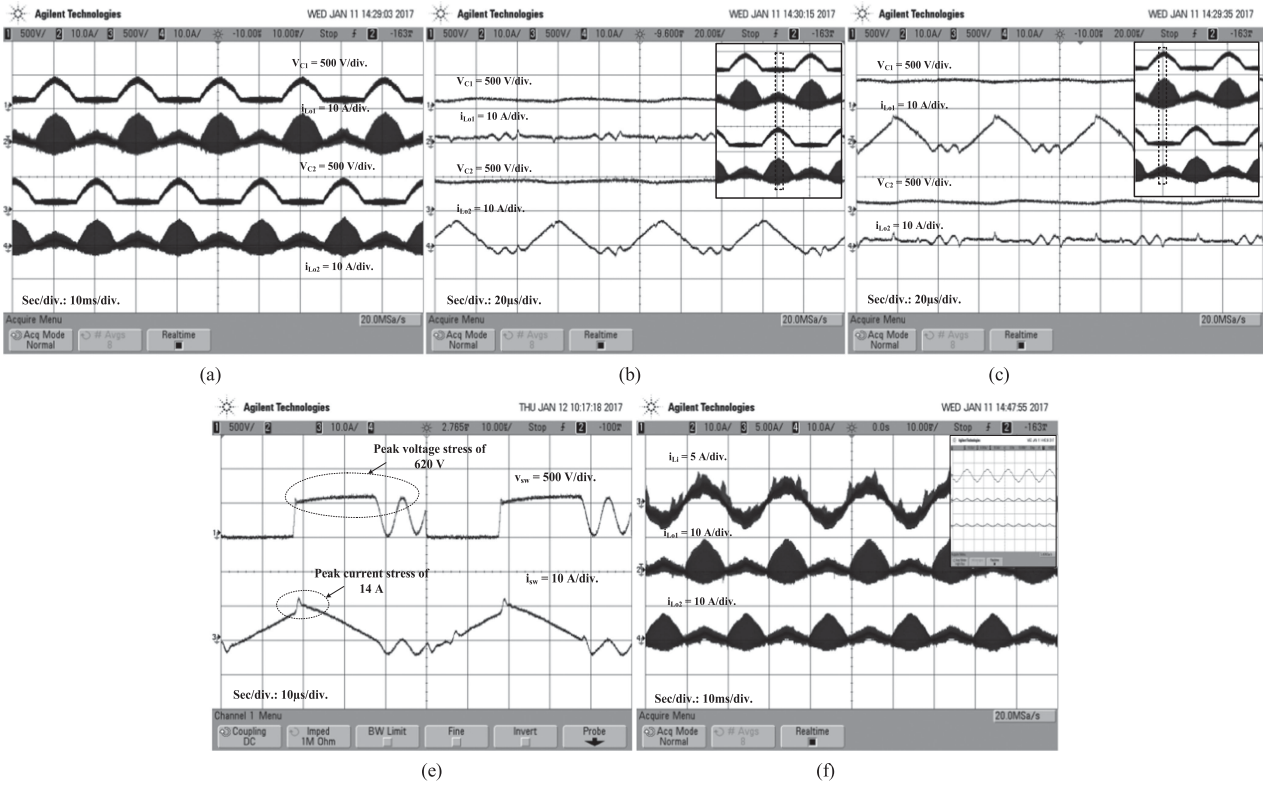

Fig. 7. Obtained results showing (a) continuous capacitor voltages and discontinuous inductor currents through two Cuk converters, (b), (c) enlarge view showing DCM of operation, (d) current through input inductor and two output inductors, and (e) peak current and voltage stress across the switch.

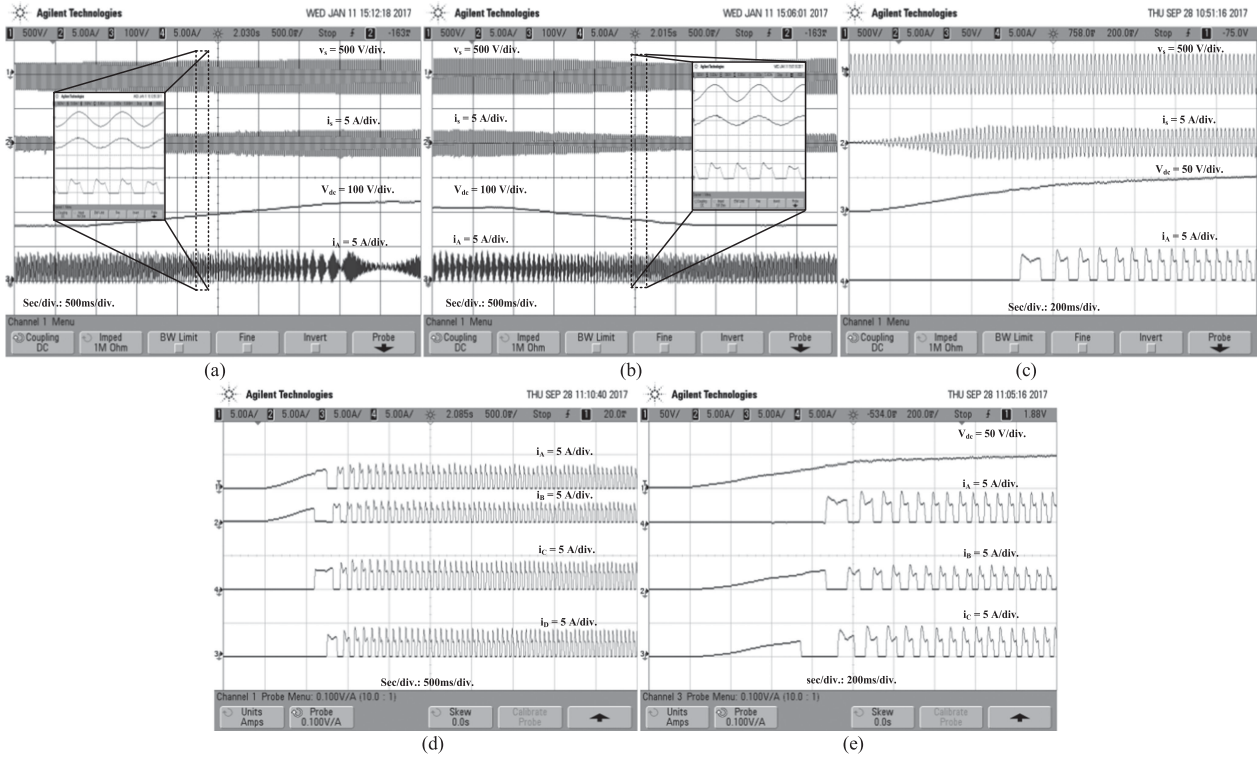

Fig. 8. Experimental results during change in V_{dc} as (a) 170–250 V, (b) 230–150 V, (c) input voltage, input current, and motor phase current during starting, (d) current in all the four motor phases during starting, and (e) motor phase current with V_{dc} as 50 V.

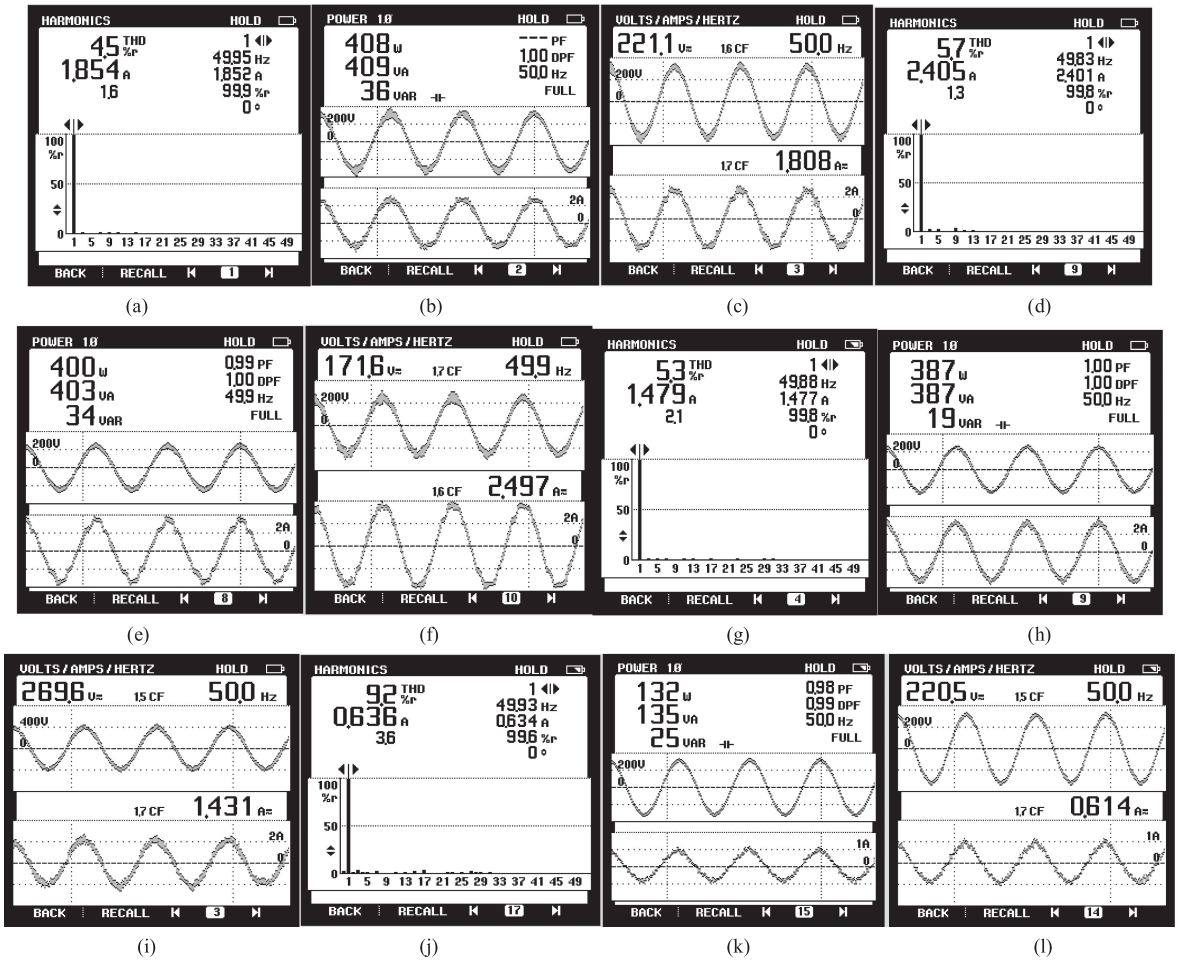

Fig. 9. Power quality results at different input voltages as: (a)–(c) $V_{ac} = 220$ V, (d)–(f) $V_{ac} = 170$ V, (g)–(i) $V_{ac} = 270$ V, and (j)–(l) at reduced dc-link voltage as 100 V and input voltage as $V_{ac} = 220$ V.

dynamics with a sudden increase in the speed with change in V_{dc}. Here, dc-link voltage is increased from 170 to 250 V such that change in the motor speed is observed from 760 to 1240 r/min. Due to large time scale of 500 m/s and limited record length of DSO, the enlarged view is demonstrated in the same figure. Fig. 8(b) shows the dynamics with a decrease in V_{dc} from 230 to 150 V such that a decrease in the motor speed is observed from 1210 to 730 r/min. These figures show the obtained speed control with stable operation of drive after dynamic condition. Similarly, the system dynamics during starting are also observed and shown in Fig. 8(c)–(e). Moreover, Fig. 8(d) shows the current through motor phases during starting and currents through three motor phases with dc-link voltage on one channel are shown in Fig. 8(e). The limited motor current is observed in the test results with reduced dc-link voltage. Therefore, test results have demonstrated satisfactory motor performance during different transient conditions.

D. PFC Operation of the Proposed Converter

Power quality indices such as power factor, input current THD, and distortion power factor are recorded using single-phase power analyzer. Fig. 9(a)–(c) show the performance at converter output and input voltage as $V_{dc} = 300$ V and $v_{ac} = 220$ V. These test results show the reduced input current THD of 4.5% at rated load condition. The power quality parameters are also evaluated for practical supply conditions with momentarily dip in supply voltage from 220 to 170 V. Moreover, at reduced voltage of 171.6 V, the input current THD obtained is 5.7%, which is shown in Fig. 9(d)–(f). Similarly, Fig. 9(g)–(i) show the obtained input current THD of 5.3% with momentarily increase in supply voltage from 220 to 270 V. The performance is evaluated at different motor speeds with different dc-link voltages. Fig. 9(j)–(l) show the drive performance at $V_{dc} = 100$ V. Moreover, the input current THD is obtained as 9.2%. Therefore, test results demonstrate the improved power quality operation of the proposed drive over a wide speed range with input current THD under acceptable limits.

E. Comparative Analysis

The performance of the proposed dual output converter-fed SRM drive is investigated and compared, which is shown in Fig. 10. The uncontrolled diode bridge rectifier (DBR)-fed SRM drive, consists of bulky dc-link capacitor, which draws peaky current from mains with short conduction period. Moreover, the Cuk converter-based SRM drive consists of conventional Cuk converter with single output voltage. V_{dc1} and V_{dc2} are obtained

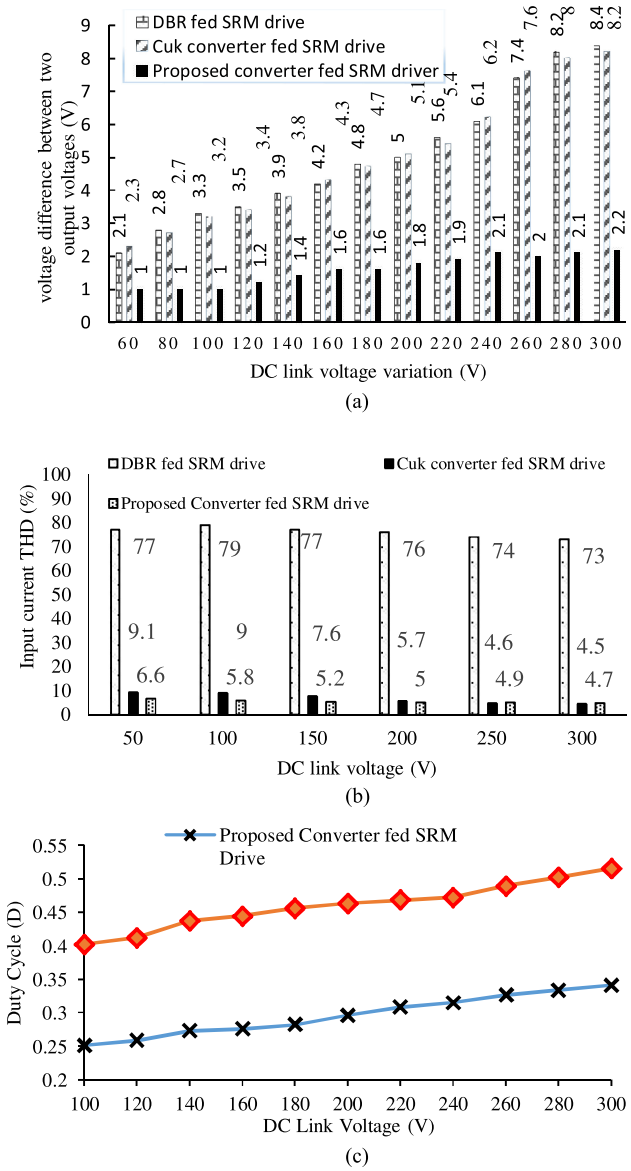

Fig. 10. Comparison between conventional converter, Cuk converter, and proposed converter at different dc-link voltages on the basis of (a) voltage variation between two output voltages, (b) input current THD, and (c) duty cycle variation with reference to change in $V_{\rm dc}$.

with voltage difference between them as 2.2 V at rated dc-link voltage. Whereas in DBR-fed SRM drive and conventional Cuk converter-fed SRM drive, the voltage differences are 8.4 and 8.2 V. Fig. 10(a) shows the detailed comparison at different dc-link voltages varying from 60 to 300 V. Fig. 10(b) shows the input current THD over different dc-link voltages. The proposed converter has high input to output voltage transfer ratio compared to conventional Cuk converter, which is shown in Fig. 10(c).

VIII. Conclusion

Test results have validated the performance of a modified dual output Cuk converter-fed SRM drive. The modified Cuk converter with two identical output voltages has been designed with discontinuous output inductor current. The selected design of an inductor has reduced the size and cost of the magnetic components. The converter output voltage is well regulated by the single voltage sensor with inherent wave shaping of the input current. The wide range of speed control has also been obtained while using only one voltage sensor at converter output. Drive performance under steady and dynamics state is found satisfactory. The input current THD of reduced value is obtained under the recommended limit of an IEC 61000-3-2 standard. Aiming at cost-effective alternative to conventional electric drives, an SRM drive turned out to be a good selection for home appliances.

Appendix

The DCM operation requires an additional time interval as compared to the CCM operation. Either the inductor current or the capacitor voltage remains zero during this time interval. Here, the first interval, i.e., switch ON period is considered as D_1T when the inductor current starts rising and reaches peak at the end and starts decreasing with the start of interval D_2T, i.e., switch OFF period. The time interval for constant or zero inductor current is here denoted by D_3T. Choosing the input inductor current as i_{L1}, voltage across the intermediate capacitor as V_{C1}, output inductor current as i_{Lo1}, and voltage across the output capacitor as $V_{\rm dc1}$ as state-space variables, therefore the state-space model equations are given as follows:

$$\dot{X} = A_1 X + B_1 V_G \tag{12}$$

$$\dot{X} = A_2 X + B_2 V_G \tag{13}$$

$$\dot{X} = A_3 X + B_3 V_G \tag{14}$$

$$V_{\rm dc} = CX. \tag{15}$$

Where X represents state vector, A_1, A_2, and A_3 are the state matrixes, B_1, B_2, and B_3 are the input matrixes. The output state matrix is represented by C matrix, therefore, the circuit equations above state matrixes can be derived as follows:

$$X = \begin{bmatrix} i_{Li} \\ V_{C1} \\ i_{Lo1} \\ V_{\rm dc1} \end{bmatrix} \tag{16}$$

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & -1/C_1 & 0 \\ 0 & 1/L_{o1} & 0 & -1/L_{o1} \\ 0 & 0 & 1/C_{\rm dc1} & -1/C_{\rm dc1}R \end{bmatrix} B_1 = \begin{bmatrix} 1/L_i \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{17}$$

$$A_2 = \begin{bmatrix} 0 & -1/L_i & 0 & 0 \\ 1/C_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1/L_{o1} \\ 0 & 0 & 1/C_{\rm dc1} & -1/C_{\rm dc1}R \end{bmatrix} B_2 = \begin{bmatrix} 1/L_i \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{18}$$

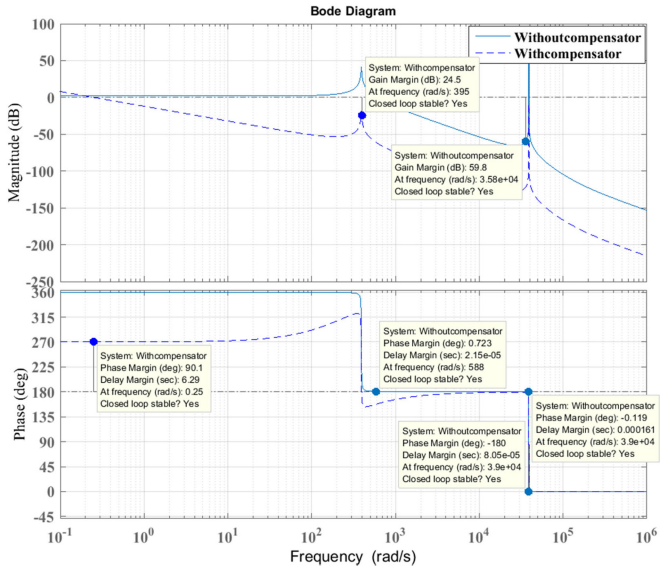

Fig. 11. Bode plot of open-loop and closed-loop transfer function showing system stability.

$$A_3 = \begin{bmatrix} 0 & -1/L_e & 0 & 1/L_e \\ 0 & 0 & 1/C_2 & 0 \\ 0 & 1/L_e & 0 & -1/L_e \\ 0 & 0 & -1/C_1 & 1/C_{\text{dc1}}R \end{bmatrix} B_3 = \begin{bmatrix} 1/L_e \\ 0 \\ -1/L_e \\ 0 \end{bmatrix}. \tag{19}$$

Whereas

$$A = A_1 D_1 + A_2 D_2 + A_3 D_3 \tag{20}$$

and

$$L_e = L_i + L_{o1}. \tag{21}$$

The interval of constant or zero inductor current can be given as $D_3 = 1 - (D_1 + D_2)$

$$G = \frac{V_o}{v_s}(s) = E[sI - A]^{-1} B. \tag{22}$$

Here G denotes the transfer function of the converter, whereas transfer function for the PI controller is given as follows:

$$G_c(s) = k_p + \frac{k_i}{s}. \tag{23}$$

The Bode plots are shown in Fig. 11, which are obtained using (22) and (23), however, these figures demonstrate good stability of the proposed system. The value of the circuit parameters for determining the system stability, are selected as$L_i = 5$ mH, $L_{o1} = 200\ \mu$H, $C_1 = 690$ nF, and $C_{\text{dc}} = 1000\ \mu$F.

Motor Rating and Controller Gains:

$P_{\text{rated}} = 400$ W; rated speed $= 1500$ r/min; $V_{\text{dc}}(V_{dc1} + V_{dc2}) = 300$ V; 8 stator poles; 6 rotor poles; motor phase $= 4$; rated torque 2.54 N·m; motor winding resistance $(R) = 0.7\,\Omega$, minimum Inductance $(L_u) = 12$ mH, aligned inductance $(L_a) = 110$ mH; $K_p = 0.01$; $K_i = 0.0008$.

REFERENCES

[1] *Limits for Harmonic Current Emissions (Equipment Input Current ≤16 A Per Phase)*, IEC61000-3-2, 2000.

[2] K. Ha, C. Lee, J. Kim, R. Krishnan, and S. G. Oh, "Design and development of low-cost and high-efficiency variable-speed drive system with switched reluctance motor," *IEEE Trans. Ind. Appl.*, vol. 43, no. 3, pp. 703–713, May/Jun. 2007.

[3] Y. Sozer and D. A. Torrey, "Optimal turn-off angle control in the face of automatic turn-on angle control for switched-reluctance motors," *IET Elect. Power Appl.*, vol. 1, no. 3, pp. 395–401, May 2007.

[4] I. Husain, "Minimization of torque ripple in SRM drives," *IEEE Trans. Ind. Elect.*, vol. 49, no. 1, pp. 28–39, Feb. 2002.

[5] J. Y. Chai, Y. C. Chang, and C. M. Liaw, "On the switched-reluctance motor drive with three-phase single-switch switch-mode rectifier front-end," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1135–1148, May 2010.

[6] K. Yao, X. Ruan, X. Mao, and Z. Ye, "Variable-duty-cycle control to achieve high input power factor for DCM boost PFC converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1856–1865, May 2011.

[7] T. Yan, J. Xu, F. Zhang, J. Sha, and Z. Dong, "Variable-on-time-controlled critical-conduction-mode flyback PFC converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 6091–6099, Nov. 2014.

[8] Z. Wang, S. Wang, P. Kong, and F. C. Lee, "DM EMI noise prediction for constant on-time, critical mode power factor correction converters," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3150–3157, Jul. 2012.

[9] T. J. Liang, K. H. Chen, and J. F. Chen, "Primary side control for flyback converter operating in DCM and CCM," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3604–3612, Apr. 2018.

[10] S. F. Lim and A. M. Khambadkone, "A simple digital DCM control scheme for boost PFC operating in both CCM and DCM," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1802–1812, Jul./Aug. 2011.

[11] J. W. Kolar, H. Ertl, and F. C. Zach, "Design and experimental investigation of a three-phase high power density high efficiency unity power factor PWM (VIENNA) rectifier employing a novel integrated power semiconductor module," in *Proc. 11th Annu Appl. Power Electron. Conf. Expo.*, San Jose, CA, USA, 1996, vol. 2, pp. 514–523.

[12] V. Bist and B. Singh, "PFC cuk converter-fed BLDC motor drive," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 871–887, Feb. 2015.

[13] V. Bist and B. Singh, "A unity power factor bridgeless isolated cuk converter-fed brushless DC motor drive," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4118–4129, Jul. 2015.

[14] B. Singh and A. Anand, "Switched capacitor converter fed SRM drive with power factor correction," in *Proc. Nat. Power Syst. Conf.*, Bhubaneswar, India, 2016, pp. 1–6.

[15] A. Anand and B. Singh, "Power factor correction in cuk-SEPIC based dual output converter fed SRM drive," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1117–1127, Feb. 2018.

[16] A. Anand and B. Singh, "Design and implementation of PFC Cuk converter fed SRM drive," *IET Power Electron.*, vol. 10, no. 12, pp. 1539–1549, 2017.

[17] A. Anand and B. Singh, "PFC-based half bridge dual-output converter-fed four-phase SRM drive," *IET Elect. Power Appl.*, vol. 12, no. 2, pp. 281–291, Feb. 2018.

Aniket Anand (S'15–M'16) was born in Lucknow, India, in 1987. He received the B.Tech. degree in electrical engineering from Uttar Pradesh Technical University, Lucknow, in 2009, and the M.Tech. degree in power electronics and drives from Madan Mohan Malaviya Engineering College, Gorakhpur, India, in 2012. He is currently working toward the Ph.D. degree at the Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, India.

His research interests include power electronics, and electrical machines and drives.

Bhim Singh (SM'99–F'10) was born in Bijnor, India, in 1956. He received the B.E. degree in electrical engineering from the University of Roorkee, Roorkee, India, in 1977, the M.Tech. degree in power apparatus and systems and the Ph.D. degree from the Indian Institute of Technology Delhi, New Delhi, India, in 1979 and 1983, respectively.

In 1983, he joined the Department of Electrical Engineering, University of Roorkee (now IIT Roorkee), as a Lecturer. He became a Reader in 1988. In December 1990, he became an Assistant Professor with the Department of Electrical Engineering, IIT Delhi, where became an Associate Professor in 1994 and a Professor in 1997. He has been the ABB Chair Professor from September 2007 to September 2012. He was the CEA Chair Professor from October 2012 to September 2017. He was the Head with the Department of Electrical Engineering, IIT Delhi, from July 2014 to August 2016. Since August 2016, he has been the Dean, Academics, with IIT Delhi. He is the JC Bose Fellow of DST, Government of India, since December 2015. He has guided 69 Ph.D. dissertations, and 167 M.E./M.Tech./M.S.(R) theses. He has been filed 31 patents. He has executed more than eighty sponsored and consultancy projects. He has coauthored a text book on power quality: *Power Quality Problems and Mitigation Techniques* (John Wiley & Sons Ltd., 2015).

His research interests include solar PV grid interface systems, microgrids, power quality monitoring and mitigation, solar PV water pumping systems, improved power quality ac–dc converters, power electronics, electrical machines, drives, flexible alternating transmission systems, and high-voltage direct current systems.

Dr. Singh is a Fellow of the Indian National Academy of Engineering, The Indian National Science Academy, The National Academy of Science, India, The Indian Academy of Sciences, India, The World Academy of Sciences, Institute of Electrical and Electronics Engineers, the Institute of Engineering and Technology, Institution of Engineers (India), and Institution of Electronics and Telecommunication Engineers, and a Life Member of the Indian Society for Technical Education, System Society of India, and National Institution of Quality and Reliability. He was the recipient of the Khosla Research Prize of University of Roorkee in the year 1991, the JC Bose and Bimal K Bose awards of The Institution of Electronics and Telecommunication Engineers (IETE) for his contribution in the field of Power Electronics, the Maharashtra State National Award of Indian Society for Technical Education in recognition of his outstanding research work in the area of Power Quality, the PES Delhi Chapter Outstanding Engineer Award for the year 2006, the Khosla National Research Award of IIT Roorkee in the year 2013, the Shri Om Prakash Bhasin Award-2014 in the field of Engineering including Energy & Aerospace, the IEEE PES Nari Hingorani Custom Power Award-2017, and the "Faculty Research Award as a Most Outstanding Researcher" in the field of Engineering-2018 of Careers-360, India.