Discontinuous-Modulation-Based Active Thermal Control of Power Electronic Modules in Wind Farms

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***Abstract*—With the increasing renewable energy injected into the electrical distribution grid, the reliability of the power converter is gaining importance for the power system. In order to address the wear-out caused failure mechanisms of power semiconductors and thereby increasing the reliability, this paper aims at balancing the thermal stress caused during operation between different power converters in a wind park. An active thermal control strategy based on the discontinuous pulsewidth modulation is proposed for reducing the thermal stress of the semiconductors under a fluctuating power profile, while maintaining good power quality. The proposed method is introduced for multiple converters, which are connected to the same grid feeder and its impact on the lifetime of the semiconductors is investigated analytically. Finally, the effectiveness of the proposed method is experimentally validated for a two-level voltage source converter.**

***Index Terms*—Active clamping angle, active thermal control, discontinuous pulsewidth modulation (DPWM), reliability, two-level converter, wind turbine.**

I. Introduction

THE INCREASING number of wind turbines, built on-shore and off-shore, leads to an increasing importance of power converters for the power system. Their importance is being reflected in the obligation to provide grid services, whereas the reliability of the converters is a potential point for improvements, because of the high costs caused by their failures and system down times [1]. Based on the finding that power semiconductors in power modules are one of the most frequently failing components [2], [3], high effort has been made to detect open- and short-circuit failures, stop immediately the operation, and send this information to a management system [4]–[7]. Although the fault detection can prevent secondary destruc-

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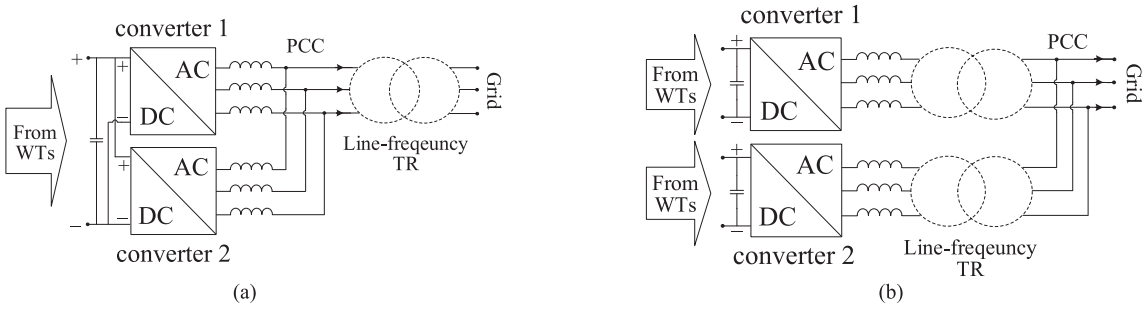

Fig. 1. Configurations of the paralleled converters connected to a same PCC. (a) With common dc-link. (b) With separated dc-link.

have a different useful remaining lifetime. This may be affected by uneven stresses or earlier failures in one of them, e.g., the replacement of a failed converter. In other words, if converters have a shorter remaining useful lifetime than other converters, their thermal stress will be reduced and therefore their lifetime will be increased with the target to improve the reliability of the overall system, whereas other converters with a longer lifetime are operated to aim at improving the power quality of the PCC.

The impact of the thermal stress on the power module's lifetime is discussed in Section II. Section III introduces the proposed strategy to reduce the thermal stress and to reduce the total harmonic distortion (THD) of the currents connected to the same PCC. The strategy to reduce the magnitude of the thermal cycles is proposed with the analysis of the loss distribution, taking into account the two-level voltage source converter in Section IV. In Section V, the evaluation of the algorithm's potential and the lifetime are carried out. Finally, the proposed method is experimentally demonstrated to verify the effectiveness of the thermal stress reduction in Section VI before the conclusion of this paper is drawn in Section VII.

II. Influence of Thermal Stress on Lifetime

The power semiconductors undergo thermal cycling and power cycling, which are affected by the mission profile. Thermal cycling is caused by ambient temperature variations, whereas power cycling is caused by the power fluctuations of the application and its resultant variation of the power converter losses. Both power cycling and thermal cycling cause thermal stress and result in the wear-out of the power semiconductors. A well-known approach to estimate the module's lifetime in dependence of the thermal cycles is the Coffin–Manson–Arrhenius model. The number of cycles to failure N_f is described as a function of the amplitude of thermal cycles ΔT_j, and the average temperature $T_{j,\mathrm{av}}$. Other coefficients a_1, a_2, and n are extracted from a dataset of multiple reliability experiments and they are adjusted for best match to the module. It can be expressed as

$$N_f = a_1 \cdot (\Delta T_j)^n \cdot e^{\frac{a_2}{T_{j,\mathrm{av}}}}. \tag{1}$$

As it can be seen in the lifetime model, the equations only indicate a single magnitude of thermal cycles ΔT_j. In contrast to this, the power semiconductors in operation undergo thermal cycles, which are superimposing each other. The common approach for taking this into account is to apply linear damage accumulation with Miner's rule. The Miner's rule is written as

$$C = \sum_{i=0}^{\inf} \frac{n_i}{N_{f(i)}} \leq 1. \tag{2}$$

In the following, an active thermal control algorithm is proposed for achieving a reduction of the thermal stress for the power semiconductors and consequently increase their lifetime. Without the application of active thermal control, the lifetime is dependent on the system design, including the quality of the components, and the mission profile. The thermal stress can be influenced with the application of active thermal control, whereby the algorithm and its limitations influence the potential increase of the lifetime.

III. Active Thermal Control of Paralleled Converters Connected to the Same PCC

This section presents the active thermal control strategy based on the discontinuous modulation in order to prolong power semiconductor's remaining useful lifetime, considering paralleled converters which shall inherently have different degradation due to the aging process [16]. In the following, the principle of the proposed method to reduce the thermal stress is theoretically explained and afterward, the modulation strategy is described to achieve both: reduced thermal stress and a good power quality at the PCC.

A. Principle of Thermal Stress Reduction

For the thermal stress reduction, active thermal control is applied to reduce the number of thermal cycles and the amplitude of the thermal cycles. The thermal stress is further related to the cooling system performance, ambient condition, and power losses generated in the semiconductor chips (IGBTs and diodes) in power module. In order to address the root cause of the thermal stress for the power semiconductors, the losses are highly relevant. These losses can be divided into the conduction losses and the switching losses.

The discontinuous modulation has been typically implemented for reducing the switching losses, whose principle is based on clamping the output voltage either at a positive or negative dc-link voltage. Therefore, during the clamping period only conduction losses are affected in the clamped devices [22]–[24]. This paper proposes to exploit the clamping angle as the control variable for manipulating the switching losses.

Consequently, the active thermal control algorithm reduces the thermal stress. As presented before, the total losses $P_{\mathrm{loss},t}$ are calculated by a summation of the conduction losses $P_{\mathrm{loss,cd}}$ and the switching losses $P_{\mathrm{loss,sw}}$, which itself can be represented as a function of the loaded power P_{load} and the clamping angle φ for the proposed method is expressed as follows:

$$P_{\mathrm{loss},t}(P_{\mathrm{load}},\varphi) = P_{\mathrm{loss,cd}}(P_{\mathrm{load}},\varphi) + P_{\mathrm{loss,sw}}(P_{\mathrm{load}},\varphi). \tag{3}$$

As analyzed in [25], the modulation methods only marginally affect the total conduction losses. Therefore, (3) can be expressed with the modified term for the conduction losses with (4), which results in a straightforward relation between the total losses and the clamping angle

$$\underbrace{P_{\mathrm{total}}(P_{\mathrm{load}},\varphi)}_{\varphi-\mathrm{dependent}} = P_{\mathrm{cond}}(P_{\mathrm{load}}) + \underbrace{P_{\mathrm{sw}}(P_{\mathrm{load}},\varphi)}_{\varphi-\mathrm{dependent}}. \tag{4}$$

The loading power is determined by the wind profile, meaning that the power of the converter cannot be manipulated without reducing the harvested power. However, the clamping angle φ affects the switching losses and the total losses, which are highlighted in (4). Therefore, it is interesting to characterize the effectiveness of the clamping angle on the losses. For the sake of simplicity, it is assumed that the power semiconductor has a linear turn-on and -off characteristics and only the fundamental component of the load current is considered (e.g., 50/60 Hz). Hence, the average switching losses over the fundamental period can be obtained with below equation [22]

$$P_{\mathrm{sw}} = f_{\mathrm{sw}} \frac{E_{\mathrm{on}} + E_{\mathrm{off}}}{2\pi} \frac{V_{\mathrm{dc}}}{V_{\mathrm{dc,ref}}} \frac{1}{I_{\mathrm{ref}}} \int_0^{\pi} f_i(\theta) d\theta \tag{5}$$

where V_{dc} is the dc-link voltage, E_{on} and E_{off} are the turn-on and -off energy for the reference dc-link voltage $V_{\mathrm{dc,ref}}$, and the reference load current, I_{ref}, respectively, and f_{sw} is the switching frequency. The load current function $f_i(\theta)$ is expressed with (6) according to the operating region. The region is either the clamping or non-clamping region, assuming the steady-state operating condition where the current is periodical sinusoidal

$$f_i(\theta) = \begin{cases} 0 & (\text{for clamping region}) \\ I_{\max} \cdot \sin(\theta) & (\text{for non-clamping region}) \end{cases} \tag{6}$$

where $I_{\max}$ is the amplitude and θ is the angle of the load current. Consequently, the effects of the clamping angle on the switching losses can be validated with SLF as (7), which normalizes the value of the switching losses by that of the continuous modulation. Furthermore, it should be noted that unity power factor is considered in the following analysis:

$$\mathrm{SLF} = \frac{P_{\mathrm{loss,sw}}[0; \frac{\pi-\varphi}{2}] + P_{\mathrm{loss,sw}}[\frac{\pi+\varphi}{2}; \pi]}{P_{\mathrm{loss,sw}}[0;\pi]} = \frac{P_{\mathrm{loss,sw,dm}}}{P_{\mathrm{loss,sw,cm}}} \tag{7}$$

where $P_{\mathrm{loss,sw,cm}}$ and $P_{\mathrm{loss,sw,dm}}$ are the switching losses with the continuous and the discontinuous modulation, respectively. The SLF as a function of the clamping angle is shown in Fig. 2 and it is shown that the clamping angle highly contributes to the switching loss reduction. Remarkably, for a clamping angle of 60°, the maximum switching loss reduction is 50%.

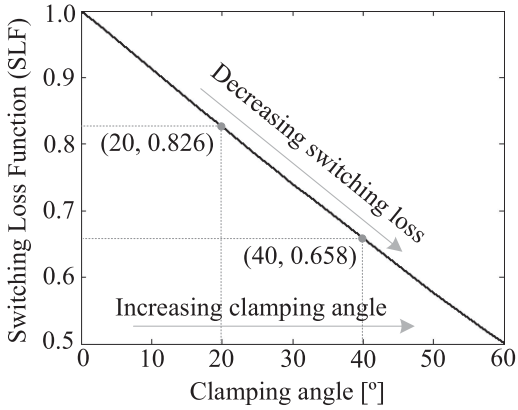

Fig. 2. Switching loss function (SLF) as a function of the clamping angle.

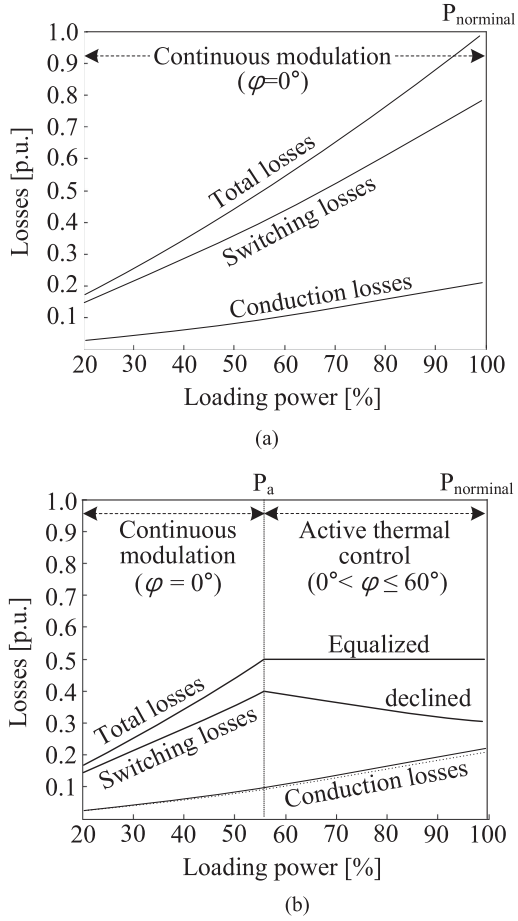

Fig. 3. Example of the loss distribution. (a) With the conventional continuous modulation. (b) With the proposed active thermal control strategy to compensate the thermal cycling of more aged converters by equalizing the total losses for a certain power range ($P_a - P_{\mathrm{norminal}}$ as a case study).

Fig. 3(a) visualizes the dependence of the losses on the power. Consequently, it can be expected that thermal cycling will be caused by power variations during system operation. The proposed method of using the clamping angle, as expressed in (4), targets to equalize the total losses for a specific power range as shown in Fig. 3(b), where the clamping angle varies from 0° to 60°. This so-called *active clamping angle* allows constant losses

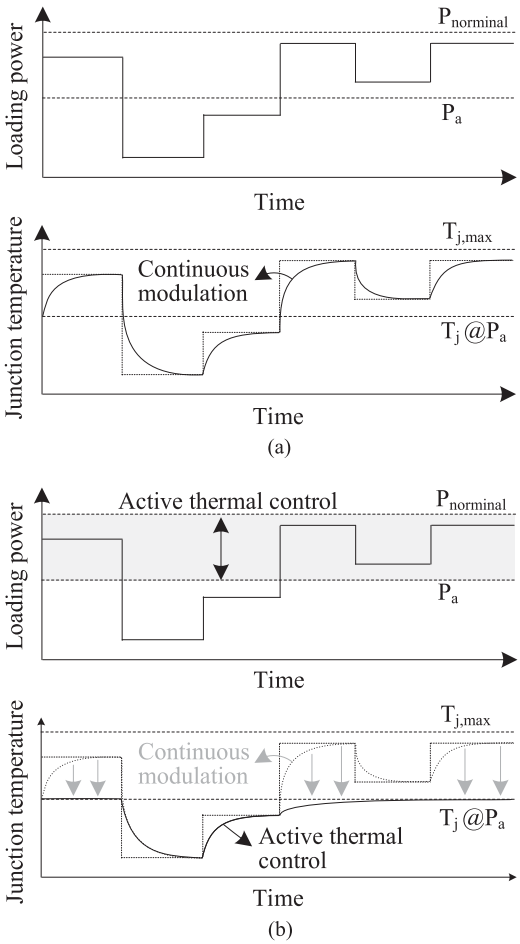

Fig. 4. Schematic junction temperature variation (bottom) under a fluctuating power profile (top) with (a) conventional continuous modulation and (b) proposed active thermal control considering the loss distribution in Fig. 3 as a case study.

in the specific power range ($P_a \leq P_{\rm load} \leq P_{\rm nominal}$), whereas the continuous modulation ($\varphi = 0^\circ$) is adopted out of the active thermal control region ($0 \leq P_{\rm load} \leq P_a$). Moreover, the proposed method features the reduced losses in the active thermal control region (heavy load) while keeping the same loss distribution in a light load region, which is an inherited advantage for the target to reduce the thermal stress. Additionally, the dominance of the switching losses is shown in order to demonstrate the capability of the proposed method for controlling the total losses.

For better understanding the effect of the proposed method on the thermal cycling reduction, Fig. 4 shows the junction temperature of power semiconductors in a module with the loss characteristic in Fig. 3 under a power profile. As it can be expected, the junction temperature fluctuations are dependent on the power profile without the active thermal control [see Fig. 4(a)], whereas the thermal cycling can be reduced in the effective power range ($P_a < P_{\rm load} < P_{\rm nominal}$ in Fig. 3) as shown in Fig. 4(b).

B. Modulation for Power Quality Improvement

The THD is an important benchmark to evaluate the power quality of voltage source converters. For the proposed thermal controller, the effect of the clamping angle on the THD is investigated. The modulation strategy consisting of two different modulation signals is proposed as shown in Fig. 5. The modulation signal for the thermal cycling compensation is shown in Fig. 5(a) and named as $v_{\rm ref,ACT}$, while Fig. 5(b) is the modulation signal ($v_{\rm ref,THD}$) for improving the current quality. Therefore, these modulation signals are injected depending on their lifetime, e.g., the converter with the lower remaining useful lifetime is modulated by $v_{\rm ref,ACT}$, whereas a converter with a higher remaining useful lifetime is modulated with $v_{\rm ref,THD}$. It is worth to mention that the power losses for the converter modulated by $v_{\rm ref,THD}$ is comparable to the case of the continuous modulation, meaning that its lifetime is not affected.

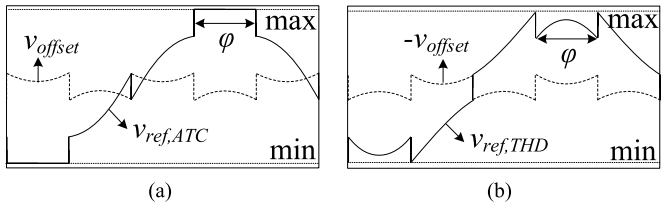

Fig. 5. Proposed modulation signal having two variants. (a) $v_{\rm ref,ATC}$ for the active thermal control for more aged converter. (b) $v_{\rm ref,THD}$ for another converter to improve the power quality.

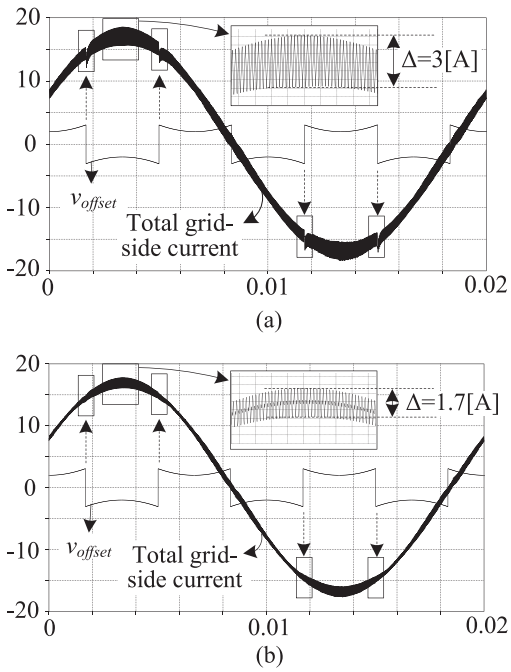

Fig. 6. Simulated current waveform in case (a) both converters are modulated by $v_{\rm ref,ATC}$ and (b) the more aged converter is modulated with $v_{\rm ref,ATC}$ and the less aged converter is modulated by $v_{\rm ref,THD}$.

Fig. 6 shows the total currents simulated for two cases, assuming that the modulating carrier signals for each converter are synchronized: the first case uses only the signal $v_{\rm ref,ATC}$ for both converters, while the second case modulates one converter with $v_{\rm ref,ATC}$ and the other one with $v_{\rm ref,THD}$, respectively. As it can be seen in the results, the ripple current is around 3 A for the first case and the current is distorted by the discontinuous behavior as shown in Fig. 6(a). However, the distortion is reduced with the proposed modulation signal as well as the ripple current is reduced to 1.7 A as shown in Fig. 6(b).

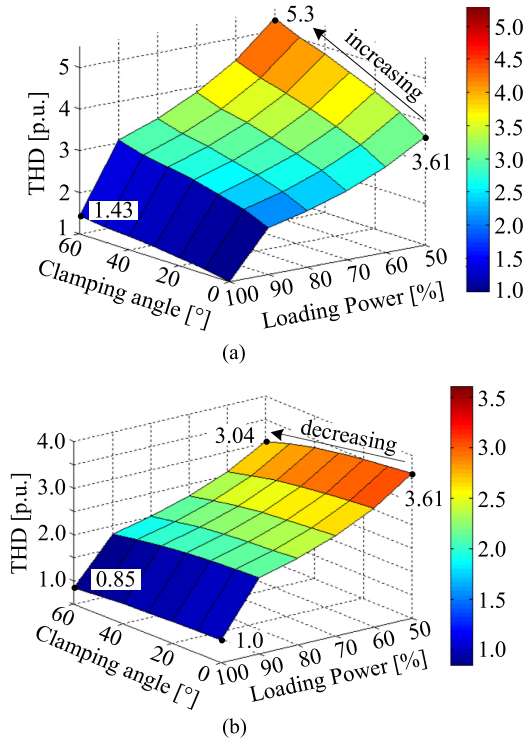

Fig. 7. THD of the grid-side currents when (a) both converters are operated with $v_{\mathrm{ref,ATC}}$ and (b) each converter is modulated by $v_{\mathrm{ref,ATC}}$ and $v_{\mathrm{ref,THD}}$, respectively.

Fig. 7 identifies the THD performance with two cases as a function of the clamping angle and the loading power. As shown in Fig. 7(a), the modulation signal $v_{\mathrm{ref,ATC}}$ negatively affects the THD performance. An increasing clamping angle impairs the performance. The THD of the output current is decreased by 43% in case of 100% power and by 46.8% (from 3.61 to 5.3), when the power is 50%. Since this might be undesired in grid-connected applications and requires a bigger filter in order to fulfill the grid-code, the less aged converters are proposed to be operated with another modulation signal in order to improve the THD of the total current at the PCC. The effect of the second case on the THD is evaluated in Fig. 7(b). The performance is significantly improved in comparison with Fig. 7(a), because the amplitude of the ripple current is reduced [see Fig. 6].

IV. Demonstration of the Proposed Active Thermal Control

As a case study, the potential of the proposed method is validated with the loss distribution simulated by MATLAB/PLECS, considering the well-established two-level converter for the grid-connected application. For this simulation, the switching frequency is set to 5 kHz, the dc-link voltage to 650 V and the power module DP25H1200T101667 (1200 V/25 A) is chosen. The losses are determined with a look-up table, which was populated using the experimental results obtained in [26]. It is assumed that the power flows from the dc-link to the electric grid with the unity power factor.

First, the influence of the clamping angle on the losses is demonstrated in Fig. 8, where the losses are normalized on the

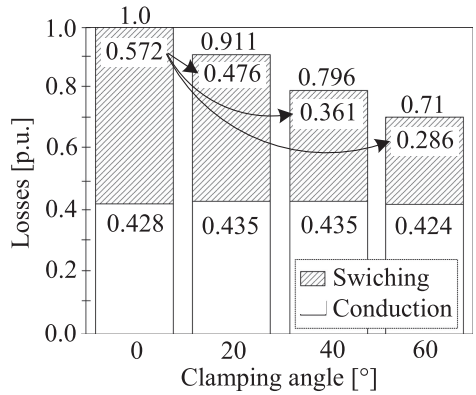

Fig. 8. Simulated loss distribution of the two-level converter with different clamping angles at nominal power.

TABLE I
Comparison of Theoretical and Simulated Analysis for the Switching Losses Reduction as a Function of the Clamping Angle

Clamping angle	0°	20°	40°	60°
Theoretical (Fig. 2)	100 %	82.6 %	65.8 %	50 %
Simulated (Fig. 9)	100 %	83.2 %	63.1 %	50 %

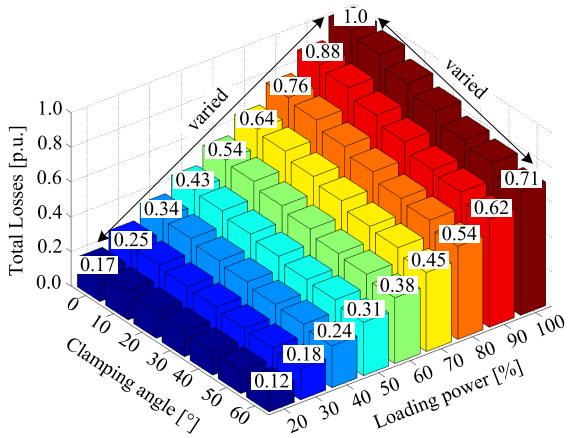

Fig. 9. Simulated loss distribution as a function of the clamping angle and the loaded power.

total losses with the continuous modulation ($\varphi = 0°$). The total losses with the continuous modulation are composed of 57.2% switching losses and 42.8% conduction losses. It can be seen that the total losses are decreased with wider clamping angle by reducing the switching losses. The simulated results in terms of the reduction of the switching losses in Fig. 8 match well with the theoretical analysis in Fig. 2, which is summarized in Table I. On the other hand, focusing on the total losses that needs to actively control to be equalized, it is reduced to 71% with the clamping angle of 60° at the nominal power.

To address the proposed strategy [in above (4) and Fig. 3(b)], the loss distribution as a function of the clamping angle and the loaded power is shown in Fig. 9, where the losses are normalized by the nominal power with the clamping angle of 0°. As it is expected, the losses are affected by the processed power and the clamping angle. This gives the opportunity to equalize the generated losses regardless of the processed power, namely the

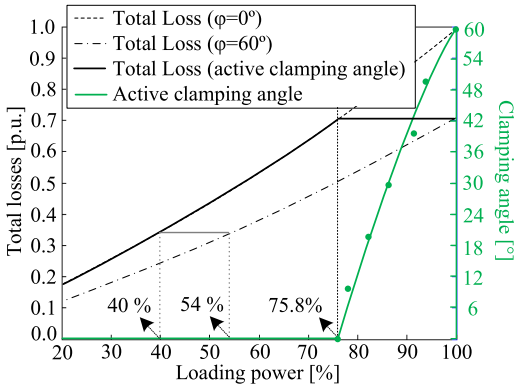

Fig. 10. Proposed active thermal control strategy to equalize the total losses in the high power range for the two-level converter as a case study.

proposed active thermal control strategy to reduce the thermal cycling caused by a power profile.

The proposed strategy is developed in Fig. 10, based on the loss distribution in Fig. 9. The difference between the loss distribution with 0° and 60° clamping angle implies that the losses can be equalized within these boundaries with the active clamping angle. (The points obtained by simulation are indicated with dots and the curve fitting is shown as a solid line). In this framework, the active thermal control region is set between 75.8% and the nominal power, but it can also be set between 40% and 54% depending on frequent fluctuating power range in a considered power profile.

Finally, it is worth noting that the proposed strategy is capable to be applied for other topologies, such as the neutral point clamping, CHB, etc.

V. Analysis of the Proposed Method

A. Potential of the Active Thermal Control

The switching losses, which are utilized for the active thermal control, depend on the switching frequency and the dc-link voltage. Both parameters are defined in the system design and determine the potential of the active thermal control algorithm.

The relation between the range for potentially constant losses and the switching frequency is shown in Fig. 11(a), where the horizontal axis is the switching frequency and the vertical axis is the range for constant losses. The region is normalized on the switching frequency of 5 kHz. For switching frequencies above 5 kHz, the area becomes larger and for a switching frequency higher than 25 kHz, the potential active thermal control region is almost twice than that of 5 kHz. Fig. 11(b) shows the dc-link voltage's influence, where the vertical axis is normalized on the value, where the ratio between the grid voltage and the dc-link voltage is $V_{\mathrm{grid}}/V_{\mathrm{dc}} = 0.87$. The variation is 6.2% (from 103.8 to 97.6%) for an increase from 0.7 to 0.95, which makes the influence of this parameter relatively low.

From the above analysis, it can be concluded that the higher switching frequency and the higher dc-link voltage allow the active thermal control region to be larger, but these design parameters should be carefully determined as the higher design

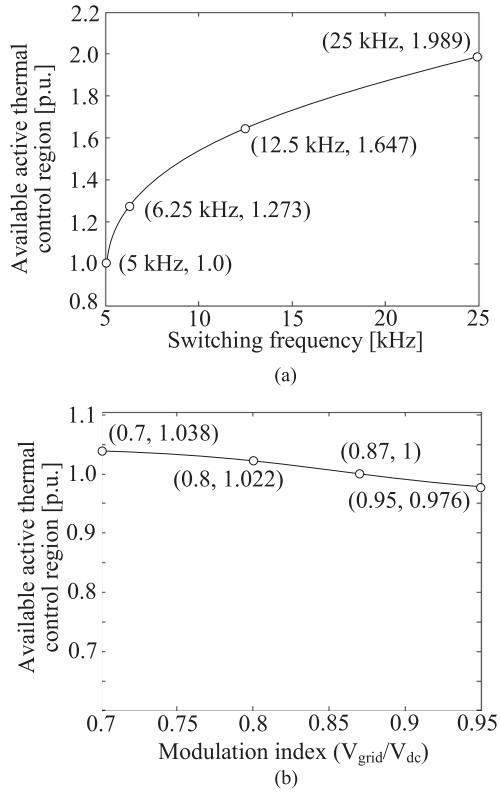

Fig. 11. Influence of (a) switching frequency and (b) dc-link voltage on the available active thermal control area.

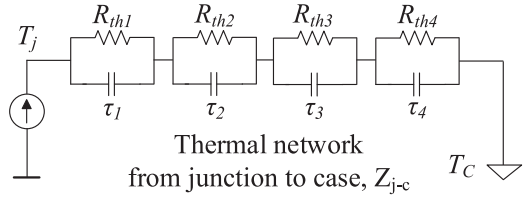

Fig. 12. RC-Foster thermal network for junction temperature of power semiconductors.

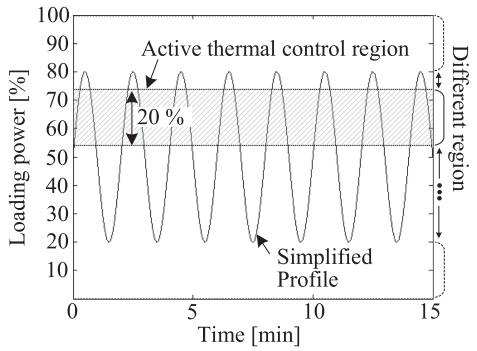

Fig. 13. Simplified power profile with different active thermal control regions to identify its impact on the lifetime.

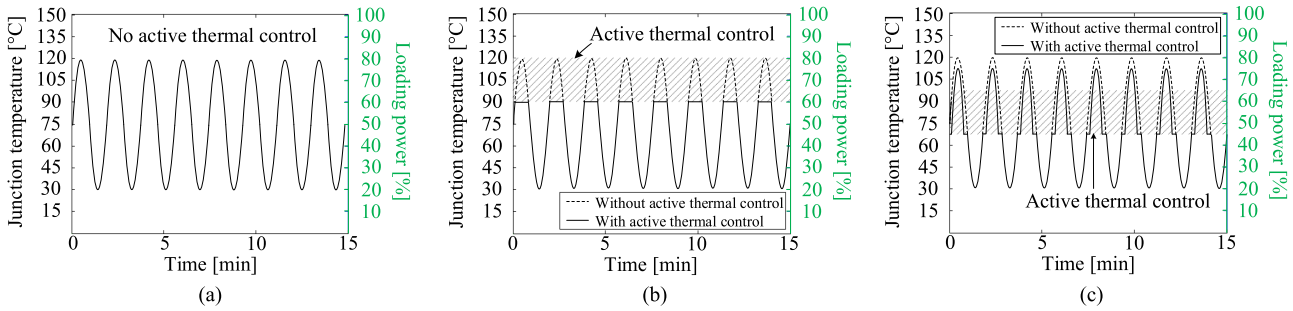

Fig. 14. Expected junction temperature depending on different active thermal control regions. (a) Case 1. (b) Case 2. (c) Case 3.

TABLE II
THERMAL PARAMETERS FOR THE RC-FOSTER NETWORK

i	1	2	3	4
$R_{thi}[K/W]$	0.09025	0.3612	0.2031	0.1403
τ_i [s]	0.0023	0.0282	0.1128	0.282

values generate more losses leading to a higher mean junction temperature. Therefore, it is recommended to design the system for having a proper active thermal control region. This impact of the active thermal control region on the lifetime will be identified through the simulation in the following.

B. Impact of the Active Thermal Control on Lifetime

The thermal stress is assumed to be the reason for the failure of the power semiconductors. As a consequence, for the analysis of the lifetime, the mission profile needs to be known to perform thermal stress analysis. Moreover, to determine how the application of active thermal control is affecting the lifetime consumption of the power semiconductors in an application, a suitable control law needs to be defined for the tuning of the controller. Since the mission profile of the wind turbines is dependent on the weather conditions, this mission profile cannot be known in advance. Apart from the mission profile, the cooling determines the relevant for the thermal stress of the power semiconductors. The thermal network of power semiconductor is shown in Fig. 12, which is modeled as the four layers Foster RC network. Here, T_j and T_c are the junction temperature and the case temperature, respectively, R_{th} is the thermal resistance and τ presents the thermal time constant. The R_{th} determines the steady-state average value of the junction temperature and the τ decides the temperature fluctuation. The thermal network parameters of Fig. 12 are defined in [26] and shown in Table II.

To analyze the influence of the clamping angle region on the accumulated damage of the power semiconductors, a variation of the clamping angle region is performed to control the losses to be constant for a specific power range and the damage is derived for a predefined profile as shown in Fig. 13.

The clamping region of the active thermal controller is set to 20% of the output power and the region is tested from (50, 70)% to (80, 100)% of the output power with a step of 2.5%. This enables to test the effect of the controller region on three representative cases which are defined as follows:

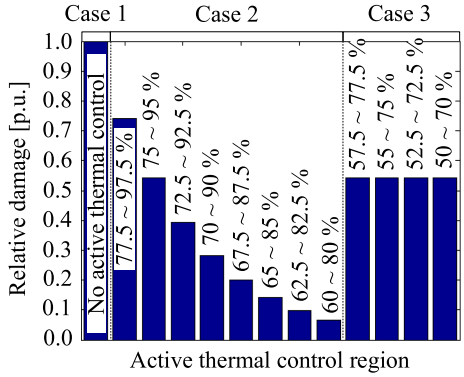

Fig. 15. Accumulated relative damage for the different clamping regions (see Figs. 13 and 14).

Case 1: No active thermal control: (80, 100)%.
Case 2: The clamping region covers the profile by reaching the top of the profile or partly covers the top of the profile: (77.5, 97.5)–(60, 80)%.
Case 3: The clamping region completely covers the profile but does not reach the top of the profile: (50, 70)–(57.5, 77.5)%.

These three cases are visualized in Fig. 14 with the clamping region and the according junction temperature variation. Additionally, Fig. 15 shows the accumulated damage derived with (1) and (2) for the power semiconductors in the different cases. The first case shown in Fig. 14(a) is without the active thermal control and its damage is defined as 100%. The second case is shown in Fig. 14(b), the top of the profile is covered and the thermal swing is partially compensated and the highest reduction of the accumulated damage is observed. Instead, in the third case [shown in Fig. 14(c)], the damage is reduced because of a smaller thermal swing compared with the first case but the damage increases compared with the second case. As a conclusion, the clamping region of the proposed active thermal algorithm should be located in the area covering the peak of the power profile to effectively improve the lifetime.

For a demonstration of the active thermal controller in a mission profile with highly fluctuation power, the effect of the thermal stress reduction is tested. The mission profile is shown in Fig. 16 and the junction temperature without the proposed algorithm and with the application of active thermal control is simulated. For the application of active thermal control, the clamping region is set to cover the peak power (76% to 96%).

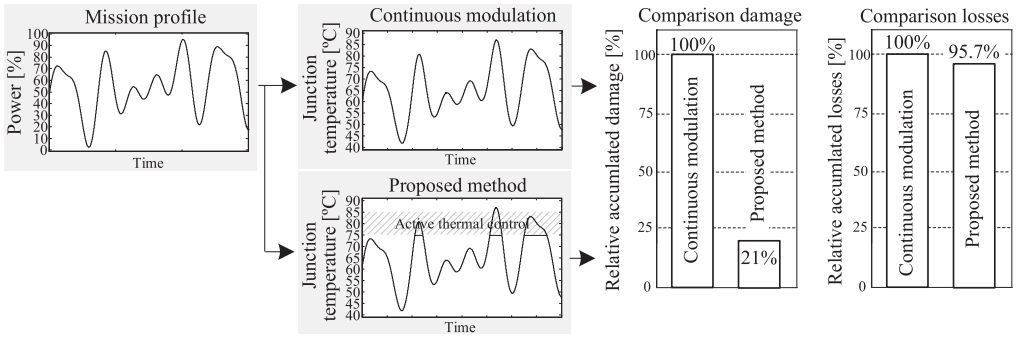

Fig. 16. Comparison of accumulated damage and losses for an arbitrary mission profile.

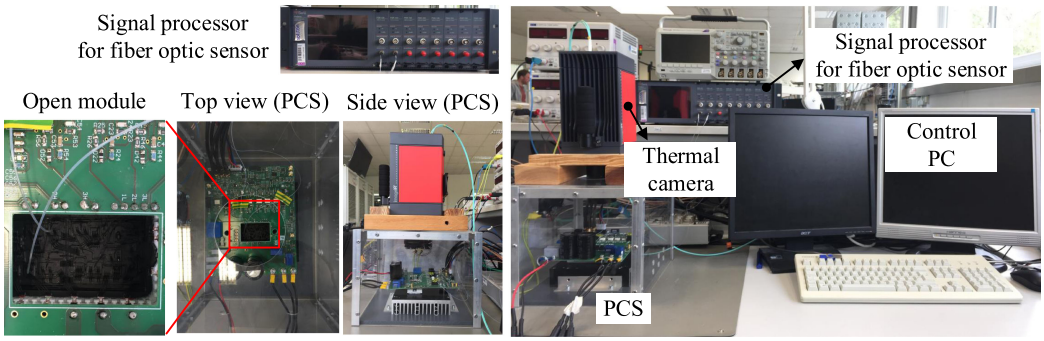

Fig. 17. Demonstrator with open power semiconductor module and thermal monitoring systems.

For the two junction temperature profiles, Rainflow counting is applied and the accumulated damage is derived. In comparison to the case without active thermal control, the damage is reduced to 21% by the proposed method and this results in a lifetime enhancement of 476%. Before finalizing this section, it would be worth to mention that the proposed method does not have a large effect on the efficiency as the conventional discontinuous method since the proposed strategy performs the discontinuous modulation within an active thermal control region only. However, the proposed method still enables lower losses than the continuous modulation and it is confirmed by comparing an accumulated losses for the considered mission profile in Fig. 16. Furthermore, it should be mentioned that the results in Fig. 16 is not an intrinsic attribute, namely the reduction of the accumulated damage would be different under different power profiles.

Through this analysis, it can be concluded that the proposed method shows the most effective performance with an active thermal control region, when the high power region is covered. Remarkably, with the proposed algorithm, the losses are also reduced by 4.3%.

VI. Experimental Results

The proposed method is demonstrated for two-level converter with an open power module (DP25H1200T101667, 1200 V/25 A) as shown in Fig. 17. The setup includes the thermal monitoring system with the thermal camera (ImageIR 8300) and the fiber optic sensors (OTG-F) to measure directly the junction temperature.

The impact of the clamping angle on the thermal stress is shown in Fig. 18 with thermal images, showing the thermal distribution in the entire region of the power module, where the loaded power is fixed at the nominal power. The temperature of the IGBT is much higher than that of the diode due to higher losses, which were discussed in Section III. Additionally, it can be observed that the maximum temperature is gradually decreasing for a wider clamping angle, in case of the IGBT from 97.4 to 92.3 °C and for the diode from 86.4 to 83.6 °C.

The dynamics of junction temperature affected by the changing clamping angle is shown in Fig. 19 with the fixed loaded power at the nominal power, measuring the temperature at specific points with the fiber optic sensors. The junction temperature is immediately reduced with the wide clamping angle as a result of Fig. 18.

Finally, the proposed concept of compensating the thermal cycles is implemented under a power profile. Fig. 20(a) shows the thermal cycling affected by the power variation from 75.8% → 100% → 60% → 75.8% → 100% without the active thermal control. Accordingly, the deviation of the junction temperature in the IGBT is 3.9, 6.4, 2.1, and 4.1 °C. For the validation of the effect of the clamping angle, Fig. 20(b) shows the junction temperature measurement for the implemented active thermal controller, whereby the region is defined from 75.8% to 100% [see Fig. 10]. The temperature variation within the active thermal control region (① → ② and ④ → ⑤) is almost completely compensated whereas the variation outside the region is 3.5 °C (② → ③) and for 2.2 °C for the variation from (③ → ④). Furthermore, the mean junction temperature within the active thermal control area is kept constant as it was targeted. In the same way, the thermal cycling in the diode is compensated by the active thermal controller. It should be noted that the thermal coupling between the diodes and IGBTs in the diodes thermal

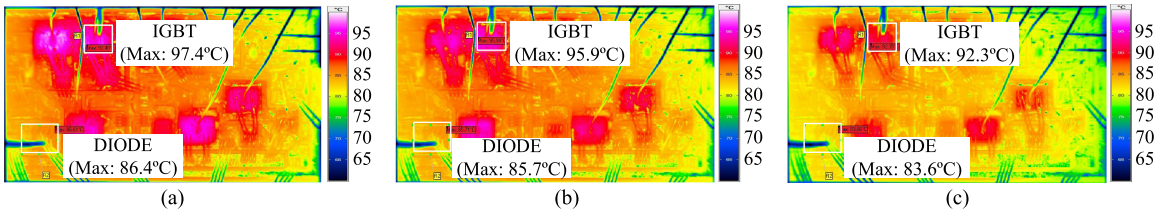

Fig. 18. Thermal image of the open module at the nominal power with (a) $\varphi = 0°$, (b) $\varphi = 30°$, and (c) $\varphi = 60°$.

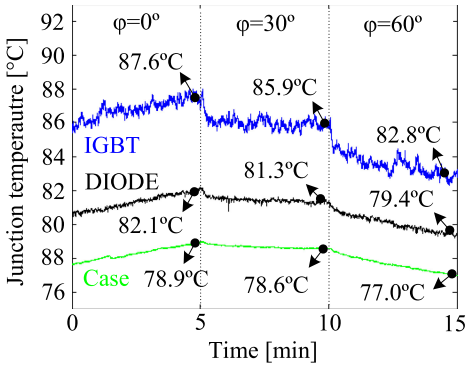

Fig. 19. Validation of the impact of the clamping angle on the junction temperature at the nominal power.

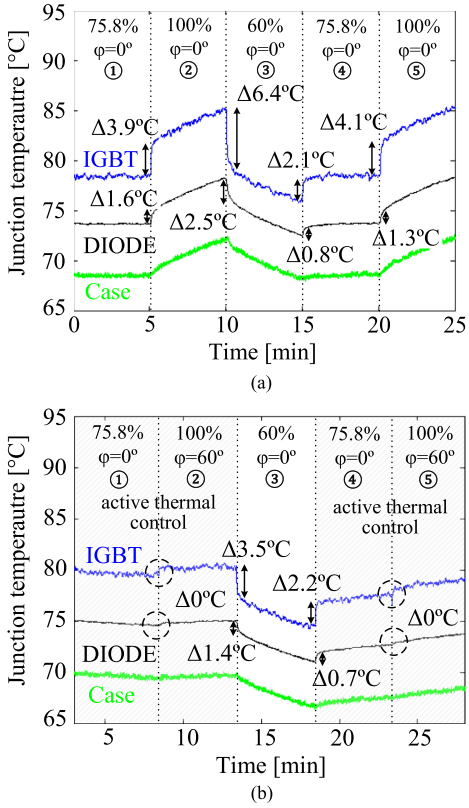

Fig. 20. Measurement of the junction temperature under varying power. (a) Without applying active thermal control (with continuous modulation). (b) With the proposed active thermal control algorithm.

cycling to be compensated by the strategy for the IGBTs, even though the impact of the clamping angle on the diodes' losses is lower than that of IGBTs.

VII. Conclusion

This paper has proposed an active thermal control algorithm for reducing the thermal stress of power semiconductors in power modules for power converters connected to the same PCC. By employing the DPWM-based active clamping angle, the total losses are demonstrated to be kept constant for a specific power range, resulting in reduced thermal stress for the power semiconductors. Furthermore, the capability of the active thermal control region depending on the switching frequency and the dc-link voltage was discussed, and the strategy to improve the power quality considering parallel connections to the same PCC was proposed. Finally, the capability of the algorithm to reduce the thermal cycles of an converter was validated experimentally in a proof-of-concept study on a two-level voltage source converter.

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