Dead-Time Effect Compensation Method Based on Current Ripple Prediction for Voltage-Source Inverters

Zewei Shen, *Student Member, IEEE*, and Dong Jiang, *Senior Member, IEEE*

***Abstract*—In voltage-source inverters (VSIs), dead time is used to prevent shoot-through over switching devices. However, the existence of the dead time will distort the output phase current, which degrades the performance of the inverter as well as influences the common-mode voltage (CMV), particularly in CMV elimination relevant modulation schemes, such as zero-common-mode (CM) pulsewidth modulation (PWM)-based paralleled inverters. In the light of the situation that the normal sampling-based dead-time compensation (DTC) methods are often disturbed by the current ripple, this paper introduces a novel DTC method for the VSI, which can mitigate the impact of the current ripple and improve the accuracy of DTC. The proposed method deduces the real-time current ripple, which can reconstruct the actual trajectory of phase-leg currents, and the peak values corresponding to rising and falling edges for PWM signals can be predicted. In this way, DTC can be implemented based on the direction of relevant instantaneous switching currents and finally improves the accuracy. Especially, the current-ripple-prediction-based DTC can help to improve the CMV distortion caused by the dead time for paralleled inverters with zero-CM PWM. Simulation and experimental results are provided to validate that the proposed method can be applied to different topologies and modulation schemes with good performance.**

***Index Terms*—Common-mode voltage (CMV), current ripple prediction (CRP), dead-time compensation (DTC).**

NOMENCLATURE

PWM	Pulsewidth modulation.
VSI	Voltage-source inverter.
DTC	Dead-time compensation.
CMV	Common-mode voltage.
CRP	Current ripple prediction.
ZCC	Zero-current clamping.
IPM	Integrated power module.

Manuscript received September 29, 2017; revised January 10, 2018 and February 18, 2018; accepted March 21, 2018. Date of publication March 28, 2018; date of current version November 19, 2018. This work was supported in part by the Delta Electronics Foundation through Project DREK201703 and in part by the National Natural Science Foundation of China through Project 51607077. Recommended for publication by Associate Editor H. H.-C. Iu. *(Corresponding author: Dong Jiang.)*

The authors are with the State Key Laboratory of Advanced Electromagnetic Engineering and Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail:

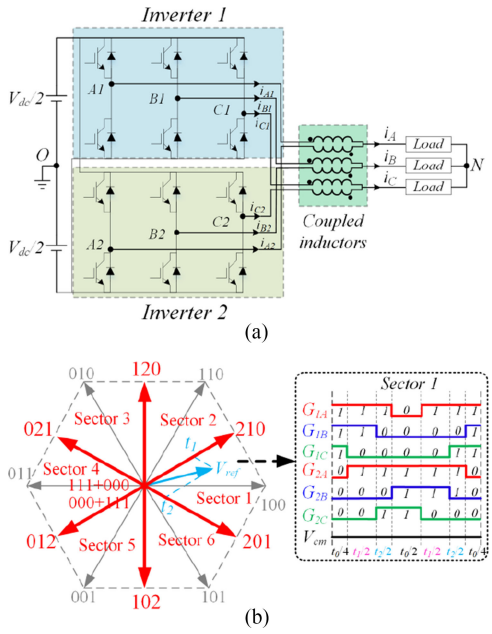

Fig. 1. Topology and modulation scheme for paralleled inverters. (a) Structure of a paralleled inverter with load. (b) Zero-CM PWM scheme.

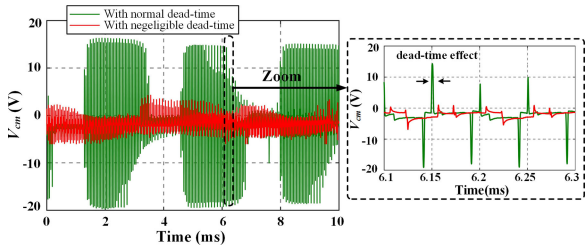

Fig. 2. CM voltage comparison between for zero-CM PWM with different dead times.

linear factors for the VSI, which can deduce the voltage error directly and realize a better compensation result. Mannen and Fujita [16] investigated the effects of the current ripple on the dead-time distortion in three-phase VSIs under different working conditions, but how to deal with the current ripple was not mentioned.

In addition, the dead time may influence the CMV sometimes [17], especially in CMV elimination schemes [19]–[21], which are sensitive to the edge positions of phase-leg voltages. Lai and Shyu [18] had proved that the performance of the CMV elimination modulation scheme is highly related to the dead time added to the system. Similarly, Jiang *et al.* [20] proposed the zero-CM PWM algorithm in paralleled inverters to eliminate the CMV. The architecture and modulation scheme in sector 1 is illustrated in Fig. 1(a) and (b), where two regular three-phase inverters are connected to the three-phase load through coupled inductors. By combining two adjacent voltage vectors for the two-level inverter shown in Fig. 1(b), six paralleled voltage vectors (210, 120, 021, 012, 102, and 201) with a zero CMV can be derived, together with two paralleled zero vectors (000 + 111 and 111 + 000), which can realize the CMV elimination effect under the ideal situation.

However, because of the dead-time effect, the performance of CMV elimination cannot be well achieved like an idea case. Fig. 2 shows the experimental results of the CMV for zero-CM PWM with normal and negligible dead times. The zero-CM PWM scheme with a negligible dead time can nearly eliminate the CMV, while the performance of CMV elimination with a normal dead time is obviously degraded with narrow pulses caused by the dead-time effect [19], [20]. So, the DTC should be implemented in the actual system to mitigate this problem. While many DTC methods based on single VSI is not suitable for paralleled inverters. In addition, the conventional DTC method without considering the current ripple's impact cannot improve the CMV elimination much. So, the novel DTC method should be designed and implemented for a more complex topology.

Jiang *et al.* [22] proposed the CRP method for a three-phase PWM inverter, which can calculate the real-time peak values of the current ripple. Considering this excellent characteristic, the novel DTC scheme that embeds the CRP model into the current-sampling-based DTC scheme can help judging the current track of phase legs. If the CRP model for different topology and modulation schemes can be deduced, the real-time trajectory of switching current can be more precisely obtained. Under this condition, the accuracy of DTC can be increased, and the system can get better performance.

The rest of this paper is organized as follows. The effect of the dead time including ZCC is analyzed, and the current's partition that decides the DTC schemes is introduced in Section II. In Section III, the modeling of the current ripple for the zero-CM PWM algorithm with paralleled inverters is proposed, and the flowchart of the novel DTC method is added for generalizing and summarizing the proposed method. In Section IV, the proposed DTC method is first tested by the space vector pulsewidth modulation (SVPWM) algorithm in a single inverter with simulation. More importantly, the CRP model for zero-CM PWM is compared with the simulation result and then utilized for DTC in paralleled inverters to check the effect on CMV elimination mitigation. The detailed experimental results are presented in Section V to prove the proposed method's validity. Finally, conclusions are summarized in Section VI.

II. Dead-Time Effect Analysis

Since normal switching devices are not ideal, which have turn-ON and turn-OFF time, a dead time should be embedded in the PWM gate signals to prevent the simultaneous conduction of two switching devices in the phase leg. In other words, a top switch of one phase leg should be turned OFF before a bottom switch of the leg is turned ON and vice versa. Compared to the ideal condition, there exists many nonideal factors in the inverter system, which will impact the output voltage and make the phase current nonsinusoidal, such as the voltage drop in a switching device and an antiparallel diode, dead time $t_{\rm d}$, turn-ON time $t_{\rm on}$, and turn-OFF time $t_{\rm off}$. In this paper, only the last three factors that influence the edge position of pole voltage are taken into consideration to deal with the dead-time effect.

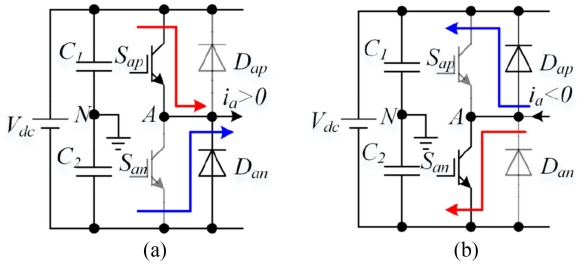

Fig. 3. Channel flow of the phase current. (a) $i_a > 0$. (b) $i_a < 0$.

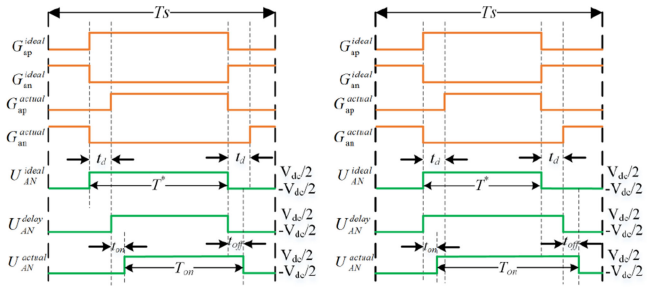

Fig. 4. Comparison of ideal and actual waveforms for gate signals and pole voltages. (a) $i_a > 0$. (b) $i_a < 0$.

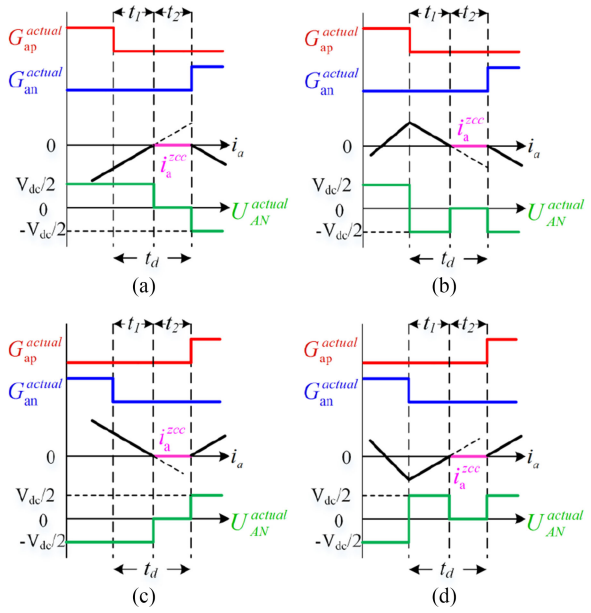

Fig. 5. All kinds of ZCC situations and the corresponding output pole voltage under the ideal condition.

Considering the direction of the phase-leg current for phase A, the channel flow of the current can be drawn and shown in the Fig. 3, where S_{ap}, S_{an}, D_{ap}, and D_{an} are the upper and lower switching devices and antiparalleled diodes correspondingly. Fig. 3(a) shows the channel flow of the phase current when $i_a > 0$. If S_{ap} is ON and S_{an} is OFF, i_a will flow through the S_{ap}; if S_{ap} is OFF and S_{an} is ON, i_a will flow through the D_{an}. When $i_a < 0$, if S_{ap} is ON and S_{an} is OFF, i_a will flow through the D_{ap}; if S_{ap} is OFF and S_{an} is ON, i_a will flow through the S_{an}, as shown in Fig. 3(b). The above two situations consist of the controllable duration for phase leg, which is overwhelming in switching cycle generally. The dead times, including turn-ON and turn-OFF time, which are the uncontrollable times in the switching period, can distort the pole of the output voltage and belong to the dead-time effect.

A. Dead-Time Effect With Normal Diode Freewheeling

Fig. 4 shows the comparison of ideal and actual waveforms for gate signals and pole voltage, where G_{ap}^{ideal}, G_{an}^{ideal}, G_{ap}^{actual}, and G_{an}^{actual} are the ideal and actual gate signals, $U_{\text{AN}}^{\text{ideal}}$ is the ideal pole voltage switching between $V_{\text{dc}}/2$ and $-V_{\text{dc}}/2$, $U_{\text{AN}}^{\text{delay}}$ is the rising edge delayed pole voltage, which inserts dead time in upper and lower switching devices, and $U_{\text{AN}}^{\text{actual}}$ is actual pole voltages considering the turn-ON and turn-OFF time in hardware. T^* and T_{on} are the ideal and actual duration of positive pole voltage, and T_s is the switching cycle. If $i_a > 0$ in the whole switching cycle, the phase current will pass through D_{an} and the output voltage of phase leg is clamped to the negative pole of the dc bus during the dead-time interval. This phenomenon is equivalent to decrease the ideal ON-period T^* of t_d in one switching cycle. In addition, the turn-ON process in which the pole voltage delay turned ON leads to decrease the ON-period T^* of t_{on}, while the turn-OFF process in which the pole voltage delay turned OFF is equivalent to increasing the ON-period T^* of t_{off}, as shown in Fig. 4(a). Fig. 4(b) shows the actual output voltage when $i_a < 0$ in the whole switching cycle. Under this condition, the phase current will pass through D_{ap} and the output voltage of phase leg is clamped to the positive pole of the dc bus during the dead-time interval. This phenomenon is equivalent to increasing the ON-period T^* of t_d, which is opposite to the situation when $i_a > 0$. Meanwhile, the turn-ON and turn-OFF process keeps the same effect for the pole voltage in this situation because the turn-ON and turn-OFF times are independent of the direction of the phase-leg current.

So, the duty cycle error Δd between the actual and ideal pole voltages can be deduced from the above analysis as

$$\Delta d = \frac{T^* - T_{\text{on}}}{T_s} = \begin{cases} \left(t_d + t_{\text{on}} - t_{\text{off}}\right)/T_s & (i > 0) \\ \left(t_{\text{on}} - t_d - t_{\text{off}}\right)/T_s & (i < 0). \end{cases} \tag{1}$$

B. Dead-Time Effect With Abnormal Diode Freewheeling—ZCC

The characteristic of the phase-leg current follows the principle that it always flow toward the decreasing direction during the dead-time interval with the trend of current nature freewheeling. So, when the phase-leg current has a relative big value, which satisfies the condition that it keeps the same direction in the whole switching cycle, there is no ZCC phenomenon because of normal freewheeling in the dead-time interval. When the phase-leg current is close to zero, it has the possibility to generate ZCC if the current changes the direction in one switching cycle. Fig. 5 shows all kinds of ZCC situations and the corresponding output pole voltage for phase leg A. Taking Fig. 5(a) for example, i_a freewheels through an antiparalleled diode and

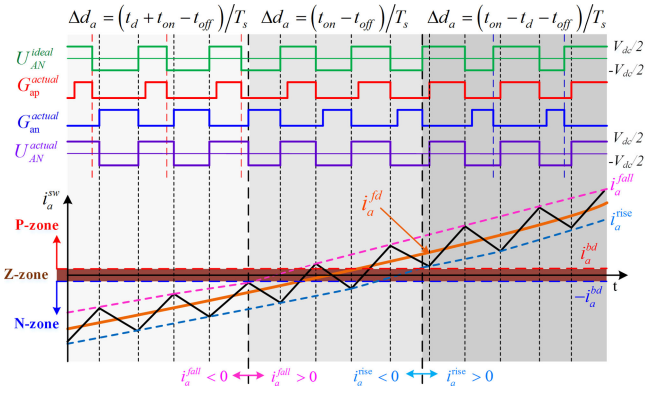

Fig. 6. Dead-time effect of the rising process of the phase-leg current.

the output pole voltage keeps to be $V_{\rm dc}/2$ in t_1 period. When i_a reaches the critical value $i_a^{\rm zcc}$, which is very close to zero at the beginning of t_2 period, the antiparalleled diode becomes reversing cutoff and generates ZCC. With the condition that the upper and lower switching devices keep OFF-state in the whole dead-time interval, the output pole voltage of the phase leg will be zero when considering nearly the same impedance of two switching devices in the phase leg. After the dead-time interval, the phase current can be controlled again and becomes negative. The left three ZCC situations have the similar mechanism and can be speculated by the same procedure.

Owing to the fact that the phase-leg current is too close to zero and freewheels in the dead-time interval, it has no ability to change the direction and lead to ZCC. Besides, the mitigation of ZCC is a challenging work, and its influence is limited because of the shorter time (less than the dead-time interval) and the lower occurrence possibility in one fundamental period. According to the principle of ZCC, the average effect of ZCC on the volt–second loss can be almost ignored or compensated by the closed-loop control together with other nonideal factors. In addition, the effect of ZCC introduces an instantaneous zero pole voltage for the phase leg, which may generate the CMV spikes for the CMV elimination scheme; this phenomenon will be shown in the following.

C. Current's Partition and the Corresponding Dead-Time Compensation Schemes

The above content shows the different effect of dead time, while the phase-leg current of the inverter always accompanies with the current ripple, which leads to the fundamental component enveloped by the instantaneous peak values. So, the dead-time effect in real pole voltage of the phase leg is more complicated and should be analyzed in depth. Fig. 6 gives a detailed description of the rising process of the phase-leg current with a simplified current ripple and pole voltage, which only consider the dead time and neglect the effect of turn-ON and turn-OFF times. The upper part shows the ideal output voltage $U_{AN}^{\rm ideal}$ with actual PWM signals $G_{ap}^{\rm actual}$ and $G_{an}^{\rm actual}$ and the output pole voltage $U_{AN}^{\rm actual}$, while the lower part shows the corresponding actual switching current $i_a^{\rm sw}$ with peak envelopes $i_a^{\rm fall}$ and $i_a^{\rm rise}$ and the fundamental current $i_a^{\rm fd}$.

For a general modulation scheme, the rising and falling edges of the PWM signal decide the extreme values of phase-leg's current in one switching cycle. In addition, these extreme values affect the dead-time effect and, finally, decide the compensation scheme. According to Fig. 6, the compensation schemes can be divided into four cases.

1) The switching phase current $i_a^{\rm sw}$ locates in the P-zone (positive zone), which has no zero-crossing point: that is to say, the minimum phase current meets the condition that $i_a^{\rm rise} \geq i_a^{bd}$, which can keep the freewheeling of current normal in the dead-time interval. i_a^{bd} is the defined boundary between the P-zone and the Z-zone (zero zone), which is generally with a small value and decided by the dead-time interval and the maximum slope of the current ripple. The freewheeling of the phase current in the dead-time interval leads the positive time of the actual output pole voltage decreased compared to the ideal output voltage $(\Delta d_a = (t_{\rm on} - t_d - t_{\rm off})/T_s)$. In order to deal with this situation, the rising edge of the upper switching device and the falling edge of the lower switching device should be in advance to compensate the volt–second loss.
2) The switching phase current $i_a^{\rm sw}$ locates in the N-zone (negative zone), which also has no zero-crossing point: Conversely, when the maximum phase current meets the condition that $i_a^{\rm fall} \leq -i_a^{bd}$ in one switching period, the switching current can also keep the normal freewheeling in the dead-time interval. $-i_a^{bd}$ is the defined boundary between the N-zone and the Z-zone. The freewheeling of current in the dead-time interval leads actual output voltage's positive time increased compared to the ideal output voltage $(\Delta d_a = (t_d + t_{\rm on} - t_{\rm off})/T_s)$, so the falling edge of the upper switching device and the rising edge of the lower switching device should be in advance in order to compensate this situation.
3) The switching phase current $i_a^{\rm sw}$ has a zero-crossing point, but all the peak values are out of the Z-zone: that is to say, the minimum phase current meets the condition $i_a^{\rm rise} \leq -i_a^{bd}$ and the maximum phase current meets the condition $i_a^{\rm fall} \geq i_a^{bd}$ in one switching period. Although the dead-time interval exists under this circumstance, there is no ZCC happening because of the margin of current freewheeling. At the same time, the dead-time effect can offset each other on duty cycle variation, and the main duty cycle variation is caused by the turn-ON and turn-OFF time $(\Delta d_a = (t_{\rm on} - t_{\rm off})/T_s)$, so only slightly changing the rising edge's position can mitigate the duty cycle error in this situation.
4) The switching phase current $i_a^{\rm sw}$ has a zero-crossing point, and one of the peak values is in the Z-zone (zero zone): that is to say, the minimum phase current $i_a^{bd} \geq i_a^{\rm rise} \geq -i_a^{bd}$ or the maximum phase current $i_a^{bd} \geq i_a^{\rm fall} \geq -i_a^{bd}$ in one switching period. As previously analyzed, the phase current may generate ZCC because of the possibility of peak currents changing directions. Considering the duration time and occurrence possibility, the DTC scheme can also take the same DTC scheme with case 3 in the whole fundamental period.

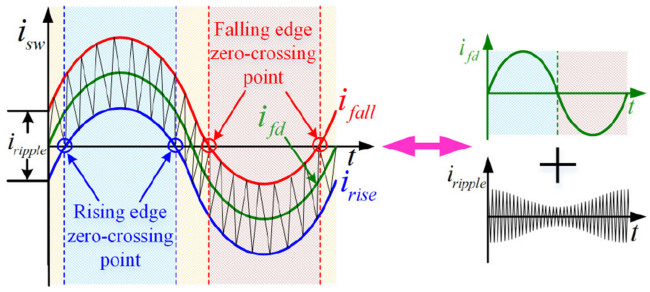

Fig. 7. Relationship among the actual phase current, the fundamental current, and the ripple current.

Based on the above analysis for all different cases, the DTC can be implemented with the three regular schemes, and the compensation duty cycle $d_{\rm com}$ can be deduced as

$$d_{\rm com} = -\Delta d_a = \begin{cases} (t_d + t_{\rm off} - t_{\rm on})/T_s, & \left(i_x^{\rm rise} > i_x^{bd}\right) \\ (t_{\rm off} - t_{\rm on})/T_s, & \left(i_x^{\rm rise} \le i_x^{bd}, i_x^{\rm fall} \ge -i_x^{bd}\right) \\ (t_{\rm off} - t_{\rm on} - t_d)/T_s, & \left(i_x^{\rm fall} < -i_x^{bd}\right). \end{cases} \tag{2}$$

But the more challenging work in this DTC scheme is the calculation of the real-time peak current $i_a^{\rm rise}$ and $i_a^{\rm fall}$, which should draw support from the corresponding software algorithm—CRP.

III. CRP for Dead-Time Compensation

For general inverters, considering the volt–second equivalent principle, the duty cycle of the impulse voltage decides the output fundamental component, and the difference between the impulse voltage and the average output voltage generates the current ripple [22]. Fig. 7 shows the inverter's output phase current $i_{\rm sw}$, which is formed by the fundamental current $i_{\rm fd}$ (low frequency) and the ripple current $i_{\rm ripple}$ (high frequency). If there only exists $i_{\rm fd}$ in the phase-leg current, the DTC is simple to realize without the interference of $i_{\rm ripple}$ because of fewer zero-crossing points for $i_{\rm sw}$. However, obvious current ripple caused by PWM cannot be ignored, especially for the case of an inverter with a low carrier ratio or a small phase inductance. Generally, the normal processor with a sampling circuit can only extract the low-frequency current and neglect the high-frequency ripple current, which can lead to compensation errors in DTC. So, if $i_{\rm ripple}$ can be predicted, $i_{\rm sw}$ can also be estimated by adding the two components (i_{fd} and $i_{\rm ripple}$) together. Finally, the DTC can be implemented more precisely by the CRP method without adding any hardware cost.

Jiang *et al.* [22] have proved that the current ripple can be predicted by instantaneous duty cycle in a normal two-level three-phase inverter using Thevenin equivalent circuits. The key point of calculating the current ripple is to deduce the instantaneous output pole voltage of the phase leg and the CMV. The CRP of a regular three-phase inverter is based on the method in [22] and is directly used in DTC in this paper.

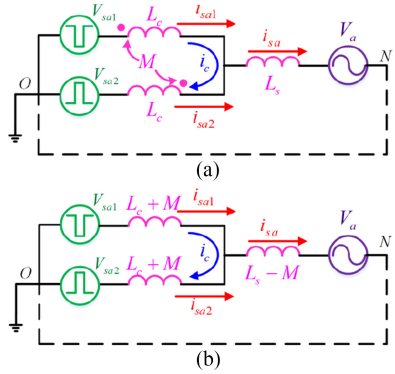

Fig. 8. Simplified equivalent circuit diagram of phase A. (a) Coupling with a coupled inductor. (b) Decoupling without a coupled inductor.

A. CRP Model for Paralleled Inverters With Coupled Inductors

For paralleled inverters with the zero-CM PWM scheme, both the topology and the modulation scheme are more complex than the conventional two-level three-phase inverter with the symmetric modulation scheme, but the CRP model can also be deduced for paralleled inverters by the similar thinking. The zero-CM PWM algorithm can keep the voltage of the ac neutral point to be zero under the ideal condition when taking the middle point of the dc bus as reference, which means eliminating the CMV for a paralleled inverter theoretically. Under this condition, the paralleled phase legs of one phase can be extracted and get the equivalent circuit; other phases can follow this method to build the similar equivalent circuit. Taking phase A for example, ignoring the resistances of the coupled inductor and the load, the simplified equivalent circuit diagram can be deduced as shown in Fig. 8(a), where V_{sa1} and V_{sa2} are the terminal voltages of A_1 and A_2 phase legs, which are switching between $V_{\rm dc}/2$ and $-V_{\rm dc}/2$ in one switching cycle, L_c and M are the self- and mutual inductances of the coupled inductor, respectively, L_s is the load inductor of phase A, i_{a1}, i_{a2}, and i_a stand for the phase-leg currents and the synthetic phase current for phase A, and V_a is the sinusoidal load voltage of phase A. In addition, by decoupling the coupled inductor, the circuit can be further simplified as shown in Fig. 8(b). The dotted line indicates that there is no actual connection for the dc-side middle point and the ac neutral point, but the potential is consistent.

From the decoupling simplified equivalent circuit, the corresponding voltage and current equations can be listed as

$$\begin{cases} V_{sa1} - (L_c + M)\dfrac{di_{sa1}}{dt} = (L_s - M)\dfrac{di_{sa}}{dt} + V_a \\ V_{sa2} - (L_c + M)\dfrac{di_{sa2}}{dt} = (L_s - M)\dfrac{di_{sa}}{dt} + V_a \\ i_{sa} = i_{sa1} + i_{sa2} \\ i_c = \dfrac{1}{2}(i_{sa1} - i_{sa2}). \end{cases} \tag{3}$$

In this case, the calculated results for the derivative of currents can be written as follows:

$$\begin{cases} \dfrac{di_{sa1}}{dt} = \dfrac{[(L_c+L_s)\,V_{sa1}-(L_s-M)\,V_{sa2}-(L_c+M)\,V_a]}{(L_c+2L_s-M)\,(L_c+M)} \\ \dfrac{di_{sa2}}{dt} = \dfrac{[(L_c+L_s)\,V_{sa2}-(L_s-M)\,V_{sa1}-(L_c+M)\,V_a]}{(L_c+2L_s-M)\,(L_c+M)} \\ \dfrac{di_{sa}}{dt} = \dfrac{di_{sa1}}{dt}+\dfrac{di_{sa2}}{dt} = \dfrac{1}{(L_c+2L_s-M)}\,(V_{sa1}+V_{sa2}-2V_a) \\ \dfrac{di_c}{dt} = \dfrac{1}{2\,(L_c+M)}\,(V_{sa1}-V_{sa2})\,. \end{cases} \tag{4}$$

Assume that V_a is a sinusoidal quantity and is equal to the quasi-duty cycle d'_a $(-1 \le d'_s \le 1)$ times half of the dc-link voltage $(V_a = d'_a \cdot V_{\rm dc}/2)$. V_{sa1} and V_{sa2} are functions of switching states and are equal to switching states S_{a1}, S_{a2} $(S_{a1} = \pm 1;\quad S_{a2} = \pm 1)$ times half of the dc-link voltage $(V_{sa1} = S_{a1} \cdot V_{\rm dc}/2;\ V_{sa2} = S_{a2} \cdot V_{\rm dc}/2)$. So, the derivative of currents can finally be simplified as follows:

$$\begin{cases} \dfrac{di_{sa1}}{dt} = \dfrac{V_{\rm dc}\,[(L_c+L_s)\,S_{a1}-(L_s-M)\,S_{a2}-(L_c+M)\,d'_a]}{2\,(L_c+2L_s-M)\,(L_c+M)} \\ \dfrac{di_{sa2}}{dt} = \dfrac{V_{\rm dc}\,[(L_c+L_s)\,S_{a2}-(L_s-M)\,S_{a1}-(L_c+M)\,d'_a]}{2\,(L_c+2L_s-M)\,(L_c+M)} \\ \dfrac{di_{sa}}{dt} = \dfrac{V_{\rm dc}}{2\,(L_c+2L_s-M)}\,(S_{a1}+S_{a2}-2d'_a) \\ \dfrac{di_c}{dt} = \dfrac{V_{\rm dc}}{4\,(L_c+M)}\,(S_{a1}-S_{a2})\,. \end{cases} \tag{5}$$

With the derivative of all relevant currents and the duration time of all switching states deduced by the duty cycle of A_1 and A_2 phase legs, the corresponding current ripples can be analytically calculated and predicted real time. Other phase-leg currents can also be calculated by the same procedure. By utilizing the above CRP model to estimate all phase-legs' switching currents, the DTC can be implemented without the limitation of the paralleled inverter topology.

B. Flowchart of the Proposed Dead-Time Compensation Method

Based on the deduced CRP model and the combination of previous analysis, the proposed DTC algorithm can be summed up, and the flowchart can be drawn in Fig. 9.

First, with current sampling for different phase legs, the low-frequency current i_x^{fd} can be obtained, and the current controller can be utilized to calculate the duty cycle *dx* for each phase. Under this condition, the rising and falling edges of PWM signals can be determined with a corresponding modulation algorithm. Next, with the information of rising and falling edges, the real-time ripple current $i_x^{\rm ripple}$ can be deduced with the CRP model; then, the phase-leg current can be reconstructed, and the peak currents $i_x^{\rm rise}$ and $i_x^{\rm fall}$ corresponding to rising and falling edges can be obtained. Finally, according to the boundary conditions of current partition, the real-time peak values of the switching current belonging to different zones can be determined, and the relevant fixed compensation scheme can be implemented to change the positions of rising and falling edges to realize the DTC.

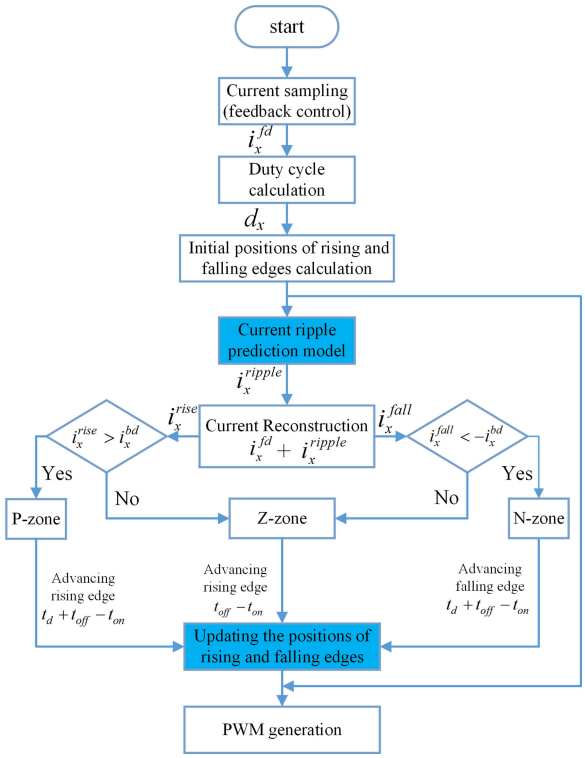

Fig. 9. Block diagram of the proposed DTC algorithm.

TABLE I
SIMULATION PARAMETERS FOR A SINGLE INVERTER

Symbol	Parameters	Value
V_{dc}	DC link voltage	200V
f_0	Fundamental frequency	50Hz
f_s	Switching frequency	10kHz
m	modulation index	0.2
L_s	Load inductance	0.52mH
R_s	Load resistance	4.7Ω
T_d	Dead-time	2μs

IV. SIMULATION RESULTS

Based on the previous analysis, the MATLAB/SIMULINK model both for a single inverter and paralleled inverters can be developed to verify the proposed method, and the three-phase series resistor and inductor is utilized as the load for the above different topologies.

A. Dead-Time Compensation for SVPWM in a Regular Three-Phase VSI

For a three-phase single inverter with the SVPWM scheme, the switching frequency is set to be 10 kHz and the fundamental frequency is set to be 50 Hz. The dead time is chosen to be 2 μs, which is a normal time interval in switching devices. The more detailed simulation parameters are shown in Table I.

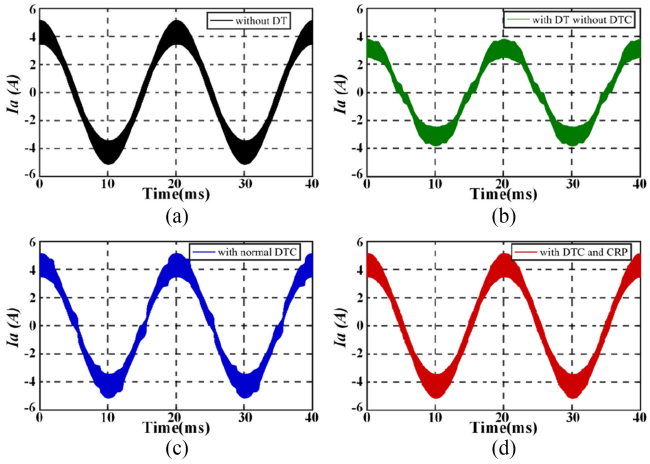

Fig. 10. Phase current comparison among the four situations. (a) Without DT. (b) With DT without DTC. (c) With normal DTC. (d) With DTC and CRP.

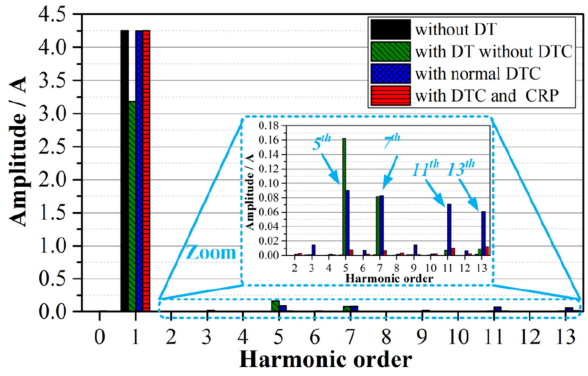

Fig. 11. FFT analysis of phase current for the four situations.

TABLE II
SIMULATION PARAMETERS FOR PARALLELED INVERTERS

Symbol	Parameters	Value
V_{dc}	DC link voltage	100V
f_0	Fundamental frequency	50Hz
f_s	Switching frequency	10kHz
m	modulation index	0.4
L_s	Load inductance	0.7mH
R_s	Load resistance	4.7Ω
L_c	Main inductance of coupled inductor	0.52mH
M	coupling coefficient of coupled inductor	0.92
T_d	Dead-time	2μs

Jiang *et al.* [22] have introduced the CRP method for SVPWM with a single inverter, and the current prediction effect has been well validated. This section is focused on verifying the effect of CRP-based DTC for a single three-phase inverter. Fig. 10 gives a detailed comparison about the phase currents among four methods: the ideal condition without the dead time, the actual condition with the dead time but without compensation (with DT without DTC), the normal DTC by only sampling phase current (normal DTC), and the modified DTC by sampling phase currents with CRP (with DTC and CRP). In order to emphasize the dead-time's impact, the low modulation index $(m = 0.2)$ is utilized.

In time-domain comparison with the ideal condition shown in Fig. 10(a), the situation with the DT without DTC leads to phase current distortion because of the generation of harmonic currents. In addition, the fundamental current is reduced in this condition because of the fundamental output voltage drop shown in Fig. 10(b). Comparing to the situation with DT without DTC, the normal DTC method can increase the fundamental current, but it cannot effectively restrain the harmonic currents, which also distort the phase current shown in Fig. 10(c). Finally, considering the CRP, the implementation of DTC has obviously better performance in terms of fundamental current recovery or harmonics suppression shown in Fig. 10(d). So, the CRP can be implemented to make DTC more accurate for a single inverter with the SVPWM scheme.

In addition, frequency-domain analysis by the fast Fourier transform (FFT) for the above phase currents is implemented as shown in Fig. 11. It can be found that the obvious $(6\,\mathrm{n} \pm 1)th$ harmonic currents occur in the situations with DT without DTC and with normal DTC caused by the dead-time effect. Contrarily, the implementation of DTC with CRP can obviously suppress the harmonic currents, which make the performance close to the idea condition. The total harmonic distortions (THDs) of the phase current for the four situations are 11.59%, 13.54%, 12.35%, and 11.62% correspondingly, which means the proposed method is valid for the THD reduction.

B. CRP Verification for Zero-CM PWM in Paralleled Inverters

For paralleled inverters with zero-CM PWM, the coupled inductor should be added between the inverter and the load. The main parameters for the coupled inductor including the main inductance and the coupling coefficient can be extracted from the actual coupled inductor to simulate the actual condition. The detailed parameters are shown in Table II.

The phase-leg currents rather than phase currents should be focused on in paralleled inverters because the phase-leg currents impact the output pole voltages of the inverter. So, the CRP model that corresponds to the phase-leg current for zero-CM PWM is chosen to verify the accuracy under this condition. Fig. 12(a) shows the simulation result of two paralleled phase-leg currents and corresponding fundamental currents in a whole fundamental period with a detailed switching cycle, where the fundamental currents are deduced from the FFT calculation. Under the same switching frequency, the ripple current of this scheme is larger than the normal SVPWM with a single inverter, which is owing to the phase shifting of PWM signals that adds the differential-mode circulating current into the phase-leg current. In addition, the current ripple of phase A_2 is with the half-switching-cycle phase shift compared to phase A_1 because of the same phase shift in the PWM signal. Fig. 12(b) shows the calculation results of the CRP model for phase legs A_1 and A_2 in one fundamental period with a detailed switching cycle; the detailed waveforms of the current ripple are similar to the detailed phase-leg currents shown in Fig. 12(a); the only difference in

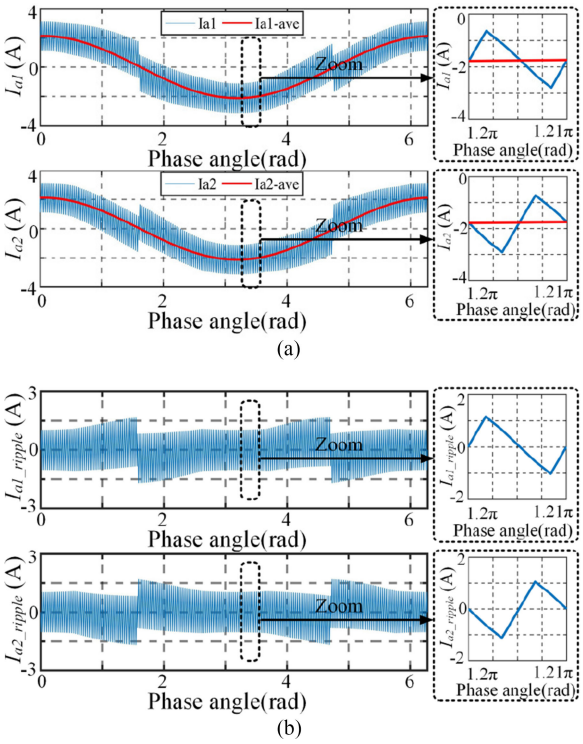

Fig. 12. Comparison of simulated phase-leg currents and the CRP result for a paralleled inverter with zero-CM PWM. (a) Simulated phase-leg currents. (b) CRP result.

the two detailed waveforms is that the switching currents add the real-time bias fundamental current.

In order to further verify the precision of the prediction model, the ripple current of phase leg A_1 in the simulation has been extracted by the FFT method to compare with the theoretical prediction value shown in Fig. 13(a). The overall waveform of the simulation is similar to the theoretical predicted result, and the enlarged details of current ripple show that the track of current ripples is almost the same in two situations. In addition, when plotting the peak values of the predicted ripple current in each switching cycle in the same figure with the ripple current by simulation in Fig. 13(b), it can be seen that the theoretical predicted ripple current peak value is very close to the envelope of the ripple current simulation result. From the above comparison, it can be proved that the CRP model is effective and can be utilized to predict the current ripple for paralleled inverters with the zero-CM PWM scheme.

C. Dead-Time Compensation for Zero-CM PWM in Paralleled Inverters

As mentioned previously, the principle of CMV elimination is owing to the simultaneously switching ON and OFF for two different phase legs, while the existence of the dead time changes the edge positions of the pole voltage, leads to the pole voltage asynchrony with the corresponding PWM signal, and, finally, causes instantaneous CMV pulses. Fig. 14(a) gives the CMV comparison between ideal (without the dead time) and nonideal (with the dead time) situations. It can be seen that the effect of

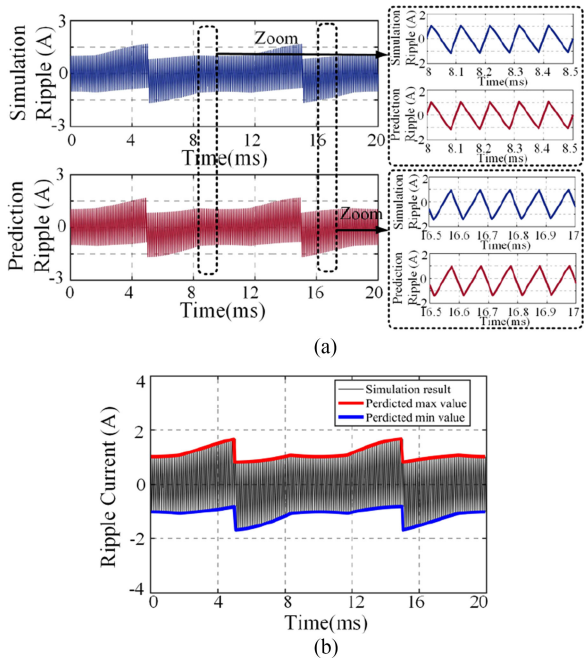

Fig. 13. Comparison of current ripple between simulation results and theoretical prediction. (a) Real-time track of current ripple comparison. (b) Peak value verification.

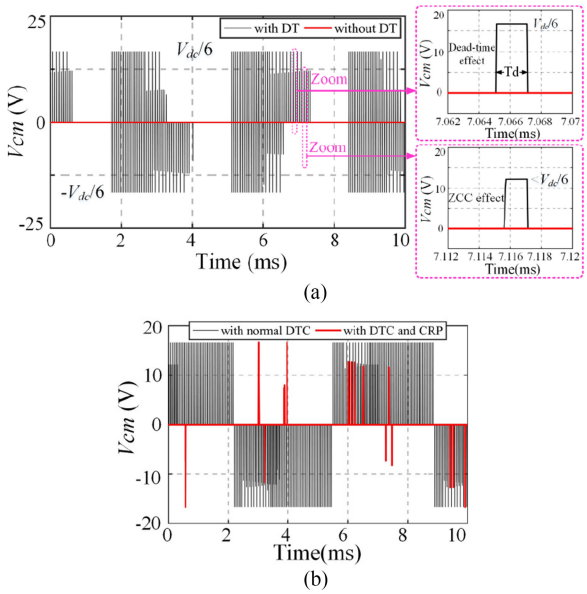

Fig. 14. CMV comparison among different situations. (a) Ideal and nonideal situations with dead time. (b) With normal DTC and with normal DTC with CRP.

CMV elimination for zero-CM PWM is degenerated under the nonideal condition because of the dead-time effect, and these pulses can be divided into two situations: the voltage pulse with the amplitude of $V_{\rm dc}/6$, which is generated by normal freewheeling of the antiparalleled diode and maintains a dead-time interval; and the voltage pulse with the amplitude less than $V_{\rm dc}/6$, which is generated by abnormal freewheeling of the antiparalleled diode (ZCC) and keeps less than a dead-time period. If the DTC can be well achieved, the instantaneous CMV

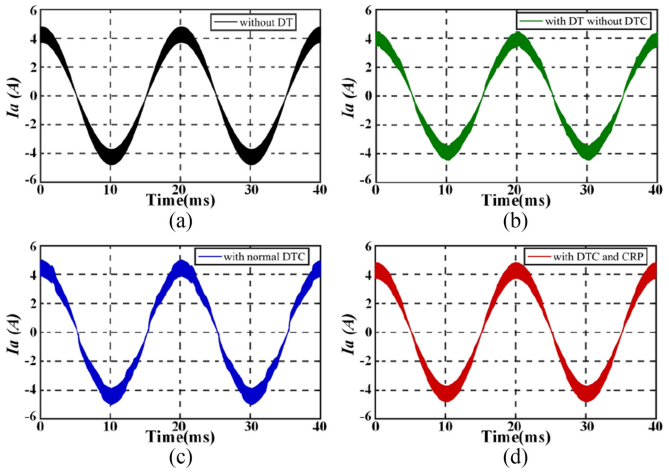

Fig. 15. Phase currents comparison among the four situations. (a) Without DT. (b) With DT without DTC. (c) With normal DTC. (d) With DTC and CRP.

pulses that are caused by the dead-time effect can be mitigated, so the performance of the DTC scheme for zero-CM PWM can be tested by the effect of CMV suppression.

In order to deal with the CMV pulses caused by the dead time, the following methods are implemented: the normal DTC by only sampling phase-leg currents (with normal DTC) and the modified DTC by sampling phase-leg currents with CRP (with DTC and CRP). The improvement performance of the CMV pulses elimination for these two schemes is shown in Fig. 14(b). Because the current ripple of the phase leg is comparable to the fundamental current under this condition, the normal DTC that ignores the current ripple can generate more CMV pulses, while the modified DTC method with CRP can eliminate most of the CMV pulses, which shows its superiority.

In addition, the performance of the output phase current should be taken into consideration. Fig. 15 gives a comparison about the phase currents for the above four schemes. Though the topology and modulation scheme changed, the effect of the dead time that generates the $(6n \pm 1)$th harmonic currents and reduces the fundamental current is similar to that of a single inverter, as shown in Fig. 15(a) and (b). The normal DTC method can help to recover the fundamental current, but cannot well restrain the harmonic currents as shown in Fig. 15(c). Finally, if CRP model is used, the DTC can not only recover the fundamental current, but also obviously improve the performance of harmonic suppression as shown in Fig. 15(d).

In addition, a frequency-domain comparison for the above phase currents by the FFT method is implemented as shown in Fig. 16. It can be seen that obvious $(6n \pm 1)$th harmonic currents occurs in the situation with DT without DTC. The normal DTC that neglects big current ripple causes more severe harmonic currents compared to the situation with DT without DTC. The implementation of DTC with CRP can obviously suppress the harmonic currents, which make the performance close to the idea condition. The THDs of the phase current for the four situations are 8.05%, 8.87%, 9.05%, and 8.06% correspondingly, which means the proposed method is valid for the THD reduction.

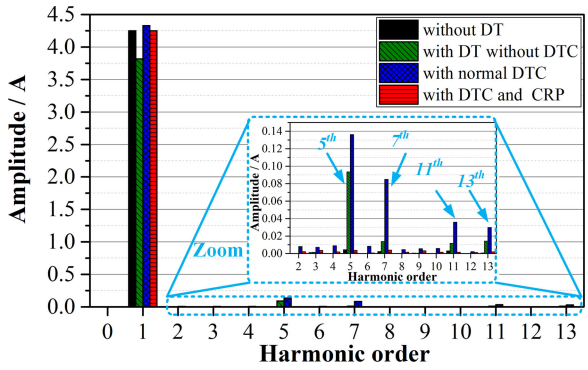

Fig. 16. FFT analysis of the phase current for the four situations.

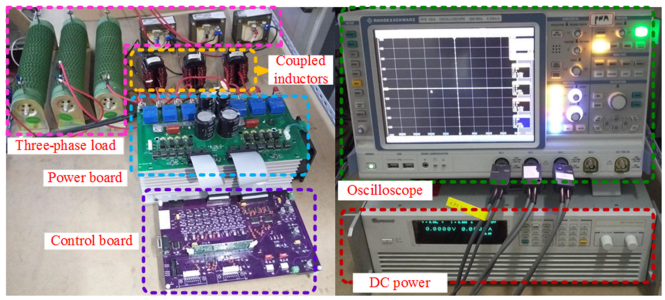

Fig. 17. Experimental platform.

So, from above simulation results, it can be found that the CRP-based DTC can improve the output current quality and the CMV elimination effect for paralleled inverters, which are both influenced by the dead time effectively.

V. Experimental Results and Discussion

A. System Implementation

In order to further verify the proposed DTC method, experiments have been done in a prototype experimental platform as shown in Fig. 17. The platform consists of a control board, a power board in which the main circuit has two conventional intelligent power modules (IPM: 6MBP20RH060, 600 V, 20 A, FUJI) connecting the common dc bus that can be used as a single inverter or paralleled inverters, three coupled inductors for paralleled inverters' ac-side output connection, and a three-phase *RL* load. The control algorithm is implemented in a digital signal processor TMS320F28335, which can generate 12 PWMs and drive two inverters simultaneously. The oscilloscope Rohde & Schwarz RTE1024 with a sampling rate of 5 GSa/s is utilized to capture the date and to make sure the precision of the time-domain waveform. The main parameters in the experiments take the same parameters from the simulation models, and only the modulation index is changed to test different steady states and dynamic conditions.

B. Dead-Time Compensation in a Three-Phase VSI With the SVPWM Algorithm

Based on the previous analysis, the proposed DTC method is first tested in a single VSI with the SVPWM algorithm. The

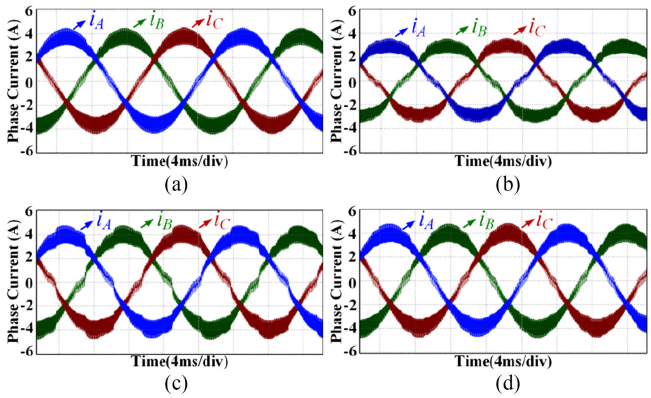

Fig. 18. Comparison of phase currents when $m = 0.2$. (a) Hypothetical ideal condition with the minimum dead time. (b) 2-μs dead time without DTC. (c) 2-μs dead time with DTC by current sampling. (d) 2-μs dead time with DTC by current sampling and CRP.

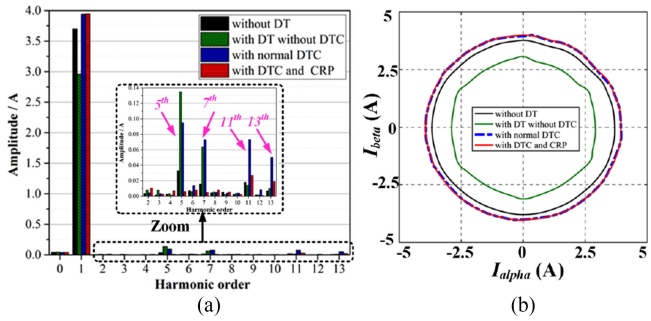

Fig. 19. Performance comparison of low-order harmonics suppression. (a) FTT analysis comparison. (b) Synthetic current vector's trajectory in $\alpha\beta$ coordinates.

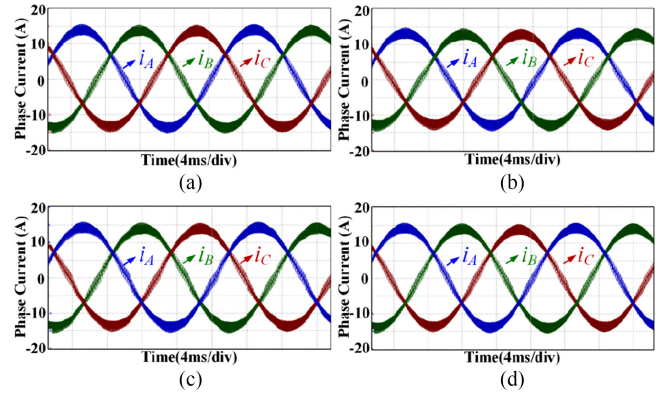

Fig. 20. Comparison of phase currents when $m = 0.7$. (a) Hypothetical ideal condition with the minimum dead time. (b) 2-μs dead time without DTC. (c) 2-μs dead time with DTC by current sampling. (d) 2-μs dead time with DTC by current sampling and CRP.

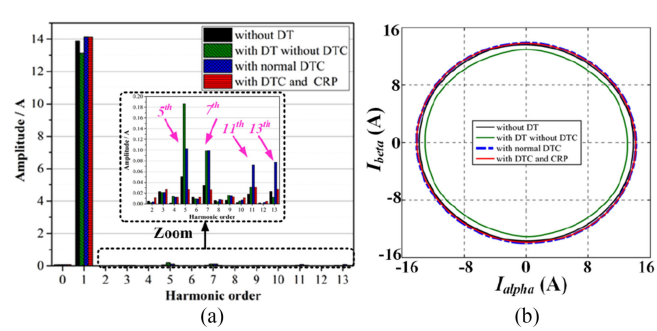

Fig. 21. Performance comparison of low-order harmonics suppression. (a) FTT analysis comparison. (b) Synthetic current vector's trajectory in $\alpha\beta$ coordinates.

low modulation index ($m = 0.2$) is used to emphasize the dead-time effect. In order to verify the effect of the proposed method, the four situations corresponding to simulation are implemented; only the ideal condition without dead time should be replaced by the small dead time of 0.5 μs (the minimum dead time for the IPM) at experiment situation. Fig. 18 gives the detailed comparison about the phase currents in the time domain for different situations. It can be found that the phase currents keep sinusoidal under the ideal condition, as shown in Fig. 18(a). With the dead-time effect shown in Fig. 18(b), the phase currents are distorted obviously, and the amplitude of the fundamental current is reduced at the same time. The amplitude of the fundamental current may keep similar to the idea condition with the normal DTC method, as shown in Fig. 18(c), but the waveform still has obvious distortion caused by the relatively big harmonic currents. Fig. 18(d) shows the phase currents by the proposed DTC method; it can be found that the waveform is nearly sinusoidal, which has a similar effect as the idea condition.

Fig. 19(a) shows the phase current comparison among the above situations in the frequency domain; the scheme with DTC and CRP can realize the best performance of low harmonics suppression, which can have the similar effect compared to the ideal condition. In addition, the THDs of the phase current for the four situations are 12.28%, 13.9%, 12.84%, and 12.22% correspondingly, which means the proposed method has the best performance for the THD reduction. The THD value for case 4 is slightly lower than that for case 1, which is owing to the fact that the fundamental current is slightly increased, and the low-frequency harmonics can be clearly found in cases 2 and 3, which adds their THD values. Fig. 19(b) extracts the three-phase fundamental with low-order harmonic currents and transforms them to the synthetic current vector's trajectory in $\alpha\beta$ coordinates. The scheme with DTC and CRP can make the trajectory of the current vector more smooth and close to the circle than the normal DTC situation. In addition, the radius of trajectory can be expanded in the idea condition. So, the proposed method is appropriate and effective for DTC in a low modulation index.

Figs. 18 and 19 have validated the proposed CRP-based DTC for a regular three-phase inverter with a low modulation index, with which the dead-time's ratio in duty cycles and current ripple's ratio in full current are big. A more general case is also studied in the experiment (with $m = 0.7$). The current waveforms for four cases are shown in Fig. 20. The current waveform distortion caused by the dead time is less obvious than that of Fig. 18. But the comparison shows similar results: with CRP based DTC, the current distortion can be improved better than with normal DTC.

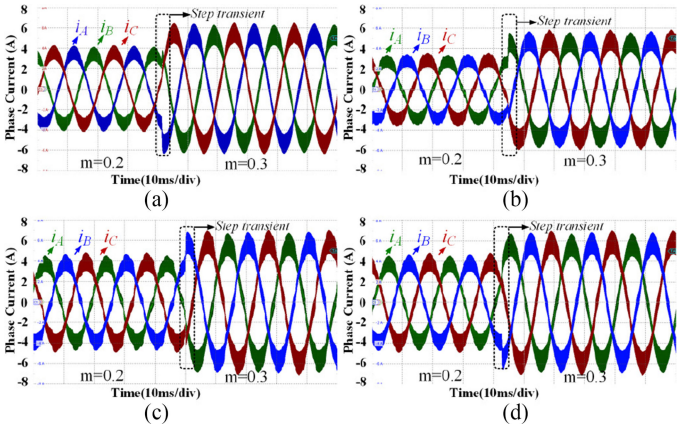

Fig. 22. Comparison of phase currents for a single inverter with step transient. (a) Hypothetical ideal condition with the minimum dead time. (b) 2-μs dead time without DTC. (c) 2-μs dead time with DTC by current sampling. (d) 2-μs dead time with DTC by current sampling and CRP.

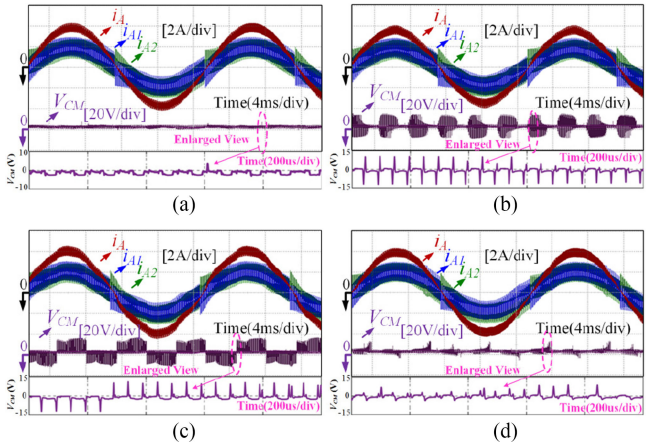

Fig. 23. Comparison of phase currents and CMVs when $m = 0.4$. (a) Hypothetical ideal condition with the minimum dead time. (b) 2-μs dead time without DTC. (c) 2-μs dead time with DTC by current sampling. (d) 2-μs dead time with DTC by current sampling and CRP.

Fig. 21(a) shows the phase current comparison among the above situations in the frequency domain. The scheme with DTC and CRP can realize the best performance of low harmonics suppression, which can get the similar effect compared to the ideal condition. In addition, the THDs of the phase current for the four situations are 7.65%, 8.2%, 7.7%, and 7.52% correspondingly, which also proves that the proposed method has the best performance for the THD reduction. Fig. 21(b) draws the synthetic current vector's trajectory in $\alpha\beta$ coordinates for different schemes. The scheme with DTC and CRP can also improve the trajectory compared to the normal DTC situation. Though the expansion of radius is not obvious, the fundamental current is also increased. So, the proposed method is also appropriate and effective for DTC in a general case with a high modulation index.

Finally, the dynamic conditions are implemented for different situations when the modulation index has a step transient from 0.2 to 0.3. It can be found that the proposed DTC method can realize similar performance compared to the ideal condition in different steady states, as shown in Fig. 22(a) and (d), while the other schemes are disturbed by the obvious harmonic currents, as shown in Fig. 22(b) and (c). In addition, considering the dynamic process, it can be found that all schemes have a similar response, which is owing to the fact that the DTC method has a little influence on the output volt–second of phase legs that cannot lead to the sudden change of phase currents; the step change of current is mainly caused by the reference instruction variation.

C. Dead-Time Compensation in Paralleled Inverters With the Zero-CM PWM Algorithm

With the employment of the zero-CM PWM algorithm in paralleled inverters, the output phase current can realize optimization, while the circulating current in paralleled phase legs aggravates; this leads to bigger current ripple in phase-leg currents compared to a single VSI.

The proposed DTC method is first tested under a relatively low modulation index ($m = 0.4$), which makes the phase-leg currents locate in the Z-zone more frequently. Following the same comparison method, Fig. 23 shows the detailed results. It can be clearly seen that the phase current keeps sinusoidal and the CMV is basically eliminated under the ideal condition, as shown in Fig. 23(a); the current jump in the phase-leg current is attributed to the modulation algorithm, which has two times instantaneous volt–second unbalance in one fundamental period. Fig. 23(b) shows the dead-time effect for zero-CM PWM, which not only generates harmonic currents but also degrades the CMV elimination effect; this phenomenon is coincided with the simulation result. The zoom-in waveform shows that the nonzero CMVs are spikes, in which the duration time is equal to or less than the dead-time interval. Fig. 23(c) shows the result of the normal DTC method, in which harmonics still distort the waveform. At the same time, the CMVs occur in the whole fundamental period, which is even worse than the without DTC scheme; this phenomenon is caused by the error judging the direction of phase-leg currents in the dead-time interval with the ignorance of a big current ripple. Fig. 23(d) shows the phase current with the proposed DTC method, which takes the current ripple into consideration by utilizing the CRP model; the output phase current keeps sinusoidal and is similar to the ideal condition. Meanwhile, the implementation of more accurate DTC makes the CMV elimination effect more realistic, in which only few CMV spikes exist. The major CMV spikes, in which the amplitude is smaller than other schemes, are caused by other nonideal factors, such as the ZCC relevant effect and the parasitic capacitance effect in switching devices, which increases the turn-ON and turn-OFF time when the phase-leg current is close to zero and extends the overlap time of switching states, which generate these CMV spikes finally [10].

The THD and low-order harmonics of phase currents are further analyzed and shown in Fig. 24. The THDs are 8.32%, 8.95%, 9.12%, and 8.14% correspondingly, which shows good

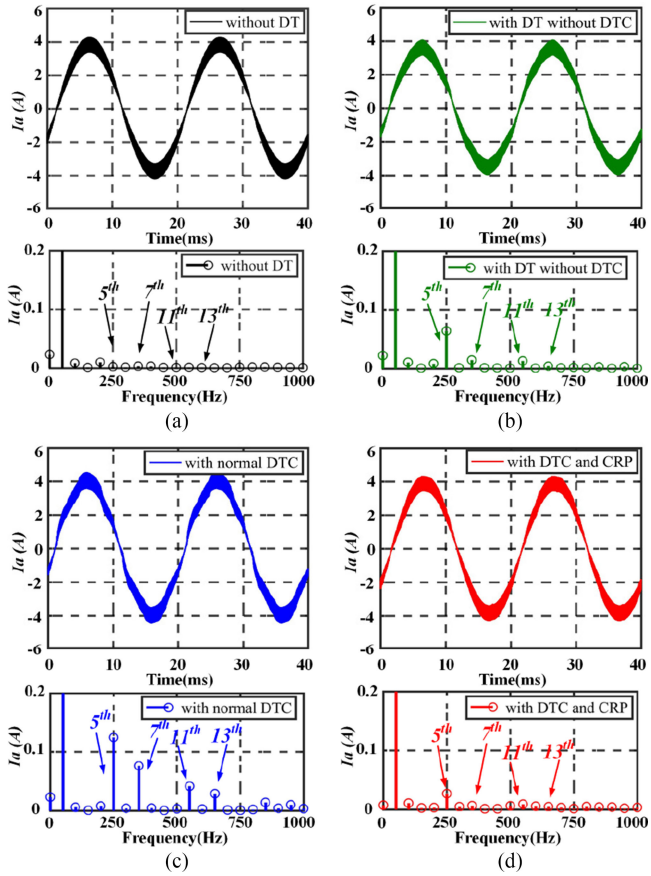

Fig. 24. Comparison of the phase current. (a) Without DT. (b) With DT without DTC. (c) With normal DTC. (d) With DTC and CRP.

performance of the proposed method. The harmonic currents caused by the dead time are obviously decreased by utilizing the proposed method. So, the proposed method is effective for DTC under this condition.

In addition, the 10-nF CM capacitance is added between the middle point of the dc link and the ac neutral point to simulate the CM stray circuit and test the effect of CM current suppression. The CM currents have been measured for the different cases with the existence of dead time and are compared in Fig. 25. The proposed DTC method can achieve the best CM current suppression either in the amplitude reduction or the dwell time. This is owing to the good performance of CMV suppression. So, the proposed DTC method can be implemented in paralleled inverters and can improve the DTC effect.

Finally, the dynamic conditions are also implemented for paralleled inverters when the modulation index has a step transient from 0.4 to 0.5, as shown in Fig. 26. The proposed DTC method can also achieve similar performance to the ideal condition with the time-domain comparison as shown in Fig. 26(a) and (d), while obvious harmonics influence other schemes in different steady states, as shown in Fig. 26(b) and (c). Meanwhile, the dynamic process of all the schemes has a similar response. The reason is owing to the fact that the influence of dead time on the output volt–second is limited; the dynamic response of

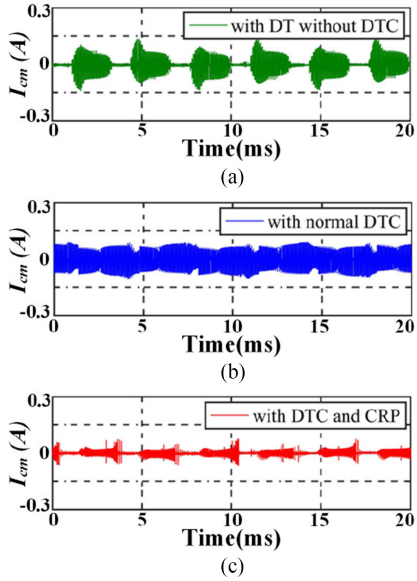

Fig. 25. Comparison of the CM current. (a) With DT without DTC. (b) With normal DTC. (c) With DTC and CRP.

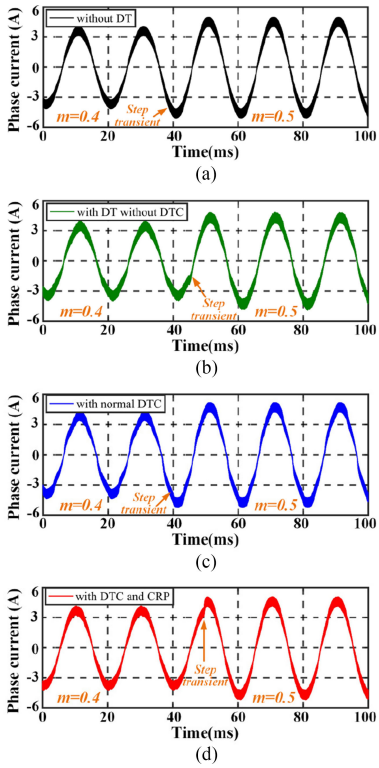

Fig. 26. Comparison of phase currents for paralleled inverters with step transient. (a) Hypothetical ideal condition with the minimum dead time. (b) 2-μs dead time without DTC. (c) 2-μs dead time with DTC by current sampling. (d) 2-μs dead time with DTC by current sampling and CRP.

current is mainly decided by the reference instruction variation regardless of different DTC methods.

VI. Conclusion

In this paper, a novel dead-time effect compensation method is proposed. The dead-time principle is first analyzed, and its

detailed influence on the output volt–seconds can be classified as four categories, in which the ZCC phenomenon appears in low probability and its effect is approximately ignored. So, three fixed DTC schemes can be implemented by judging the peak values of the phase-leg current in one switching cycle, which corresponds to the rising and falling edges of the PWM signal. Based on this requirement, the innovative DTC method that takes real-time current ripple into consideration can be utilized by the CRP model. The proposed method can make DTC more accurate compared to the normal current-sampling-based DTC method. Few conclusions can be derived as follows.

1) The impact of the dead time on the output voltage is associated with the current direction, which is also impacted by the current ripple especially for the zone near zero. The dead-time compensation method with a low sampling rate of current cannot meet good compensation requirement.
2) The proposed dead-time compensation method combines the sampled fundamental current and the predicted current ripple. It can precisely compensate the impact of the dead time on the output voltage and improve the current quality.
3) The CM voltage elimination effect is also influenced by the dead time for the zero-CM PWM with paralleled inverters. The proposed dead-time compensation method with CRP can improve the CM voltage elimination effect.

The simulation and experimental results show that the proposed method is effective to implement the DTC under different working conditions.

REFERENCES

[1] E. Levi, R. Bojoi, F. Profumo, H. A. Toliyat, and S. Williamson, "Multiphase induction motor drives—A technology status review," *IET Electr. Power Appl.*, vol. 1, no. 4, pp. 489–516, Jul. 2007.

[2] G. Jeong and M. H. Park, "The analysis and compensation of deadtime effects in PWM inverters," *IEEE Trans. Ind. Electron.*, vol. 38, no. 2, pp. 108–114, Apr. 1991.

[3] K. M. Cho, W. S. Oh, Y. T. Kim, and H. J. Kim, "A new switching strategy for pulse width modulation (PWM) power converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 330–337, Feb. 2007.

[4] L. Chen and F. Z. Peng, "Dead-time elimination for voltage source inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 574–580, Mar. 2008.

[5] Y. K. Lin and Y. S. Lai, "Dead-time elimination of PWM-controlled inverter/converter without separate power sources for current polarity detection circuit," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2121–2127, Jun. 2009.

[6] A. R. Munoz and T. A. Lipo, "On-line dead-time compensation technique for open-loop PWM-VSI drives," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 683–689, Jul. 1999.

[7] A. Lewicki, "Dead-time effect compensation based on additional phase current measurements," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4078–4085, Jul. 2015.

[8] B. Weber, T. Brandt, and A. Mertens, "Compensation of switching dead-time effects in voltage-fed PWM inverters using FPGA-based current oversampling," in *Proc. 31st Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 3172–3179.

[9] H.-S. Kim, H.-T. Moon, and M.-J. Youn, "On-line dead-time compensation method using disturbance observer," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1336–1345, Nov. 2003.

[10] N. Urasaki, T. Senjyu, T. Kinjo, T. Funabashi, and H. Sekine, "Dead-time compensation strategy for permanent magnet synchronous motor drive taking zero-current clamp and parasitic capacitance effects into account," *Proc. Inst. Elect. Eng.—Electr. Power Appl.*, vol. 152, no. 4, pp. 845–853, Jul. 2005.

[11] N. Urasaki, T. Senjyu, K. Uezato, and T. Funabashi, "Adaptive dead-time compensation strategy for permanent magnet synchronous motor drive," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 271–280, Jun. 2007.

[12] S. Y. Kim, W. Lee, M. S. Rho, and S. Y. Park, "Effective dead-time compensation using a simple vectorial disturbance estimator in PMSM drives," *IEEE Trans. Ind. Electron.*, vol. 57, no. 5, pp. 1609–1614, May 2010.

[13] S. H. Hwang and J. M. Kim, "Dead time compensation method for voltage-fed PWM inverter," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 1–10, Mar. 2010.

[14] D. H. Lee and J. W. Ahn, "A simple and direct dead-time effect compensation scheme in PWM-VSI," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3017–3025, Sep. 2014.

[15] Z. Zhang and L. Xu, "Dead-time compensation of inverters considering snubber and parasitic capacitance," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 3179–3187, Jun. 2014.

[16] T. Mannen and H. Fujita, "Dead-time compensation method based on current ripple estimation," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 4016–4024, Jul. 2015.

[17] G. Grandi, J. Loncarski, and R. Seebacher, "Effects of current ripple on dead-time distortion in three-phase voltage source inverters," in *Proc. IEEE Int. Energy Conf. Exhib.*, 2012, pp. 207–212.

[18] Y.-S. Lai and F.-S. Shyu, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part I: Basic development," *IEEE Trans. Ind. Appl.*, vol. 40, no. 6, pp. 1605–1612, Nov./Dec. 2004.

[19] X. Zhang, R. Burgos, D. Boroyevich, P. Mattavelli, and F. Wang, "Improved common-mode voltage elimination modulation with deadtime compensation for three-level neutral-point-clamped three-phase inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 15–19, 2013, pp. 4240–4246.

[20] D. Jiang, Z. Shen, and F. Wang, "Common-mode voltage reduction for paralleled inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3961–3974, May 2018.

[21] A. Videt, M. Messaoudi, N. Idir, H. Boulharts, and H. Vang, "PWM strategy for the cancellation of common-mode voltage generated by three-phase back-to-back inverters," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2675–2686, Apr. 2017.

[22] D. Jiang and F. Wang, "Current-ripple prediction for three-phase PWM converters," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 531–538, Jan./Feb. 2014.

Zewei Shen (S'17) was born in Hubei, China, in 1990. He received the B.S. degree in automation from the Huazhong University of Science and Technology, Wuhan, China, in 2012, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include paralleled converters and high-power-density motor drives.

Dong Jiang (S'05–M'12–SM'16) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2005 and 2007, respectively, and the Ph.D. degree from the University of Tennessee, Knoxville, TN, USA, in December 2011.

He started his Ph.D. research at the Center for Power Electronics Systems, Virginia Tech, in 2007 and was transferred to the University of Tennessee with his advisor in 2010. He was a Senior Research Scientist/Engineer at the United Technologies Research Center, East Hartford, CT, USA, from January 2012 to July 2015. Since July 2015, he has been a Professor with the Huazhong University of Science and Technology, Wuhan, China. He has authored or coauthored more than 40 published IEEE journal and conference papers. His major research interests include power electronics and motor drives.

Dr. Jiang is a recipient of two best paper awards in IEEE conferences. He is an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS.