Dead-Time Distortion Shaping

Fernando Chierchie, Eduardo Emilio Paolini, and Leandro Stefanazzi

***Abstract*—A fully digital algorithm to shape the spectrum of dead-time distortion in power inverters is presented. Dead-time is required to avoid short circuits of the power source by the legs of a power inverter due to the finite turn-ON and turn-OFF times of the switches. Dead-time modifies the pulsewidths of the pulsewidth modulated (PWM) signal causing high harmonic distortion. The proposed approach is based on the time-to-digital conversion of the pulsewidths at the output of the power stage and does not require to measure the sign of the current, which is the preferred approach for dead-time compensation algorithms. The effect of the parasitic capacitance of the switching device that distorts the switching waveform is also analyzed and corrected. Furthermore, the quantization noise produced by digital PWM is also reduced by the proposed approach and has a minimal computational cost. Hardware-in-the-loop simulations are provided to show the effectiveness of the proposed approach, and experimental results using an H-bridge voltage-source inverter are included. A minimum total harmonic distortion plus noise (THD+N) of 0.027% was achieved for a 1-kHz input driving an inductive load.**

***Index Terms*—Dead-time, noise shaping (NS), pulsewidth modulation (PWM), time encoding, total harmonic distortion (THD).**

I. Introduction

SWITCHING voltage-source inverters with different applications such as power waveform generation, switching amplifiers (class-D), and high-power electronic applications are very efficient but suffer from various noise and distortion problems. Digital pulsewidth modulation (PWM) intrinsically introduces distortion due to its nonlinear amplitude to time conversion; several solutions have been proposed in the literature [1]–[4]. Still, the power stage also introduces noise and distortion because of several physical limitations of its components [5]. Some of the most important phenomena are the following [6].

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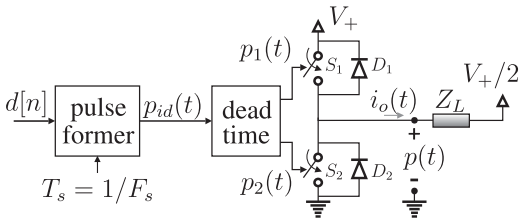

Fig. 1. Basic topology for the analysis of the dead-time.

imperfections can be used without compromising the stability. The proposed approach has low computational complexity requiring only a few multiplications and additions, which makes it possible to implement on a standard digital signal processor (DSP), a field-programmable gate array, or a digital integrated circuit.

The proposed approach eliminates several problems associated with previously reported dead-time compensation methods.

1) The compensation is fully digital.
2) No delay is introduced in the signal path.
3) The sign of the load current is not required.
4) The duty cycles are measured using a digital counter (time-to-digital converter); no analog–digital or digital–analog converters are needed.
5) The compensation strategy is independent of the algorithm used for the PWM modulation.

In Section II, the dead-time effect is explained and the duty-cycle error is defined. In Section III, the proposed DTDS algorithm is presented. Simulations are provided in Section IV, and experimental results with a power stage are presented in Section V.

II. Dead-Time Effect

The effects of dead-time can be explained with the help of Fig. 1. Two semiconductors switches S_1 and S_2 are connected in series conforming a leg of a power inverter. Each switch has freewheeling diodes D_1 and D_2 connected in parallel. To simplify the analysis, the dc power supply is assumed to have a normalized value of $V_+ = 1$ V. The load Z_L is connected between the middle point of the leg and a dc voltage of $V_+/2$ V, allowing the load current $i_o(t)$ to be either positive or negative. The analysis can be easily extended to H-bridge inverters, switching amplifiers, or three-phase inverters. In what follows, it is assumed that the energy in the inductance is enough to keep current conduction through the freewheeling diode during dead-time.

Due to the nonideal behavior of the power transistors, it is necessary to add dead-time to ensure that one switch is completely OFF before turning ON the complementary switch.

The pulse former takes the normalized pulsewidths $0 \leq d[n] < 1$ and produces the ideal PWM signal $p_{\text{id}}(t)$ (no dead-time), which has a PWM frequency of $F_s = 1/T_s$. Without loss of generality, we use double-edge symmetric PWM: the pulses of width $d[n]T_s$ are centered around the PWM period. The "dead-time" block is in charge of generating the signals $p_1(t)$ and $p_2(t)$ that drive the upper and lower switches. Signal

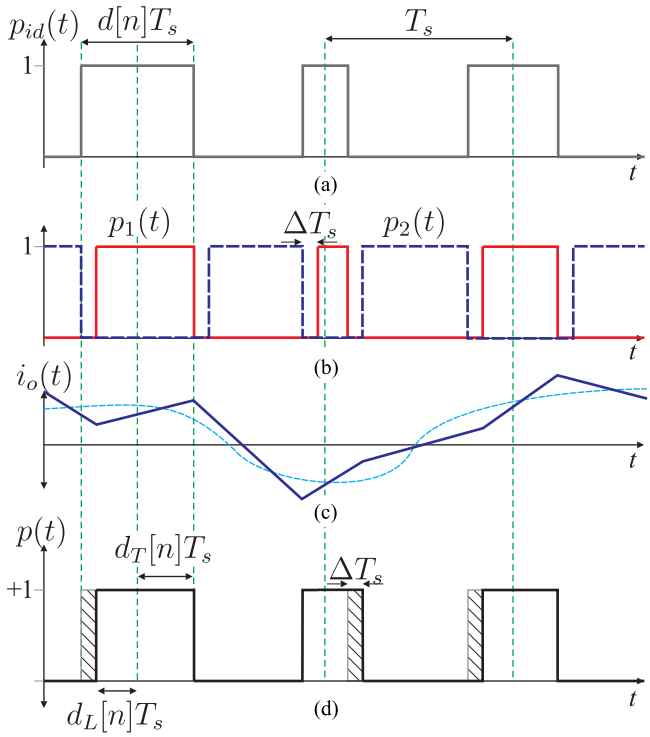

Fig. 2. Waveforms. (a) Ideal PWM signal. (b) Switches S_1 and S_2 control signals. (c) Output current $i_o(t)$ (average of $i_o(t)$ shown with a dashed line). (d) Output PWM signal.

$p_1(t)$ is generated by introducing a delay ΔT_s in the rising edges of $p_{\text{id}}(t)$, while $p_2(t)$ is obtained by complementing the signal $p_{\text{id}}(t)$ and applying a delay of ΔT_s seconds to the rising edges of the resulting signal, where $0 \leq \Delta < 1$ is the normalized dead-time with $\Delta \ll 1$. Fig. 2(a) and (b) shows typical waveforms for $p_{\text{id}}(t)$, $p_1(t)$, and $p_2(t)$.

The PWM signal $p(t)$ is the power-amplified PWM signal. During the dead-time intervals Δ, where both control signals $p_1(t)$ and $p_2(t)$ are zero, $p(t)$ depends on the sign of the load current $i_o(t)$, which, in turn, depends on the load impedance $Z_L(s)$. If during the dead-time interval, $i_o(t) > 0$, then $i_o(t)$ flows through D_2 and $p(t)$ goes to 0 V (ground). On the other hand, if $i_o(t) < 0$, the current circulates through D_1 and $p(t)$ goes to V_+. Fig. 2(c) and (d) depicts qualitatively the current $i_o(t)$ showing also its averaged waveform (dashed) and the resultant PWM signal $p(t)$.

A. Duty-Cycle Error

As can be seen from the shaded areas in Fig. 2, the effect of the dead-time is to shorten or enlarge the duty cycle $d[n]T_s$ of the ideal PWM signal $p_{\text{id}}(t)$ by a fixed value ΔT_s resulting in $p(t)$. The actual pulses in $p(t)$ are no longer symmetric as in $p_{\text{id}}(t)$, resulting in baseband distortion. To model this disruption in the symmetry of the pulses, we distinguish the normalized "trailing-edge duty cycle" $d_T[n]$ from the normalized "leading-edge duty cycle" $d_L[n]$, both of which are shown in Fig. 2(d). They represent the semiduty cycle between the center of the ideal pulse (half the PWM period) and the trailing and leading edges, respectively. With zero dead-time, $d_T[n] = d_L[n] = d[n]/2$ and

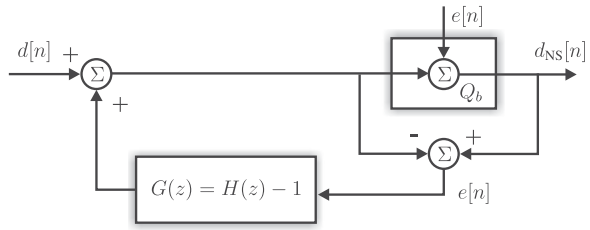

Fig. 3. Standard NS algorithm.

$d[n] = d_T[n] + d_L[n]$. The trailing and leading edge errors are defined as

$$e_T[n] = d_T[n] - d[n]/2$$
$$e_L[n] = d_L[n] - d[n]/2. \quad (1)$$

III. Dead-Time Distortion Shaping

We start this section with a brief review of the noise-shaping (NS) technique [2].

A. Overview of Standard NS

NS is a technique used to displace the spectrum of additive noise to higher frequencies above the frequency band of interest. It has applications in digital–analog converters and digital PWM, where, usually, the sampling or PWM frequency is much higher than the maximum frequency of the input signal, and the error can be modeled as an additive noise signal source. The technique can be explained with the help of Fig. 3. The block Q_b represents a distorting memoryless element, and its effect can be modeled as an additive noise $e[n]$ that can be recovered by comparing the input and the output of this block. For quantization NS, Q_b represents a b-bit quantizer.

The error $e[n]$ is recovered by subtracting the output and the input of the Q_b block and then filtered with a filter with the z-transform $G(z)$. In the z-transform domain, the NS input–output relation is given by

$$D_{\text{NS}}(z) = D(z) + E(z)(1 + G(z)) = D(z) + E(z)H(z) \quad (2)$$

where $D(z)$, $D_{\text{NS}}(z)$, and $E(z)$ are the transforms of $d[n]$, $d_{\text{NS}}[n]$, and $e[n]$, respectively. This equation reveals that: 1) the input $D(z)$ passes unaltered to the output and 2) the spectrum of the noise source $E(z)$ is shaped by $H(z) = 1 + G(z)$. Since, from (2), the transfer function between the output $D_{\text{NS}}(z)$ and the input $D(z)$ is $D_{\text{NS}}(z)/D(z) = 1$, no delay is added in the path of the signal independently of the choice for $G(z)$. This is an intrinsic characteristic of the NS technique.

A typical choice for the filter is

$$G(z) = H(z) - 1 \quad (3)$$

with $H(z) = (1 - z^{-1})^K$ being a high-pass FIR filter. Generally, the filter order is kept low, $3 \leq K \leq 5$. For the NS algorithm to work properly, F_s must be several times higher than the bandwidth F_m of the input signal to ascertain that there is a frequency band between F_m and $F_s/2$ where the quantization noise is shaped.

B. Dead-Time Distortion Shaping

The use of an NS structure for DTDS and design criteria for the digital filter $G(z)$ are discussed in this section.

The trailing and leading error signals $e_{T,L}[n]$ can be expressed as a function of the sign of the current $i_o(t)$ at the time instants of the ideal trailing and leading edges given by $t_T[n] = (n + 0.5 + d[n]/2)T_s$ and $t_L[n] = (n + 0.5 - d[n]/2)T_s$, respectively, giving $e_{T,L}[n] = -(\Delta/2)(1 \pm \text{sgn}\,(i_o\,(t_{T,L}[n])))$. Dead-time affects either the rising and/or the falling edge of the pulse, and the error signal depends on the sign of the current on the same PWM period (memoryless distortion). The ideal duty cycle $d[n]$ is affected by an *additive noise* $e_{T,L}[n]$, which results in the actual semiduty cycles $d_{T,L}[n] = d[n]/2 + e_{T,L}[n]$. Due to this modeling of the dead-time distortion as an additive noise source, it is possible to apply the NS structure to shape its spectrum.

The error can be computed using the sign function and the output current, but, in our approach, $e_{T,L}[n]$ is directly computed using (1) and the measurement of $d_{T,L}[n]$ without measuring the current or its sign. Under normal operating conditions, if the inductance keeps the current $i_o(t)$ circulating through the diodes during dead-time, the errors $e_T[n]$ and $e_L[n]$ have a fixed amplitude: $e_T[n]$ is either 0 or Δ and $e_L[n]$ is either 0 or $-\Delta$. The errors $e_T[n]$ and $e_L[n]$ take either of the two possible values depending on the sign of the current $i_o(t)$, which, in turn, depends on the load impedance Z_L and the input duty cycles $d[n]$, i.e., the errors $e_T[n]$ and $e_L[n]$ are correlated with the input signal. For periodic signals, such as sinusoids, this correlation results in an spectra of $e_{T,L}[n]$ with the energy content in the harmonics of the fundamental frequency, which, in turn, produces output voltages $p(t)$ and currents $i_o(t)$ with harmonic distortion.

Dead-time modifies the pulsewidth but also produces pulses that are asymmetric with respect to the center of the PWM period, which results in the generation of harmonics. The proposed architecture uses a double NS loop: one for the trailing edge $d_T[n]$ and the other for the leading edge $d_L[n]$.

A block diagram is shown in Fig. 4. The PWM signal $p(t)$ is scaled (resistor divider) and passed through a Schmitt-trigger comparator to obtain $\hat{p}(t)$. The duty cycles $d_T[n]$ and $d_L[n]$ are measured using a time-to-digital converter, usually implemented with a high-speed counter in a DSP implementation. The measurements are available with one sample delay noted as $d_T[n-1]$ and $d_L[n-1]$. The z^{-1} block is used to equalize for this delay. Since $G(z) = H(z) - 1$ and $H(z)$ is an FIR filter of the form $H(z) = 1 + h[1]z^{-1} + h[2]z^{-2} + \cdots + h[N]z^{-N}$, then $G(z) = h[1]z^{-1} + h[2]z^{-2} + \cdots + h[N]z^{-N}$ has an intrinsic one sample delay. Defining the DTDS filter as

$$zG(z) = h[1] + h[2]z^{-1} + \cdots + h[N]z^{-N+1} \quad (4)$$

the measurement delay and the z^{-1} block shown in Fig. 4 do not introduce any additional delay to the error filter $G(z)$: the measurement delay is used as the intrinsic filter delay.

The duty cycles $d_L^{\text{DS}}[n]$ and $d_T^{\text{DS}}[n]$ computed with the DTDS algorithm are then passed to the pulse former block, which is a standard double-update digital PWM modulator that updates the PWM comparison value at the beginning of the PWM period

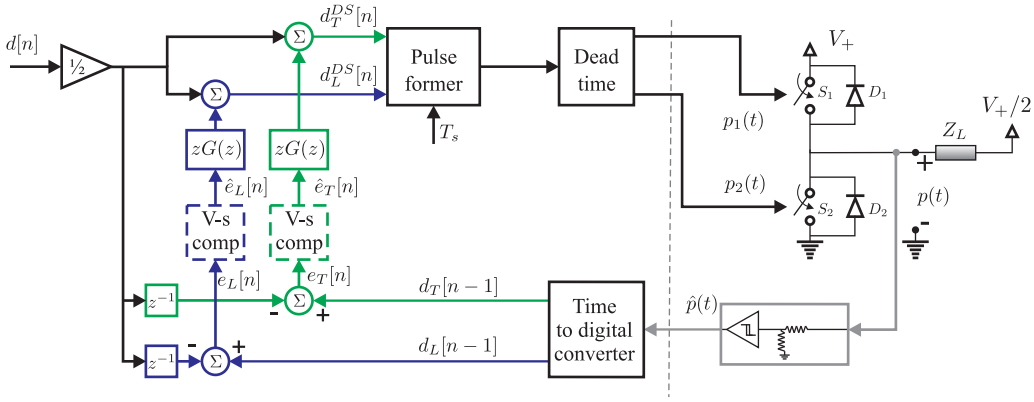

Fig. 4. Complete DTDS block diagram.

to account for the leading edge and at half for the trailing-edge update because the rising and falling edges need to be adjusted independently. The "V-s comp" block shown in Fig. 4 is used to circumvent some practical issues and will be explained in Section V-A1.

One advantage of the proposed approach is that since the measured duty-cycles account for both the dead-time effect and the duty-cycle quantization due to finite resolution in the digital PWM modulator, both noises are shaped by $H(z)$. Another advantage is that since there is no delay introduced in the signal path [see (2)], additional outer feedback loops could be used to compensate for other perturbations.

C. DTDS Filter for Nonperiodic Inputs

For arbitrary (band-limited to $F_m \ll F_s$) discrete-time signals that are not periodic, dead-time will produce error signals $e_T[n]$ and $e_L[n]$, whose spectrum spread over the frequency band 0 to $F_s/2$. This could be the case of a switching amplifier or an arbitrary power waveform generator. The standard high-pass filter $H(z) = (1 - z^{-1})^K$ can be used to shape dead-time distortion. For $K = 4$, we have

$$H(z) = 1 - 4z^{-1} + 6z^{-2} + -4z^{-3} + z^{-4}$$
$$zG(z) = -4 + 6z^{-1} + -4z^{-2} + z^{-3}. \quad (5)$$

For this case, the bandwidth $(F_m, F_s/2)$ is used to shape the distortion out of the band of interest. The PWM frequency F_s should be several times higher than the maximum frequency F_m of the input: typical values of F_s/F_m are 10 or higher.

D. DTDS Filter for Periodic Inputs

When the input is a periodic signal with the fundamental frequency $F_m = F_s/N$, as in the case of power dc–ac inverters, where the energy of the duty-cycle errors $e_T[n]$ and $e_L[n]$ is concentrated in the harmonics of the input signal, a better choice is a comb filter with zeros of its transfer function at F_m and its harmonics below $F_s/2$. A straightforward implementation is

$$zG(z) = -z^{-N+1} \quad (6)$$

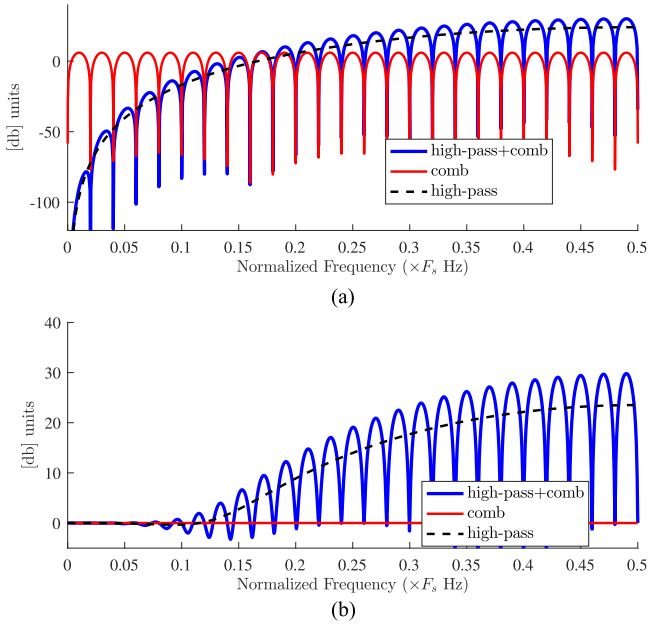

Fig. 5. Magnitude of the frequency responses of the proposed filters for $H(z)$ and $zG(z)$. (a) $|H(z)|$ with $z = e^{j\omega}$. (b) $|zG(z)|$ with $z = e^{j\omega}$.

with $N = F_s/F_m$. This comb filter requires no multiplications and only a buffer for storing $N - 1$ past samples of the input.

When other noise sources are present, such as quantization noise of the duty-cycles, a combination of the high-pass standard filter (3) and the comb filter (6) can be used. The system function of such a filter using a high-pass filter of order $K = 5$ is

$$zG(z) = -4 + 6z^{-1} - 4z^{-2} + z^{-3} - z^{-N+1} + 4z^{-N} - 6z^{-N-1} + 4z^{-N-2} - z^{-N-3}. \quad (7)$$

This filter can be implemented using a buffer for storing $N + 3$ samples and computing only three products because of the symmetry of its coefficients.

The magnitude of the frequency responses for the three types of proposed filters $H(z)$ is shown in Fig. 5(a) for $N = F_s/F_m = 50$. The magnitude of $zG(z)$ is also shown in Fig. 5(b), as described by (6); for the comb filter, $zG(z)$ becomes a pure delay, as shown by the constant magnitude in Fig. 5(b).

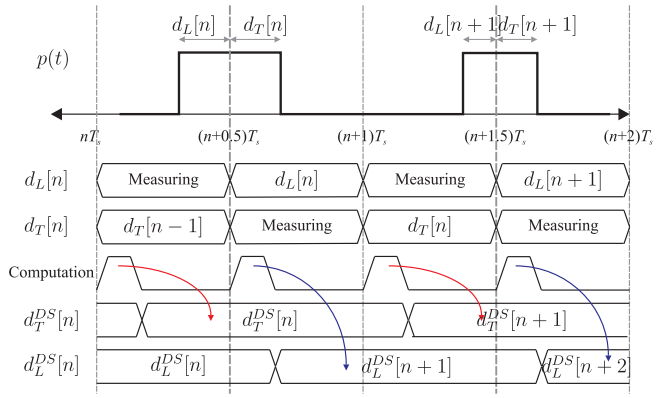

Fig. 6. Timing diagram of the DTDS algorithm.

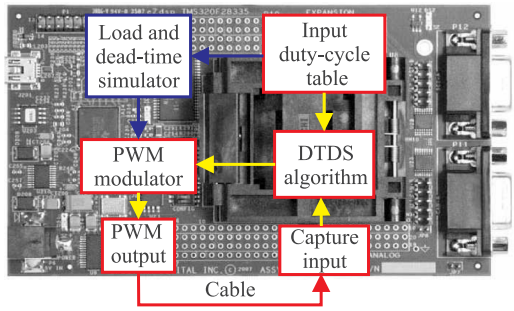

Fig. 7. Hardware-in-the-loop simulation.

E. Implementation and Timing

Fig. 6 shows a timing diagram of the DTNS algorithm implementation. The leading edge $d_L[n]$ and the trailing edge $d_T[n]$ are measured in the power stage during each corresponding half PWM period. Usually, many DSPs have built-in modules that can be configured to measure time events [16], which can be used as the time-to-digital converter in Fig. 4. The measured values are available during the next half PWM period for the computation of the DTDS algorithm. For example, the measurement of $d_L[n]$ is available at $(n+0.5)T_s$ and the measurement of $d_T[n]$ at $(n+1)T_s$. Once they are available, the other half of the PWM period can be used to compute the DTNS algorithm. In other words, when the leading edge is being measured, the trailing-edge DTDS is being computed and vice versa.

The resulting duty cycles $d_L^{\mathrm{DS}}[n+1]$ and $d_T^{\mathrm{DS}}[n+1]$ are available before the beginning of the next semiperiod at $(n+1)T_s$ and $(n+1.5)T_s$, respectively. Thus, the new PWM period can be updated with the duty-cycle values $d_L^{\mathrm{DS}}[n+1]$ and $d_T^{\mathrm{DS}}[n+1]$, which will result in the actual PWM signal in the power stage with duty cycles $d_L[n+1]$ and $d_T[n+1]$, and the algorithm starts all over again.

Two types of experimental results are presented in this paper: one with a simulation of the power stage (hardware-in-the-loop (HIL) simulation) and the other using an actual power stage. In both cases, the DTDS algorithm is running in real time on a DSP (TMS320F28335).

IV. HIL Simulation

In this experience, the dead-time effect and the load are simulated, and no actual power stage is used. The algorithm is running in real time on the DSP implemented, as shown in Fig. 7, with the timing shown in Fig. 6. The duty cycles $d[n]$ corresponding to one period of the input signal are stored in a table. These duty cycles are used as input to the DTDS algorithm and also for the load and dead-time simulator. This block uses the duty cycles to compute the averaged output current using a dynamical-discrete-time model for the impedance of the load. The sign of the simulated current is used by the simulator to modify independently the leading and trailing edges in the PWM modulator block according to the freewheeling diode conduction produced during dead-time and analyzed previously. The actual PWM signal is feedback into a digital input (capture unit [16]) using a cable to measure both the rising and falling edges with respect to the center of the PWM period. These measurements are used by the DTDS to compute the duty cycles $d_T^{\mathrm{DS}}[n]$ and $d_L^{\mathrm{DS}}[n]$.

This HIL simulation permits to verify the operation of the algorithm in real time. It also allows us to check the proposed scheme for duty-cycle measurement using the capture unit of the DSP, which includes the finite resolution of the digital counter. At the same time, it is useful to verify the validity of the proposed approach under controlled conditions: the assumption of continuous conduction of the freewheeling diodes during dead-time is verified, and other parasitic effects of the power stage are avoided (in the following section, the impact of those practical phenomena is analyzed in detail).

The simulated load $Z_L(s)$ is an *LCR* low-pass filter with values $L = 200\ \mu$H, $C = 0.2\ \mu$F, and $R = 4\ \Omega$; for the HIL simulation, the second-order transfer function was converted into a discrete-time equivalent using the zero-order hold approximation. The input is a 1-kHz sinusoidal signal and the PWM frequency is $F_s = 50$ kHz. A dead-time value of $\Delta T_s = 200$ ns that represents a $\Delta[\%] = 1\%$ of the PWM period was set. To evaluate the performance of the DTDS, the PWM was low-pass filtered, and its frequency spectrum was computed using the AP-2700 signal analyzer. The results of the HIL simulation are shown in Fig. 8. Without DTDS, the spectra reveal the pattern of harmonics produced by dead-time. Fig. 8(b) and (c) shows the performance of the algorithm using two different filters: the first one is a comb filter (6), and the second one is the combination of the high-pass and comb filter (7). In both cases, the harmonics related to dead-time are eliminated. Certain amount of noise floor is present for both filters, but, in the case of the combined filter, the noise is shaped into high frequencies, leaving a frequency band between 0 and 6 kHz with reduced noise floor. This noise is caused by the finite resolution of the PWM modulator and of the capture unit used to measure the pulsewidths.

V. Experimental Results With a Power Stage

An H-bridge converter with each leg implemented with MOSFETs that include the freewheeling diodes was used. The dc voltage is $V_+ = 13.5$ V. The load is a series resistance plus inductance with $R = 5\,\Omega$ and $L = 166\,\mu$H. The PWM signal is

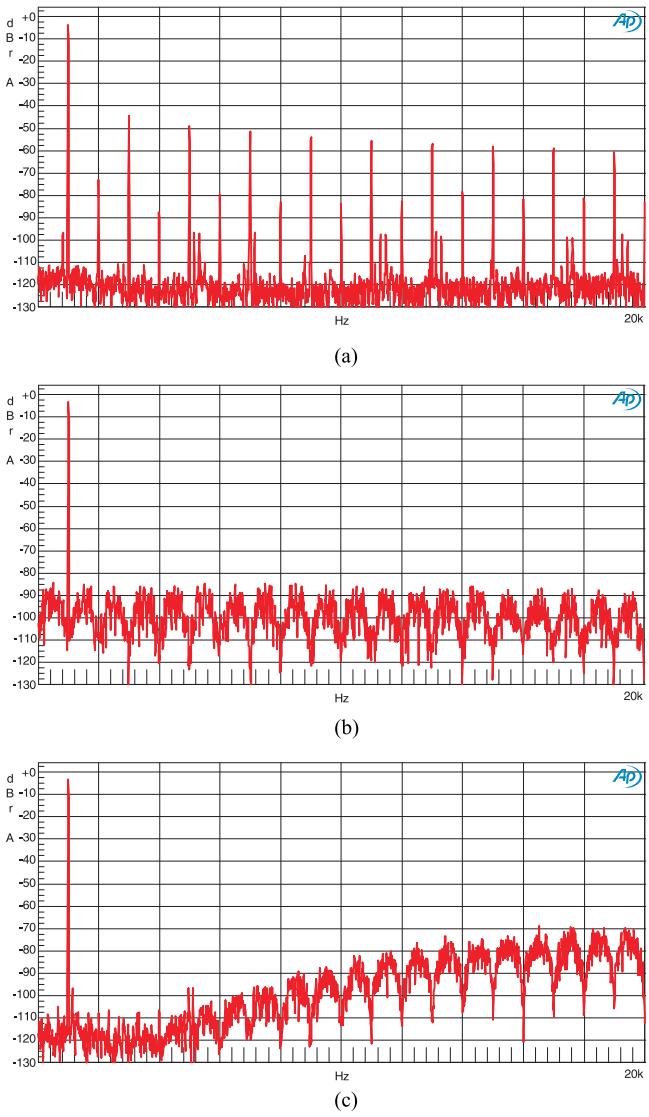

Fig. 8. Measured baseband spectra of the PWM signal for simulated load and dead-time effect (HIL). The input is a sinusoidal signal of 1 kHz, the PWM frequency is 50 kHz, and the dead-time is $\Delta\% = 1\%$. X-axis: frequency in hertz; Y-axis: normalized dB units. (a) Without DTDS: dead-time distortion. (b) DTDS: comb filter. (c) DTDS: comb + high-pass filter.

feedback only in one of the legs of the H-bridge, and complementary control signals are used to drive the other leg. Other parameters are those of the HIL simulation. The dead-time value varies for different experiences. A photograph of the experimental setup is shown in Fig. 9. The instruments used for the experimental test are Oscilloscope LeCroy WaveRunner 204MXi-A 2 GHz-10 GS, Agilent E3646A 60-W dual-output power supply, the AP SYS2722 digital signal analyzer for spectrum and total harmonic distortion plus noise (THD+N) measurements, the SRS SIM965 analog filter for PWM demodulation, Tektronic A622 current probe 100 mV/A. The main devices of the power stage are the MCP14700 dual-input synchronous MOSFET driver, IRF8313 power MOSFETs ($V_{\mathrm{DS(max)}} = 30$ V and $I_{D\,(\mathrm{max})} = 8$ A), and the SN74AHC1G14 Schmitt-trigger gate to measure the PWM signal.

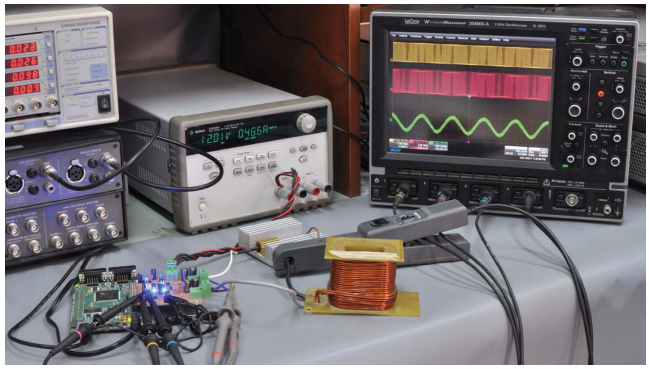

Fig. 9. Experimental setup: DSP, power stage, and load.

A. *Effect of the Parasitic Capacitance in the Switching Node*

During the zero crossing of the load current, when its magnitude is small, the parasitic capacitance of the switching devices affects the transition of the PWM signal $p(t)$ in the switching node (SN) [17]–[20]. The effect is analyzed separately for the rising and falling edges with the help of Fig. 10, which exhibits the parasitic capacitance of the switching devices.

For the rising edge, and before the dead-time interval, capacitor C_2 is discharged and C_1 charged. For $i_o > 0$ [see Fig. 10(a)], the switch S_2–D_2 was conducting, and this behavior continues during dead-time. After dead-time, S_1 turns ON, C_1 is short circuited, and the SN switches to its high level. However, for $i_o < 0$ [see Fig. 10(b)], capacitor C_1 must discharge before diode $D1$ can conduct the negative output current: if $i_o \ll 0$ (its magnitude is high), the discharge of C_1 is fast and the transition occurs at the beginning of dead-time, as expected. For $i_o \approx 0$, the discharge is slow and the transition time from low to high depends on the magnitude of i_o. Fig. 10(b) depicts different possible slopes for the transition. If the slope is below V_+/Δ, the dead-time interval finishes, $S1$ turns ON, and the SN switches to V_+. In short, for the raising edge and positive values of i_o, the rise time can be considered almost independent of the magnitude of the current. On the other hand, for $i_o < 0$, the rise time increases for lower magnitudes of i_o. A similar analysis can be carried out for the falling edge, as depicted in Fig. 10(c) and (d).

Fig. 11 shows a high-persistence measurement of the voltages after the resistor divider ($p(t)$ scaled) and after the Schmidt-triggered buffer ($\hat{p}(t)$), as indicated in Fig. 4. Most of the transitions are concentrated at the beginning or at the end of the dead-time ($|e_{L,T}[n]|$ is 0 or Δ), but some of them occur slowly due to the effect of the parasitic capacitance. Also indicated in Fig. 11 is the small delay added by the Schmidt-trigger comparator.

1) Volt–Second Compensation for Slow Transitions: We assume that the charging and discharging of the capacitor can be approximated with a straight line, as suggested by the measurements in Fig. 11. The basic idea is that the area under the triangle or trapezoid produced by the slow transition is assigned to an equivalent "corrected pulse" with the same area. The position of the corrected edge slightly differs from the position of the logic buffer output $\hat{p}(t)$, which is the measured signal. Because the magnitude of the dead-time error is either 0 or

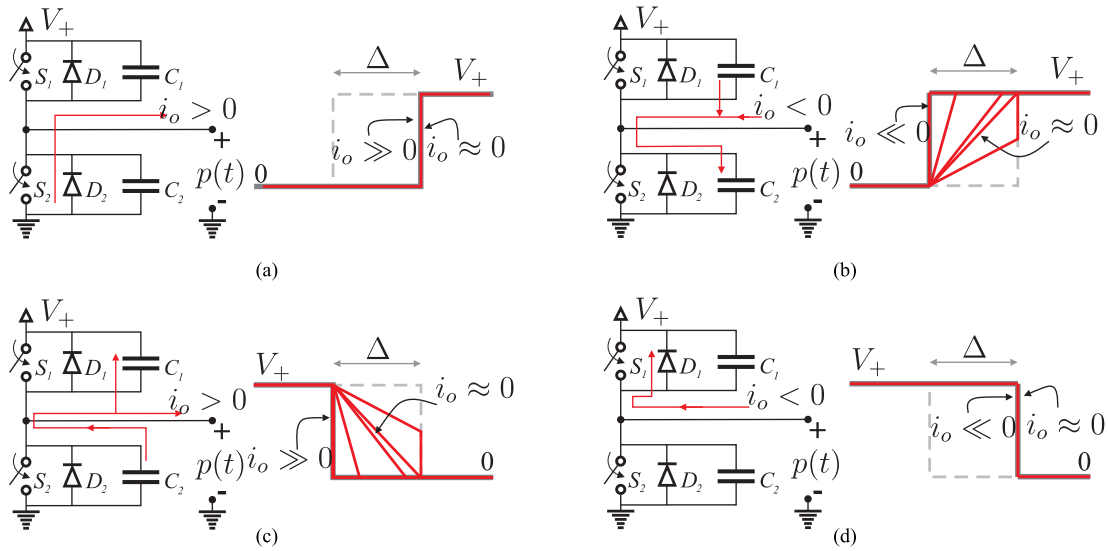

Fig. 10. Switching node waveform during dead-time taking into account parasitic capacitance of the switching devices. (a) Rising edge, $i_o > 0$. (b) Rising edge, $i_o < 0$. (c) Falling edge, $i_o > 0$. (d) Falling edge, $i_o < 0$.

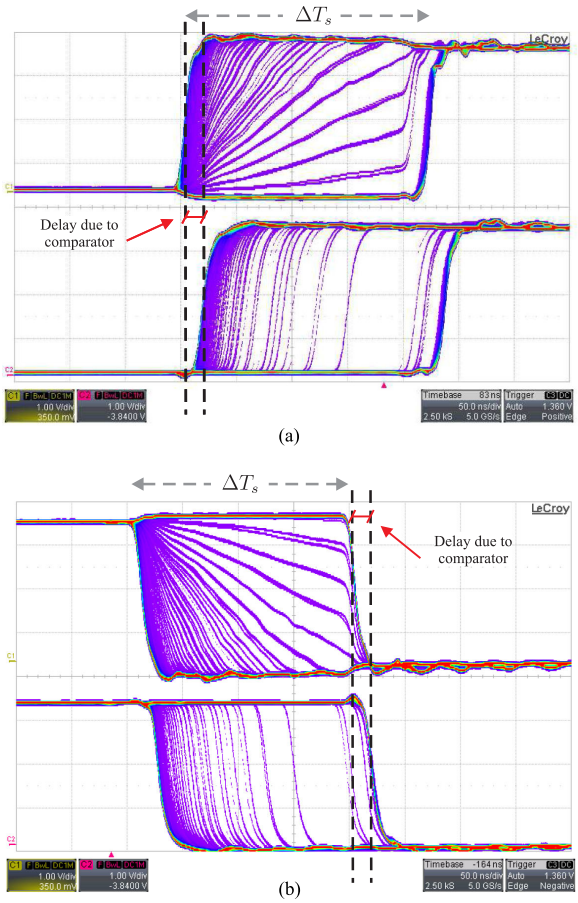

Fig. 11. Upper trace: switch node (scaled with resistor divider). Lower trace: output of comparator. Several instances of the signals are shown using the high persistence of the oscilloscope. X-axis: time 50 ns/div. Y-axis: voltage 1 V/div. (a) Leading-edge. (b) Trailing-edge.

Δ (with no capacitive effect), a measurement of the error of less than Δ ($|e_{T,L}[n]| < \Delta$) is indicative of a slow transition. Therefore, the area correction described here is only applied if $0 < |e_{T,L}[n]| < \Delta$.

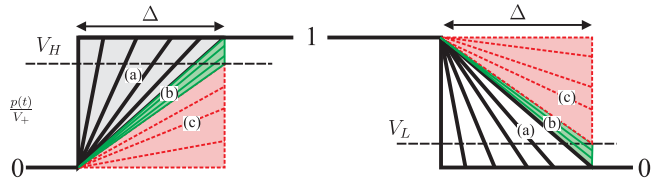

Fig. 12. All three possible regions for slow transitions in $p(t)$ during low-magnitude output current.

To compensate for the parasitic capacitance effect, three cases should be considered, as shown in Fig. 12 and indicated as (a)–(c). The cases are identified based on the duty-cycle error measurement $e_L[n]$ and $e_T[n]$ and also V_L and V_H, which are the normalized high-to-low and low-to-high threshold values of the Schmitt trigger. All magnitudes involved in the analysis are normalized.

Case (a): The peak of the triangle reaches the normalized bus voltage of 1 V (or 0 V for the trailing edge) before the end of the dead-time period Δ. A particular example of case (a) is shown in Fig. 13(a). The normalized height of the triangle is always 1, and the normalized bases of the leading- and trailing-edge triangles $\tau_L[n]$ and $\tau_T[n]$ are defined as the time that takes to charge (discharge) the SN capacitance from 0 to 1 (1 to 0) divided by the switching period, as indicated in (*i*) in Fig. 13(a). The leading- and trailing-edge normalized errors $e_L[n]$ and $e_T[n]$ are indicated in (*ii*) in Fig. 13(a). Assuming that the voltage waveforms of the charge/discharge of the parasitic capacitor can be approximated by the shapes shown in (*i*) in Fig. 13(a), the slope of the leading-/trailing-edge transitions can be expressed as

$$\frac{1}{\tau_L[n]} = \frac{V_H}{|e_L[n]|}, \qquad \frac{1}{\tau_T[n]} = \frac{(1-V_L)}{|e_T[n]|}. \tag{8}$$

To detect that a slow PWM transition is under case (a), the limit between regions (a) and (b) should be considered. At this point, $p(t)/V_+$ reaches 1 exactly at the end of the dead-time

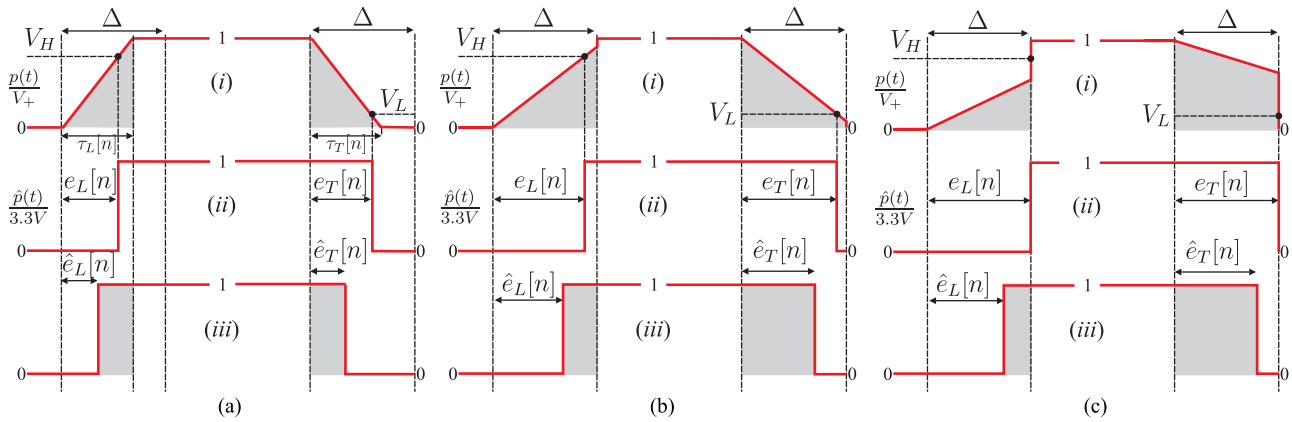

Fig. 13. Area correction to compensate measurements of slow transitions. (a)–(c) show examples for the three possible regions. The waveforms in each subfigure are (*i*) normalized voltage at SN $p(t)/V_+$, (*ii*) normalized Schmitt-trigger output $\hat{p}(t)/3.3$ V, and (*iii*) equivalent PWM signal with corrected errors.

period as follows: $\tau_T[n] = \tau_L[n] = \Delta$. Replacing this result in (8) gives the higher bound for $|e_L[n]|$ and $|e_T[n]|$. Then, to assert a case (a) transition, the measured errors must be in the range

$$0 < |e_L[n]| \leq V_H\Delta \qquad 0 < |e_T[n]| \leq (1 - V_L)\Delta. \tag{9}$$

Once case (a) is detected, the error signals are corrected. The normalized areas under the triangles are $A_L[n] = \tau_L[n]/2$ and $A_T[n] = \tau_T[n]/2$. Replacing (8) and equating the shaded areas in (*i*) and (*iii*) in Fig. 13(a) gives

$$\hat{e}_L[n] = \frac{\tau_L[n]}{2} = \frac{e_L[n]}{2V_H} \quad \hat{e}_T[n] = \frac{\tau_T[n]}{2} = \frac{e_T[n]}{2(1 - V_L)}. \tag{10}$$

For cases (b) and (c), the normalized voltage at the parasitic capacitance does not reach 1 V (or 0 V for the trailing edge) during the dead-time period. This results in a triangular transition shape with a height lower than 1 for the leading edge and in a trapezoid for the trailing edge. In these cases, the normalized length of the bases is fixed as follows: $\tau_T[n] = \tau_L[n] = \Delta$. From a circuital perspective, when the end of the dead-time period is reached, the corresponding power switch turns ON and the parasitic capacitance is either rapidly charged or discharged through a low-impedance path to the power source.

Case (b): The normalized voltage of the parasitic capacitance at the end of the dead-time period is higher than V_H but lower than 1 for the leading edge and is lower than V_L for the trailing edge. An example is shown in Fig. 13(b). This case could be detected from $e_L[n]$ and $e_T[n]$, since the threshold levels V_H and V_L are crossed before the end of the dead-time period. Considering the transition in the border condition between cases (a) and (b), to assert a case (b) transition, the measured errors must be in the range

$$V_H\Delta < |e_L[n]| < \Delta \qquad (1 - V_L)\Delta < |e_T[n]| < \Delta. \tag{11}$$

For the leading edge, the height of the triangle is $\Delta V_H / |e_L[n]|$, which can be used to compute its area $A_L[n] = \Delta^2 V_H / (2|e_L[n]|)$. For the trailing edge, the height of the right side of the trapezoid is $1 - \Delta(1 - V_L)/|e_T[n]|$, which can be used to compute its area as $A_T[n] = \Delta - \Delta^2(1 - V_L)/(2|e_T[n]|)$. Equating the gray areas in Fig. 13(b), the correction for the duty-cycle error signal is

$$\hat{e}_L[n] = \Delta - \frac{\Delta^2 V_H}{2e_L[n]} \qquad \hat{e}_T[n] = \Delta - \frac{\Delta^2(1 - V_L)}{2e_T[n]}. \tag{12}$$

Case (c): In (*i*) in Fig. 13(c), the height of the triangle is lower than V_H and the length of the right side of the trapezoid is greater than V_L. This case cannot be detected using the comparator output $\hat{p}(t)$, since, as shown in (*ii*) in Fig. 13(c), the leading and trailing edges will be interpreted as a typical dead-time error $|e_L[n]| = |e_T[n]| = \Delta$. However, the error that is introduced when ignoring this case can be bounded. In the worst case for the leading edge, the triangle will have a height of V_H [limit between cases (b) and (c)], which gives an area $A_L[n] = V_H\Delta/2$. This gives an equivalent error $\hat{e}_L[n] = (1 - V_H/2)\Delta$. Then, the measurement error produced by ignoring case (c) is bounded by

$$|e_L[n] - \hat{e}_L[n]| \leq \Delta\frac{V_H}{2}. \tag{13}$$

For the trailing edge, the worst case is attained if the right side of the trapezoid equals V_L, which gives an area for the trapezoid $A_T[n] = (1 + V_L)\Delta/2$, giving an equivalent error $\hat{e}_T[n] = \Delta(1 + V_L)/2$ bounding the error as

$$|e_T[n] - \hat{e}_T[n]| \leq \Delta\frac{(1 - V_L)}{2}. \tag{14}$$

In other words, given the results in (13) and (14), the worst duty-cycle measurement error produced by not taking into account case (c) for typical values of $V_H \approx 0.8$ and $V_L \approx 0.3$ is bounded by 0.4Δ and 0.35Δ, respectively.

To summarize, once the errors are corrected, $\hat{e}_{T,L}[n]$ are used to compute the DTDS algorithm, indicated with the "V-s comp" block in Fig. 4. A similar approach was proposed in [18] but using a current measurement and a lookup table that relates the magnitude of this current and the slope of the slow transitions. In our proposed method, only V_L and V_H are needed, which could be determined from the datasheet of the Schmitt trigger or addressed experimentally as part of a calibration routine.

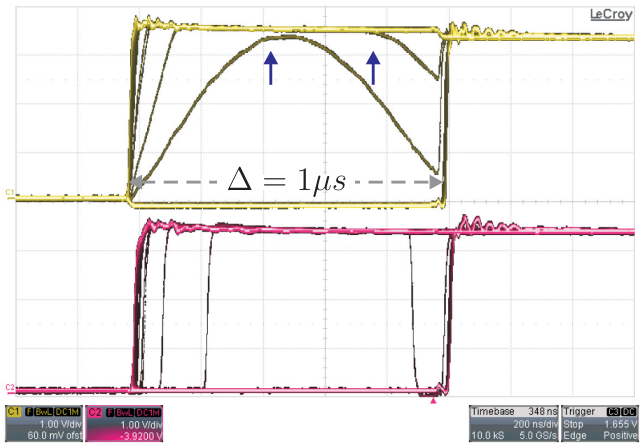

Fig. 14. Discontinuous conduction during dead-time for $\Delta\% = 5\%$. Upper trace: SN (scaled with a resistor divider). Lower trace: output of the comparator. Several instances of the signals shown using the high-persistence mode of the oscilloscope. Arrows indicate the point at which conduction becomes discontinuous. X-axis: time 200 ns/div. Y-axis: voltage 1 V/div.

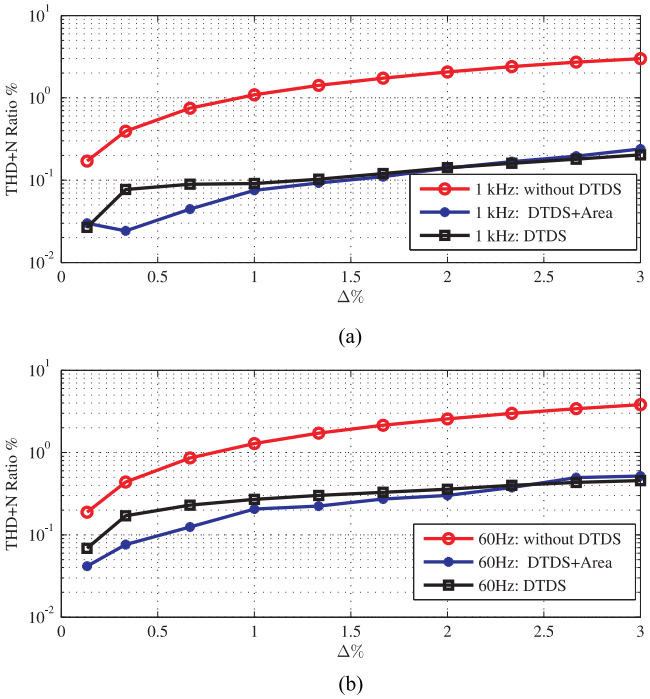

Fig. 15. THD+N% as a function of dead-time $\Delta\%$ for sinusoidal inputs of (a) 1 kHz and (b) 60 Hz.

B. Discontinuous Conduction Mode During Dead-Time

Continuous conduction during dead-time must be guaranteed in the sense that the inductance should have enough energy to keep the freewheeling diodes conducting during dead-time. For very large values of dead-time or very small values of inductance, this may not be the case. Fig. 14 shows a measurement for a large value of $\Delta\% = 5\%$ dead-time, in which discontinuous conduction is observed in some of the transitions. In this case, the performance will be reduced compared to continuous conduction, but, as shown in next section, distortion will still be reduced.

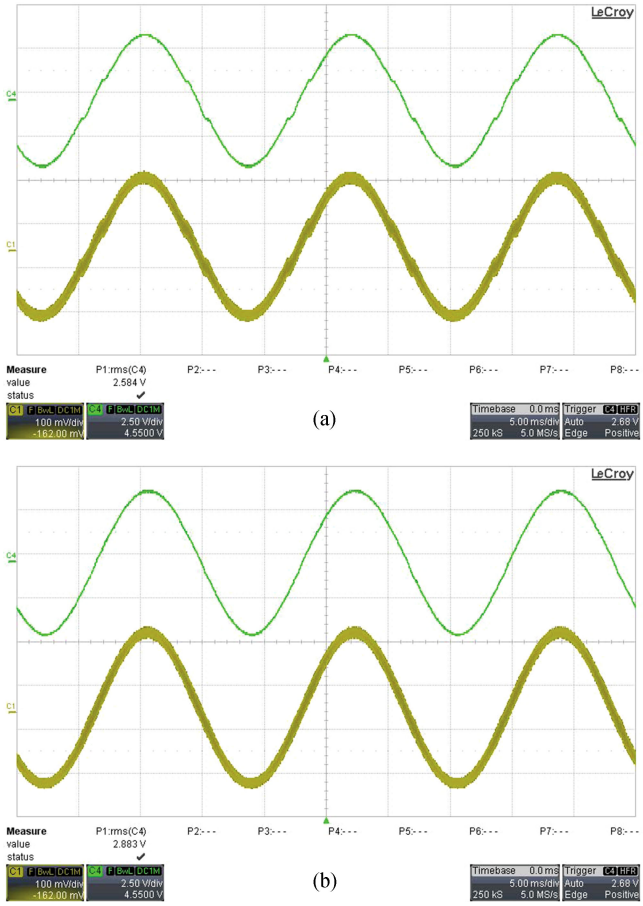

Fig. 16. For (a) and (b), top scope trace (C4) voltage $p(t)$ (single leg) filtered; bottom scope trace (C1) $i_o(t)$. Input 60-Hz signal and dead-time $\Delta\% = 2.6\%$. Uncorrected output (a) shows amplitude reduction and waveform distortion resulting in a THD+N = 3.4%. The DTDS algorithm restores the amplitude and reduces the distortion to THD+N = 0.4%. X-axis: time 5 ms/div. Y-axis: 2.5 V/div (C4), 1 A/div (C1). (a) Without DTDS. (b) With DTDS.

C. DTDS Results

To show the performance of the DTDS algorithm, the THD+N was measured. The PWM frequency is fixed at 50 kHz, while the dead-time varies from $\Delta\% = 0.13\%$ to $\Delta\% = 3\%$. The results are shown in Fig. 15(a) for a 1-kHz input signal and in Fig. 15(b) for a 60-Hz signal using the combined comb and high-pass filter given by (7). The THD+N is computed in the frequency range 0–6 kHz for both signals, using 6 and 60 harmonics, respectively. This is the frequency range, in which distortion and noise are expected to be reduced, since the system function $H(z)$ (7) attenuates the errors in this frequency range.

The DTDS results are shown in Fig. 15 with the area compensation proposed in (10) disabled and enabled. For the two input frequencies, a reduction of approximately one order of magnitude in the THD+N was achieved. When the area compensation approach is used, the THD+N is generally further reduced. For large dead-times, a slight increase is observed; this could be attributed to the discontinuous conduction explained before: for dead-time values around $\Delta\% > 2.3\%$, the phenomenon depicted in Fig. 14 begins to manifest, but despite this, the proposed algorithm still dramatically reduces distortion

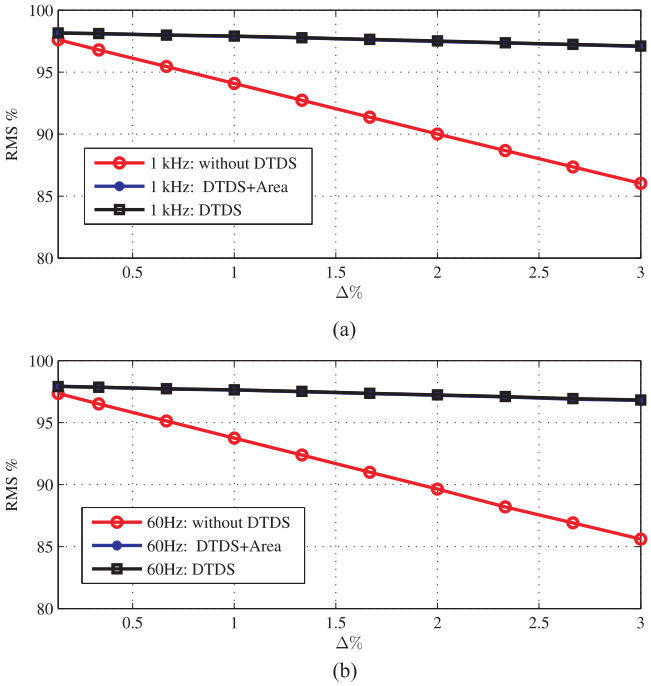

Fig. 17. Reduction of RMS value (in %) as a function of dead-time ($\Delta\%$) for sinusoidal inputs of (a) 1 kHz and (b) 60 Hz.

(either with the area compensation enabled or disabled). No noticeable improvements were measured when also detecting the slow transition in case (b) (see Fig. 12) and using the area compensation in (12); this is attributed to the fact that there is a small error in considering case (b) as part of case (a), and this small difference is masked by other noise sources such as limited time resolution

For the minimum applicable dead-time allowed by the MOSFETs used, $\Delta T_s \approx 26.7$ ns ($\Delta\% = 0.13\%$), and the 1-kHz input signal, the THD+N is 0.17518% without DTDS and reduced to 0.02665% when using DTDS plus area compensation. These distortion levels are comparable to those achieved with a similar experimental setup [21] but without an inductive load, which is the responsible for dead-time distortion.

For a dead-time $\Delta\% = 2.6\%$, the time-domain results can be seen in Fig. 16, which shows the filtered voltage waveform produced in one leg of the inverter and the inductance current measured with a current probe. Without the DTDS, the dead-time distortion produced in the voltage waveform during the zero crossings of $i_o(t)$ is clearly appreciated (THD+N 3.4%), while this distortion is reduced to 0.4% with DTDS and cannot be appreciated in the oscilloscope measurement.

The normalized RMS value of the demodulated voltage waveform as a function of dead-time is shown in Fig. 17. The RMS reduction is well known as one of the most serious drawbacks of dead-time. The measured RMS value R_m is normalized using the modulation index m_i of the sinusoidal and the dc voltage V_+ as RMS% $= [R_m/(m_i V_+/\sqrt{2})] \times 100$. When no algorithm is operating, the RMS value is reduced linearly with dead-time, achieving a reduction to almost 85% of the ideal value for $\Delta\% = 3\%$. When the DTDS is operating, the RMS is restored to around

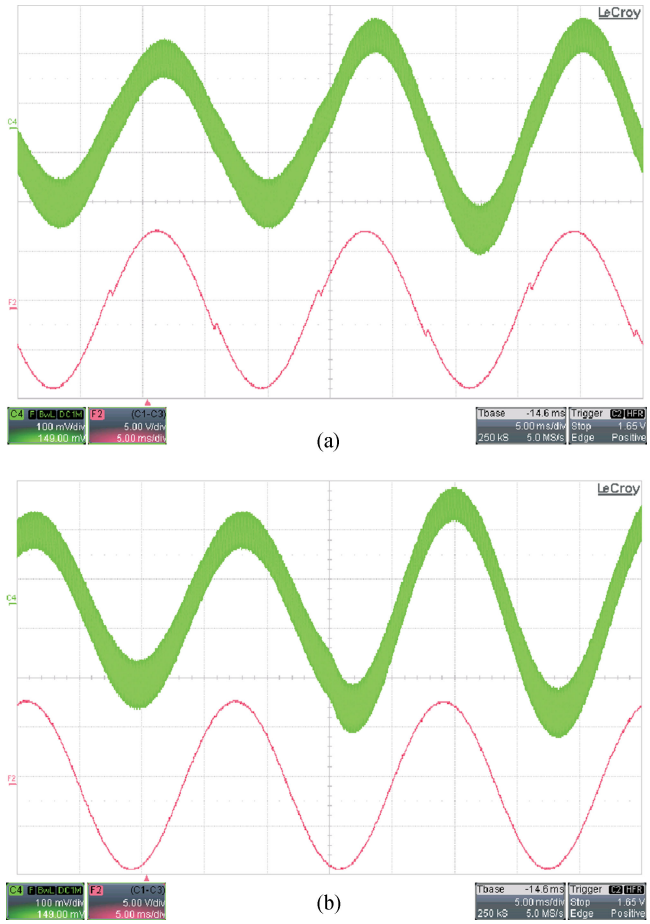

Fig. 18. Load step. Top scope trace (C4): load current $i_o(t)$; bottom scope trace: demodulated PWM signal (filtered). Input 60 Hz and dead-time $\Delta\% = 2\%$. X-axis: time 5 ms/div. Y-axis: 5 V/div (lower-trace), 1 A/div (C4). (a) Without DTDS. (b) With DTDS.

98% of the ideal value and is kept almost constant and independent of dead-time. The 2% difference is attributed to the voltage drop during the switches' ON-state (MOSFET ohmic region).

Finally, a load step change was carried out. For this test, $L = 3.77$ mH, and a load step from 5 to 3.5 Ω was performed (43% change). Results are shown in Fig. 18, where the output current and the demodulated (filtered) PWM signal can be observed. Fig. 18(a) and (b) shows the load step without and with the DTDS algorithm. No stability issues are observed, and the algorithm manages to remove the dead-time distortion before and after the load step.

VI. Conclusion

A novel algorithm to reduce the distortion produced by dead-time was presented. The algorithm uses a time-to-digital converter to measure the pulsewidths in the power stage, and it has a low computational complexity. The algorithm is fully digital and does not require an analog–digital converter. No delay is added in the signal path, which simplifies the design of additional outer feedback loops. Experimental results show a reduction of one order of magnitude in the THD+N and a restoration of the RMS value of the output voltage waveform.

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