A Soft-Switching Step-Down PFC Converter With Output Voltage Doubler and High Power Factor

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***Abstract*—In this paper, a new soft-switching bridgeless single-phase power factor correction (PFC) converter is presented and analyzed. Employing an auxiliary switch, the input current dead angle that is the main drawback of the existing buck-type PFCs is omitted, and thus, the power factor (PF) is improved, which is the main contribution of the paper. Proposed PFC converter operates under discontinuous conduction mode (DCM) and draws sinusoidal input current from power supply inherently. All switches and diodes are turned ON and OFF under soft switching, which leads to low switching losses and elimination of diode reverse recovery problems. Also, minimum numbers of semiconductor devices are in the power flow path that reduce the conduction losses. A 120-W laboratory prototype is implemented and experimental results verify the validity of theoretical analysis and show efficiency of 92.1%. In addition, total harmonic distortion (THD) of 3.3% is achieved and the input current harmonics complies with IEC61000-3-2 Class D requirements.**

***Index Terms*—Bridgeless buck converter, dead angle, power factor correction (PFC), soft switching.**

I. Introduction

TODAY, the incredible growth in the use of computers, servers, telecommunication systems, and some applications such as battery chargers for electrical vehicles employing more and more power supplies have increased worldwide energy consumption and global warming and economic issues. Therefore, the standards such as the California Energy Commission (CEC) were set to control the energy efficiency and reduce the energy consumption [1]. Also, in order to minimize the power grid damages resulted by injected harmonics and to achieve high power factor (PF) and low total harmonic distortion (THD) in electrical equipment, standards such as IEC61000-3-2 should be met. Thus, researchers have focused on improving power factor correction (PFC) topologies.

A boost converter is widely used as a PFC converter due to its high PF and simplicity. However, a boost converter cannot provide low output voltage. High output voltage of a boost PFC converter usually increase cost and conduction losses of the post regulator. Although a boost converter is the best candidate for

Manuscript received August 29, 2017; revised November 12, 2017 and January 28, 2018; accepted March 18, 2018. Date of publication March 26, 2018; date of current version November 19, 2018. Recommended for publication by Associate Editor R. Redl. *(Corresponding author: Ehsan Adib.)*

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three semiconductor devices are in power flow path and cannot fulfill bridgeless topology purpose. Also, since all switches operate at hard switching condition in [15]–[20], electromagnetic interference (EMI) noise is problematic and results in limited operating frequency, leading to high converter size and cost due to increment of heat sink size. A bridgeless PFC operating in discontinuous capacitor voltage mode (DCVM) is explained in [21]. Unlike the regular buck PFC, its input current is continuous that reduces input filter size. However, this type of PFC cannot achieve acceptable PF at light loads. Also, it suffers from high switch voltage stress and zero-crossing dead angle in its input current. In bridgeless flyback PFC [22], RCD snubber is necessary to protect switches against stored energy in leakage inductance that increases switching losses and size. To reduce switching losses and enhance the switching frequency, zero voltage transition (ZVT) and zero current transition (ZCT) techniques are adopted for bridgeless converters [23]–[30]. In [23], the diode of an auxiliary circuit is in the power path. In [24], the circulating energy of the converter is high, and when switches are OFF, three semiconductors are in the power flow path that increases conduction losses. Structures of auxiliary circuits in [25]–[28] are complex. In [29], the auxiliary switch cannot operate under soft-switching condition that decreases efficiency. Also, converter of [30] is based on SEPIC converter and the number of passive elements in the power path is high. The main drawback of applying ZVT and ZCT techniques is increased number of passive elements and semiconductors that reduce power density and increase the implementation cost. Based on the aforementioned explanations, soft-switching step-down PFC converter with high PF and low THD is required. Therefore, in this paper, a new step-down bridgeless PFC converter is introduced by applying the switched resonator method [31] into a bridgeless PFC converter [8] while eliminating the input current dead angle with a simple technique, as shown in Fig. 1. The introduced bridgeless PFC in [8] suffers from dead angle in the input current and hard switching condition, which increases THD and reduces efficiency, respectively. Switching losses in buck-type PFC converters are very high since the switch turns OFF under output current, which is very large. All diodes and switches of the proposed PFC in this paper turn ON and OFF under zero-current-switching (ZCS) condition. Voltage stress of switches S_1 and S_2 is lower than SEPIC and Cuk PFC and minimum number of semiconductors are in the power flow path. In addition, by using reverse voltage blocking switches (such as RB-IGBT) as the unidirectional switch for high-voltage applications, series diodes with the main switches can be eliminated [8], [21], [32]. These features result in the reduction of conduction and switching losses. Furthermore, it should be noted that switching losses are very low too due to achieved ZCS condition and elimination of tailing current losses. The resonant capacitors and inductors used in the proposed converter are smaller than passive elements used in conventional SEPIC and Cuk PFCs that reduce the size and cost. The proposed PFC operates in DCM that leads to inherent PFC and reduced reverse recovery problems. As demonstrated in Fig. 1(b), the inductors L_{m1} and L_{m2} in PFC Type 1 are coupled on the same magnetic core to reduce size. In order to omit the dead angle when

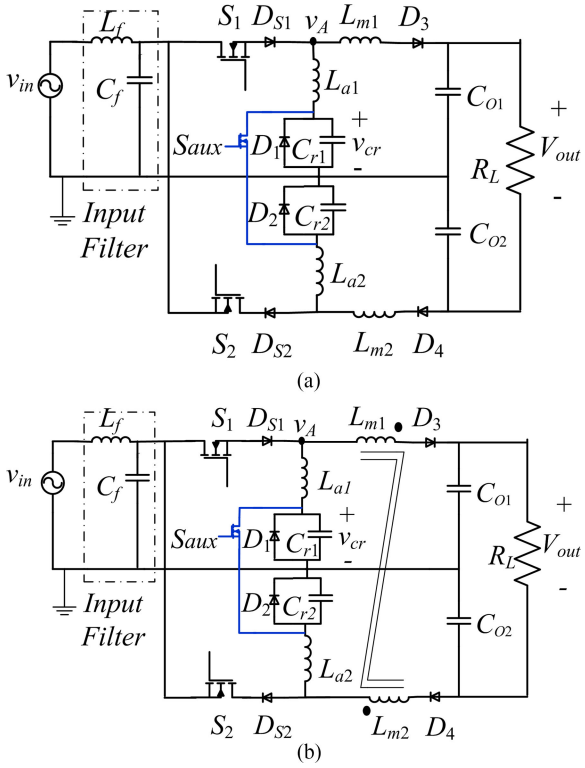

Fig. 1. Proposed soft-switching PFC converters with unity PF. (a) Type 1. (b) Type 2.

the output voltage is higher than the input voltage and improve PF, auxiliary switch S_{aux} is employed. It is shown that S_{aux} is switched under zero-voltage-switching (ZVS) condition. The proposed PFC operates under soft-switching condition that leads to low EMI noise. Also, the common mode noise of this structure is low [8]. In this paper, only the proposed bridgeless PFC Type 1 will be discussed. In the next section, the PFC circuit structure and operation modes are explained. In Section III, design procedures of elements and guidelines are focused. Experimental results are provided in Section IV to verify the validity of theoretical analysis.

II. Operating Principles

In this section, proposed bridgeless PFC operating in DCM mode will be analyzed in detail. During the positive half-line cycle D_1, D_3,D_{S1},S_1, S_{aux}, L_{m1}, L_{a1}, and C_{r1} are active, and during the negative half-line cycle D_2, D_4, D_{S2}, S_2, S_{aux}, L_{m2}, L_{a2}, and C_{r2} are used. Main switches can be triggered by same floating signal and sensing positive and negative half-line cycles is not required. Because of converter symmetrical operation, only the positive half-line cycle of Type 1 converter is analyzed. Also, before analyzing the circuit, it is assumed that all semiconductor devices are OFF, stored energy in resonant elements is zero, and load is supplied by output capacitors.

A. Operating in $v_{in}(t) > V_{O1}$

When the input voltage is higher than half of the output voltage, the proposed PFC operation modes are described in

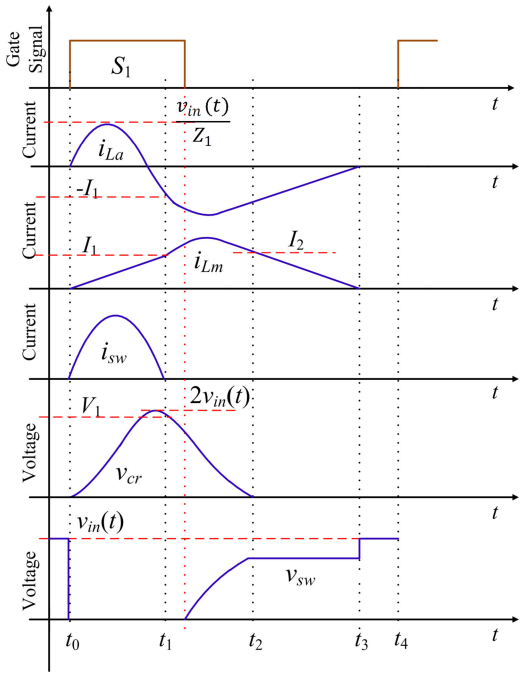

Fig. 2. Theoretical key waveforms in $v_{\text{in}}(t) > V_{o1}$.

this section. In this section, S_{aux} is OFF and S_1 keeps switching. Theoretical key waveforms and circuit operations of proposed PFC during a switching period are illustrated in Figs. 2 and 3, respectively.

Mode 1 [t_0–t_1]*:* At the beginning of this mode, S_1 and diodes D_{S1} and D_3 are turned ON at ZCS due to existence of L_{a1} and L_{m1}. L_{m1} current (i_{Lm}) increases linearly by a slop of $\frac{v_{\text{in}}(t)-V_{o1}}{L_{m1}}$. Also, L_{a1} starts a resonance with C_{r1} through S_1 and L_{a1} current (i_{La}) increases in sinusoidal fashion. At the end of this mode, i_{La} and i_{Lm} become equal and reach I_1. Also, resonant current and voltage equations are given by

$$i_{Lm}(t) = \frac{v_{\text{in}}(t) - V_{o1}}{L_{m1}}(t - t_0) \tag{1}$$

$$i_{La}(t) = \frac{v_{\text{in}}(t)}{Z_1}\sin\omega_1(t - t_0) \tag{2}$$

$$v_{cr}(t) = v_{\text{in}}(t) \times [1 - \cos(\omega_1(t - t_0))] \tag{3}$$

$$Z_1 = \sqrt{\frac{L_{a1}}{C_{r1}}} \tag{4}$$

$$T_1 = \frac{2\pi}{\omega_1} = 2\pi \times \sqrt{\mathrm{L_{a1}.C_{r1}}}. \tag{5}$$

Mode 2 [t_1–t_2]*:* At the beginning of this mode, since i_{La} and i_{Lm} are equal, S_1 current is zero. Thus, S_1 is turned OFF under ZCS condition. In addition, L_{m1} is in series with L_{a1} and C_{r1} and begins a resonance until C_{r1} voltage reaches zero and diode D_1 turns ON. Furthermore, based on (7), all of these happen approximately less than half of the resonance period. Hence, duration of this mode is considered as $\frac{1}{2}T_2$. At the end of this mode, i_{Lm} and i_{La} reach I_2. According to (6), i_{Lm} is sum of two sinusoidal terms, one of them increases and the other one decreases. Therefore, during this mode, the amplitude of inductors current does not change considerably with respect to its initial value at the beginning of this mode and I_2 and I_1 are almost equal

$$i_{Lm}(t) = -\mathrm{i}_{La}(t) = \frac{V_1 - V_{o1}}{Z_2} \times \sin(\omega_2(t - t_1)) + I_1\cos(\omega_2(t - t_1)) \tag{6}$$

$$V_{cr}(t) = V_{o1} + (V_1 - V_{o1}) \times \cos(\omega_2(t - t_1)) - Z_2 I_1 \sin(\omega_2(t - t_1)) \tag{7}$$

$$T_2 = \frac{2\pi}{\omega_2} = 2\pi \times \sqrt{(L_{a1} + L_{m1})C_{r1}} \tag{8}$$

$$Z_2 = \sqrt{\frac{L_{a1} + L_{m1}}{C_{r1}}}. \tag{9}$$

Mode 3 [t_2–t_3]*:* At t_2, diode D_1 turns ON under ZVS. Also, i_{La} and i_{Lm} currents decrease with the slop of $\frac{V_{o1}}{L_{m1}+L_{a1}}$ since the output voltage is reversely placed across them. At the end of interval, i_{Lm} and i_{La} reach zero and D_1 and D_3 turn OFF under ZCS that eliminates reverse recovery problems

$$i_{Lm}(t) = -i_{La}(t) = I_2 - \frac{V_{o1}}{L_{a1} + L_{m1}}(t - t_2). \tag{10}$$

According to (10) and description in mode 2, duration of this mode is

$$t_3 - t_2 = \frac{L_{a1} + L_{m1}}{V_{o1}} I_1. \tag{11}$$

Mode 4 [t_3–t_4]*:* In this interval, all the semiconductors are OFF and capacitors C_{o1} and C_{o2} supply load. This mode continues to the end of switching period.

B. *Operating in* $v_{in}(t) < V_{O1}$

When the input voltage is smaller than half of the output voltage, the proposed PFC operation modes are explained in this section. During this section, S_{aux} and S_1 are switched together. Thus, two additional modes exist as described. It is noted that two next modes happen before mode 1. Theoretical key waveforms and circuit operations of proposed PFC during a switching period are illustrated in Figs. 4 and 5, respectively.

Mode 1a [t_{a0}–t_{a1}]*:* At the beginning of this stage, S_1 and S_{aux} are synchronously turned ON at ZCS and L_{a1} starts storing energy and its current rises linearly until control unit turns S_{aux} OFF under ZVS. At the end of this mode, i_{La} reaches I_{a1}. The duty cycle of S_{aux} is considered as D_{aux}

$$i_{La}(t) = \frac{v_{\text{in}}(t)}{L_{a1}}(t - t_{a0}) \tag{12}$$

$$I_{a1} = \frac{v_{\text{in}}(t) \times D_{\text{aux}} \times T_{\text{sw}}}{L_{a1}}. \tag{13}$$

Mode 2a [t_{a1}–t_{a2}]*:* At this mode, C_{r1} and L_{a1} start a resonance. At the end of this mode, L_{a1} current reaches zero and C_{r1} voltage becomes maximum. At this moment, switch S_1 current is zero and can be turned OFF under ZCS. Then, i_{La} becomes

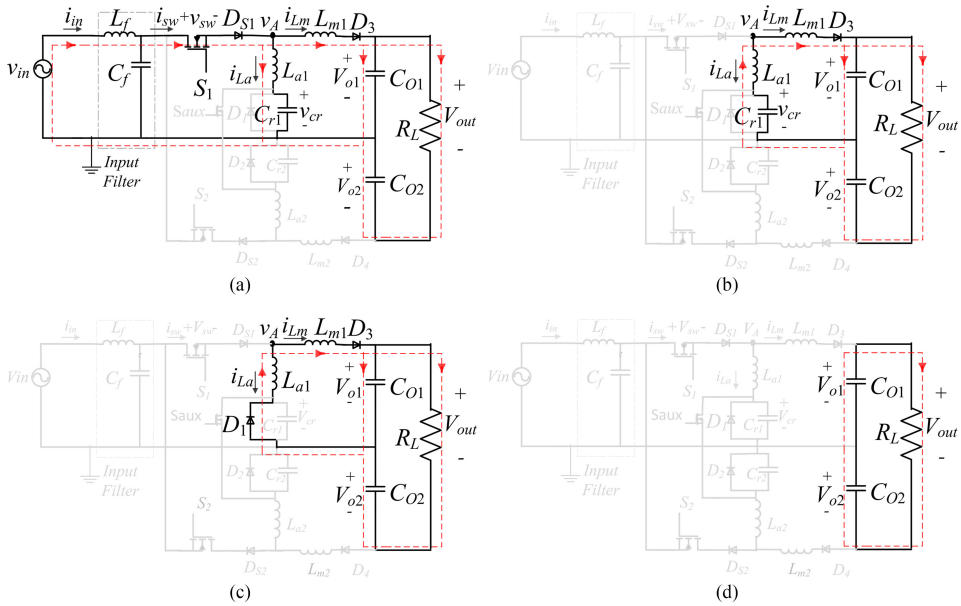

Fig. 3. Equivalent circuits of modes in $v_{\text{in}}(t) > V_{o1}$. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

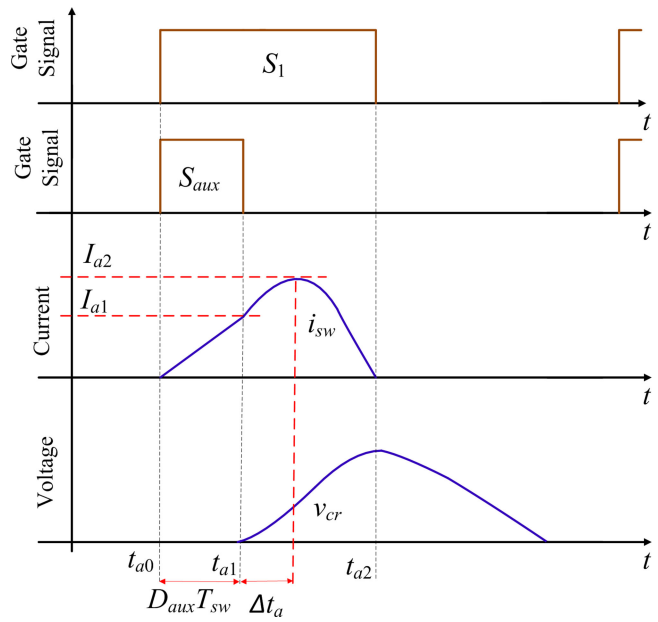

Fig. 4. Theoretical key waveforms in $v_{\text{in}}(t) < V_{o1}$.

negative and continues resonance with C_{r1} and L_{m1}. The next three operation modes are similar to the modes 2, 3, and 4

$$i_{La}(t) = \frac{v_{in}(t)}{Z_1}\sin(\omega_1(t-t_{a1})) + I_{a1}\cos(\omega_1(t-t_{a1})) \tag{14}$$

$$I_{a2} = \frac{v_{\text{in}}(t)}{\sqrt{2}}\left(\frac{1}{Z_1} + \frac{D_{aux}}{f_{sw}\times L_{a1}}\right) \tag{15}$$

$$t_{a2} - t_{a1} = \frac{1}{\omega_1}\times\left[\pi - \arctan\left(\frac{D_{aux}\times\omega_1}{f_{\text{sw}}}\right)\right]. \tag{16}$$

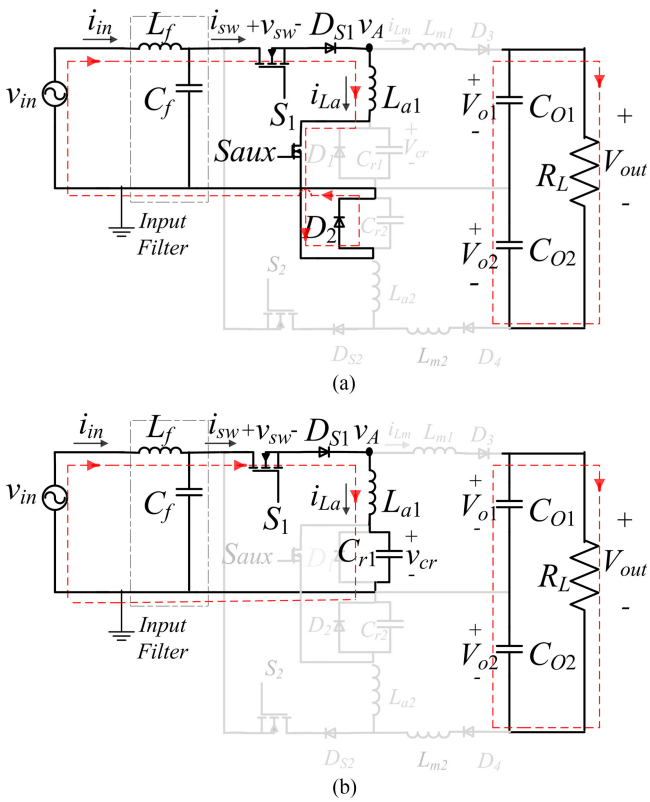

Fig. 5. Equivalent circuits of modes in $v_{\text{in}}(t) < V_{o1}$. (a) Mode 1a. (b) Mode 2a.

III. Design Procedure

In order to extract equations, it is convenient to define PFC gain and inductors ratio as $G = \frac{V_{o1}}{V_{\text{in}}}$ and $K = \frac{L_{m1}}{L_{a1}}$, respectively. According to the description in mode 1 and Section III-D, i_{La} and i_{Lm} should meet each other at $\frac{5}{8}T_1$ to ensure S_1 can be

turned OFF under zero current. By equating (1) and (2) in $\frac{5}{8}T_1$, *K* can be defined by PFC gain (*G*)

$$K = \frac{5\pi\sqrt{2}}{4}(1-G). \tag{17}$$

A. Calculating Input and Output Power

According to Fig. 3(a), the input current is equal to the average of main switch current over one switching period. Also, switch S_1 only conducts during first mode. Therefore, by integrating $i_{\rm sw}(t)$ over the first mode ($t_1 - t_0 = \frac{5}{8}T_1$), $i_{\rm sw,avg}(t)$ can be determined

$$i_{\rm sw,avg}(t) = \frac{1}{T_{\rm sw}}\left(\int_0^{\frac{5}{8}T_1} i_{La}(t)\,dt + \int_0^{\frac{5}{8}T_1} i_{Lm}(t)\,dt\right). \tag{18}$$

By performing the integral, $i_{\rm sw,avg}(t)$ can be represented as follows:

$$i_{\rm sw,avg}(t) = v_{\rm in}(t) \times C_{r1} \times f_{\rm sw}\left[\frac{7.11\times(1-G)}{K} + 1.707\right]. \tag{19}$$

The instantaneous input voltage, input current, and input power are given by (20)–(22), respectively

$$v_{\rm in}(t) = \sqrt{2} \times V_{\rm in,rms} \times \sin(\omega t) \tag{20}$$

$$i_{\rm in}(t) = \sqrt{2} \times I_{\rm in,rms} \times \sin(\omega t) \tag{21}$$

$$p_{\rm in}(t) = v_{\rm in}(t) \times i_{\rm in}(t) = 2 \times V_{\rm in,rms} \times I_{\rm in,rms} \times \sin^2(\omega t) = P_{\rm in,max} \times \sin^2(\omega t). \tag{22}$$

Therefore, by using (17), (19), and (22), the instantaneous input power can be represented by

$$p_{\rm in}(t) \cong 3.09 \times C_{r1} \times v_{\rm in}^2(t) \times f_{\rm sw}. \tag{23}$$

If dead angle is eliminated completely, the average of output power can be equal to (24), where η is the converter efficiency

$$P_{o,\rm avg} = 0.5 \times \eta \times P_{\rm in,max}. \tag{24}$$

B. Design of C_{r1}

In PFC converter, input voltage and current are sinusoidal waveforms and their values vary between zero and their maximum amplitude that lead to change in instantaneous amplitude of input power. Therefore, according to (23), the resonant capacitor (C_{r1}) should have the capability of transferring the maximum input power. Furthermore, operating under maximum switching frequency ensures that there is no deadtime in the switching period, and subsequently, the maximum power is being transferred to the load. So, according to these assumptions, C_{r1} should be determined in maximum input power and switching frequency. C_{r1} can be calculated as follows:

$$C_{r1} = \frac{P_{\rm in,max}}{3.09\ V_{\rm in,max}^2 f_{\rm sw,max}}. \tag{25}$$

C. Design of L_{a1} and K

In order to design L_{a1}, sum of the modes 1, 2, and 3 durations should be less than $\frac{1}{f_{\rm sw,max}}$ to ensure that converter will not operate in continuous conduction mode (CCM). Therefore, L_{a1} should be small enough to force PFC to work in DCM condition. Note that safety factor (SF) is used in (26) to guarantee that proposed PFC will not operate in boundary conduction mode

$$L_{a1} \le \frac{\left[1 + \frac{4\times\sqrt{1+K}}{5} + \left(1+\frac{1}{K}\right)\times\left(\frac{1}{G}-1\right)\right]^{-2}}{C_{r1}\times\left(1.25\pi\times SF\times f_{\rm sw,max}\right)^2}. \tag{26}$$

MATLAB solution of (26) shows that L_{a1} is minimum only when input voltage is maximum. Subsequently, *K* is designed for maximum input voltage too.

D. Maximum and Minimum Main Switches Duty Cycle

According to the first mode, in order to achieve ZCS for main switch, i_{La} and i_{Lm} must meet each other at the time $t_1 \le \frac{3}{4}T_1$ (i_{La} reaches its maximum negative value at $t_1 = \frac{3}{4}T_1$). Otherwise, the amplitude of i_{La} decreases and they will not meet each other at all. However, lower t_1, results in reduced duration of the first mode and causes extra switch peak current. Therefore, duration of this mode should be considered almost equal to $\frac{3}{4}T_1$. Thus, the control unit should turn main switches OFF after $\frac{5}{8}T_1$ and less than $\frac{3}{4}T_1$. When switch current in the first mode reaches zero, D_{S1} becomes reverse biased and node "A" voltage reaches its maximum value ($V_{A,\max} > v_{\rm in}(t)$) and then its voltage reduces to $v_{\rm in}(t)$. Then diode D_{S1} becomes forward biased and S_1 current begins to rise again and S_1 cannot be turned OFF under ZCS. Therefore, the maximum allowable time that control circuits can keep S_1 on should be calculated. Based on Fig. 3, node "A" voltage is as follows when switch current is zero:

$$v_A(t) = v_{\rm cr} - \left(\frac{v_{cr} - V_{o1}}{L_{a1}+L_{m1}} \times L_{a1}\right). \tag{27}$$

The switch should be turned OFF before v_A reaches $v_{\rm in}(t)$. By solving (27) in MATLAB software, it is concluded that when input voltage is in its maximum value, v_A reaches $v_{\rm in}(t)$ faster and proper duration for switch on time becomes minimum. Therefore, the maximum allowable ON-time duration to guarantee ZCS must be calculated for $V_{\rm in,max}$. Thus, by replacing $V_{\rm in,max}$ in $v_{\rm cr}$ and equating (27) to $V_{\rm in,max}$, the maximum period that control circuit is allowed to keep S_1 ON will be achieved.

E. Auxiliary Switch Duty Cycle

It is noteworthy to say that in order to increase PF, the input current should not change abruptly when the input voltage becomes larger than half of the output voltage. The phase angle where the input voltage becomes higher than half of the output voltage ($V_{o1} = 0.5 \times V_{\rm out}$) is equal to $\theta = \sin^{-1}\frac{V_{o1}}{V_{\rm in,max}}$. In order to achieve pure sinusoidal input current, the amplitude of the input current at this point should be equal to $I_{\rm in,max} \times \sin\theta$, where $I_{\rm in,max} = \frac{P_{\rm in,max}}{V_{\rm in,max}}$. In order to simplify calculations, switch current waveform, which is shown in Fig. 4,

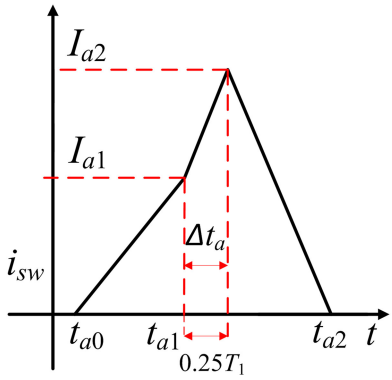

Fig. 6. Approximated switch current waveform in $v_{\text{in}}(t) < V_{o1}$.

can be approximated by waveform in Fig. 6. Also, it is assumed that Δt_a is equal to $0.25T_1$. Therefore, $i_{\text{in}}(t)$ and $i_{\text{sw,avg}}(t)$ are calculated as follows:

$$\begin{aligned} i_{\text{in}}(t) &= i_{\text{sw,avg}}(t) = \frac{D_{\text{aux}}^2 \times v_{\text{in}}(t)}{2 \times L_{a1} \times f_{sw}} + 0.125 \times v_{\text{in}}(t) \\ &\times T_1 \times f_{\text{sw}} \left(I_{a2} + \frac{D_{aux}}{L_{a1} \times f_{\text{sw}}} \right) \\ &+ 0.5 \times v_{\text{in}}(t) \times I_{a2} \times f_{\text{sw}} \\ &\times \left[\frac{1}{\omega_1} \times \left(\pi - \arctan \left(\frac{D_{aux} \times \omega_1}{f_{\text{sw}}} \right) \right) - 0.25 \times T_1 \right]. \end{aligned} \tag{28}$$

F. Maximum Voltage and Current Stress of Semiconductor Devices

Since the minimum voltage of the resonant capacitor is zero, the main switches voltage stress is clamped to the input voltage and the voltage stress of diodes D_3 and D_4 are clamped to $0.5V_{\text{out}}$. The voltage stress of the auxiliary switch, D_1, and D_2 are equal to the peak voltage of resonant capacitors, which occurs at the maximum input voltage, which is almost equal to $2V_{\text{in,max}}$. In the first mode, the sum of L_{a1} and L_{m1} currents run through the main switch. Thus, according to (1) and (2), the maximum current stress of the main switch is

$$\left(\frac{V_{\text{in,max}}}{Z_1} + \frac{V_{\text{in,max}} - 0.5V_{\text{out}}}{L_{m1}} \times 0.5T_1 \right).$$

IV. Experimental Results

A laboratory prototype of the proposed Type 1 PFC ($V_{\text{in}} = 110\ V_{\text{rms}}$ and 50 Hz, $f_{\text{sw}} = 100$ kHz, $V_{\text{out}} = 48$ V, $P_{\text{out}} = 120$ W) is designed and implemented to verify the validity of theoretical analysis. The components of the prototype are presented in Table I. In order to increase the efficiency, IGBTs with reverse blocking capability (RB-IGBT) can be employed as main switches [8], [21], [32] for high-voltage applications. In the proposed prototype converter, MOSFET switch with a series diode is used since the input voltage is low. In low-voltage applications, usually a series combination of MOSFET and a diode has lower conduction voltage than an RB-IGBT switch. However, at high-input-voltage applications, since the conduction voltage of high-voltage diodes are relatively large and also the drain-source on resistance of high-voltage MOSFET switches are high, RB-IGBT is a better choice. The proposed converter is compared with existing PFCs in Table II. Note that, in [8], [9], and [21], semiconductor devices are turned ON or OFF under hard switching conditions. Therefore, their soft-switching conditions are illustrated as partial in Table II. The implementation cost of proposed converter and converter of [21] are slightly higher due to three switches applied in proposed converter and applied semiconductors devices with high voltage rating for converter of [21]. In addition, PSPICE simulations are performed for the proposed PFC and PFCs in [8], [9], and [21] and the efficiency results are reported in Table II. Introduced PFCs in [8] and [9] are less expensive than proposed Type 1 PFC but their efficiency and THD are not desirable.

TABLE I
Design Parameters of the PFC

Symbol	Parameter
L_f & C_f	2mH & 230nF
L_{a1}~L_{a2}	1.9 μH
L_{m1}~L_{m2}	8.85 μH
C_{r1}~C_{r2}	36 nF
C_{o1}~C_{o2}	4.7 mF
D_1~D_2	MUR860
D_3~D_4	BYV32-200
S_1~S_2	IRFP260
D_{S1}~D_{S2}	BYV32-200
S_{aux}	IRF740

It can be observed from Fig. 7(a) that the measured harmonic contents of the input current for various input voltage up to 19th harmonic are well below the IEC61000-3-2 Class D limits. As shown in Fig. 7(b), even at 25% nominal load, the efficiency of the proposed converter varies about only 1%, making the proposed PFC appropriate for applying in electronic devices. Fig. 8 reports the conduction losses of MOSFETS, diodes D_{S1}–D_{S2}, diodes D_1–D_4, and capacitors and inductors. The simulation and experimental results and datasheet parameters of elements are used to calculate the losses breakdown. A photo of laboratory prototype of the proposed PFC is provided in Fig. 9.

The experimental waveforms of the input voltage and input current and the FFT of the input current with a series filter are shown in Fig. 10. In Fig. 10(a), the dead angle of the input current is clearly visible when the auxiliary switch is OFF. However, in Fig. 10(b), the auxiliary switch operates during the dead angle interval and regulates the input current. It is obvious that the dead angle is omitted and the input current shape is perfectly sinusoidal and is in phase with the input voltage. In Fig. 10(c), the waveforms of the input voltage and current at

TABLE II
COMPARISON OF THE PROPOSED PFC AND THE OTHER TOPOLOGIES USING PSPICE SIMULATION RESULTS

Item		Type 1	[8]	[9]	[21]
No.of main switch		2 (IRFP260)	2 (IRFP260)	2 (IRFP460)	2 (IRFP460)
No.of auxiliary switch		1 (IRF740)	0 -	0 -	0 -
No.of Diode		6	4	3	5
No.of Magnetic Element		4	2	1	3
No.of conducting simultaneously semiconductor devices	Switch ON	2	2	2	3
	Switch OFF	1	1	1	1
Soft switching Condition		Full	Partial	Partial	Partial
Zero crossing dead angle		No	Yes	No	Yes
Cost/Power		Medium	Low	Low	Medium
Full Load Efficiency (%)		92.7	89.1	90.9	90

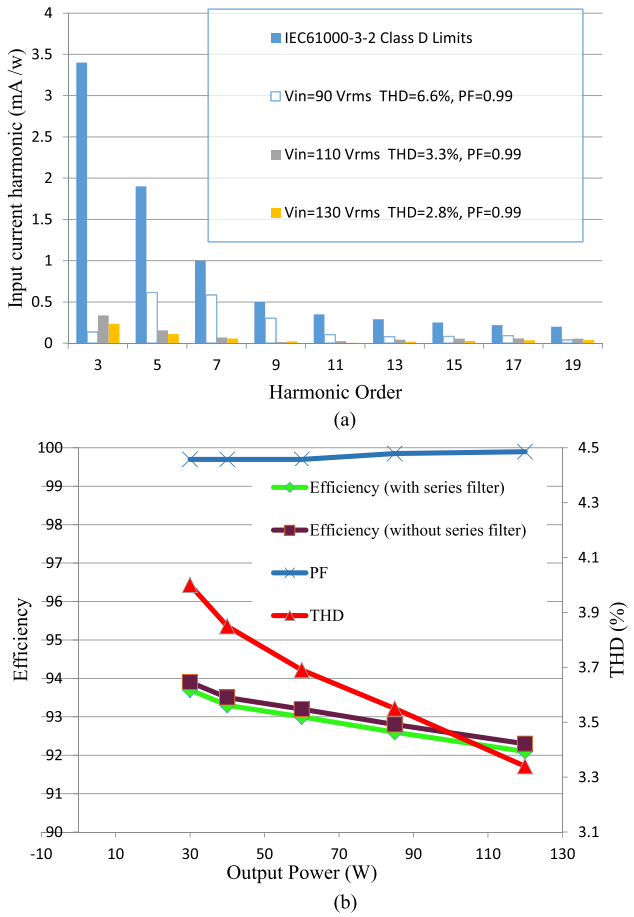

Fig. 7. (a) Measured input current harmonics. (b) Efficiency, PF, and THD.

light load are depicted. It shows that the proposed PFC can draw sinusoidal current even at light-load condition. In Fig. 10(d), the measured input current harmonics are reported. Also, the experimental waveforms of the input voltage and input current

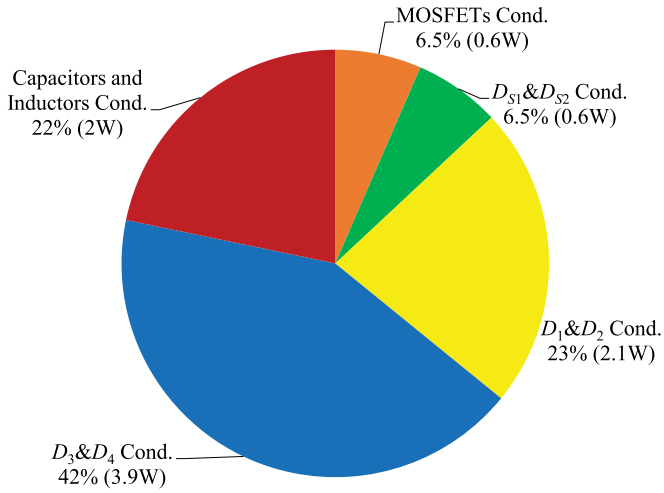

Fig. 8. Losses breakdown at nominal load at $V_{in} = 110\,V_{rms}$.

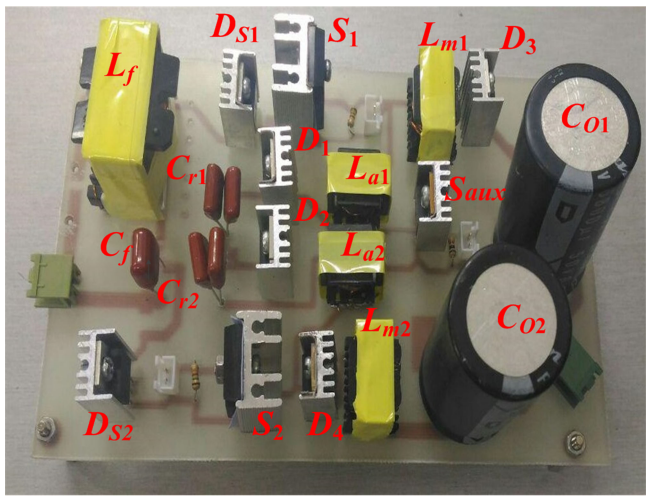

Fig. 9. Photo of the implemented prototype.

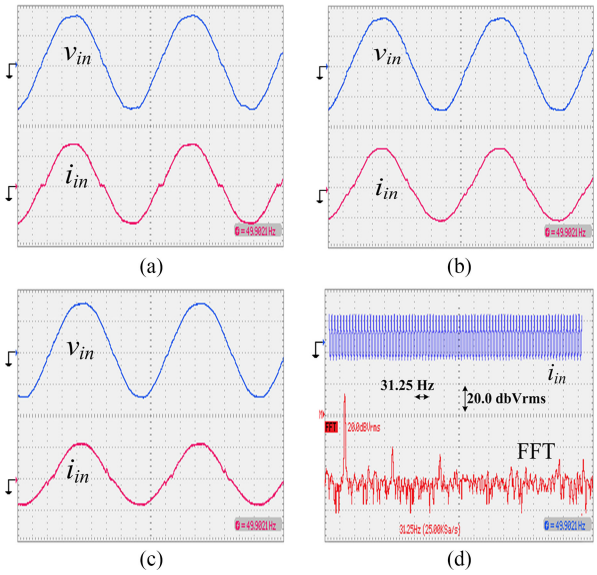

Fig. 10. Experimental waveforms of input voltage, input current, and FFT (with series filter). (a) Input voltage and current at full load without using auxiliary switch. From top to bottom: v_{in} (100 V/div), i_{in} (1.3 A/div), and time (2.5 ms/div). (b) Input voltage and current at full load by using auxiliary switch. From top to bottom: v_{in} (100 V/div), i_{in} (1.3 A/div), time (2.5 ms/div). (c) Input voltage and current at light load (30% of the nominal load) by using auxiliary switch. From top to bottom: v_{in} (100 V/div), i_{in} (0.5 A/div), and time (2.5 ms/div). (d) Input current harmonics at full load.

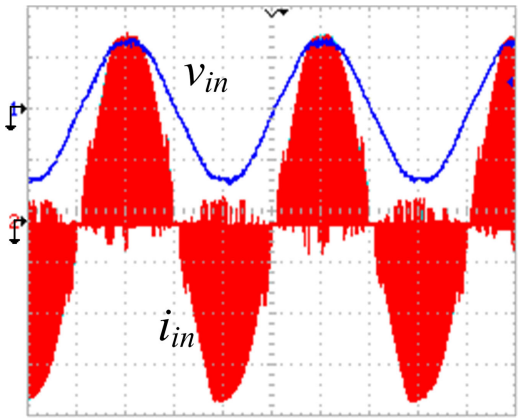

Fig. 11. Experimental waveforms of input voltage and input current (without series filter). From top to bottom: v_{in} (100 V/div), i_{in} (10 A/div), and time (5 ms/div).

without series filter are shown in Fig. 11. V_{o1}, V_{o2}, and output voltage are shown in Fig. 12. As can be observed, one of the capacitors is discharged in positive half-line cycle and the other one discharged in negative half-line cycle. Thus, low-frequency ripple of C_{o1} and C_{o2} cancel each other and V_{o} ripple, which the sum of V_{o1} and V_{o2}, is very low. Fig. 13(a) demonstrates the drain-source voltage, gate-source voltage, and current waveforms of the switch S_1. It is clear that switches and diodes are turned ON and OFF under ZCS conditions, which reduce switching losses, thereby improving the efficiency. In addition, the adverse effects of diode reverse recovery in conventional converters are resolved. In Fig. 13(b), the drain-source voltage, gate-source voltage, and current waveforms of the auxiliary switch are shown, which confirms that S_{aux} is turned ON under

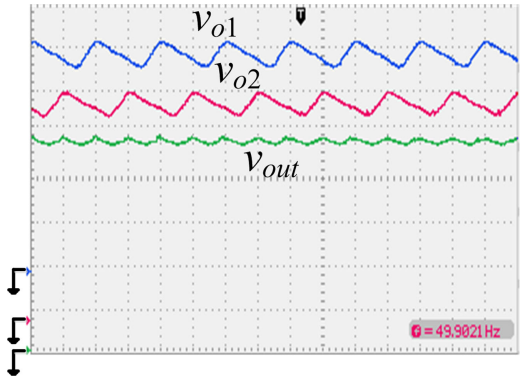

Fig. 12. Experimental waveforms of output voltages. From top to bottom: v_{o1} (5 V/div), v_{o2} (5 V/div), and v_{out} (10 V/div) (time 10 ms/div).

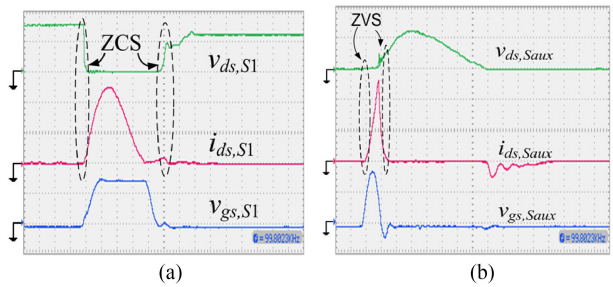

Fig. 13. Experimental waveforms of switches. (a) Main switch, from top to bottom: $v_{ds,S1}$ (100 V/div), $i_{ds,S1}$ (12 A/div), $v_{gs,S1}$ (10 V/div), time (250 ns/div), for $V_{\text{in}} = 150$ V. (b) Auxiliary switch, from top to bottom: $v_{ds,S\text{aux}}$ (50 V/div), $i_{ds,S\text{aux}}$ (1 A/div), $v_{gs,S\text{aux}}$ (10 V/div), time (250 ns/div) for $V_{\text{in}} = 24$ V.

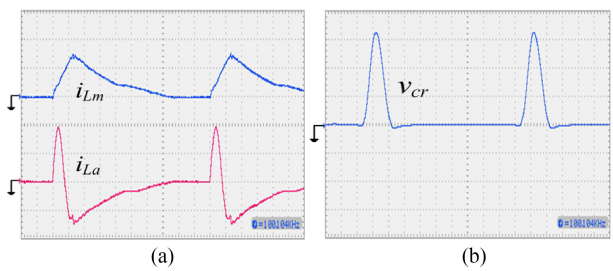

Fig. 14. Experimental waveforms of the inductor currents and capacitor voltage. (a) From top to bottom: L_{m1} current (12 A/div), L_{a1} current (12 A/div), time (1 μs/div), (b) C_{r1} voltage (100 V/div), time (1 μs/div) for $V_{\text{in}} = 150$ V.

ZVS and turned OFF under almost ZVS condition. In Fig. 14, waveforms of i_{La}, i_{Lm}, and v_{cr} are provided.

V. Conclusion

A soft-switching step-down bridgeless PFC converter has been proposed in this paper. Employing an auxiliary switch, which operates under ZVS, the dead angle in the input current is omitted. The proposed PFC reduces switching losses by providing ZCS condition for main switches and diodes without using any auxiliary circuits. Also, the number of semiconductors in power flow path is minimized. Both of these features result in improved efficiency. The experimental results verify that soft-switching condition is achieved for all semiconductors and the dead angle is omitted. Also, efficiency of 92.1% and THD of 3.3% at 110 V_{rms} input and 120 W output power are achieved.

The improvement on the efficiency of the proposed PFC can be justified by the fact that the number of semiconductors in the power flow path and switching and reverse recovery losses of diodes are minimized. Also, the proposed PFC can improve the THD significantly even at low input voltages.

REFERENCES

[1] California Energy Commission (CEC). Code of Conduct on Energy Efficiency of External Power Supplies, 2005. [Online]. Available: http://www.energy.ca.gov/papers/2005-03-03_WILSON.PDF

[2] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-based MHz totem-pole PFC rectifier," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 799–807, Sep. 2016.

[3] H. Ma, J. J. Lai, C. Zheng, and P. Sun, "A high-efficiency quasi-single-stage bridgeless electrolytic capacitor-free high-power AC–DC driver for supplying multiple LED strings in parallel," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5825–5836, Aug. 2016.

[4] B. Su and Z. Lu, "An interleaved totem-pole boost bridgeless rectifier with reduced reverse-recovery problems for power factor correction," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1406–1415, Jun. 2010.

[5] M. H. Rashid, *Power Electronics Handbook: Devices Circuits and Applications*. New York, NY, USA: Academic, 2010.

[6] X. Wu, J. Yang, J. Zhang, M. Xu, and S. Member, "Design considerations of soft-switched buck PFC converter with constant on-time (COT) control," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3144–3152, Nov. 2011.

[7] X. Wu, J. Yang, J. Zhang, and Z. Qian, "Variable on-time (VOT)-controlled critical conduction mode buck PFC converter for high-input AC/DC HB-LED lighting applications," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4530–4539, Nov. 2012.

[8] Y. Jang, Y. Jang, and M. M. Jovanović, "Bridgeless high-power-factor buck converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 602–611, Feb. 2011.

[9] M. Malekanehrad and E. Adib, "Bridgeless single-phase step-down PFC converter," *IET Power Electron*, vol. 9, no. 14, pp. 2631–2636, Nov. 2016.

[10] X. Xie, C. Zhao, L. Zheng, and S. Liu, "An improved buck PFC converter with high power factor," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2277–2284, May 2013.

[11] X. Xie, C. Zhao, Q. Lu, and S. Liu, "A novel integrated buck-flyback nonisolated PFC converter with high power factor," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5603–5612, Dec. 2013.

[12] J. Zhang, C. Zhao, S. Zhao, and X. Wu, "A family of single-phase hybrid step-down PFC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5271–5281, Jul. 2017.

[13] G. Spiazzi and S. Buso, "Power factor preregulators based on combined buck-flyback topologies," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 197–204, Mar. 2000.

[14] X. Xie, J. Li, K. Peng, C. Zhao, and Q. Lu, "Study on the single-stage forward-flyback PFC converter with QR control," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 430–442, Jan. 2016.

[15] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4153–4160, Sep. 2011.

[16] H. Farzaneh-Fard and M. Mahdavi, "Bridgeless CUK power factor correction rectifier with reduced conduction losses," *IET Power Electron.*, vol. 5, no. 9, pp. 1733–1740, Nov. 2012.

[17] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, "New bridgeless DCM sepic and Cuk PFC rectifiers with low conduction and switching losses," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 873–881, Mar. 2011

[18] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "New efficient bridgeless cuk rectifiers for PFC applications," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3292–3301, Jul. 2012.

[19] J. Yang and H. Do, "Bridgeless SEPIC converter with a ripple-free input current," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3388–3394, Jul. 2013.

[20] H.-T. Yang, H.-W. Chiang, and C.-Y. Chen, "Implementation of bridgeless cuk power factor corrector with positive output voltage," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3325–3333, Jul. 2015.

[21] A. A. Fardoun, E. H. Ismail, N. M. Khraim, A. J. Sabzali, and M. A. Al-Saffar, "Bridgeless high-power-factor buck-converter operating in discontinuous capacitor voltage mode," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3457–3467, Sep.-Oct. 2014.

[22] J. Shin, S. Choi, and B. Cho, "High-efficiency bridgeless flyback rectifier with bidirectional switch and dual output windings," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4752–4762, Sep. 2014.

[23] M. Mahdavi and H. Farzanehfard, "Zero-current-transition bridgeless PFC without extra voltage and current stress," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2540–2547, Jul. 2009.

[24] M. Alam, W. Eberle, D. S. Gautam, and C. Botting, "A soft-switching bridgeless AC–DC power factor correction converter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7716–7726, Oct. 2017.

[25] M. R. Amini, H. Farzanehfard, A. Emrani, and M. Mahdavi, "Soft switching bridgeless power factor correction with reduced conduction losses and no stresses," *IET Power Electron*, vol. 5, no. 3, pp. 334–340, Mar. 2012.

[26] M. Ramezani and S. M. Madani, "New zero-voltage-switching bridgeless PFC, using an improved auxiliary circuit," *IET Power Electron*, vol. 4, no. 6, p. 732, Jul. 2011.

[27] C.-C. Hua, Y.-H. Fang, and C.-H. Huang, "Zero-voltage-transition bridgeless power factor correction rectifier with soft-switched auxiliary circuit," *IET Power Electron*, vol. 9, no. 3, pp. 546–552, Mar. 2016.

[28] H. Y. Tsai, T. H. Hsia, and D. Chen, "A family of zero-voltage-transition bridgeless power-factor-correction circuits with a zero-current-switching auxiliary switch," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1848–1855, May 2011.

[29] I. D. Kim, E. C. Nho, S. H. Choi, and J. S. Lai, "A simple ZVT PWM single-phase rectifier with reduced conduction loss and unity power factor," *J. Power Electron.*, vol. 7, no. 1, pp. 55–63, 2007.

[30] M. Mahdavi and H. FarzanehFard, "Zero-voltage transition bridgeless single-ended primary inductance converter power factor correction rectifier," *IET Power Electron*, vol. 7, no. 4, pp. 895–902, Apr. 2014.

[31] H. Farzanehfard and M. Reza Amini, "Switched resonator DC/DC converter with a single switch and small inductors," *IET Power Electron*, vol. 7, no. 6, pp. 1331–1339, Jun. 2014.

[32] B. Zhao, A. Abramovitz, and K. Smedley, "Family of bridgeless buck-boost PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6524–6527, Dec. 2015.

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